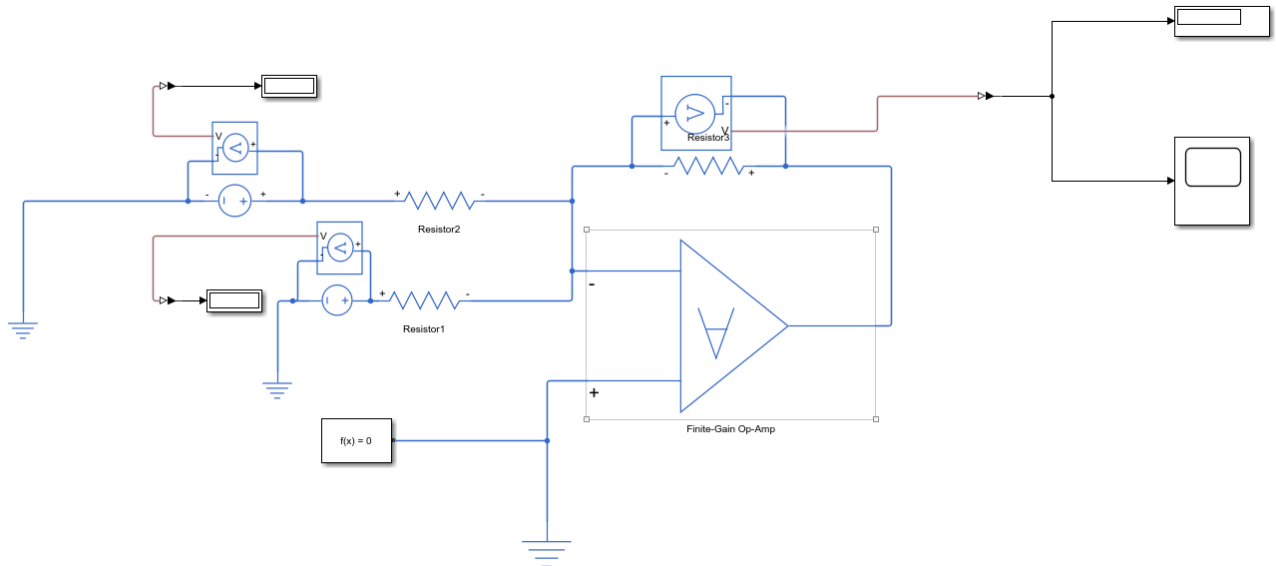


Team02 - Lab 01 - Weighted Summer Report

- Task Deliverables:

- Construct the circuit using Simscape simulation and a single op amp of the LM324 quad op amp IC.
- Provide 5 different combinations of DC inputs to the terminals labeled V1 and V2.

Circuit schematic:



Ideal Op-Amp Configuration:

1. Inf. Gain (A very Large)
2. $R_{in} \rightarrow \infty$
3. $R_{out} \rightarrow 0$

And then clarify the supply voltage values with your own Choice

Finite-Gain Op-Amp

Settings

Description

NAME

VALUE

▼ Main

> Gain, A

100000000000

> Input resistance, Rin

1e10

GOhm

▼

> Output resistance, Rout

0

kOhm

▼

> Minimum output, Vmin

-15

V

▼

> Maximum output, Vmax

15

V

▼

> Noise

Auto Apply

Note: Our Choice was +15 & -15 for the supply voltages in the simulation

Used Laws:

- 1- Superposition to deduce the equation for V_o of weighted summer

$$V_o = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \dots + \frac{V_n}{R_n} \right)$$

- 2- Gain for inverting configuration >>

$$V_o/V_i = -R_2/R_1 = -R_f/R_n \text{ (we sum them if there's more than single R in input)}$$

And since in our circuit $R_1 = R_2 = R_3$, from the weighted summer eqn. We can say the relation is as follows:

$$V_o = - (V_1 + V_2)$$

Readings Table 1:

V1 (V)	V2 (V)	O/P (Mathematical) (V)	O/P (Practical) (V)	$ \varepsilon_t $ % (Absolute Error Percentage)
1.05	-2.01	0.96	0.97	1 %
3.01	-1.01	-2	-1.98	2 %
1	-1.02	0.02	0	2 %
4.04	-2.03	-2.01	-2.05	4 %
10.04	-13.02	2.98	2.96	2 %
14.92	-5.17	-9.75	-4.4	535 % (Saturation)

Note: We used +5 & -5 for the supply voltages in the lab in order to be able to vary the input voltages from the Lab station, so any value exceeding it for the V_o would be Capped due to Saturation

- Circuit Simulation:

The simulation was done in [simulink](#) environment an add-on product to [MATLAB](#) package, where we selected each component corresponding to the circuit schematic of our weighted summer, adjust configurations ,setup and tailored v1, v2 and validated measurements.

- HW Lab session (29.10.2028):

For this part, we didn't face any issues in the beginning, but due to small hardware components and for our readings to be accurate it was a challenge to make sure the circuit schematic was executed correctly, as well as the relation between V_o & input Voltages v1 & v2

Note: for testing the saturation effect, we added an extra reading just to illustrate how signal gets capped due to limitations in the amplifying process and the solution is to inc. supply voltage which inc. the cost as well.....

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