

Credit Hours system

Computer Department

Cairo University

Faculty of Engineering

CMPN/S301-Computer Architecture

**Computer Architecture Project**

Submitted to: Eng.

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1. Instruction format

A screenshot of a computer

Description automatically generatedA screenshot of a computer

Description automatically generated

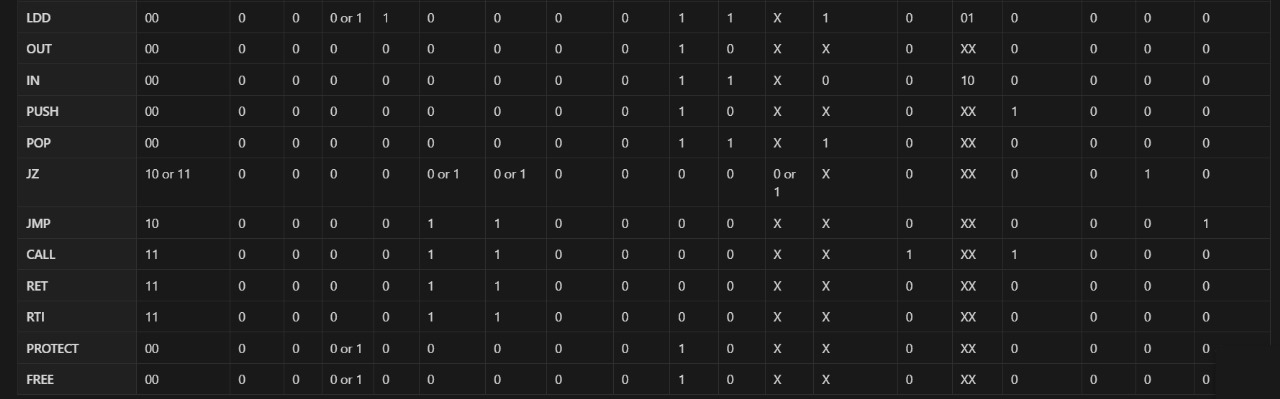
A screenshot of a computer

Description automatically generated

1. Control Signal Table

A black screen with white text

Description automatically generated



Details:

PC\_INC\_TYPE: choose between regular increment, Rdst from decode, Rdst from execute,output from memory

RST: resets all registers

INT: interrupt signal

IMM: does this inst have an immediate value?

FLUSH\_IF\_ID: flushes on branch execution,taken prediction or exceptions

FLUSH\_ID\_EX: flushes on branch execution or exceptions

FLUSH\_EX\_MEM: flushes on memory exceptions

PC\_WRITE: hazard detection unit allows writing to PC?

reg\_WE: enable wb to register file

Predictor: 1-bit global branch predictor

ALUorMEM: choose between ALU result or Memory result

CALL: is this a call inst?

RFC: chooses between immediate , Rsrc2, and input port

mem\_WE: is the instruction allowed to write in memory?

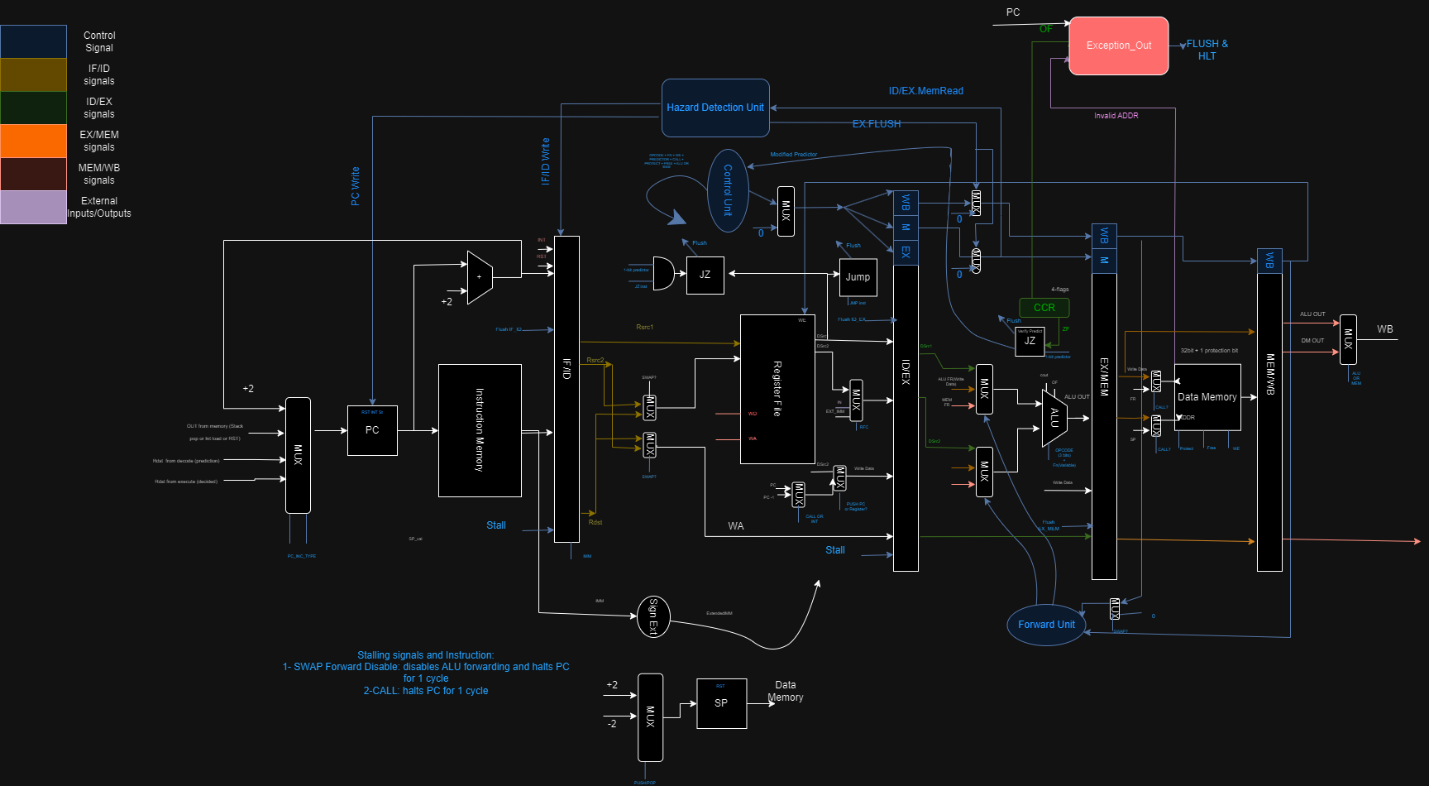
SWAP: is this a swap inst?

JZ\_Inst: is this a JZ inst?

JMP\_Inst: is this an unconditional jump?

Forwarding selectors: choose between ALU forward, direct buffer value, memory forward

1. Schematic diagram



1. Pipeline stages

Fetch-Decode Buffer -> 36 bit

Decode-Execute Buffer -> 99 bit

Execute-Memory Buffer ->73 bit

Write Back Buffer->105 bit