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**INTRODUCTION**

The Transistor is the driving horse for the semiconductor industry nowadays. It is more than a trillion dollar industry. From early 70s, Transistor scaling have been the main concern for device engineers and scientists. This seems to be reaching its’ fundamental limit nowadays but CMOS Scaling is being pushed for the next decade or maybe more.

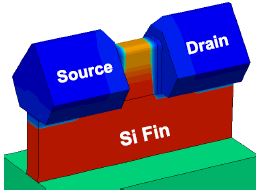
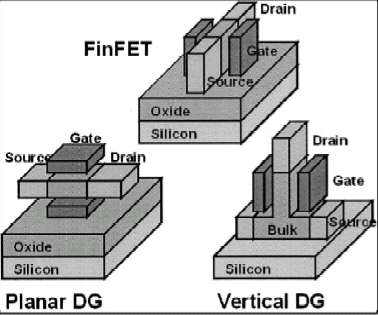
**Objective**

This project is concerned with the simulation and optimization of 180nm NMOS and PMOS technology node using TCAD Silvaco ( Atlas & Athena). Parameters of main concern are the gm and vth.

**State of Art Technology**

CMOS technology has started in the 70s. Transistor lengths of about 5 um were available at that time. Since then, CMOS scaling have been the driving force in our semiconductor industry. Scaling transistors means the ability to integrate more of them on the chip, increasing speed, reducing power, having higher logic density. It has been a long way scaling down transistors especially after going below the 1um channel length when short channel effects began to appear. Several modifications started to appear like replacing the metal electrode with polysilicon. Going deep in the submicron technology more problems started to appear and several solutions emerged like replacing the SiO2 with high-K materials.

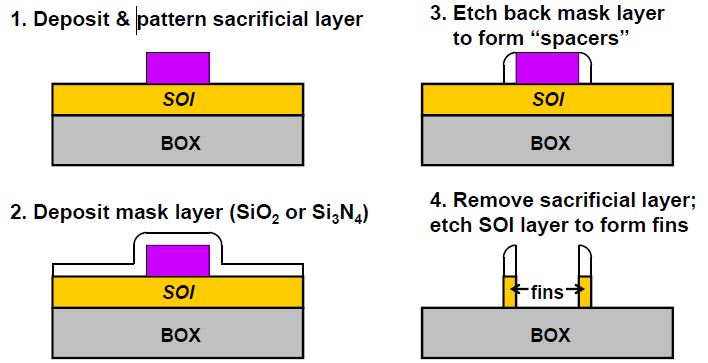
in the mean time, since going below 100nm limit the major problem lied in the loss of control on the channel using the Gate, It seemed that the traditional structure must be changed. SOI –Silicon on insulator- technology started to appear to cancel the substrate problems and double gated structures appeared. Next there were the SiGe and strained silicon technology which achieved very high mobility enhancement occurred. Transistors were ready to leave the planar era and go 3D. The current state art technologies starting from 22nm, 14 nm and the upcoming 10nm are based on FinFets.



The structure shown is called the TriGate FinFet because the channel is surrounded by the gate from 3 directions. This is the technology used by intel in the 22nm and 14nm technology. It is clear that it needs much more difficult processing steps and lithography for sharp edges seen in the right figure.

FinFets can be grown on bulk or as SOI. Both need difficult processing steps. The steps that we will show here are for the SOI.

Process steps:



After simple oxidation and photolithography steps the final structure can be achieved.

**PMOS**

The design of PMOS transistor passed through similar stages as that of the NMOS device. First of all, the specs of the required devices were obtained from several resources on the internet and FAB websites.

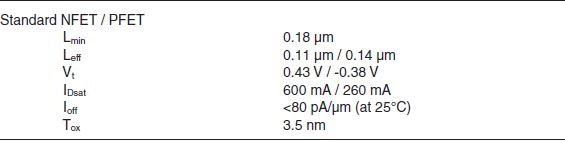


Fig. (1) The above specs are obtained from IBM 0.18 um technology

The above specs can vary between different FABs. For example, the oxide thickness is on the order 3-5 nm, V threshold around 0.4 V, On current sometimes is tolerated down to > 1nA/um. So in general we tried during optimization to keep track of the values used to make a template for later optimization .

**IV characteristics of the device :**

After optimizing the threshold voltage to around 0.4 V. Family of curves for the resulting transistor was plotted to extract the main physical parameters. The plot shows several interesting characteristics. The threshold voltage is around 0.4 volts as extracted from *Silvaco Atlas*. The obtained ON current is around

200 uA/um which is close to the required value. An interesting fact that the maximum Transconductance (gm) starts to reach a saturated value at higher drain voltages of about 225 uS/um. After trying to investigate this value it was clear that it is around the typical values for transistors used in analog circuits. 0.18 um PMOS transistors usually have uCox= 80 uA/V^2. If we assume gm = sqrt(2\*K\*Id) we can simply find numbers of about 200 uS/um as an expected value for the PMOS device.

The log plot shows off currents in the ranging between 10^-11 and 10^-10 for all operating voltages up to VDD=1.8v which is the high voltage value assigned for PMOS 0.18 um logic transistors. This value is considered on the border line for the max tolerance in this technology node.

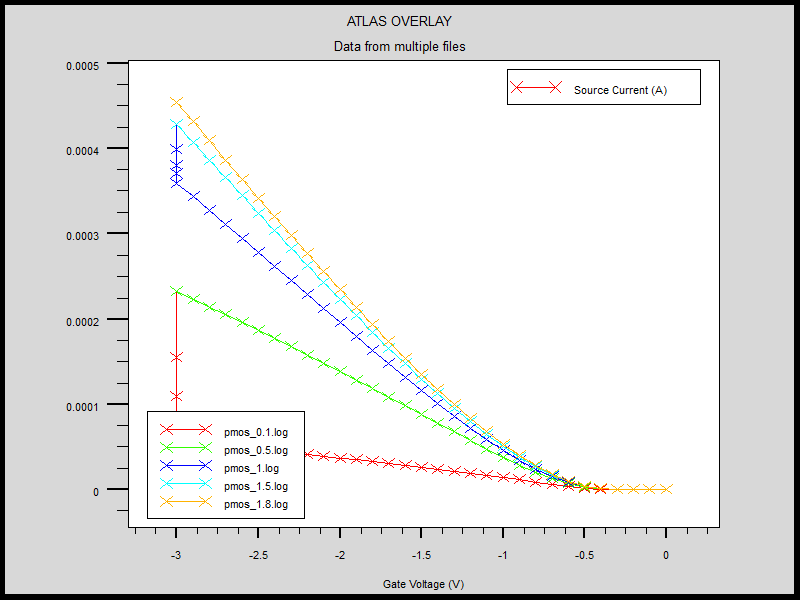
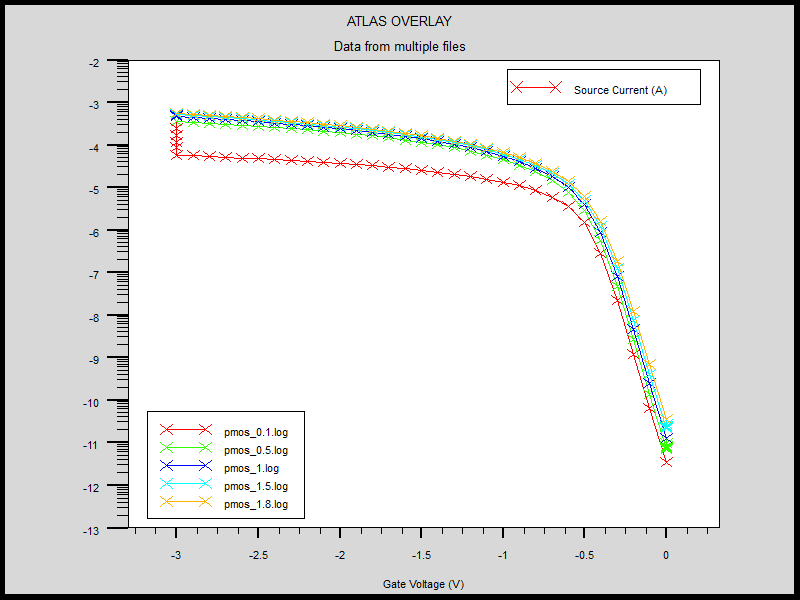


Fig.(2). Is/VGS plot at different VDS voltages



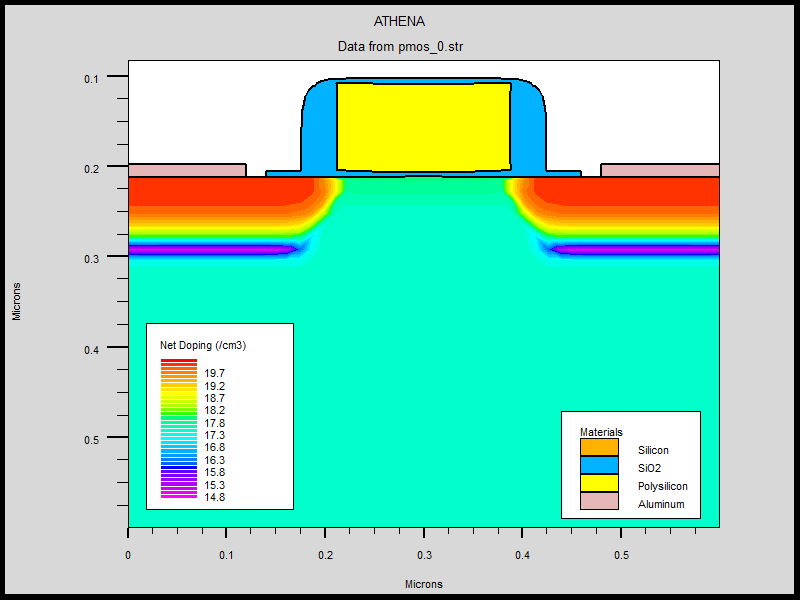
Fig(3). Log(I)/Vgs at different drain voltages

**DEVICE STRUCTURE:**

The device structure itself is now examined for the chosen values. Using the suitable extraction commands Junction depth, Oxide thickness and channel doping concentration are obtained.

Junction Depth of about 78 nm was found which is very close to the literature value found in the Spice model. Oxide thickness of 4.2 nm which is very typical and finally a channel doping concentration=5.86e17 cm-3 which is also almost identical to the reference value of 5.92e17 cm-3. Directly obvious from the plot, The doping concentration in the source and the drain was around 5e19 cm-3.

P-doped polysilicon was used as a contact material instead of N-doped polysilicon as N-poly will result in a large offset in the VFB which may cause difficult control of the Vth.



Fig(4) PMOS structure and doping profiles

**OPTIMIZATIONS:**

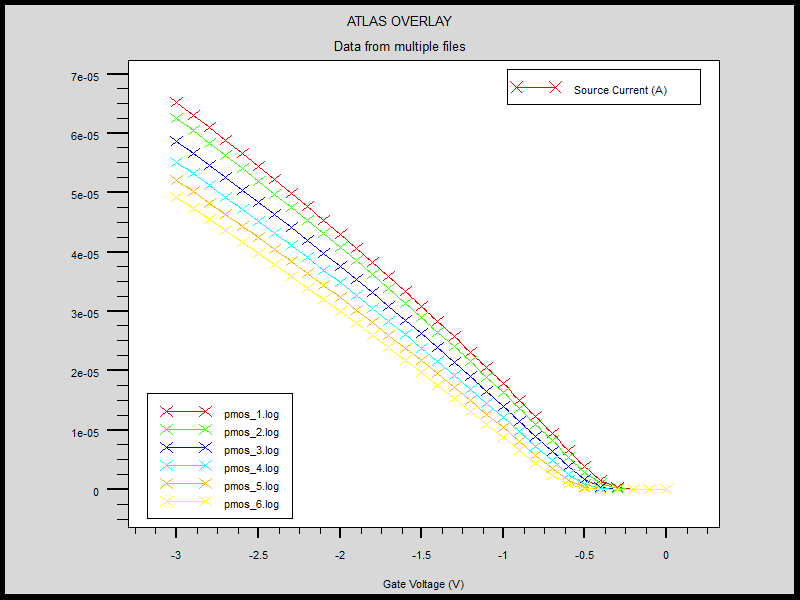
There are four main parameters under investigation for the optimization of the PMOS device:

1. Channel Doping concentration
2. Source/Drain Doping
3. LDD Doping
4. Oxide thickness

**Channel Doping:**

The Channel doping was being changed as the only optimization parameter for 6 successive runs and a family of curves was plotted to notice the changes in Vth and gm.

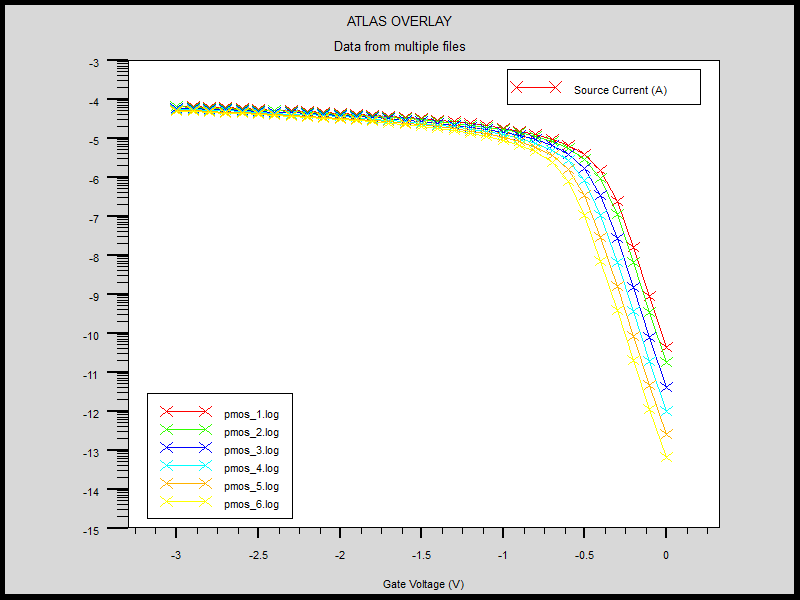
The curves plotted her are at Vds=0.1V. This change was done during the Vth adjustment step by varying the dose form 1.0e11 cm-2 to 1.25e12 cm-2 in steps of 2.5e11cm-2.



Fig(5) IS/VGS for different channel concentrations

It can be seen from the previous plot we can have lower Vth and a slightly better gm at the same time with lower channel doping. The table below shows that the threshold voltage changes dramatically.

But as seen from the plot the gm increases only slightly when channel doping is decreased. Another important limiting factor is the off current which varies over 3 orders of magnitude. We conclude that the value of plot(3) which gives Vth=0.4 is the most suitable one as a compromise between low Vth, High gm and low off current <10 pA.



Fig(6) log plot of IS/VGS for different channel concentrations

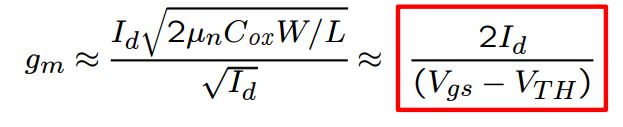
|  |  |  |
| --- | --- | --- |
| **Channel Concentration(cm-3)** | **Vth (V)** | **gm(uS/um)** |
| **9.88e17** | 0.55 | 211 |
| **8.54e17** | 0.50 | 216 |
| **7.20e17** | 0.45 | 220 |
| **5.86e17** | 0.41 | 226 |
| **3.52e17** | 0.34 | 233 |
| **3.71e17** | 0.31 | 237 |

The Governing physical equation which explains the previous effect is:

vth.JPG

As the channel doping increases the magnitude of Vth increases as well.

Fig(7) table of Vth and gm with varying Channel conc.



The equation above shows that for a given overdrive voltage the transconductance parameter is proportional to the drain current. This is consistent with the simulated data because the [Id α (Vgs-Vth)^x] . I choose here x not 2 because in short channels the relation may not be perfectly quadratic. In total the gm will be proportional to the same factor with power (x-1) which is equal to 1 in longer channels. This explains the weak dependence. The equations above will be very important in next optimizations.

**Source/Drain Doping:**

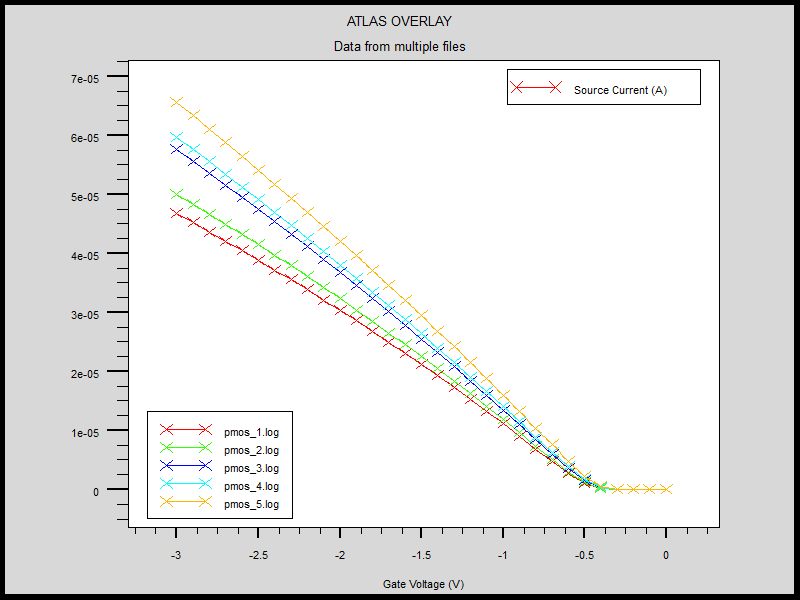
Theortically the source/drain doping should have no effect on the Vth but we expect some changes because the regions penetrate for some distance under the gate.

The dose of source/drain implant was ramped from 5e14 cm-2 to 5e16 cm-2 by increasing the value half an order of magnitude each time.

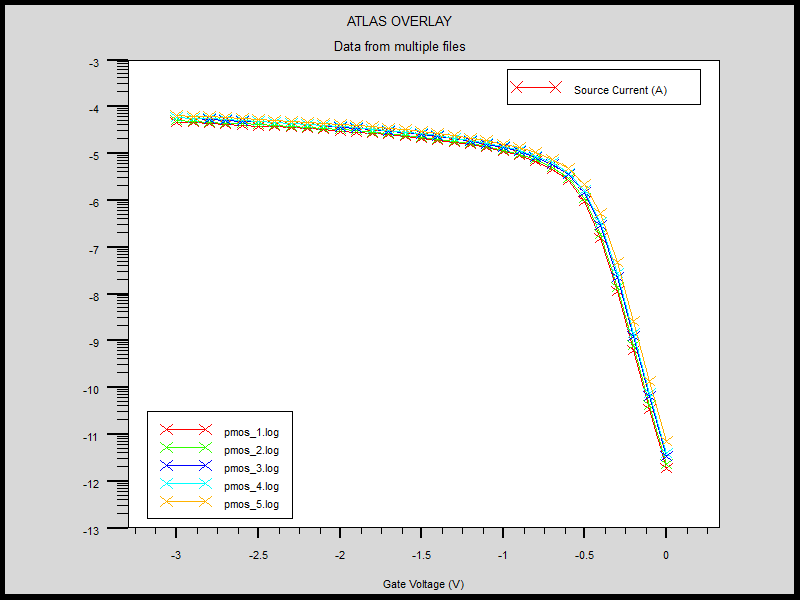
The results show that the Vth has a very weak dependence on the doping. Which shows that the channel is well isolated from the implants, while gm increases as the doping of source/drain increases. The values start from 188 uS/um for lowest dose up to 246 uS/um for the maximum dose but on the other hand the off current changes from 10^-12 to 10^-11 so the optimum point is the current used dose of 5e15.

The dependence of gm on source/drain doping is expected as both heavily doped regions act as reservoirs of charges for minority carriers that makes the inversion layer and pass through the channel. Having higher concentration means the ability to drive higher currents for smaller voltages and higher gm. This is probably not obvious in the equation because the simple model treats drain/source as infinite reservoirs that have no effect on the process itself.

The next page shows figures for the plots in linear and log scale.



Fig(8) Is/Vgs after varying source /drain

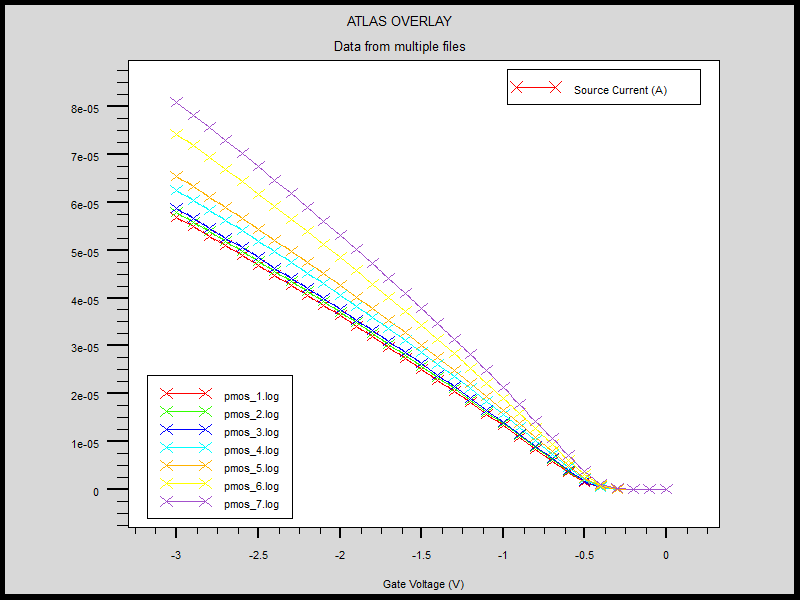


Fig(9) log( Is) /Vgs after varying source /drain

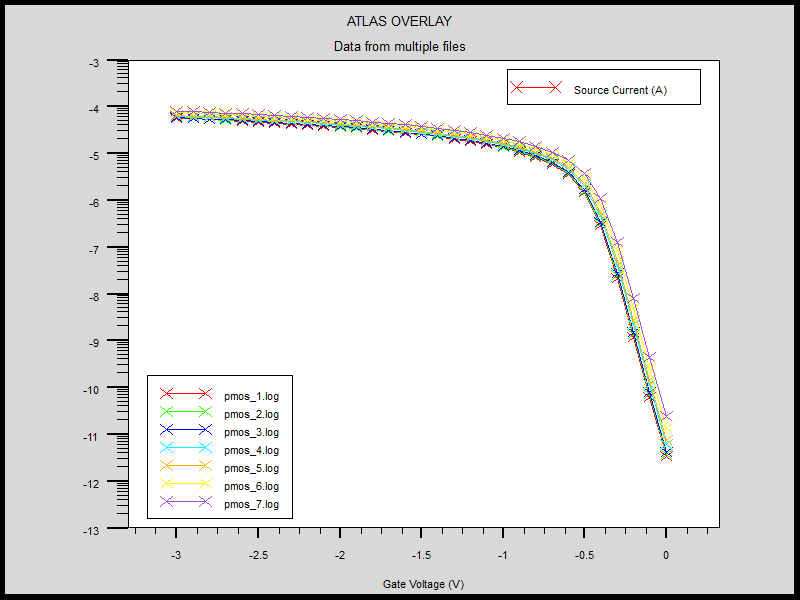
**LDD DOPING:**

The LDD is mainly placed to decrease the value of the electric field inside the channel to avoid hot electron effects and to decrease leakage current through the oxide. Theoretically the LDD should have very little effect on the Vth while it will degrade the gm.

The LDD dose was ramped from 1e13 to 1e15 in steps of half order of magnitude each time. The Vth extraction showed a decrease in Vth by about 0.01-0.02 V for each step starting from 4.2V down to 3.6V. This is expected because the boron decreases the n-type channel concentration and decreases Vth slightly. On the other hand, gm is deeply affected by the LDD change as increasing the doping directly improves gm for the reasons mentioned above But the off current falls by almost an order of magnitude from 4e-11 to 5e-10 so moderate LDD dose of 1e13 is chosen.



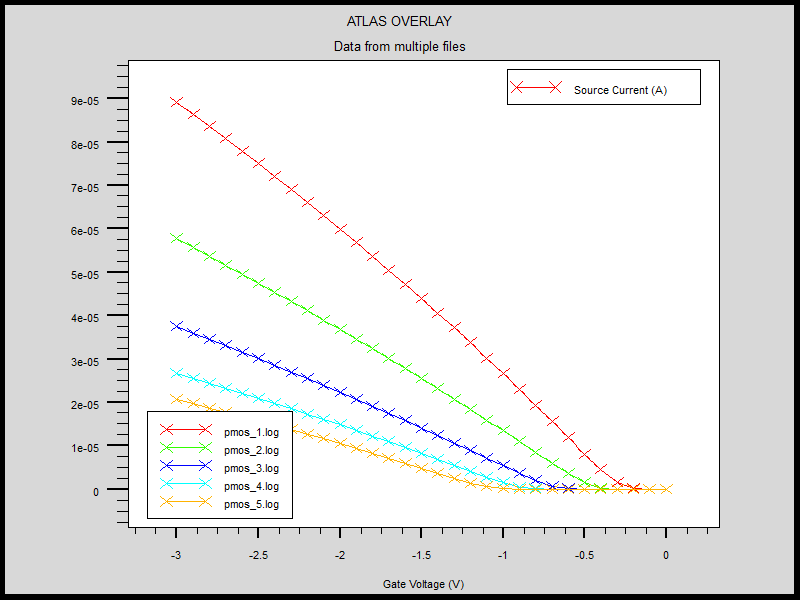
Fig(10). Is/Vgs with changing LDDdoping



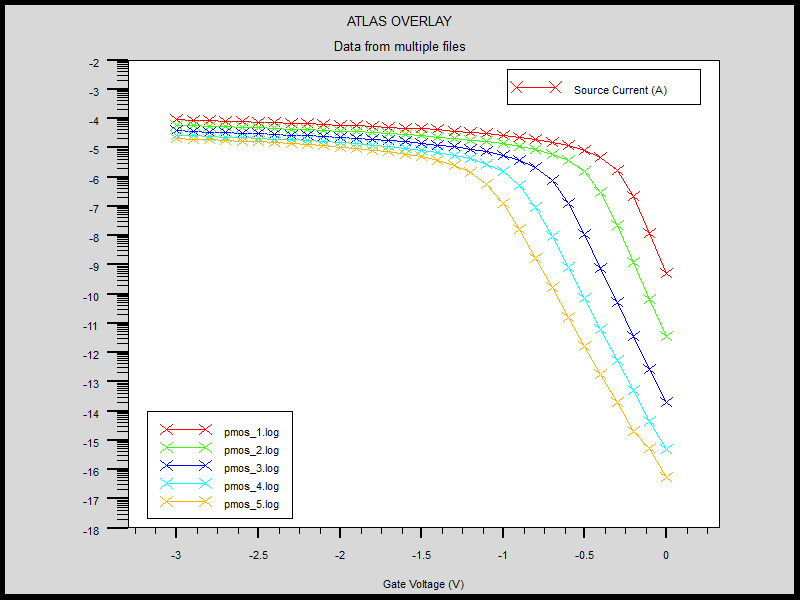
Fig(11).log( Is)/Vgs with changing LDDdoping

**Gate Oxide:**

The Gate oxide is considered one of the most important parameters in any mosfet. The target is always to decrease the oxide as possible to get lower Vth and better control on the gate barrier but this can cause several problems including leakage current and the failure of transistor action itself. The gate oxide targeted was 4.2 nm and this was achieved by dry oxidation for 4 minutes. We tried to vary the thickness by growing for 1,4,8,12,16 minutes to find the optimum value for the gate oxide. It is clear from the plot that the threshold voltage depends highly on oxide thickness, this is because as tox increases it decreases Cox which in turn increases the magnitude Vth. gm increases slightly as vth decreases for the reasons mentioned before. Finally, The off current also depends heavily on the oxide thickness starting from 10e-9 downto 10e-17. Again the optimum value for the oxide chosen is 4.2 nm achieved with growth of 4 minutes. This choice gives low Vth , high gm and acceptable leakage current.



Fig(12) Is/Vgs plots with changing oxide thickness



Fig(12) log(Is)/Vgs plots with changing oxide thickness

**Process Parameters:**

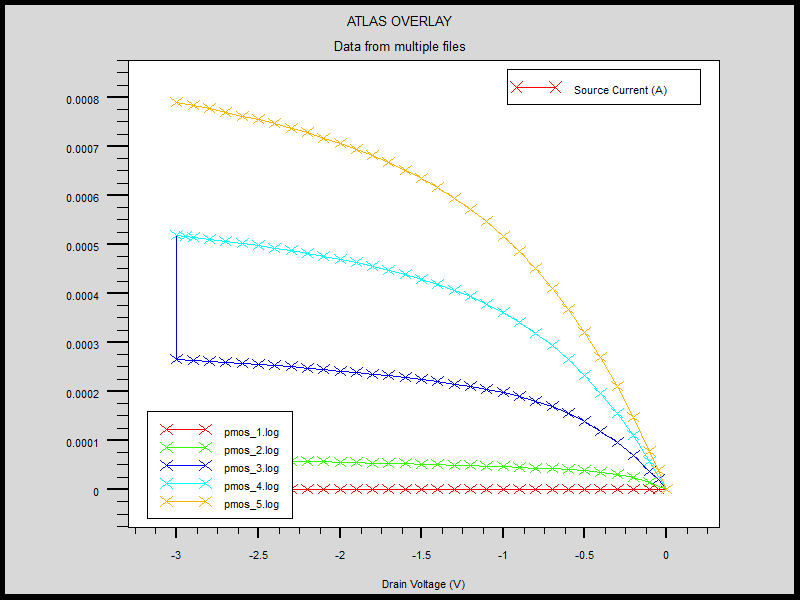
|  |  |
| --- | --- |
| Gate Oxide | time=4 temp=900 dryo2 press=1.00 hcl=3 |
| N-Well Doping | Phosphorus(amorphous) dose=1.0e13 energy=100 pearson |
| LDD | bf2 dose=1.0e13 energy=10 pearson |
| Source/drain Doping | bf2 dose=5.0e15 energy=12 pearson |
| Channel Doping | phosphorus dose=5.0e11 energy=8.0 pearson |

**Optimized Device:**

The targeted intial template proved to be the optimum point between the desired values of gm, Vth without having high leakage current. The plots in the first pages can be referred to.

The output characteristics of the device are plotted:

They show the expected behavior of a well-tempered MOSFET.



Fig(14) Is/Vds plots of optimized transistor

**PMOS Code:**

**Process:**

go athena

#

# Set up a mesh suitable for a single MOSFET device....

#

line x loc=0.0 spac=0.1

line x loc=0.1 spac=0.006

line x loc=0.21 spac=0.006

line x loc=0.3 spac=0.01

#

line y loc=0.0 spac=0.002

line y loc=0.063 spac=0.002

line y loc=0.1 spac=0.005

line y loc=0.6 spac=0.015

#

# Start off by defining silicon with 1e14 phos doping...

init orientation=100 c.phos=1e13 space.mult=2

#

diffus time=30 temp=1000 dryo2 press=1.00 hcl=3

#

etch oxide thick=0.02

#

#N-well Implant

implant amorphous phos dose=1.0e13 energy=100 pears

#

diffus temp=950 time=100 weto2 hcl=3

# welldrive

diffus time=220 temp=1200 nitro press=1

#

etch oxide all

#

#sacrificial "cleaning" oxide

diffus time=20 temp=1000 dryo2 press=1 hcl=3

#

etch oxide all

#

#gate oxide grown here:-

diffus time=4 temp=900 dryo2 press=1.00 hcl=3

#

# Extract a design parameter.....

extract name="gateox" thickness oxide mat.occno=1 x.val=0.05

#

#vt adjust implant amorphous

implant phos dose=5.0e11 energy=8.0 pearson

depo poly thick=0.1 divi=10

#

#from now on the situation is 2-D

#

etch poly left p1.x=0.21

#

method fermi compress

diffuse time=1 temp=900 weto2 press=1.0

#

# PLDD implant amorphous

implant amorphous bf2 dose=1.0e13 energy=10 pearson

#

# spacer

depo oxide thick=0.030 divisions=8

#

etch oxide dry thick=0.030

#

# P++ Implant

implant bf2 dose=5.0e15 energy=12 pearson

# Final anneal.

method fermi compress

diffuse time=1 temp=900 nitro press=1.0

#

# pattern s/d contact metal

etch oxide left p1.x=0.14

deposit alumin thick=0.015 divi=2

etch alumin right p1.x=0.12

# mirror the structure.....

structure mirror right

# extract the surface conc under the channel....

extract name="pchan surf conc" surf.conc impurity="Net Doping" material="Silicon" mat.occno=1 x.val=0.45

# extract final S/D Xj...

extract name="pxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1

# Extract a design parameter.....

extract name="gateox" thickness oxide mat.occno=1 x.val=0.005

# Name the electrodes...

electrode name=gate x=0.3 y=0.1

electrode name=source x=0.1

electrode name=drain x=0.5

electrode name=substrate backside

# output the structure

structure outfile=pmos\_0.str

# plot it

#tonyplot pmos\_0.str

############# PVt Test : Returns PVt, PBeta and PTheta ################

go atlas

# set material models

models cvt srh print

contact name=gate p.poly

interface qf=3e10

method newton

solve init

# Bias the drain a bit...

solve vdrain=-0.1

# Ramp the gate

log outf=pmos\_1.log master

solve vgate=0 vstep=-0.1 vfinal=-3.0 vdrain=-0.1 name=gate

save outf=pmos\_0.str

# extract device parameters......

tonyplot pmos\_1.log

quit

**Extraction:**

go atlas

# extract device parameters

extract init inf="pmos\_1.log"

extract name="pvt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) - abs(ave(v."drain"))/2.0)

extract name="dydx" max(deriv(v."gate", i."drain")) outfile="dydx.dat"

quit