Rapport LABO éléments mémoire

Description d'éléments mémoire en VHDL

HEIG-VD

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CSN

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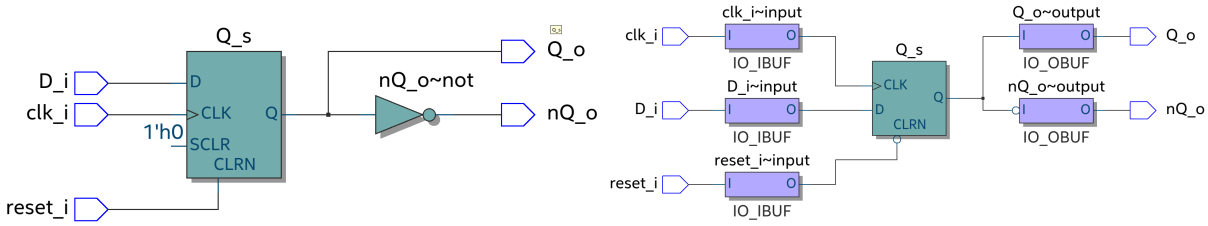
Etape 1 DFF_AR:

Vue RTL et Technology:



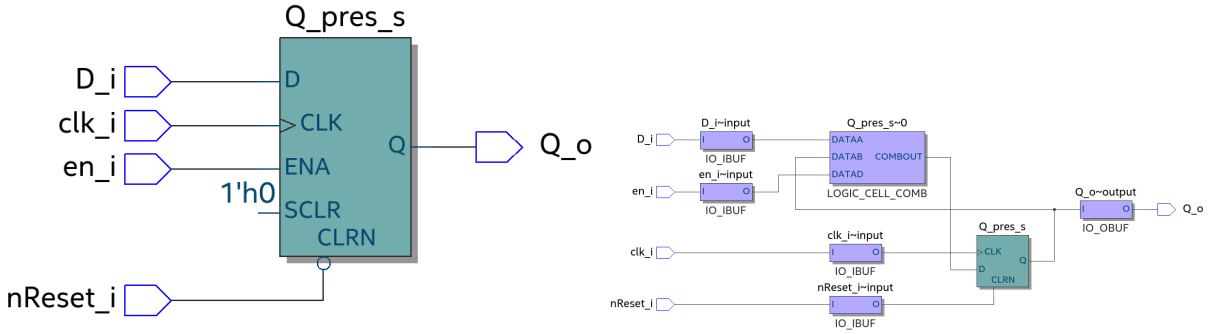
Logs de la simulation:

```
# vsim -voptargs=""+acc"" work.dff_ar_tb
# Start time: 14:52:15 on Apr 12,2023
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.dff_ar_tb(test_bench)#1
# Loading work.dff_ar(comport)#1
VSIM 2> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /dff_ar_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 552 ns  Iteration: 0  Instance: /dff_ar_tb
# ** Note: >>Fin de la simulation
#    Time: 552 ns  Iteration: 0  Instance: /dff_ar_tb
```

Le chargement des composants et la simulation automatique se sont déroulé sans erreur.

Etape 2 DFF_EN:

Vue RTL et Technology:



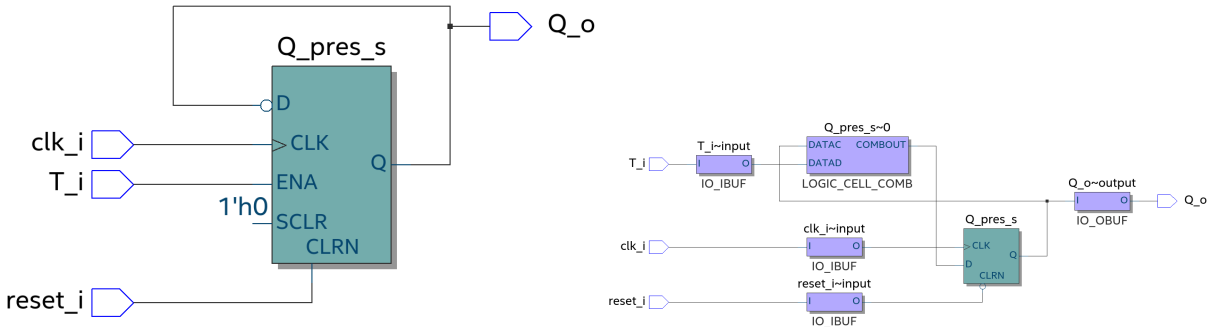
Logs de la simulation:

```
# vsim -voptargs=""+acc"" work.dff_en_tb
# Start time: 22:06:09 on Apr 11,2023
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.dff_en_tb(test_bench)#1
# Loading work.dff_en(comport)#1
VSIM 4> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /dff_en_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 652 ns  Iteration: 0  Instance: /dff_en_tb
# ** Note: >>Fin de la simulation
#    Time: 652 ns  Iteration: 0  Instance: /dff_en_tb
```

Le chargement des composants et la simulation automatique se sont déroulé sans erreur.

Etape 3 flip flop t:

Vue RTL et Technology:



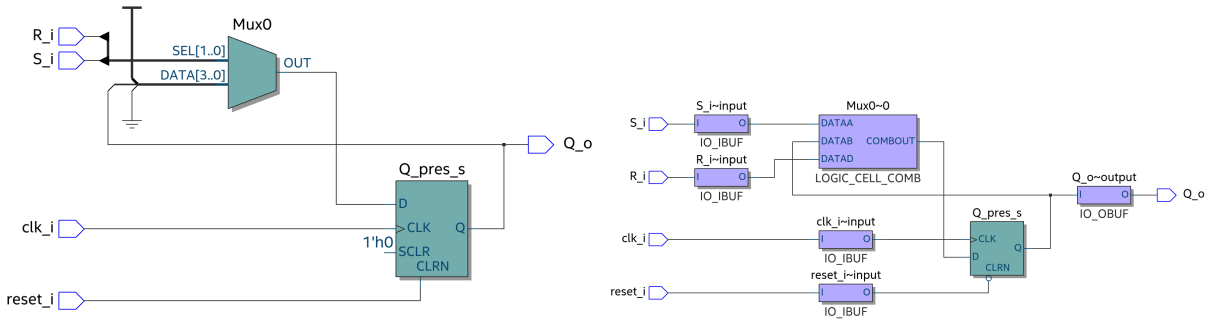
Logs de la simulation:

```
# vsim -voptargs=""+acc"" work.flipflop_t_tb
# Start time: 10:33:56 on Apr 12,2023
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.flipflop_t_tb(test_bench)#1
# Loading work.flipflop_t(comport)#1
VSIM 10> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /flipflop_t_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 652 ns  Iteration: 0  Instance: /flipflop_t_tb
# ** Note: >>Fin de la simulation
#    Time: 652 ns  Iteration: 0  Instance: /flipflop_t_tb
```

Le chargement des composants et la simulation automatique se sont déroulé sans erreur.

Etape 4 flip flop RS:

Vue RTL et Technology:



Logs de la simulation:

```
# vsim -voptargs=""+acc"" work.flipflop_rs_tb
# Start time: 14:31:06 on Apr 12,2023
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.flipflop_rs_tb(test_bench)#1
# Loading work.flipflop_rs(comport)#1
VSIM 4> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /flipflop_rs_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 1352 ns  Iteration: 0  Instance: /flipflop_rs_tb
# ** Note: >>Fin de la simulation
#    Time: 1352 ns  Iteration: 0  Instance: /flipflop_rs_tb
```

Le chargement des composants et la simulation automatique se sont déroulé sans erreur.