ENSTA ParisTech université PARIS-SACLAY

Systèmes Numériques et FPGA

Hervé Le Provost

DRF/Irfu - CEA Saclay
herve.le-provost@cea.fr

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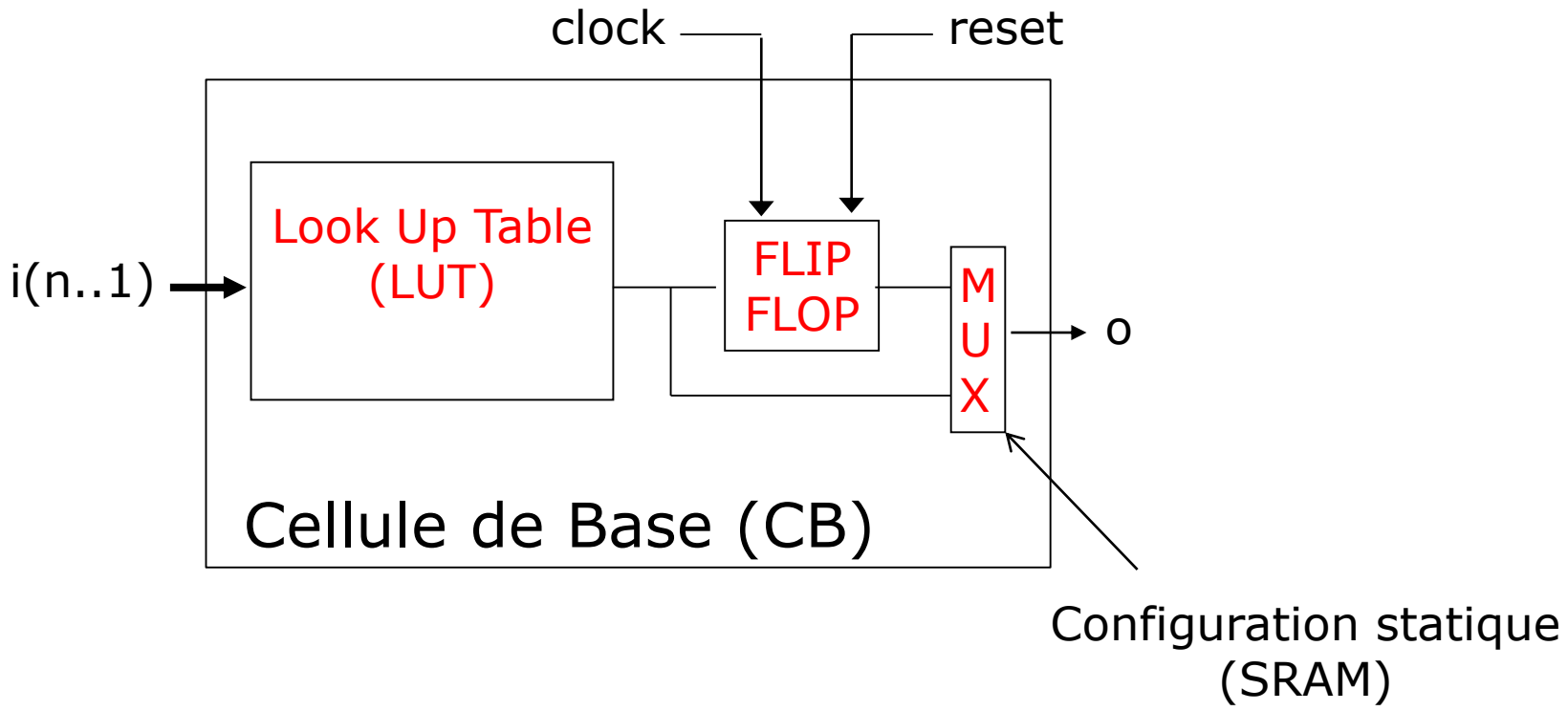
FPGA - Cellule de Base

FPGA : Field Programmable Gate Array



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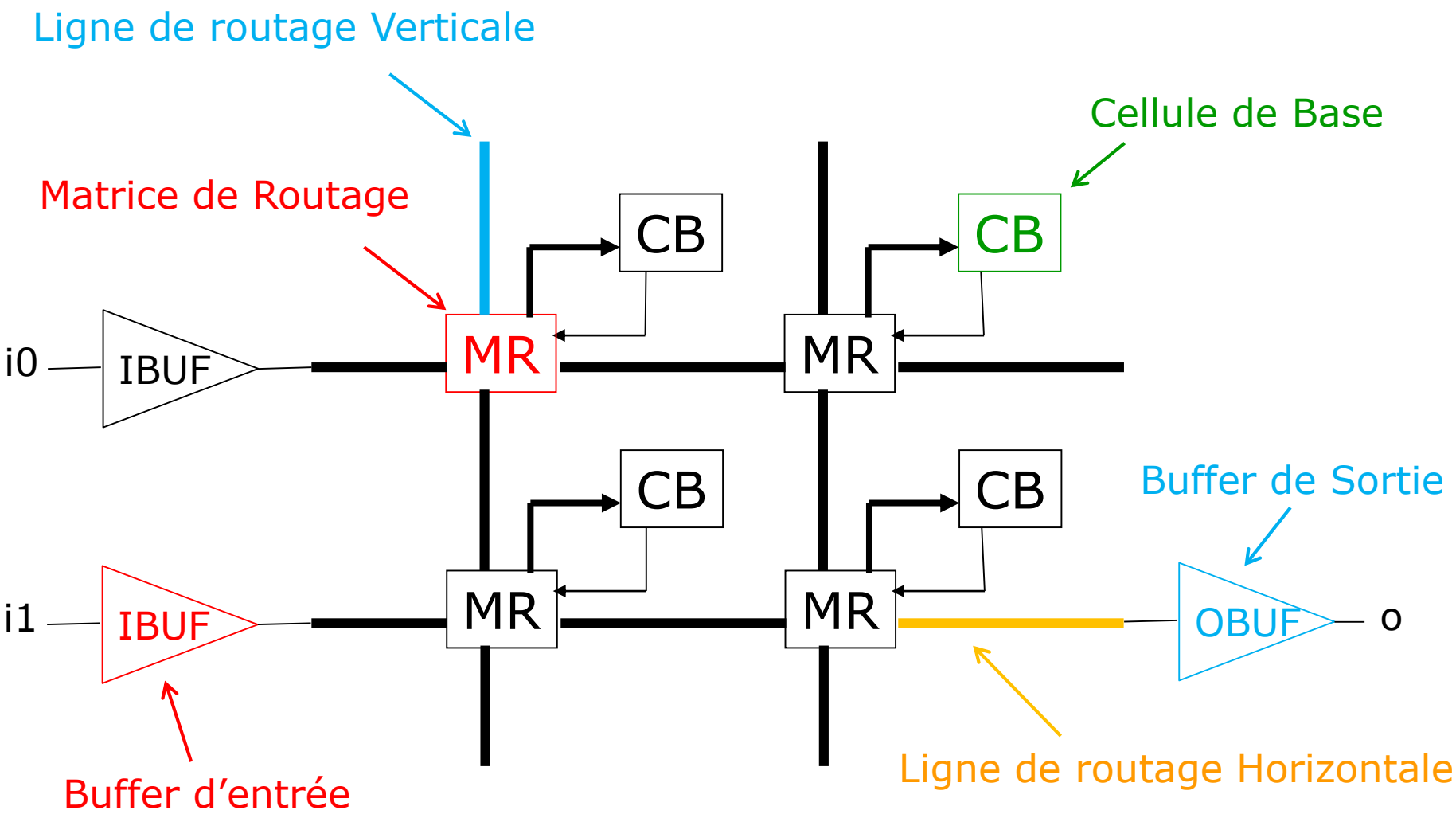
FPGA - Lego



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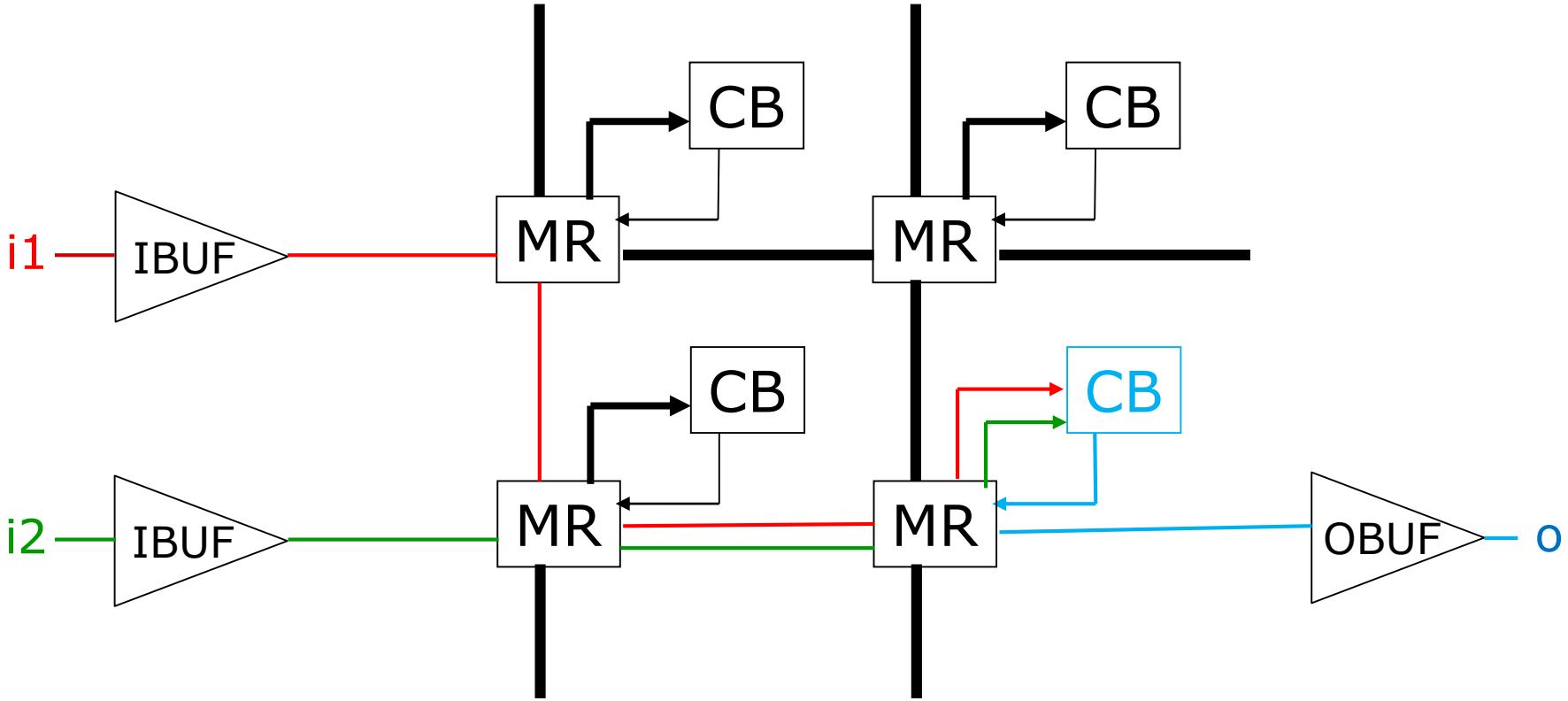
FPGA - Lego

o <= i1 and i2;



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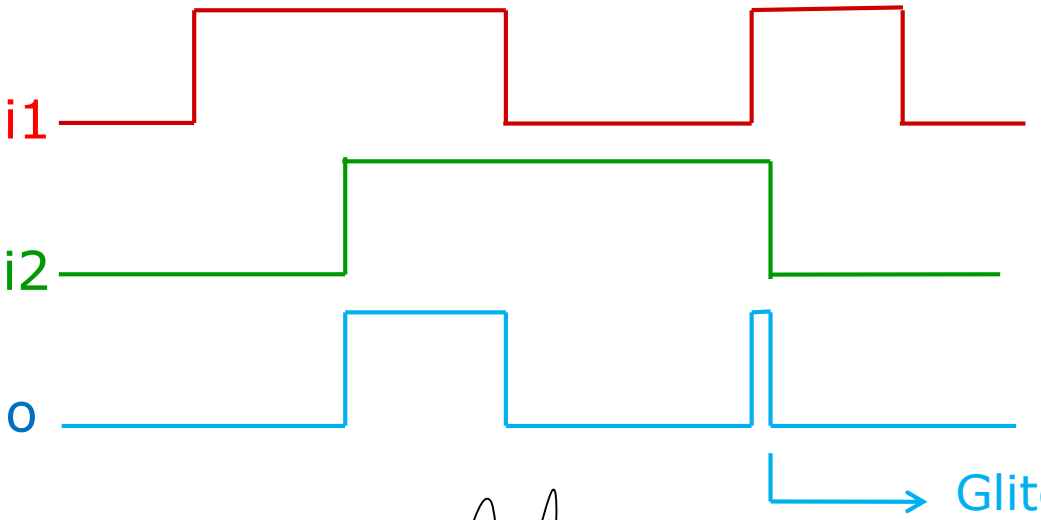
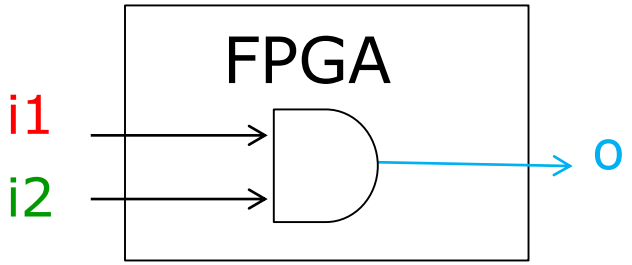
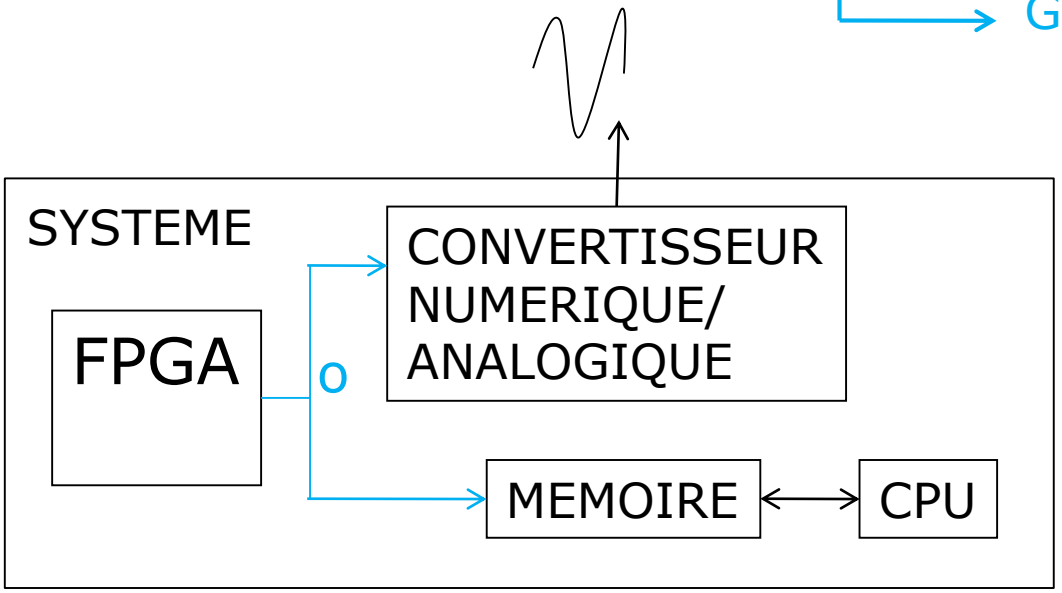
FPGA-Logique Asynchrone







Analyse au niveau système des conséquences d'un glitch :

- Ordre de conversion N/A erroné
- Ecriture mémoire erronée

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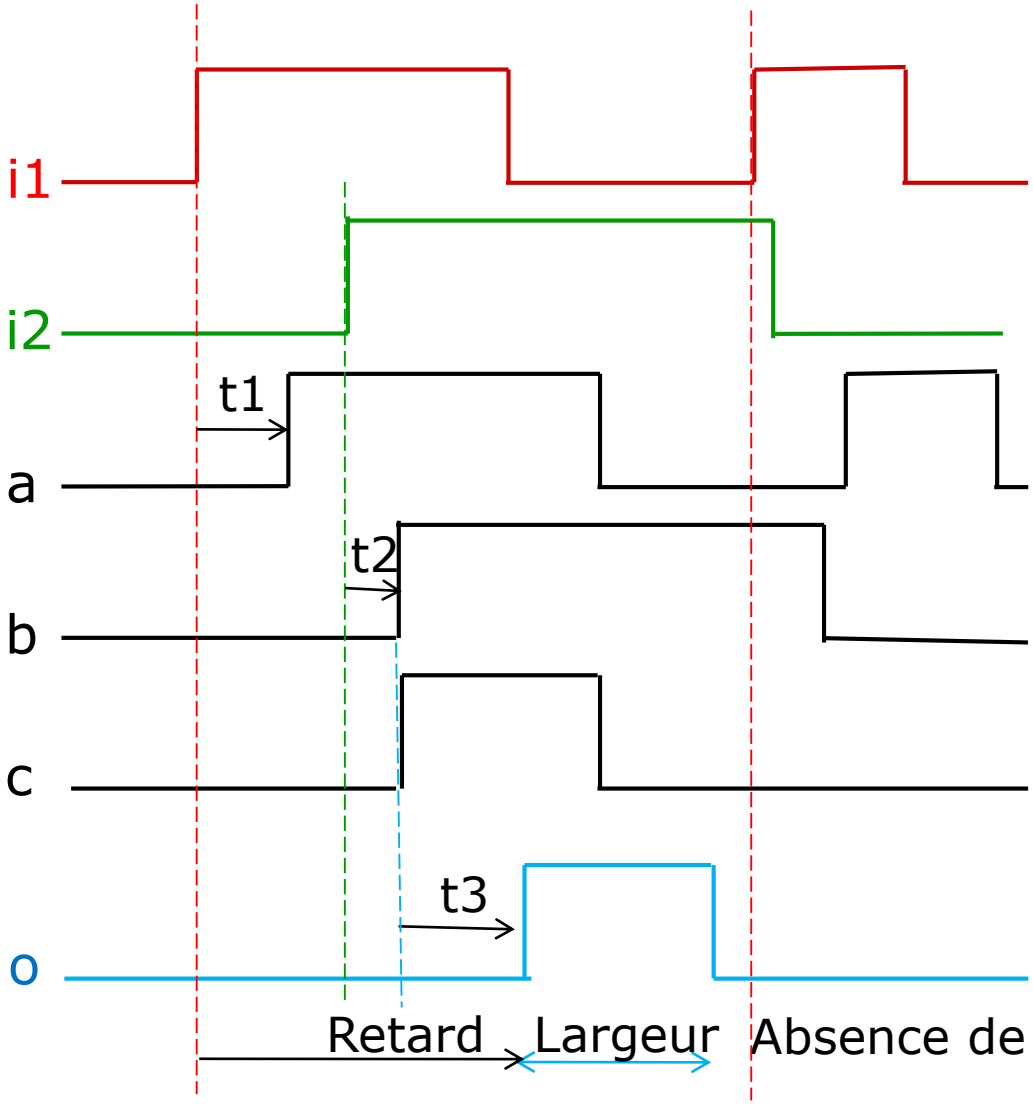
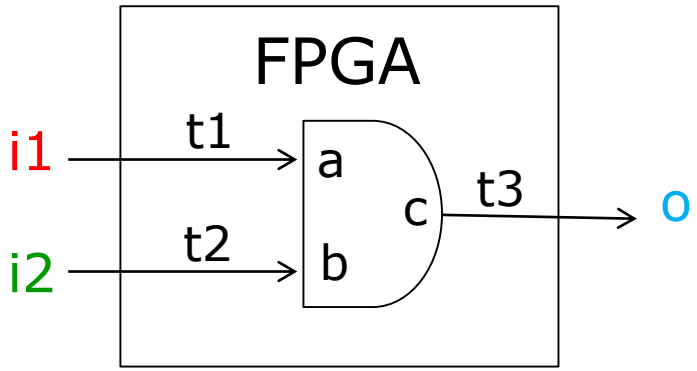
FPGA-Logique Asynchrone





Prise en compte des délais de routage

- modification fonctionnelle
- Reproductivité des délais de routage

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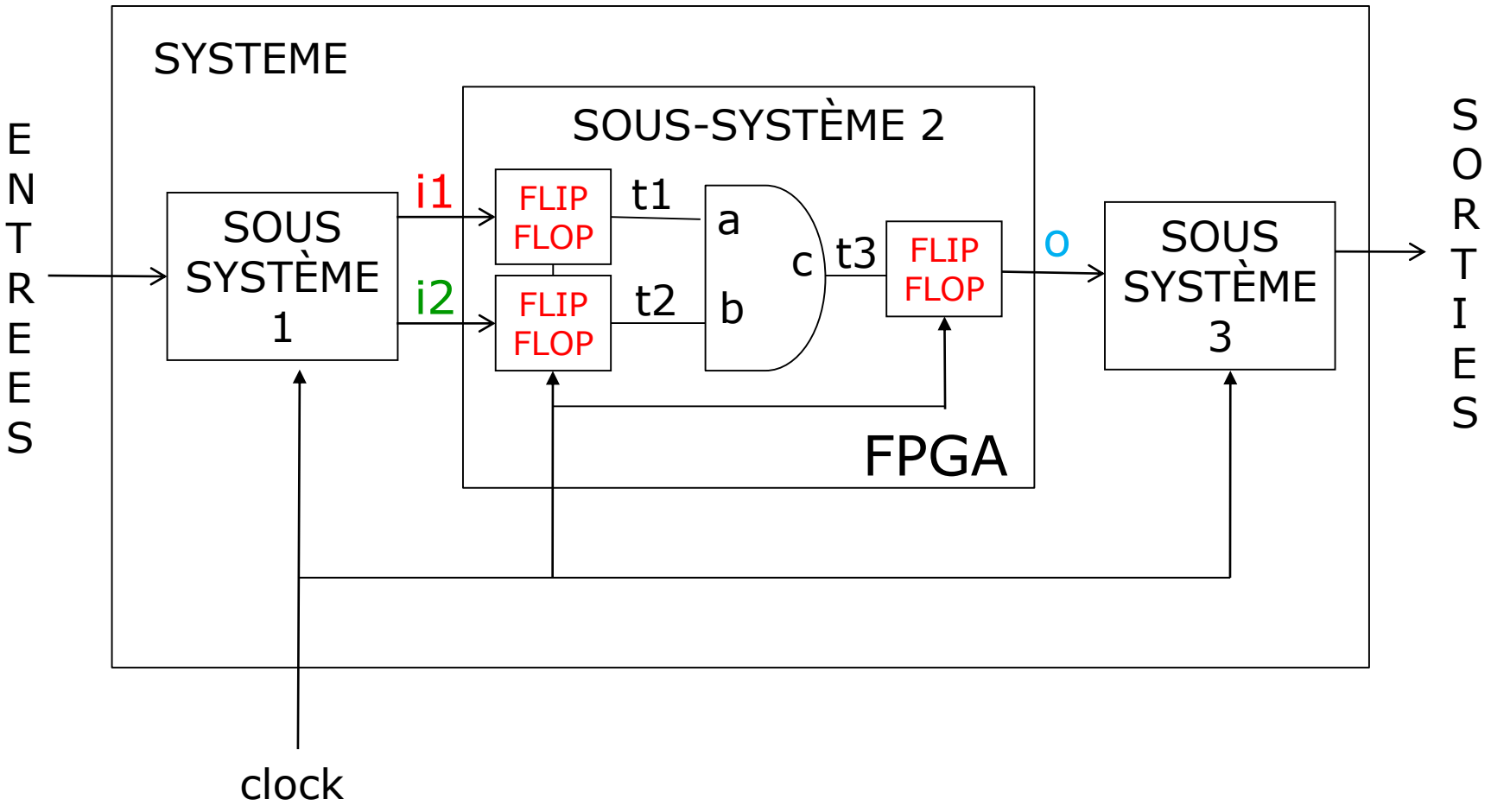
FPGA-Logique Synchrone



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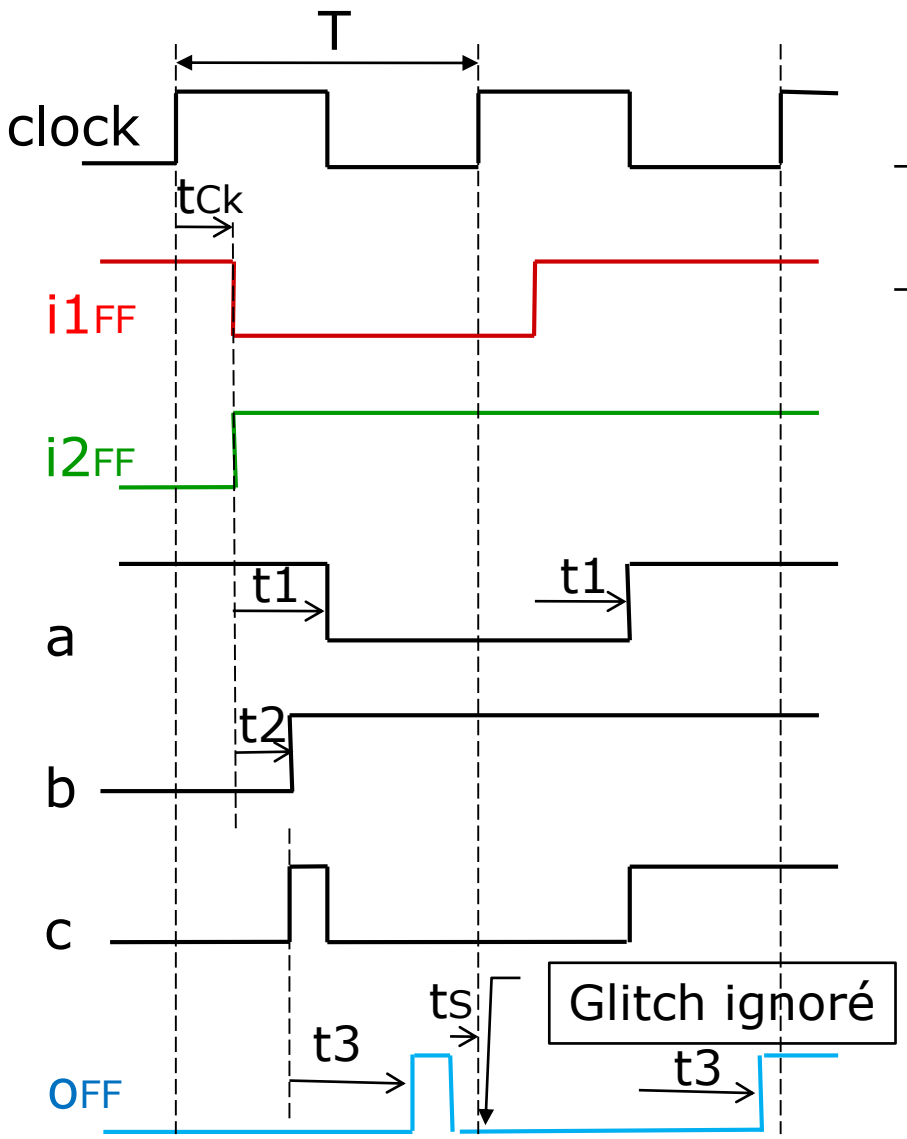
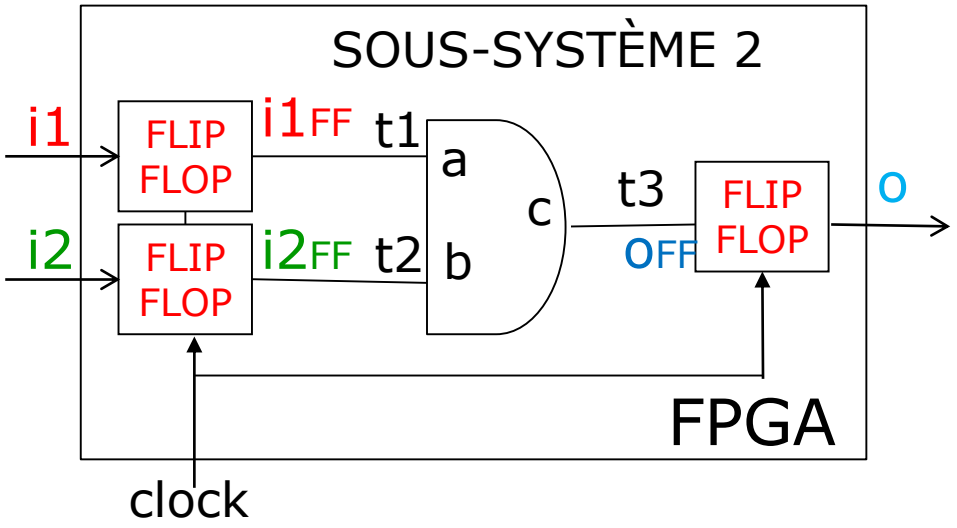
FPGA-Logique Synchrone





Période T, Fréquence F=1/T

temps de propagation

tCk: horloge vers sortie (maximum)

t1, t2, t3 : routage (maximum)

Temps de setup tS (minimum)

Fréquence maximale applicable

$F_{MAX} = 1/(t_{Ck}+t1+t2+t3+t_S)$

Comportement déterministe du système pour $F <= F_{MAX}$

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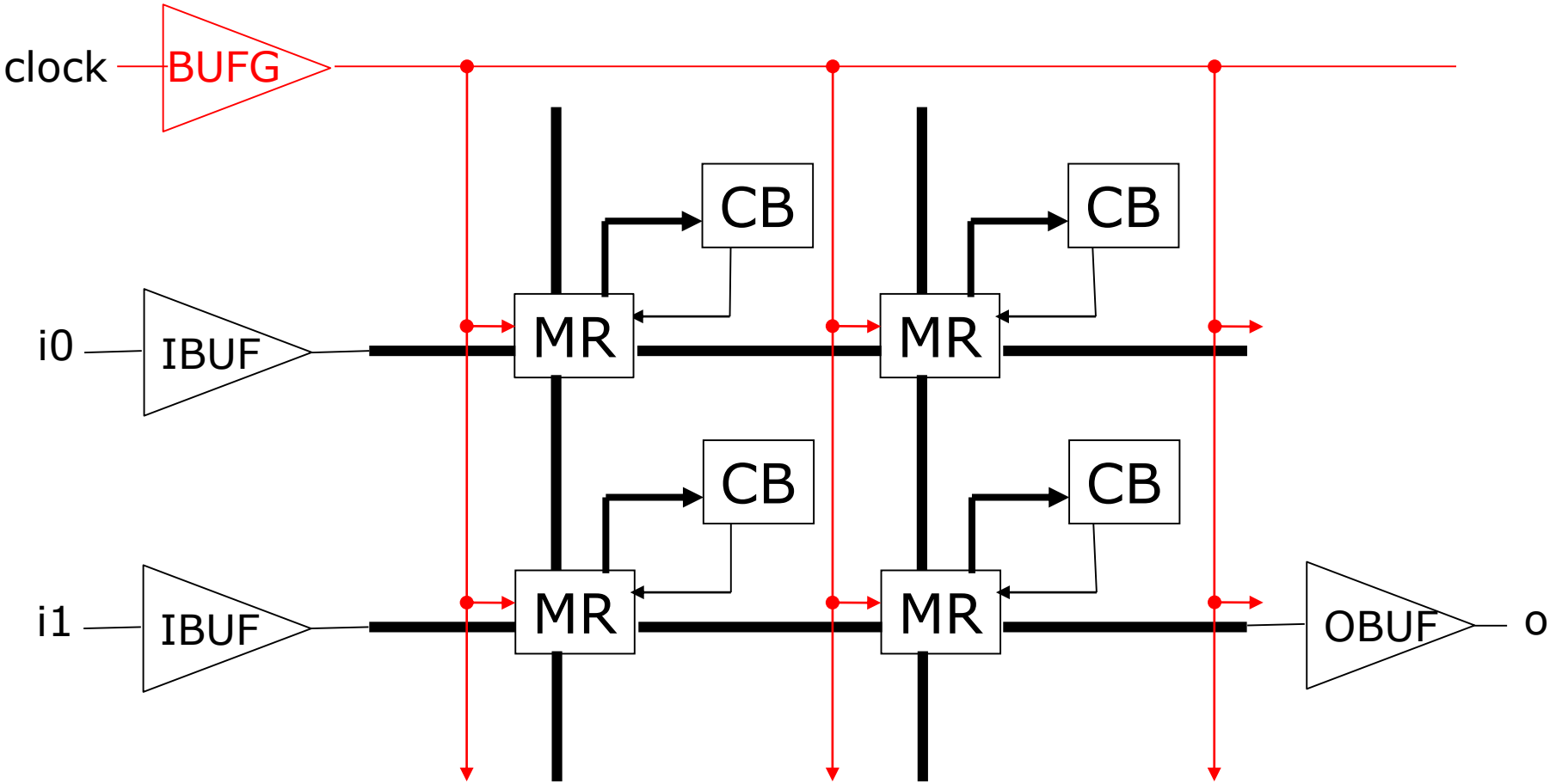
FPGA-Buffers Globaux

Distribution de l'Horloge sur des lignes dédiées–
Equilibrage de l'arbre d'horloge



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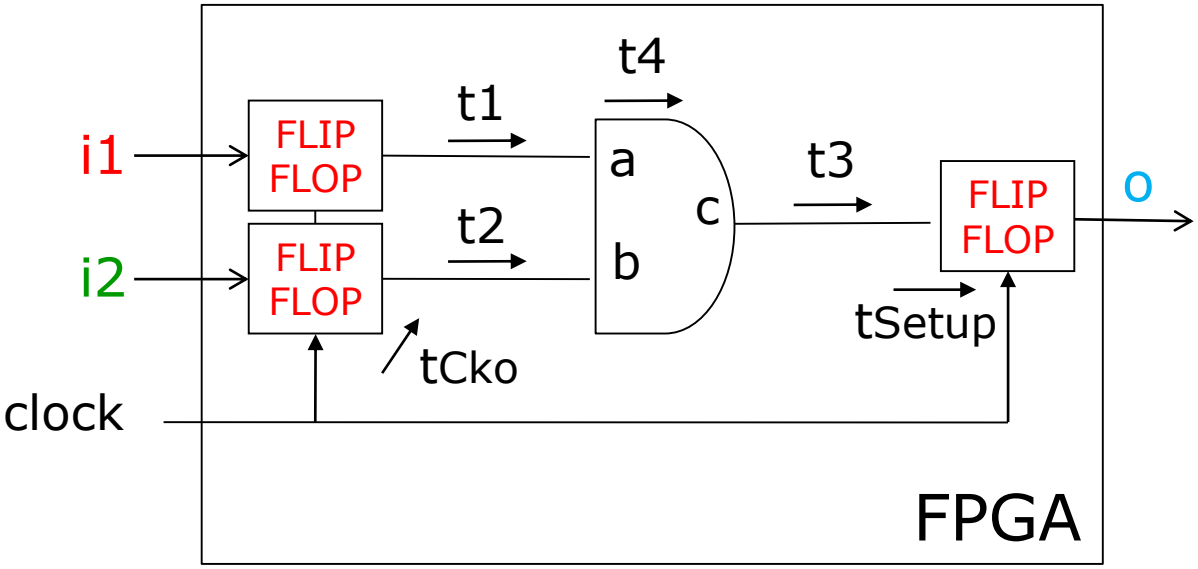
FPGA – Fréquence d'opérations

tCko=1.016 ns tSetup=0.742ns

t1=0.379 ns t3=2.491 ns

t2= 0.378 ns t4=0.643 ns

Pour l'exemple :
- les 3 FLIP-FLOP sont associés à la broche (registre IOB)
- broche 'O' physiquement opposée aux broches 'i1' et 'i2'



Fréquence Maximale ?

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FPGA – Fréquence d'opérations

$$F_{MAX} = 1/(t_{Cko} + t_1 + t_4 + t_3 + t_{Setup}) = 189.7MHz$$

calcul de F_{MAX} exact ?

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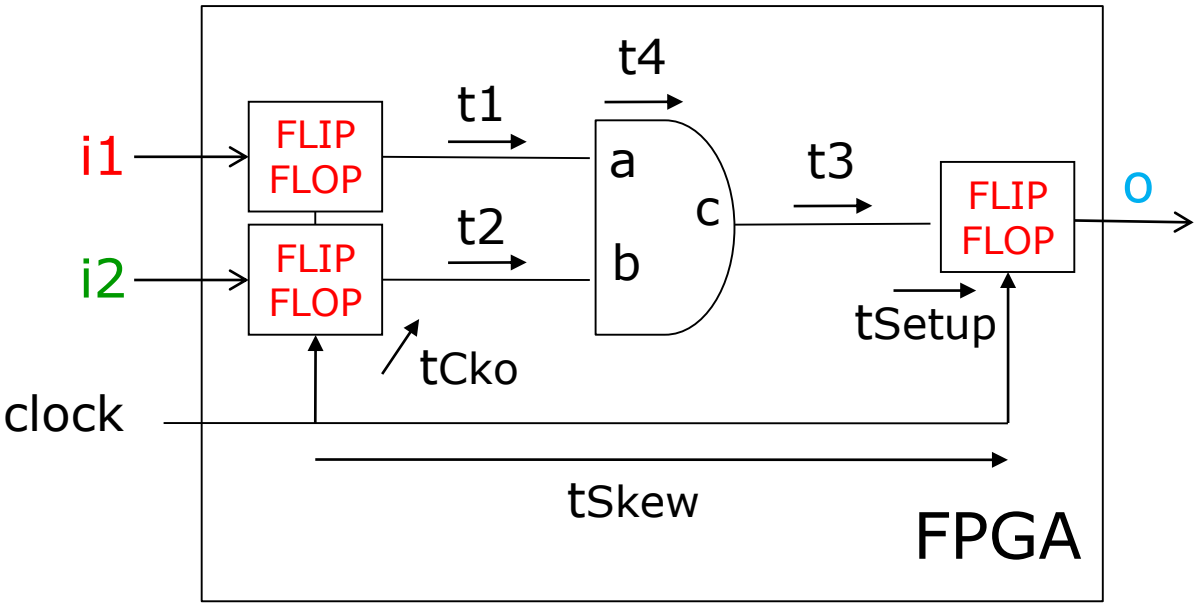
FPGA – Fréquence d'opérations

tSkew = -0.127 ns



$F_{MAX}=1/(tCko+t1+t4+t3+tSetup+tSkew)=185.2$ MHz

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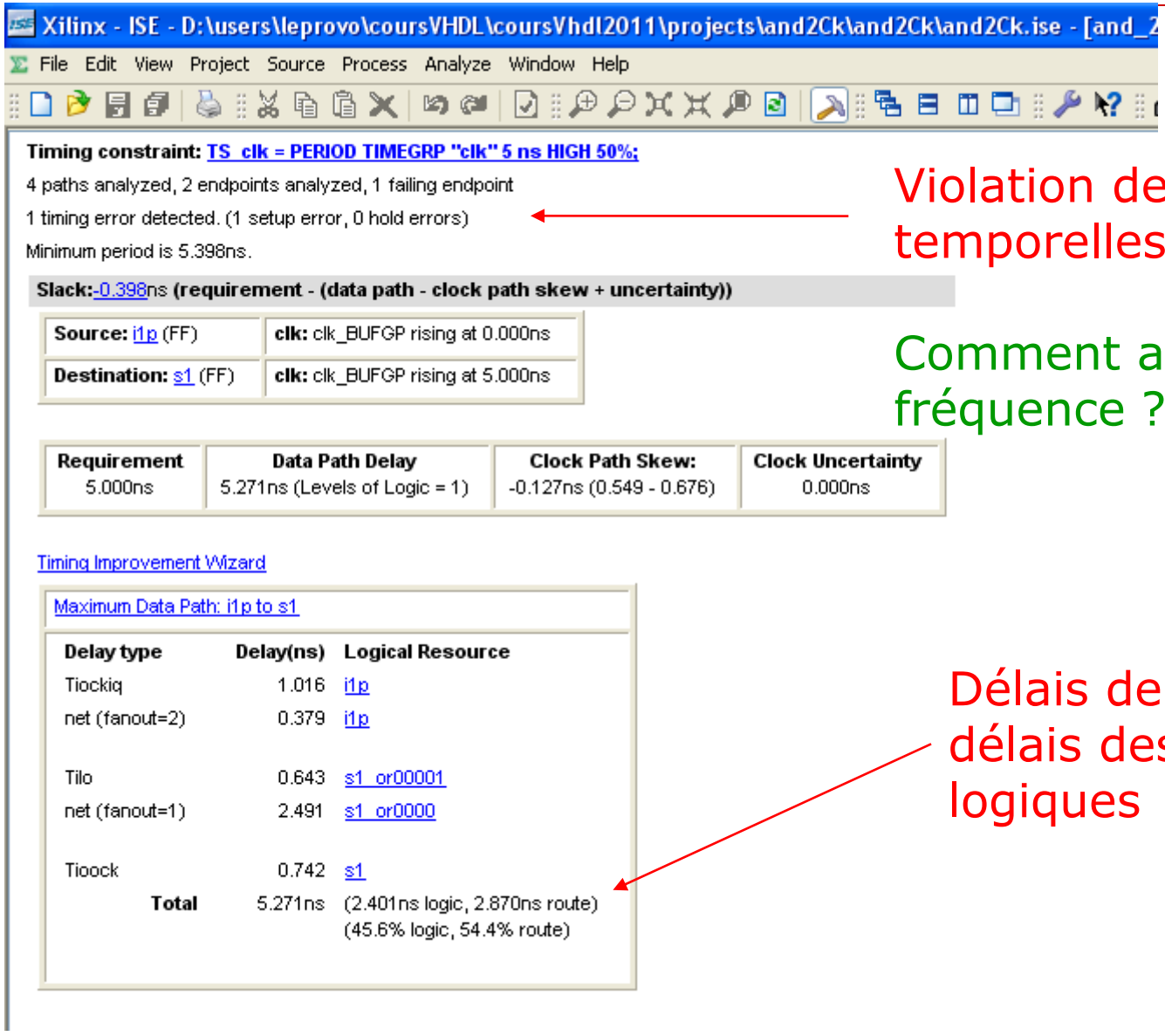
FPGA – Fréquence d'opérations



Violation des contraintes temporelles (F=200 MHz)

Comment augmenter la fréquence ?

Délais de routage vs délais des opérations logiques

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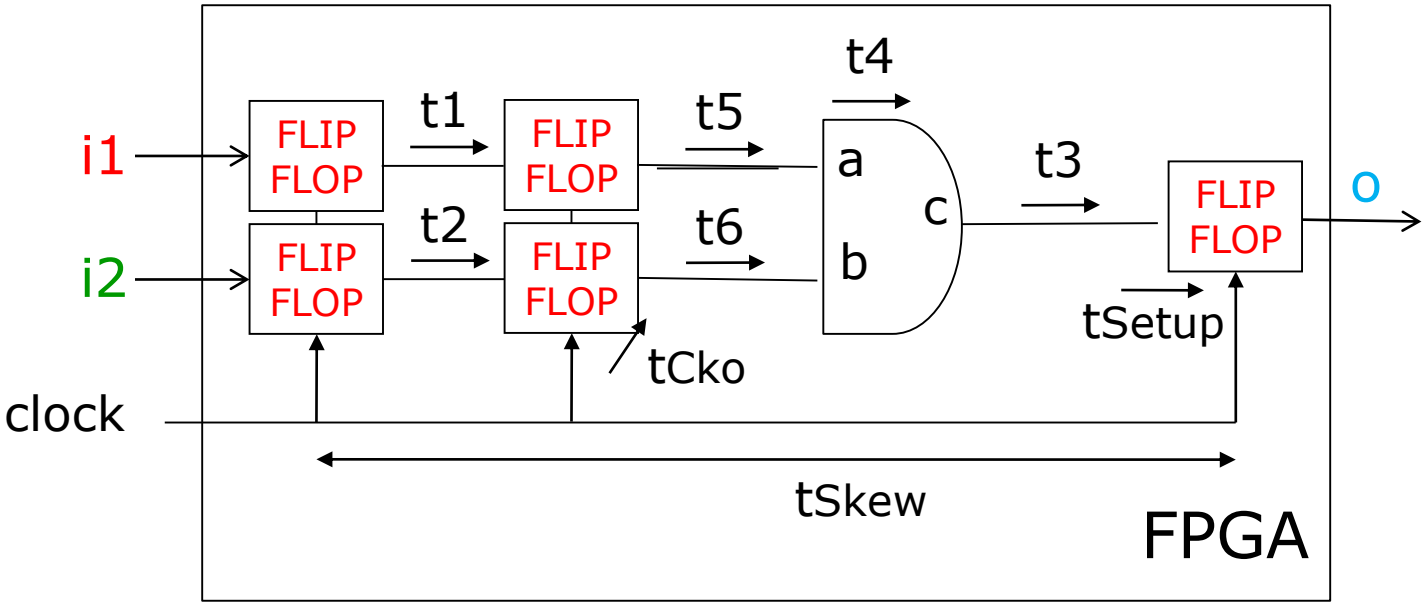
FPGA – Fréquence d'opérations



Diminution des délais de routage

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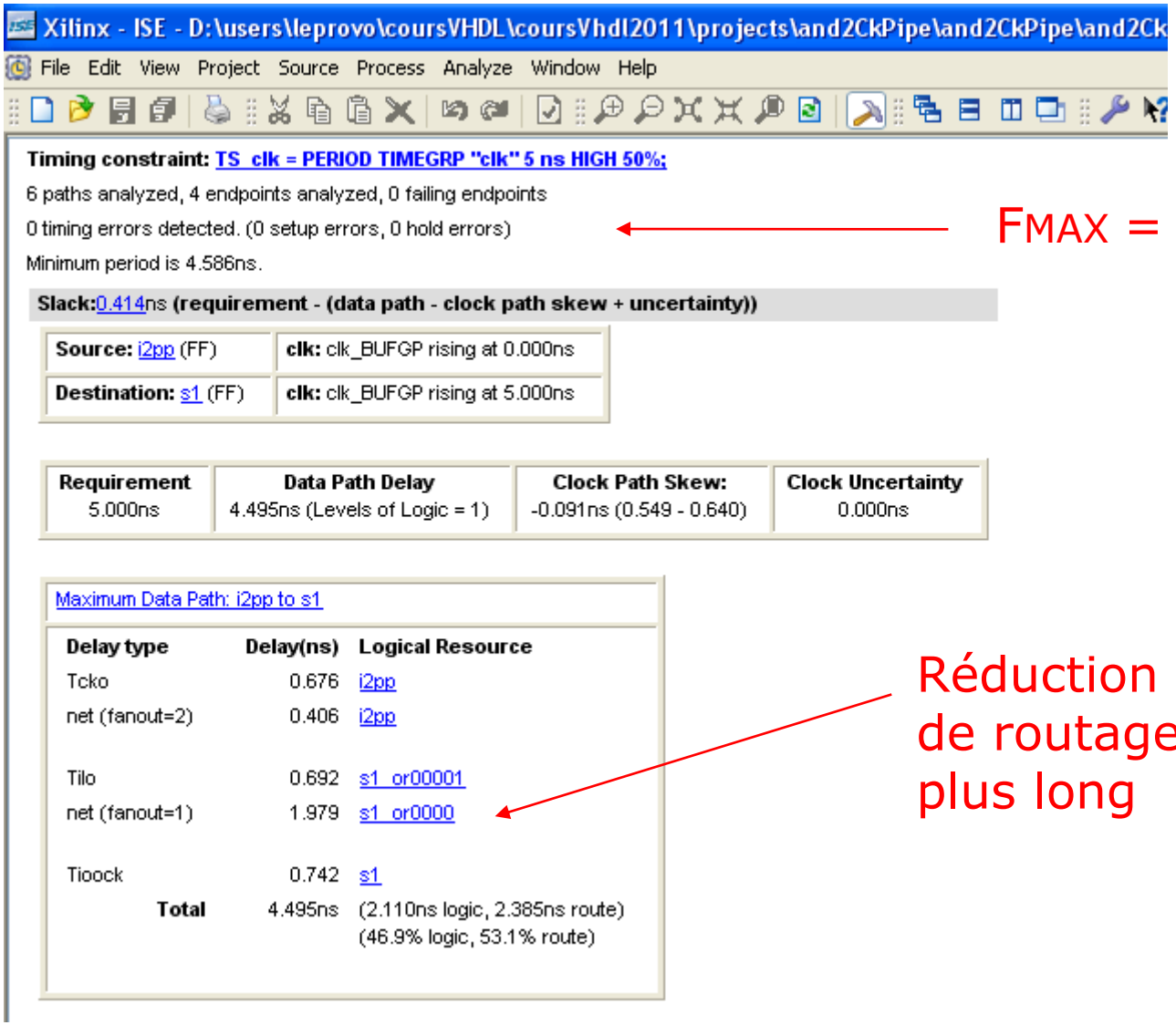
FPGA – Fréquence d'opérations



FMAX = 218 MHz

Réduction du délai de routage du fil le plus long

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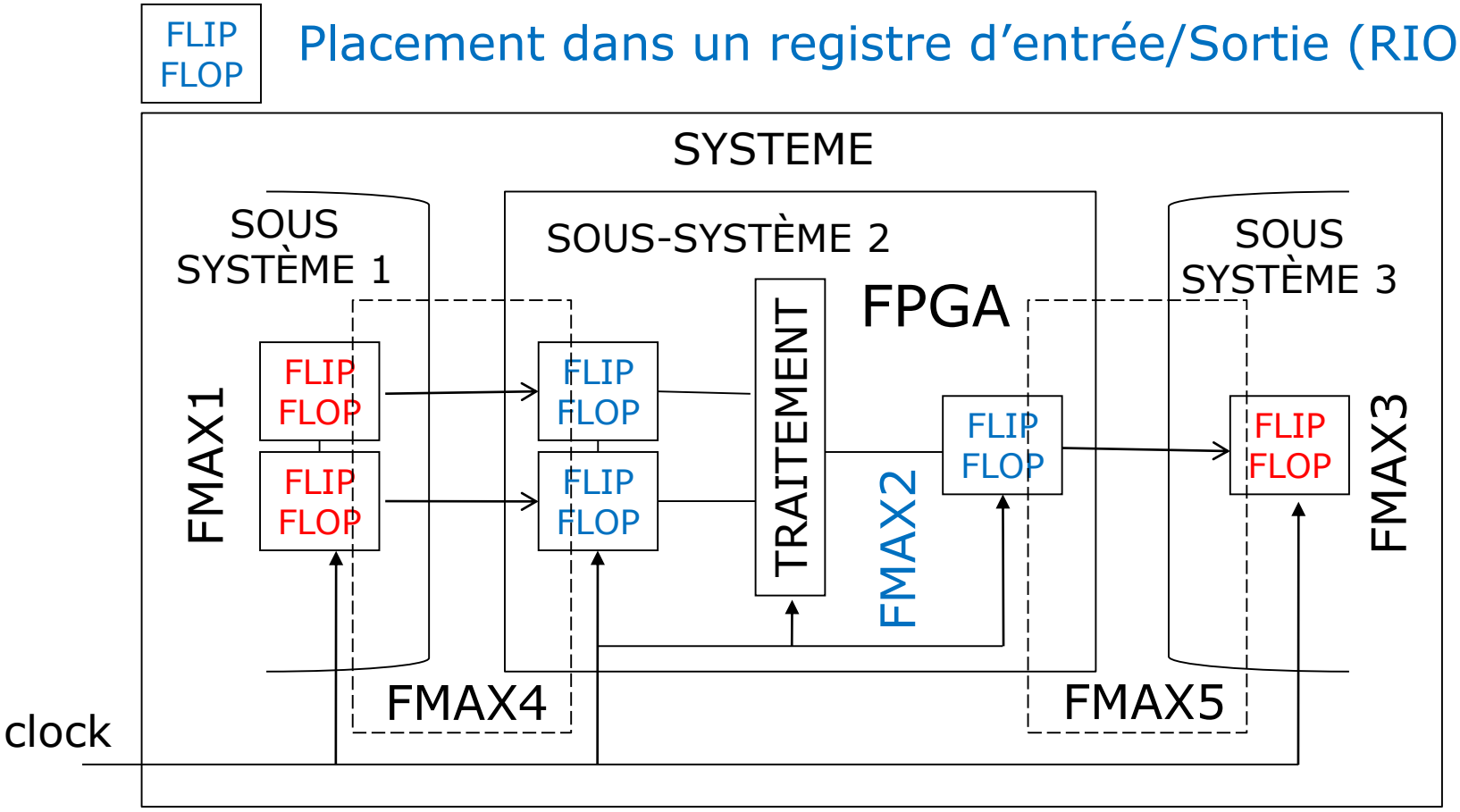
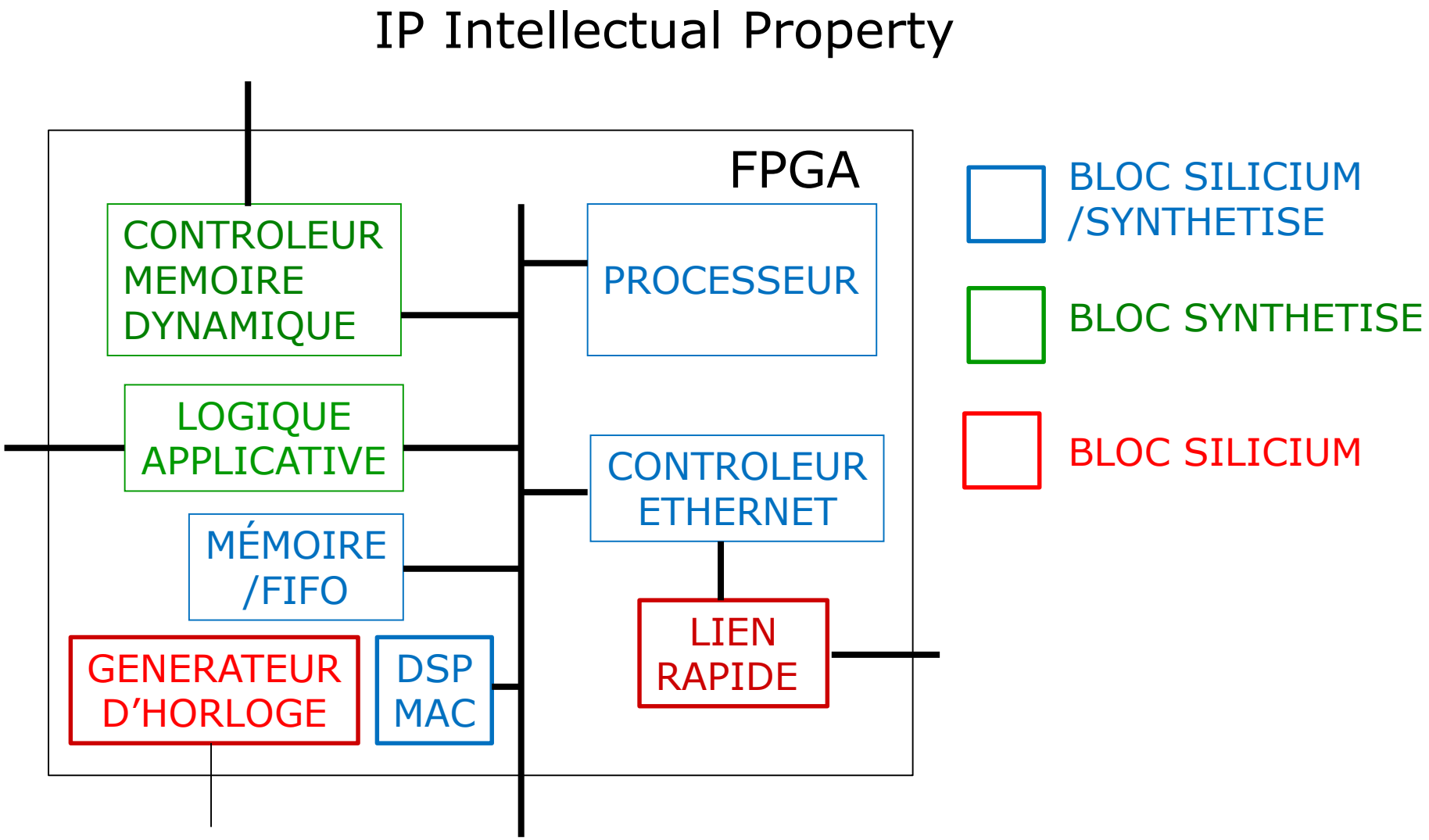
FPGA – Fréquence d'opérations



Fréquence Maximale du système = min (FMAX1,FMAX2, FMAX3, FMAX4, FMAX5). RIOB : FMAX4 et FMAX5 indépendants des délais de routage interne non reproductibles du FPGA

herve.le-provost@cea.fr

FPGA – Les blocs de conception IP



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FPGA – Exemple Famille XILINX

Ressources /Blocs en dur	XCE6VHX565T (VIRTEX-6)	XC5VFX200T (VIRTEX-5)	XC3SD3400A (SPARTAN-3A)
LUT	354240 LUT-6	122880 LUT-6	47744 LUT-4
FLIP-FLOP	708480	122880	47744
PROCESSEUR	0	2 PPC440@400MHz	0
RAM/FIFO	156 x 36Kbits	456 x 36Kbits	126 x 18Kbits
TRANSCEIVER	24 9,95 Gb/s -11,18 Gb/s	24 150 Mb/s -6,5 Gb/s	0
CONTROLEUR ETHERNET (MAC)	4	8	0
TAILLE MÉMOIRE DE CONFIGURATION	153,2 Mbits	70,9 Mbits	11,7 Mbits

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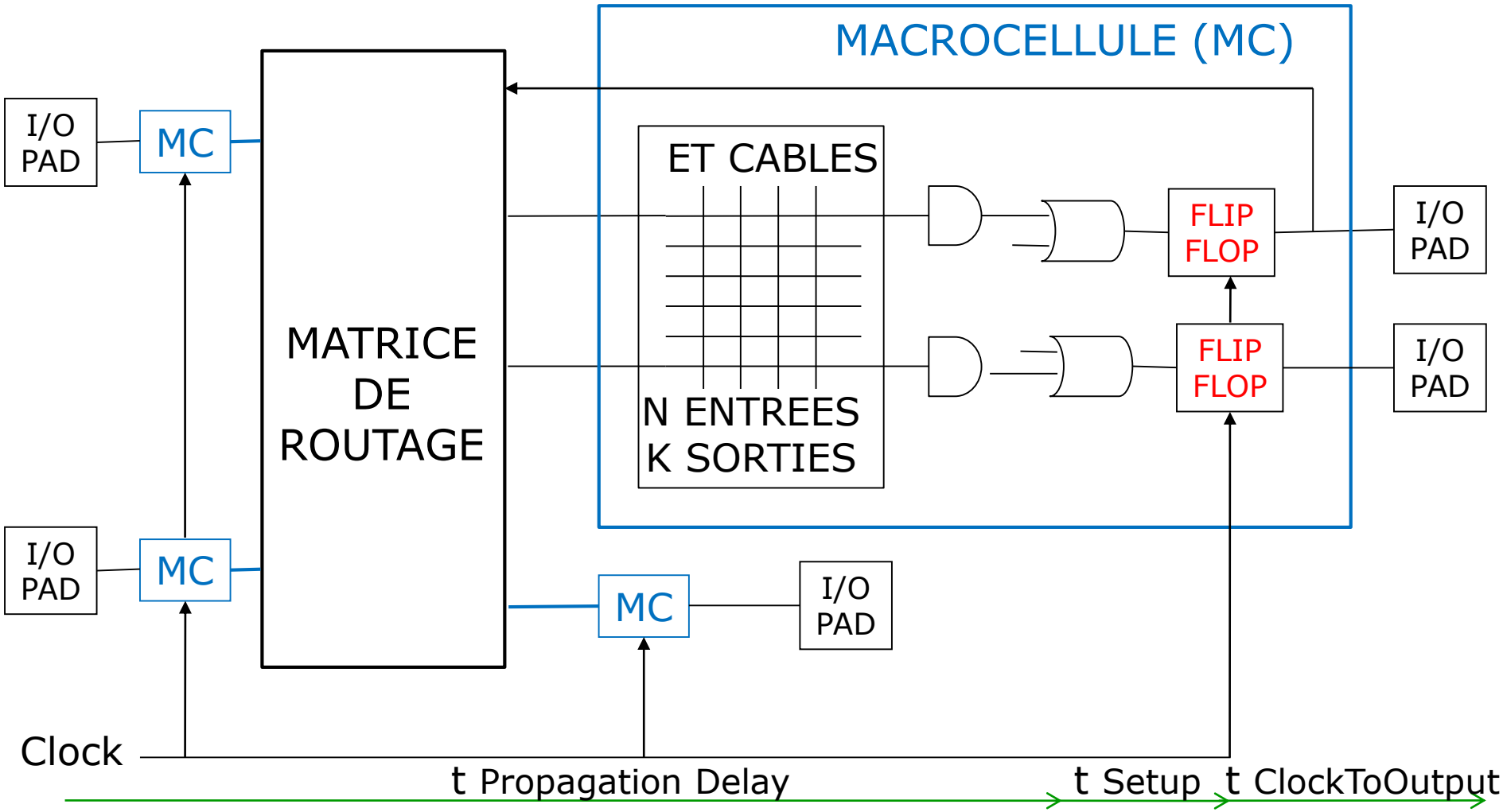
FPGA- versus CPLD



Valeurs Typique : FMAX=250 MHz, Nombre de MC=256

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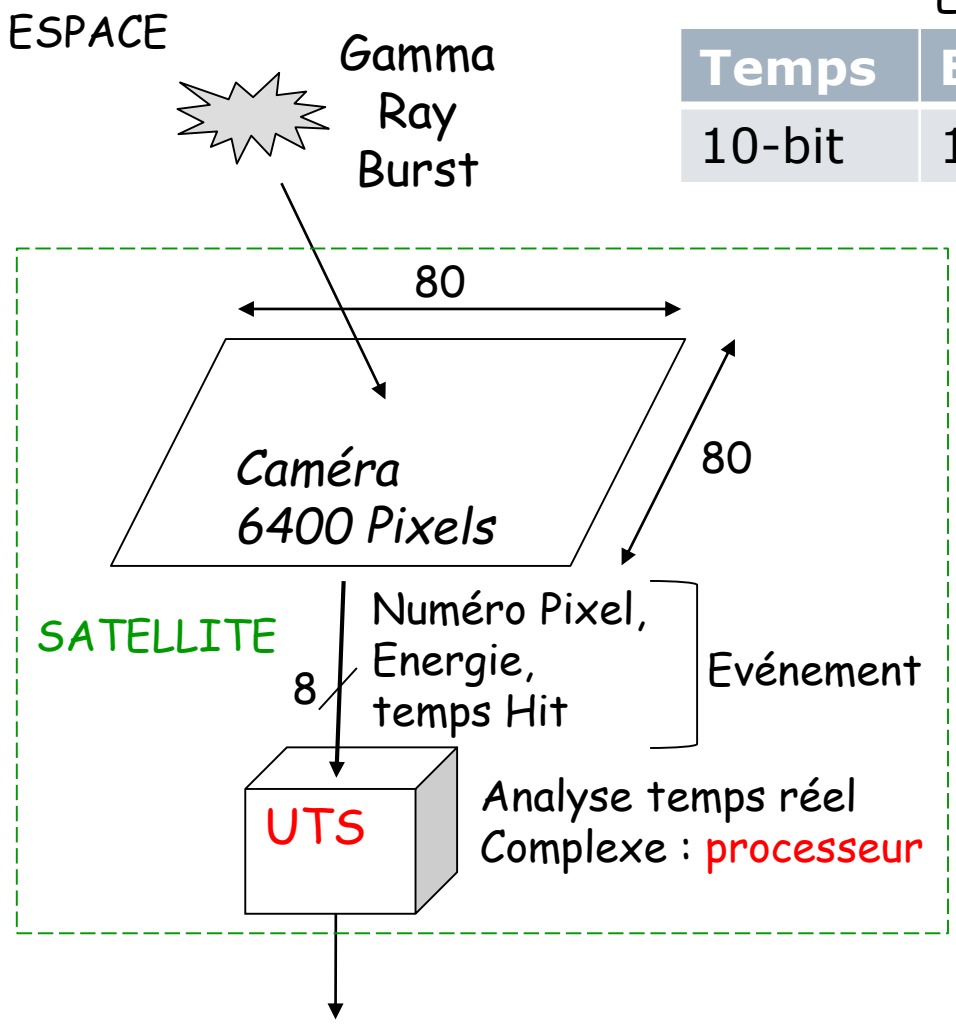
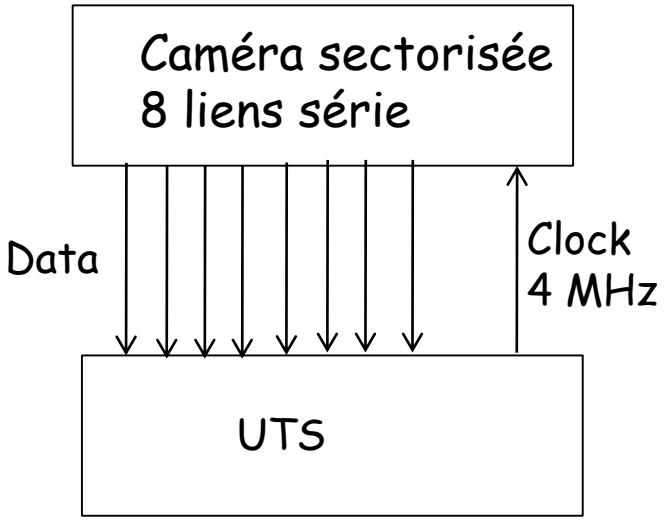
FPGA- un design, les entrées



Evénements Photon

Temps	Energie	Numéro Pixel
10-bit	12-bit	10-bit (0 à 799)



Saturation Caméra 100 000 coups/s

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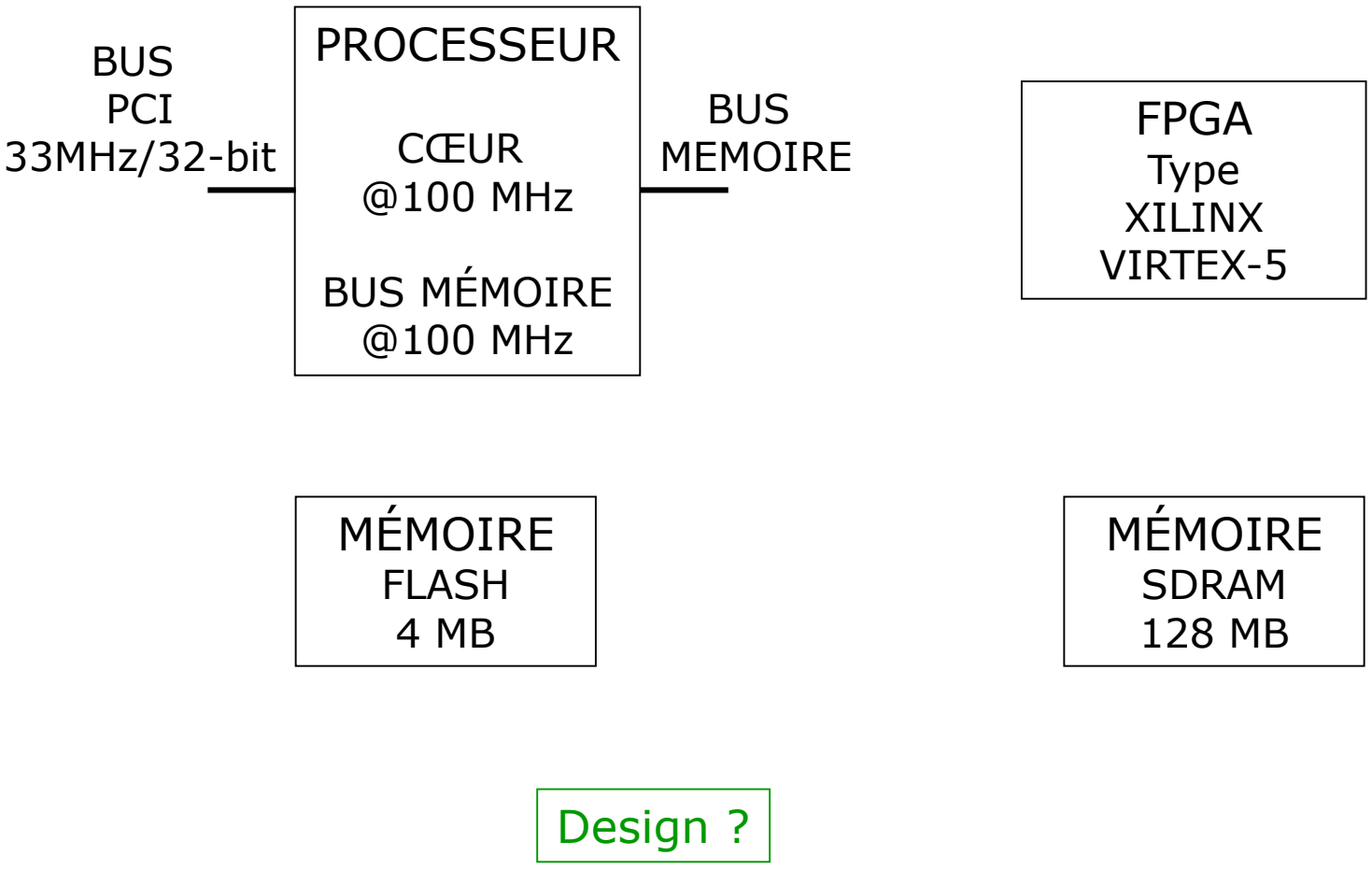
FPGA – Un design, les composants



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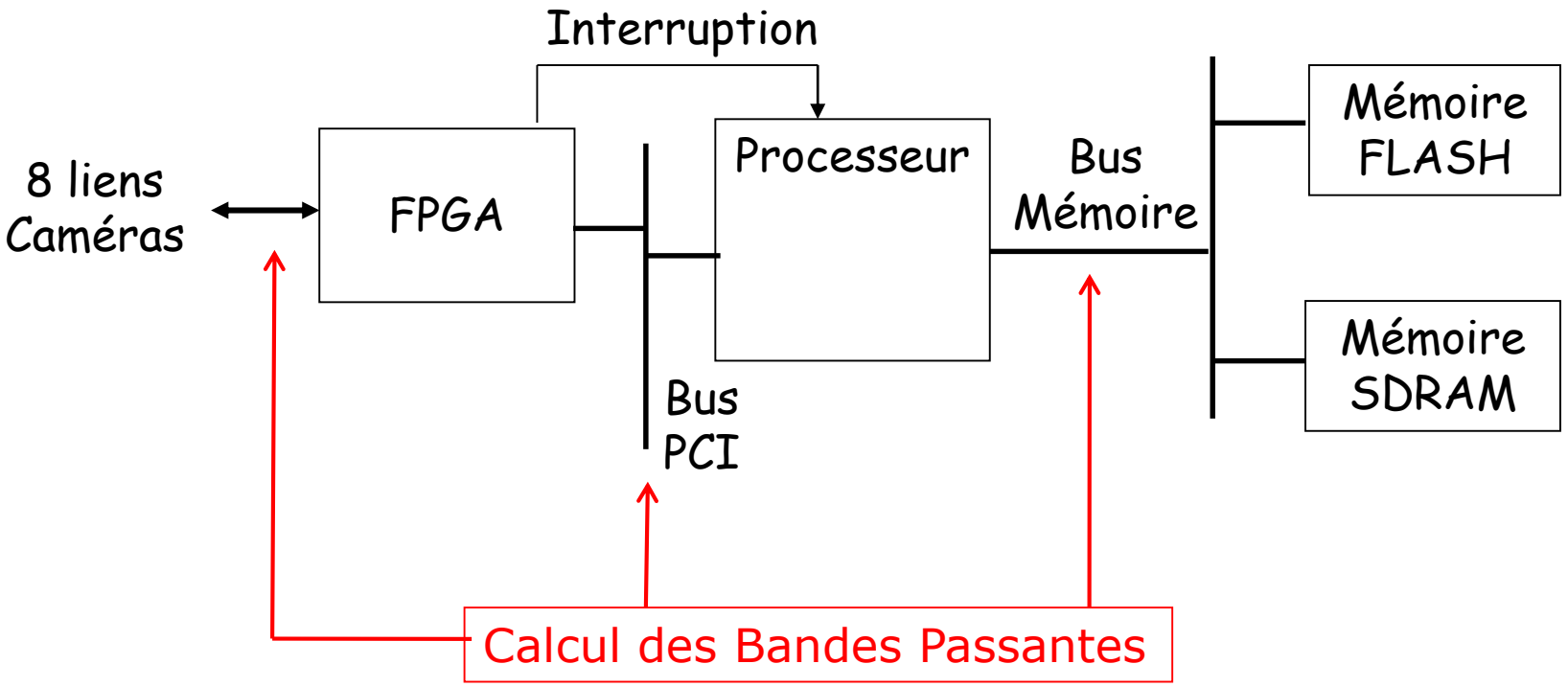
FPGA- Un design



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FPGA- Un design

	Caméra (Max)	Caméra (Saturation)	Bus PCI	Bus Mémoire
Largeur bus (bit)	1	32	32	32
Fréquence (MHz)	4	0,1	33	100
Nombre de bus	8	1	1	1
Bande Passante (M octet/s)	4	0,4	132	400

Bande passante maximale,
efficacité des protocoles non prise en compte

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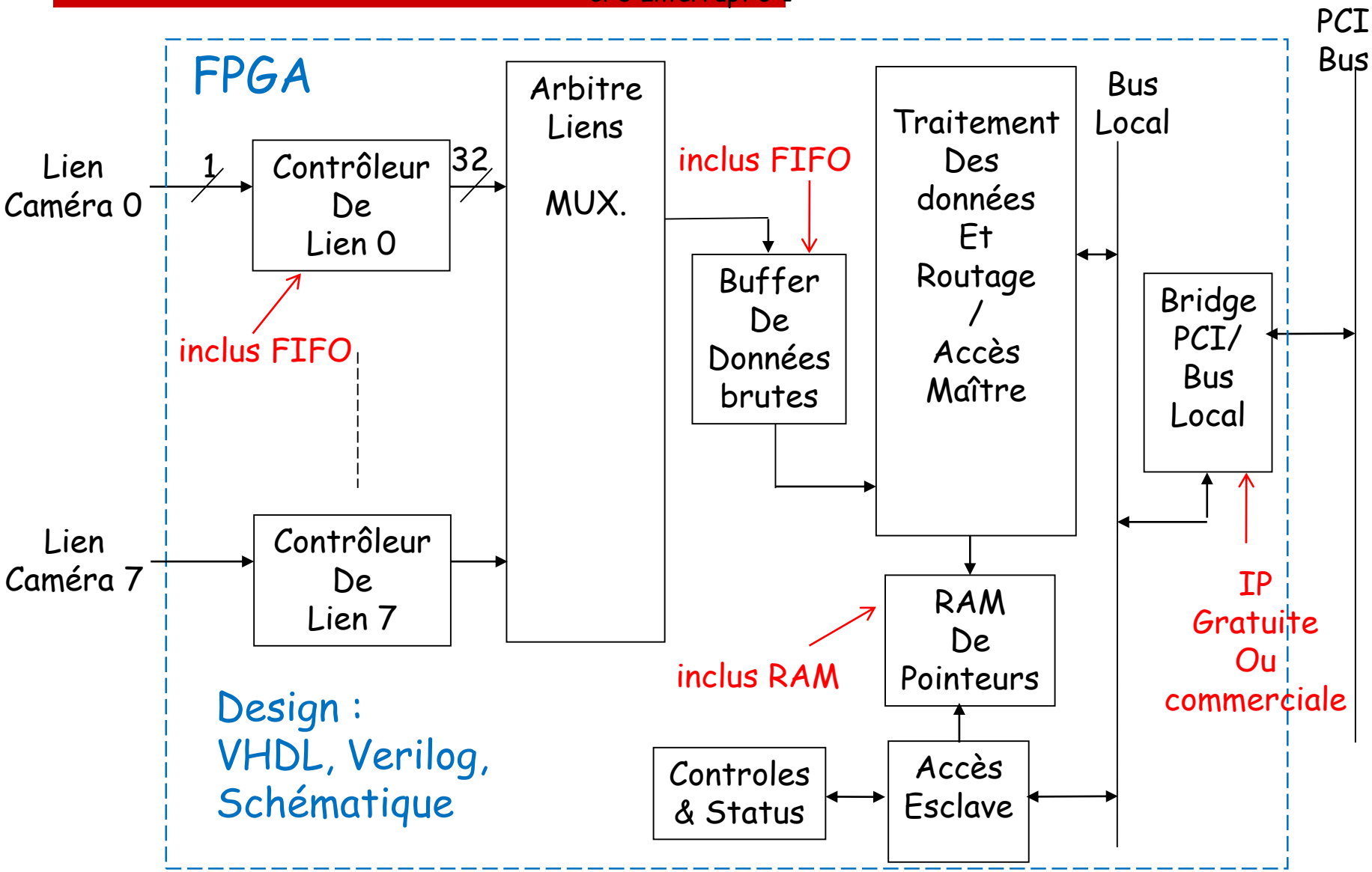
FPGA- Un design



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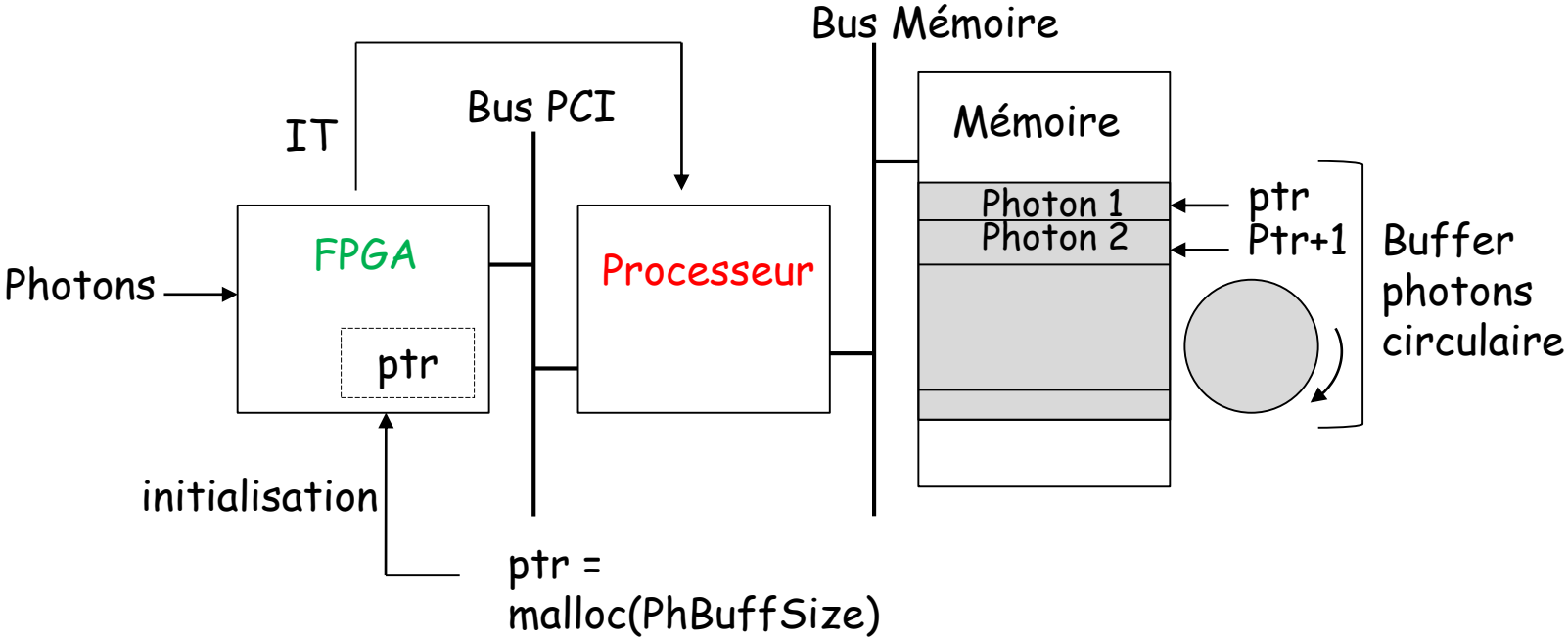
FPGA-un design

interruption toutes les 10 ms
Programme d'interruption :
lecture du registre FPGA contenant
le nombre de photons écrits



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