

EEDG 6370: DESIGN AND ANALYSIS OF
RECONFIGURABLE COMPUTING
SYSTEMS

Assignment 3: GCD Hardware Design

Group Name – BSS

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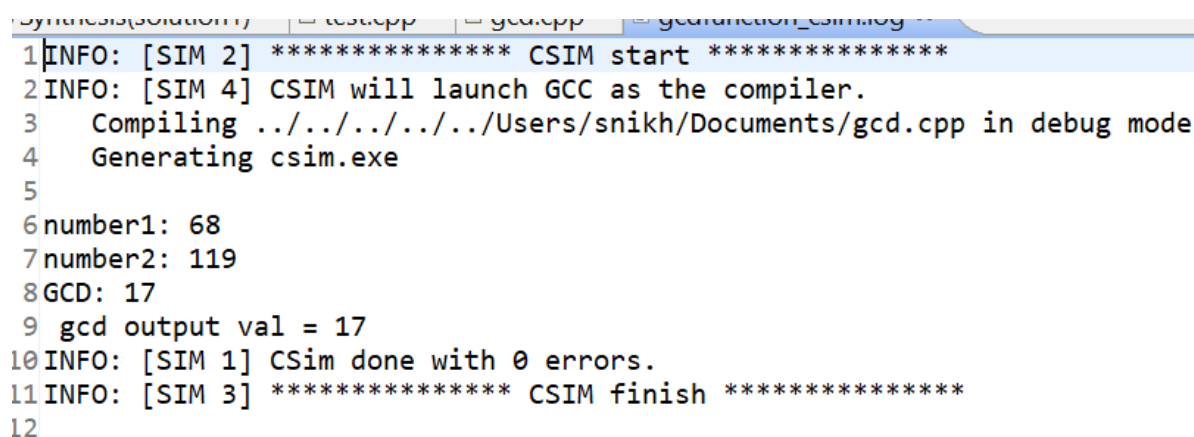
Objective:

To design and implement hardware for calculating the greatest common divisor (GCD) between two positive 16-bit integers.

Design and analysis of the GCD function:

The C++ code for the GCD function was written in Vivado HLS and simulated to check the correctness of the GCD function. The test bench was also written in CPP which was used in the simulation process to send sets of inputs and get the outputs. Synthesis of the design was done where the CPP code was converted to an RTL Code. The RTL was exported as an IP to use in Vivado. A block design was created in Vivado where the IP was connected to the zynq processing system and the Direct memory access (DMA) through the AXI bus. Synthesis, Implementation and generation of bitstream were done. Also, the HDL Wrapper code was generated and the hardware was exported along with the bitstream to launch the Xilinx SDK. In the SDK, The FPGA board was first configured with the bitstream. Two different codes were written in SDK- one to implement the design on the ARM Core(Software) and one to implement the design on the programmable logic where the processor is interfaced with the IP through the AXI DMA. A few sets of inputs were used for each of the codes to test the functionality of the design. To Speed up the design, the modulo operation in the CPP Code was replaced by a straightforward statement that performed the same operation.

Screenshot of C Simulation in Vivado HLS:



```
1|INFO: [SIM 2] ***** CSIM start *****
2|INFO: [SIM 4] CSIM will launch GCC as the compiler.
3|   Compiling ../../../../../../Users/snikh/Documents/gcd.cpp in debug mode
4|   Generating csim.exe
5|
6|number1: 68
7|number2: 119
8|GCD: 17
9| gcd output val = 17
10|INFO: [SIM 1] CSim done with 0 errors.
11|INFO: [SIM 3] ***** CSIM finish *****
12|
```

Screenshot of Synthesis Report:

Synthesis Report for 'gcdfunction'

General Information

Date: Wed Feb 23 16:47:41 2022
Version: 2018.1 (Build 2188600 on Wed Apr 04 19:04:02 MDT 2018)
Project: gcdfind
Solution: solution1
Product family: zynq
Target device: xc7z010clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	4.94	1.25

Latency (clock cycles)

Summary

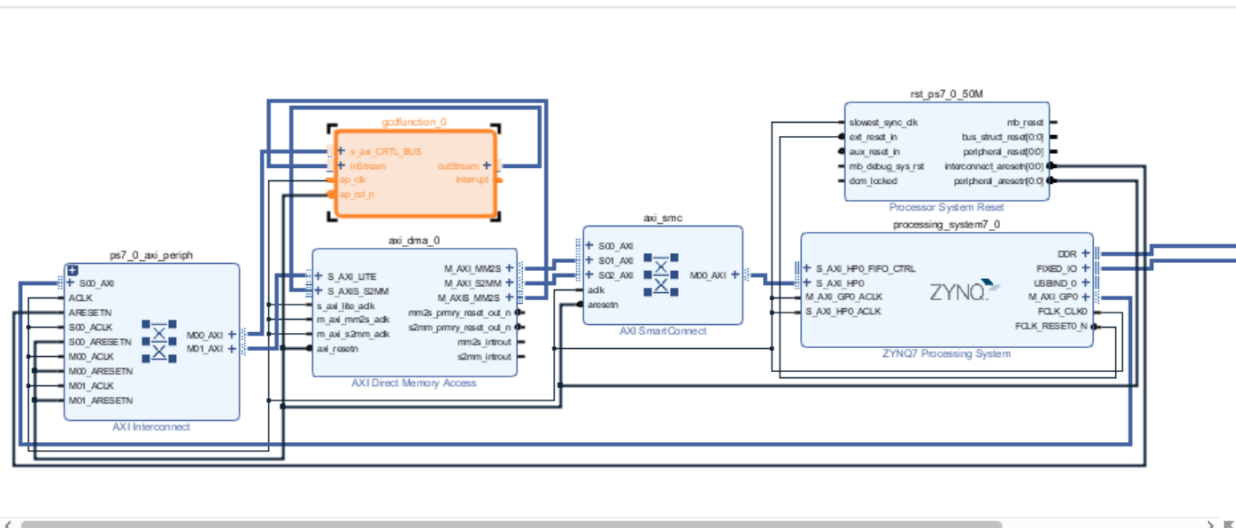
Latency		Interval		Type
min	max	min	max	
?	?	?	?	none

Detail

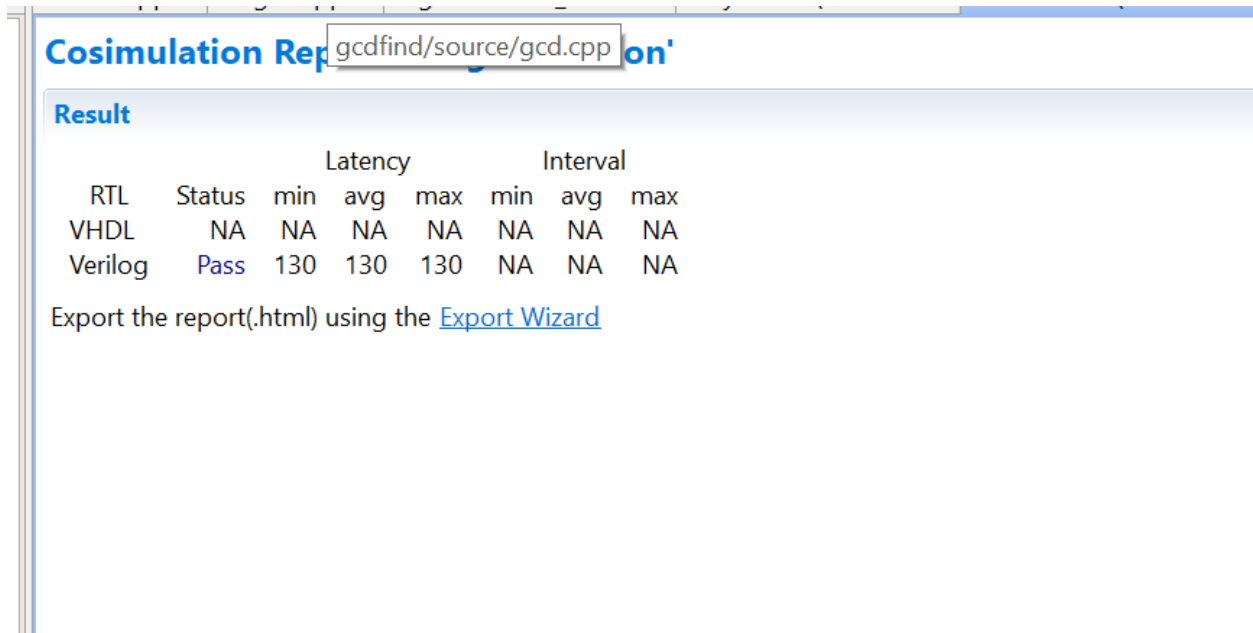
Instance

Loop

Screenshot of Block design in Vivado:



Screenshot of Cosimulation report(C/RTL):

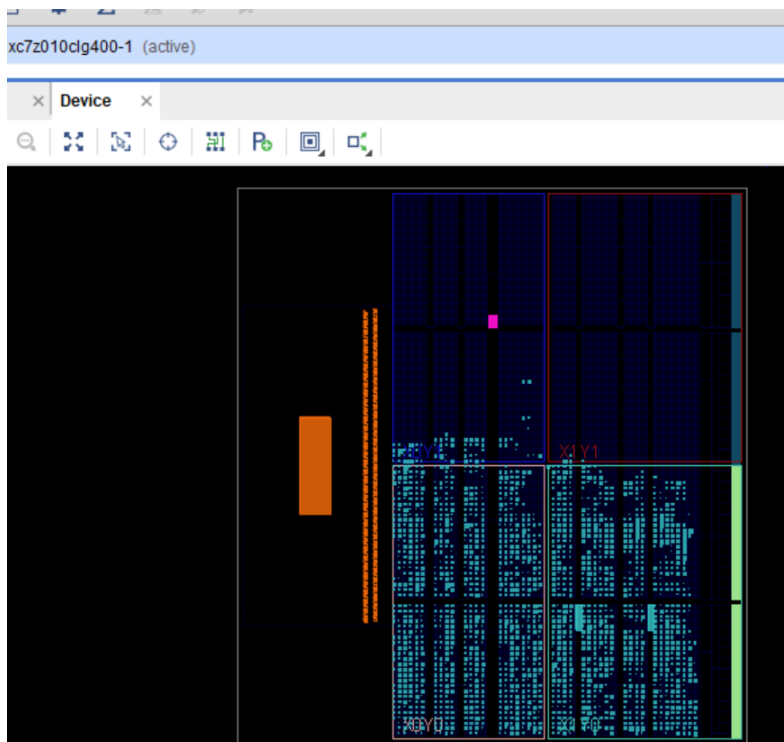


The screenshot shows a window titled "Cosimulation Report" with a text box containing "gcdfind/source/gcd.cpp" and a button labeled "on". Below the title bar is a section labeled "Result" containing a table with latency and interval data for RTL and Verilog components.

RTL	Status	Latency			Interval		
		min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	130	130	130	NA	NA	NA

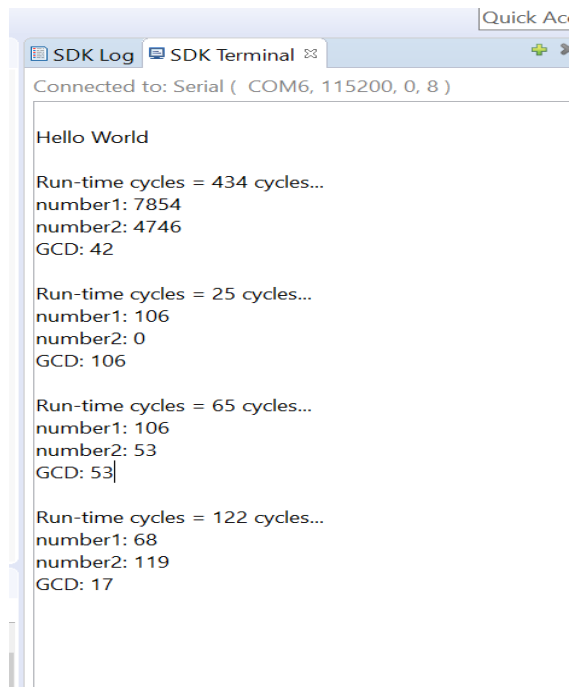
Export the report(.html) using the [Export Wizard](#)

Screenshot of implemented Design:



The screenshot shows a window titled "xc7z010clg400-1 (active)" with a "Device" tab. Below the title bar is a toolbar with various icons. The main area displays a logic analyzer or timing diagram with multiple channels of digital data. A red box highlights a specific region of the data, and a yellow box highlights another region. The data is displayed in a grid format with columns and rows of bits.

Screenshot of SDK output for ARM core implementation:



The screenshot shows the SDK Terminal window with the following output:

```
Connected to: Serial ( COM6, 115200, 0, 8 )

Hello World

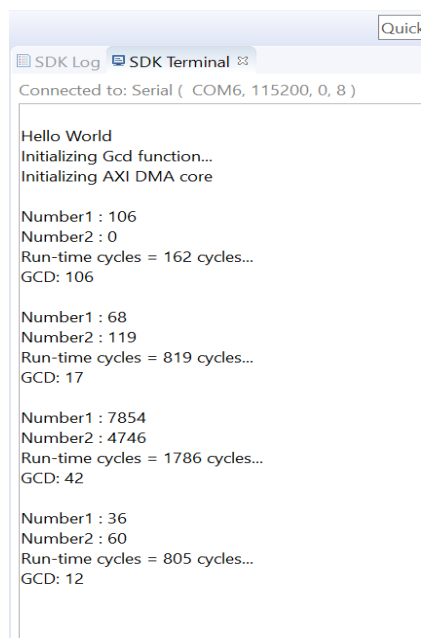
Run-time cycles = 434 cycles...
number1: 7854
number2: 4746
GCD: 42

Run-time cycles = 25 cycles...
number1: 106
number2: 0
GCD: 106

Run-time cycles = 65 cycles...
number1: 106
number2: 53
GCD: 53

Run-time cycles = 122 cycles...
number1: 68
number2: 119
GCD: 17
```

Screenshot of SDK Output for FPGA Implementation:



The screenshot shows the SDK Terminal window with the following output:

```
Connected to: Serial ( COM6, 115200, 0, 8 )

Hello World
Initializing Gcd function...
Initializing AXI DMA core

Number1 : 106
Number2 : 0
Run-time cycles = 162 cycles...
GCD: 106

Number1 : 68
Number2 : 119
Run-time cycles = 819 cycles...
GCD: 17

Number1 : 7854
Number2 : 4746
Run-time cycles = 1786 cycles...
GCD: 42

Number1 : 36
Number2 : 60
Run-time cycles = 805 cycles...
GCD: 12
```

Conclusion:

Thus, the GCD function was implemented in the Zybo FPGA Board where it was implemented on both the ARM Core as well as the programmable logic. The clock cycles required to run both the designs were also reported.