Design and Simulation of State-of-Art ZigBee Transmitter for IoT Wireless Devices

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***Abstract*—The rapid development in wireless networking has been witnessed in past several years, which aimed on high speed and long range applications. The increasing demand for low data and low power networking led to the development of ZigBee technology. This technology was developed for Wireless Personal Area Networks (WPAN), directed at control and military applications, where low cost, low data rate, and more battery life were main requirements. ZigBee is a standard, which defines set of communication protocols. ZigBee based devices operate in 868 MHz, 915 MHz and 2.4 GHz frequency bands. It has maximum data rate of 250K bits per second. This paper explores the architectural blocks of digital ZigBee transmitter. The advancement in VLSI technology led to the development of more efficient, accurate, small, and fast design. ZigBee has potential application in Internet of Things (IoT), because of the fact that it is a low power and low data rate device. The main focus of the project is to design a ZigBee transmitter using Verilog for IoT applications. A basic digital ZigBee transmitter consists of cyclic redundancy check, Bit-to-Symbol block, Symbol-to-Chip block, and a Modulator. This paper presents digital design and Verilog-HDL simulation of the Cyclic Redundancy Check and Bit-to-Symbol block of the ZigBee transmitter.**

***Keywords*—ZigBee, IoT, CRC, Bit-to-Symbol, Verilog**

I. Introduction

ZigBee is a specification for a high-level communication using small, low-power and low-cost radios[1]. It is based on IEEE 802.15.4 Standard for Personal Area Network. This IEEE standard describes physical and MAC layer only. ZigBee data transmission rate is 250 Kbps. ZigBee devices can use system-on-chip solutions with integrated radio and 60-250 of flash memory[2]. ZigBee basically operates on three frequency bands; 868 MHz in Europe, 915 MHz in America and 2.4 GHz all over world. The transmission range is from 10 to 100 meters[3]. It supports three types of network topologies; star topology, mesh topology, and combined topology[2]. The ZigBee concentrate on the low data rate and low power consumption, directed towards remote control and military applications. The ZigBee standard is maintained by ZigBee alliance. Figure 1 displays a commercial ZigBee transmitter and receiver pair manufactured by Digi International. It operates on 2.4 GHz with data rate of 250 Kbps[4].

ZigBee uses very low data rate and has a long battery life, which makes it widely useful in monitoring and control

Fig. 1. A commercial ZigBee transmitter and receiver pair manufactured by Digi International[4]

applications[5]. Therefore, markets as building automation, industrial control, lighting in smart homes, personal health care, and commercial control are perfect fits. The human interface devices such as keyboards, mice, joysticks etc. and high end remote control for consumer electronics are also good fits. ZigBee devices are now getting more attention towards Internet of Things (IoT).

In today's world everything is going smart, smart power grids, smart sensor networks, smart homes, and smart water distribution systems. The common perspective for these systems is usually associated with one single concept, known as Internet of Things (IoT). The IoT make use of intelligently connected devices, and systems to transfer data over a network without requiring human-to-human or human-to-computer interaction. For example, in a smart home, air conditioner can communicate with your car so that when car is nearby, it could automatically switch on or when you enter home the light automatically glows up. For these interconnected networks, Wireless Sensor Networks (WSN) could become the important technology. The ZigBee is appropriate for WSN, whether it is a home or an agriculture field. Hence, ZigBee could be the future of IoT.

This project mainly focuses on the designing of ZigBee

transmitter on the architectural or hardware point of view for the IoT applications. ZigBee transmitter can be designed using analog components. The analog devices use bigger components, and also data transmission is poor. As a result, data transmission is relatively not accurate. Therefore, need of digital design of ZigBee transmitter is necessary. The digital version will allow accurate data transmission. Moreover, power supply requirements of digital devices are less. Due to these advantages, digital ZigBee transmitter is suitable for IoT applications. The IoT doesn't require high data rates, because IoT devices mainly use control signals. Additionally, less power is consumed in ZigBee as compared to other wireless technologies. Moreover, it is more secure than bluetooth devices. The design and simulation of Cyclic Redundancy Check (CRC), and Bit-to-Symbol blocks of a digital ZigBee transmitter using Verilog HDL has been presented in this paper.

The organization of the paper is as follows: Section II in this paper provides the overview of the ZigBee transmitter, which includes the detailed study of acknowledgment frame format and block diagram of the ZigBee transmitter. Further, Section III focuses on CRC block of the ZigBee transmitter followed by the basic functionality of Bit-to-Symbol block in Section IV. Section V presents the simulation results and discussion. Finally, Section VI and Section VII comes up with the future work plans and conclusion, respectively.

II. ZIGBEE TRANSMITTER

In this project, we focus on 2.4 GHz band application which has 16 channels with the spacing of 5 MHz. The data rate is kept at 250 Kbps. The ZigBee standard employs Direct Sequence Spread Spectrum (DSSS) technique to avoid interference[6]. The modulation is done using Offset-Quadrature Phase Shift Key (O-QPSK) modulator, which sum the in-phase signal with a half cycle delayed quadrature phase signal[7]. The ZigBee transmitter has been designed for the use of acknowledgment frame format, which is the simplest MAC sub layer frame format without Medium Access Control (MAC) payload[8]. It provides the active feedback from the receiver to sender that the packet has been received without error. The fig. 2 represents the acknowledgment frame format:

A. Medium Access Control (MAC) Layer

The MAC layer comprises of MAC Header (MHR) and MAC Footer (MFR). The MHR consists of MAC frame control and data sequence number, while MAC Footer (MFR) constitutes Frame Control Sequence (FCS). Frame control is a 16-bit long field, which gives information about the frame types, source and destination addressing modes. Frame types indicate whether the frame is beacon type, ACK frame, MAC command frame etc. The Data Sequence Number (DSN) is an 8-bit value, which is used when stream of data is sent. It acts as a counter that increments itself after each frame. Frame Control Sequence is a 16-bit field which contains 16-bit CRC for detecting errors during transmission. This frame is passed to the Physical (PHY) layer as the Physical Service Data Unit (PSDU), which becomes PHY payload.

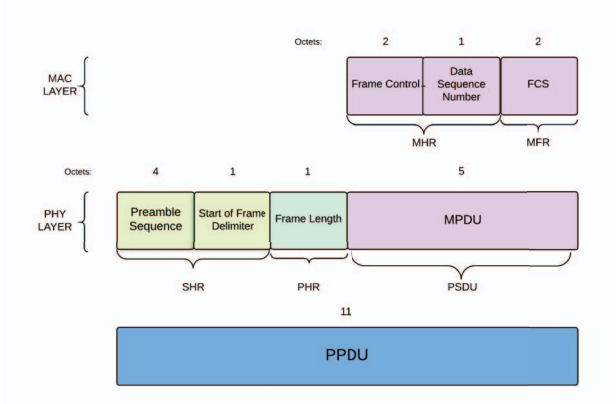

Fig. 2. Acknowledgment frame and the physical layer packet format

B. Physical (PHY) Layer

The PHY Payload which actually comes from acknowledgment frame (PSDU) is prefixed with Synchronous Header (SHR) and PHY Header (PHR). The SHR has preamble sequence and start of frame delimiter. The preamble sequence is a 32-bit field used for synchronization between transmitter and receiver. It consists of string of 0s and 1s. After detecting sync field, the receiver starts synchronization with the incoming signal. Start of frame delimiter is an 8-bit long field which indicates beginning of the frame. Frame length is an 8-bit long field, where 7-bits indicate length of PSDU and reserved 1-bit indicates if packet is received or not.

Table I summarizes the bit length and value of each field employed in this project, which sums up into the total length of PPDU i.e. 88 bits.

TABLE I
BIT LENGTH OF EACH FIELD IN THE PPDU FOR THE PROJECT

FIELD	BIT LENGTH
Preamble Sequence	32 (set at logic 0)
SFD	8(11100101)
PHR	8(10100000)
Frame Control	16(0100010000000000)
Sequence Number	8(10000000)
FCS	16(from CRC)
TOTAL	88

A ZigBee transmitter comprises of four blocks viz.: CRC, Bit-to-Symbol, Symbol-to-Chip, and O-QPSK Modulator. Fig. 3 shows the basic block diagram of a ZigBee transmitter.

Cyclic Redundancy check is a data transmission error detecting technique. This block calculates 16 bit CRC, which is appended at the end of data bits. The CRC is calculated over the data of MHR and MFR payloads of MAC layer. The output from CRC block is fed to the input of Bit-to-Symbol block. Thus, this block takes 88 bits as input and maps that binary information into symbols. The 4 LSBs (b0, b1, b2, b3) of each octet are mapped into one data symbol

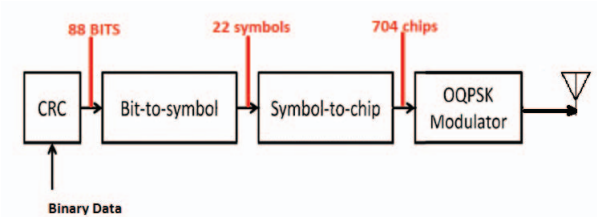

Fig. 3. Basic Block Diagram of ZigBee Transmitter

(S1) and 4 MSBs (b4, b5, b6, b7) of each octet are mapped into other data symbol (S2). Thus, a total of 22 symbols are taken out from the Bit-to Symbol block. In Symbol-to-Chip block, DSSS technique is performed where 32-bit PN sequence is generated for every symbol. The ZigBee standard uses O-QPSK modulating technique. This modulator is used to avoid inter-symbol interference and other transmission noises.

III. CYCLIC REDUNDANCY CHECK CODES

Error detecting is a technique of detecting bit errors occurring due to noise or attenuation during data transmission[9]. Error detecting codes can neither correct the errors nor detect which bit is having error. It can only determine whether a data stream contains errors. If an error is detected, the transmitter retransmits the signal to enable error free communication[10]. The main error detecting techniques are parity checking, checksum, redundancy checking, and cyclic redundancy checking. The CRC calculation is based on the polynomial arithmetic[11]. The bits of the binary data represent the coefficients of the polynomial. For example, the message 11001001 represents a polynomial of $x^7+x^6+x^3+1$. The sender and receiver, both have the generator polynomial. The arithmetic involved in CRC calculation is modulo-2 division. Let us suppose, we have a message polynomial M(x) and a generator polynomial G(x) of degree r. To calculate CRC, append r zeros at the end of message. Now divide the message bits with the generator bits using modulo-2 division. The remainder left after the division is CRC code and it is appended at the end of message bits which is finally transmitted. At the receiving end, the transmitted data is again divided by generator polynomial. If the remainder comes out to be zero, then the transmitted data is correct.

A. Design Methodology

The CRC can be implemented using linear feedback shift registers (LFSR) as shown in the fig. 4. In this project, CRC-CCITT has been used, which have generator polynomial $x^{16}+x^{12}+x^5+1$. The implemented CRC is serial in nature; therefore output will come only after all the input bits are fed to the CRC block.

The CRC is calculated over the data of MHR and MFR payloads of MAC layer. The algorithm used for this CRC calculation is given below:

1) Initialize all linear feedback shift registers to zero.
2) Enter the data (LSB first) into registers of the divider.

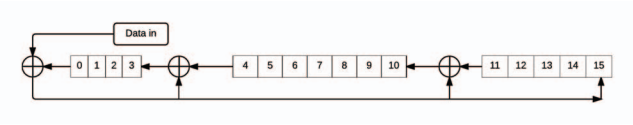

Fig. 4. CRC-CCITT generator polynomial G(x) = $x^{16}+x^{12}+x^5+1$

3) After the last bit entered in the divider, the remainder consists of FCS of 16-bit.
4) The FCS is then appended at the end of data bits to obtain the transmitted frame.[12]

IV. BIT-TO-SYMBOL

Bit to Symbol block, as the name represents, maps bits into symbols. The 88 bit binary information from the output of the CRC block is fed as input to this block. This 88 bits data is passed through Bit-to-Symbol block sequentially, starting with the preamble field and ending with last octet of the PPDU i.e. FCS which is generated by CRC. Fig. 5 shows how one octet is divided into corresponding symbols.

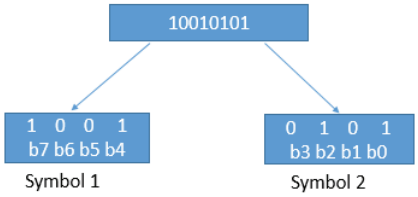

Fig. 5. Bit to Symbol mapping

Therefore, it takes 11 octets as input, where the 4 LSBs (b0, b1, b2, b3) are mapped into one data symbol (S1) and the 4 MSBs (b4, b5, b6, b7) are mapped into next data symbol (S2). Thus, 11 octets maps into 22 symbols.

V. RESULTS AND DISCUSSION

The characteristics of CRC and Bit-to-Symbol block has been simulated by using Verilog code of each. The simulation is done on the ISE Design Suite 14.5. The design was also synthesized and RTL schematic was generated. The inputs were given according to Table I. The frequency of operation was kept at 250 KHz i.e. 1 clock cycle is 4 μs.

A. CRC Simulation Waveform

The 40-bit data is fed serially to the CRC block to compute 16-bit Frame Check Sequence (FCS). A clock of 250 KHz was applied to the design. First of all, registers were reset using reset pin. After the synthesis of the CRC block, RTL schematic was generated as shown in fig. 6. The simulation results of CRC block are shown in the fig. 7. The CRC was generated after 168 μs when all bits entered into the block.

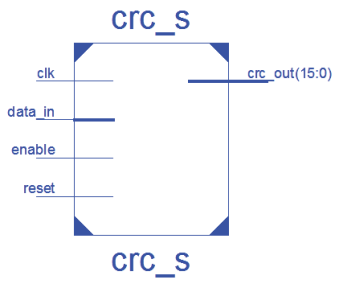

Fig. 6. RTL schematic view of CRC

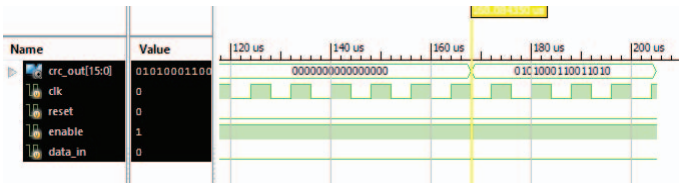

Fig. 7. Simulation waveform of CRC

B. Bit-to-Symbol Simulation Waveform

The 88-bits from the output of CRC block, which is PPDU, was fed as data input to this block. The 88-bits were mapped into 22 symbols. The fig. 8 shows the RTL schematic of Bit-to-Symbol block. When reset is high, all symbols were set to logic 0. The simulation waveform of Bit-to-Symbol block is given in fig. 9.

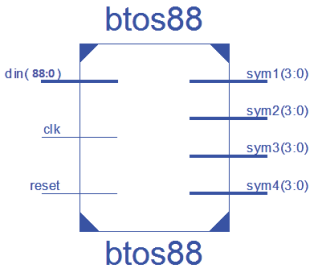

Fig. 8. RTL schematic view of Bit-to-Symbol

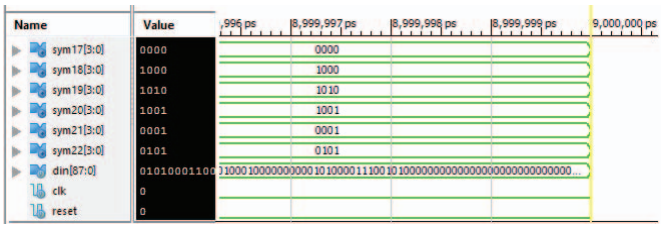

Fig. 9. Simulation waveform of Bit-to-Symbol

VI. Future Work

The design of Symbol-to-Chip block (where DSSS technique is performed and 32-bit PN sequence number is generated for every symbol) is currently in progress. The Offset Quadrature Phase Shift Keying (O-QPSK) modulation technique to avoid inter-symbol interference and other transmission noises, will also be enlisted as future work. It is noted that use of parallel CRC might increase the throughput, therefore design of parallel CRC is also considered very important for future. After completion of the design, ZigBee transmitter will be further optimized to work as an IoT device.

VII. Conclusion

This paper describes the design of first two blocks viz., CRC block and Bit-to-Symbol block as a part of the ZigBee transmitter for 2.4 GHz frequency band. CRC was employed to detect the errors during transmission of data. The binary data was sent to CRC and CRC codes were generated. The output of CRC block was fed to Bit-to-Symbol block, where 88 bits were mapped into 22 symbols. The corresponding codes were built in Verilog to characterize these two block's behaviors. These blocks were then simulated and synthesized.

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