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EEE313 – Section 3
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EEE 313 Electronic Circuit Design – Lab Report 2

1. Introduction:

In this lab assignment, we were tasked with creating a Zener diode, voltage regulation circuit. We chose the resistance values of the Zener diode circuit. Then we calculated the source regulation from measurements and analytically then from these 2 computations we calculated the resistance of the Zener diode. Finally, we calculated the load regulation both analytically and from measurements.

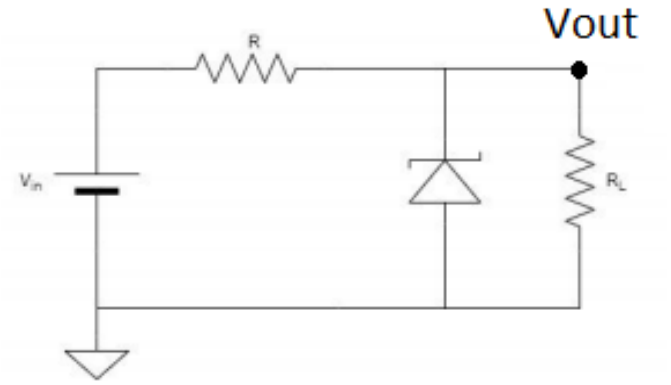

Figure 1: Circuit schematic we used in the lab

I set up this circuit in the lab on a breadboard. Then took my measurement using an oscilloscope.

2. Lab Work:

a. Part A:

In part A our R_l is 500Ω, V_{in} is 10V ,and break down voltage of the Zener diode is 5.1 V. For these values we are asked to choose an R resistance value such that Zener current is between 10 mA and 100 mA when the input changes between 9 and 11 volts.

Zener diodes act like normal diodes but they have a stable break down voltage. So here in our circuits, Zener break down voltage is 5.1 volts and when we apply a voltage greater than the Zener diodes break down voltage it goes in to break down state and lets current flow through it freely but there is a limit to how much current can flow through it without damaging it and there is a minimum amount of current that needs to flow through it to keep it in the breakdown state. The 10mA and 100mA conditions come from that restriction.

Here we can ignore the internal resistance of the Zener diode because we are trying to choose a resistance value that satisfies the given condition and the value range for this resistor is wide

enough that a small error from ignoring the internal resistor won't affect us. Also, we will check the given conditions by constructing the circuit on a breadboard.

To calculate the value range of R, I used corner analysis. We know I_z will be lowest when V_{in} is 9V and I_z will be highest when V_{in} is 11V. So first calculate the maximum value of R for V_{in} = 9V. for this we will write KCL at V_{out}.

$$\frac{V_{out} - V_{in}}{R} + I_z + \frac{V_{out}}{R_L} = 0 \tag{1}$$

We know V_{out} will be 5.1V because of the Zener diode. We also, know the V_{in} and R_L's values so we pluck them into the equation (1).

$$\frac{5.1 - 9}{R} + I_z + \frac{5.1}{500} = 0$$

$$I_z = \frac{3.9}{R} - \frac{5.1}{500}$$

$$\frac{3.9}{R} - \frac{5.1}{500} = I_z > 0.01$$

$$\frac{3.9}{R} - \frac{5.1}{500} > 0.01$$

$$\frac{3.9}{R} > 0.0202$$

$$193.07 > R \tag{2}$$

Now we will calculate the minimum value of R for V_{in} = 11V. for this we will once again write KCL at V_{out}.

$$\frac{V_{out} - V_{in}}{R} + I_z + \frac{V_{out}}{R_L} = 0 \tag{3}$$

Once again we know V_{out} will be 5.1V because of the Zener diode and we also know V_{in} and R_L's values so we pluck them into the equation (3).

$$\frac{5.1 - 11}{R} + I_z + \frac{5.1}{500} = 0$$

$$I_z = \frac{5.9}{R} - \frac{5.1}{500}$$

$$\frac{5.9}{R} - \frac{5.1}{500} = I_z < 0.1$$

$$\frac{5.9}{R} - \frac{5.1}{500} < 0.1$$

$$\frac{5.9}{R} < 0.1102$$

$$53.53 < R \quad (4)$$

From equation (3) and (4) we can see $53.53 < R < 193.7$ so I choose R as 120Ω because it is close to the middle point of the range of values and more importantly there are 120Ω resistors in the lab.

After this, I assembled the circuit on a breadboard to cheek if my choice of R is correct. While doing so because there isn't a 500Ω resistor in the lab I used a 470Ω and a 27Ω resistor in series which equates to 497Ω.

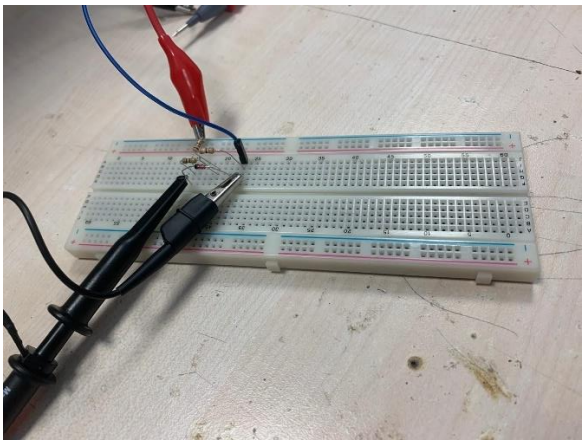

Figure 2: My circuit on the breadboard

I used a DC voltage source for the input signal V_{in}.

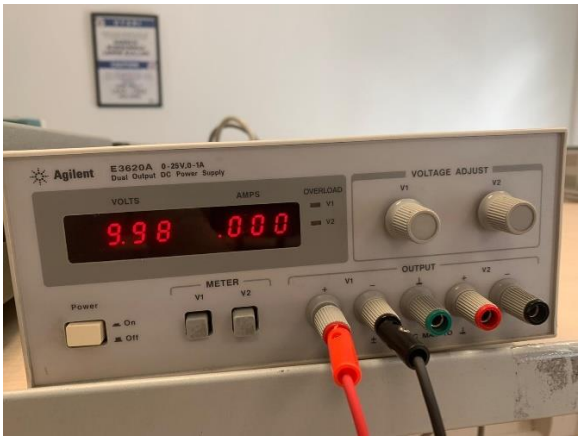

Figure 3:DC voltage source.

I gave both 9V and 11V to the circuit the measured the current on the Zener diode using a multimeter. I measured 77.5mA for 9V and 95.1mA for 11V. These values are in the desired range so I succeeded in choosing a sufficient resistor value.

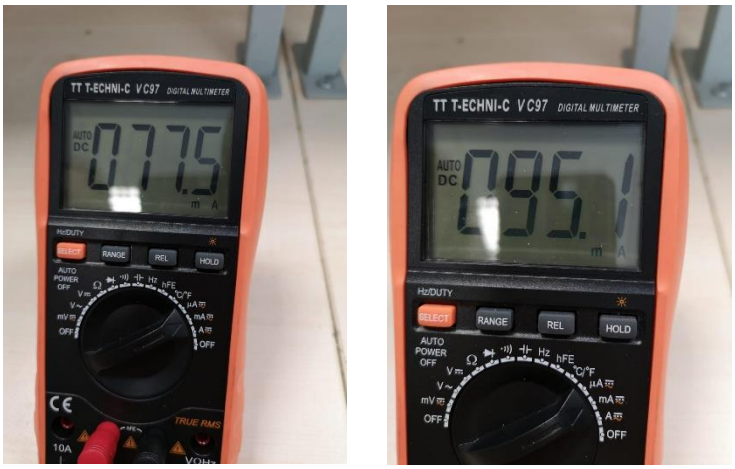

Figure 4: I_Z for 9V input (left) and 11V input (right)

b. Part B:

In this part, we are asked to calculate the source regulation of the circuit from measurement then we will calculate source regulation analytically and equate it to our measured result. From this equation, we will pull the value of internal resistance of the Zener diode.

Source regulation of a circuit is equal to $\frac{\Delta V_{out}}{\Delta V_s} \cdot 100\%$ to calculate this from measurement I gave the input signal of $V_{in} = 10 + 0.1 \cdot \sin(200\pi \cdot t)$V. to generate this signal I connected a signal generator and a DC voltage source.

Figure 5: Picture of the signal generator

After giving the input signal to the circuit I measured V_{in} and V_{out} simultaneously using 2 probes connected to a single OPAMP.

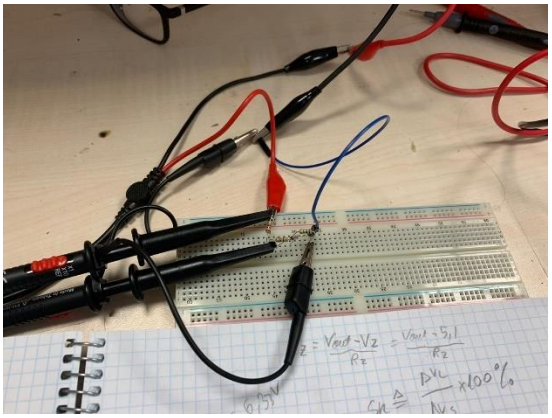

Figure 6:Picture of the circuit for part B (2 OPAMP probes and the input is DC sifted sin signal)

Because the sin component of the input signal was too small the OPAMP wouldn't trigger because of this It could not could show the signal from the V_{out} terminal properly. To fix this I increased the amplitude of the sin component of the input signal until the sin component of the signal from the V_{out} terminal was visible. It became visible at an amplitude of 0.5V.

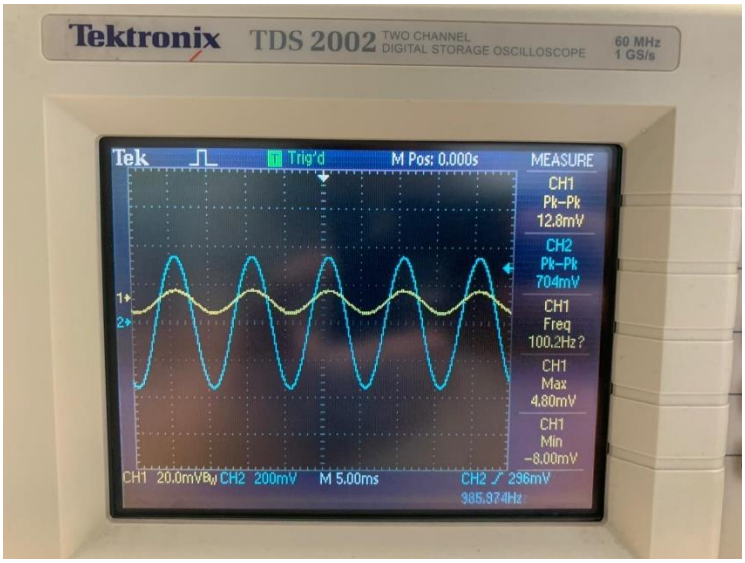

Figure 7: graph of Vout (CH2) and Vin (CH1) versus time for a DC shifted sin input signal.

We can see from figure 7 a change in V_{in} signal creates a proportional change in V_{out} signal. We can see the change in V_{in} as ΔV_s and the change in V_{out} as ΔV_{out} from the source regulation equation. Then to calculate the source regulation we can dived the V_{Pk-Pk} of the voltages and multiply by 100%.

$$Source\ Regulation = \frac{\Delta V_{out}}{\Delta V_s} \cdot 100\% = \frac{12.8}{704} \cdot 100\% = 1.82\% \quad (5)$$

We will also calculate source regulation analytically. To explain how I put the figure 8.

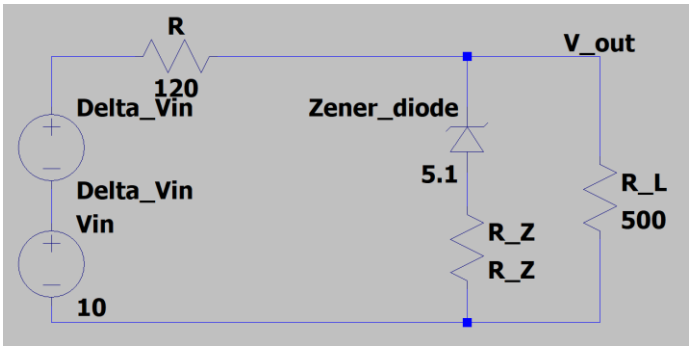

Figure 8: Schematic of the circuit

To calculate source regulation, we need to calculate $\frac{\Delta V_{out}}{\Delta V_s}$. To do so we can use superposition and just solve the circuit for ΔV_{in}.

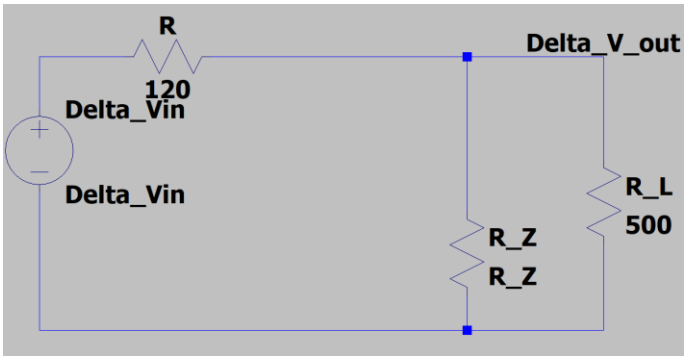

Figure 9: Schematic of the circuit for only the superposition of ΔV_{in}

To find $\frac{\Delta V_{out}}{\Delta V_s}$ by writing a voltage divider at V_{out}.

$$\Delta V_{out} = \frac{R_Z // R_L}{R_Z // R_L + R} \Delta V_{in}$$

$$\Delta V_{out} = \frac{\frac{R_Z \cdot R_L}{R_Z + R_L}}{\frac{R_Z \cdot R_L}{R_Z + R_L} + R} \Delta V_{in}$$

R is equal to 170Ω here because of the internal resistor of the signal generator.

$$\Delta V_{out} = \frac{\frac{R_Z \cdot 500}{R_Z + 500}}{\frac{R_Z \cdot 500}{R_Z + 500} + 170} \Delta V_{in} \tag{6}$$

We know R_Z very small compared to 500Ω So we can say $\frac{R_Z \cdot 500}{R_Z + 500} \cong R_Z$ then if we insert this into equation (6) we get:

$$\Delta V_{out} = \frac{R_Z}{R_Z + 170} \Delta V_{in}$$

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{R_Z}{R_Z + 170}$$

$$Source\ regulation = \frac{\Delta V_{out}}{\Delta V_{in}} \cdot 100\% = \frac{R_Z}{R_Z + 170} \cdot 100\% \tag{7}$$

We can now equate equation (5) and (7) to each other and find R_Z.

$$1.82\% = \frac{R_Z}{R_Z + 170} \cdot 100\%$$

$$R_Z = 3.15\Omega$$

c. Part C:

In this part, we are asked to calculate the load regulation of the circuit from analytic analysis using the R_Z value from part B. Then we are asked to calculate the load regulation from measurement and compare the results.

We know load regulation is $\frac{V_{L,no\ load} - V_{L,full\ load}}{V_{L,full\ load}} \cdot 100$. First, we will calculate $V_{L,no\ load}$.

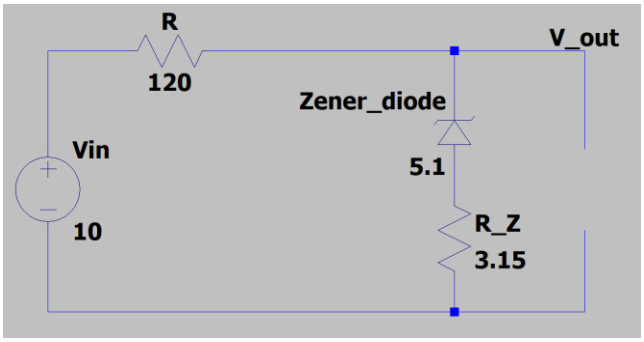

Figure 10: Schematic of the circuit for no load.

From a voltage divider at V_{out}, we can calculate $V_{L,no\ load}$

$$V_{L,no\ load} = V_z + (V_{in} - V_z)\frac{R_z}{R_z + R}$$

$$V_{L,no\ load} = 5.1 + (10 - 5.1)\frac{3.15}{3.15 + 120}$$

$$V_{L,no\ load} = 5.1 + (10 - 5.1)\frac{3.15}{3.15 + 120}$$

$$V_{L,no\ load} = 5.225V \quad (8)$$

Then we will calculate $V_{L,full\ load}$.

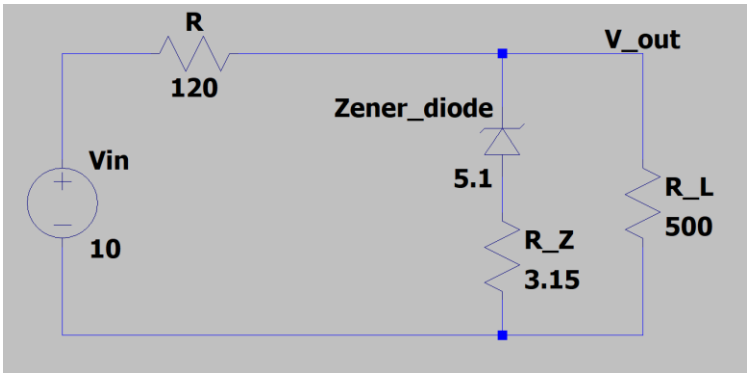

Figure 11:schematic of the circuit for full load

We can calculate $V_{L,full\ load}$ by writing KCL at V_{out}

$$\frac{V_{L,full\ load} - V_{in}}{R} + \frac{V_{L,full\ load} - V_Z}{R_Z} + \frac{V_{L,full\ load}}{R_L} = 0$$

$$\frac{V_{L,full\ load} - 10}{120} + \frac{V_{L,full\ load} - 5.1}{3.15} + \frac{V_{L,full\ load}}{500} = 0$$

$$V_{L,full\ load} = 5.19V \quad (9)$$

Then we can use equation (8) and (9) to calculate load regulation.

$$load\ regulation = \frac{V_{L,no\ load} - V_{L,full\ load}}{V_{L,full\ load}}100\% = \frac{5.225 - 5.19}{5.19}100\%$$

$$load\ regulation = 0.67\% \quad (10)$$

Then to calculate load regulation from measurement I measured $V_{L,no\ load}$ and $V_{L,full\ load}$ values on the circuit with an OPAMP. Then used these measurements in the load regulation equation to calculate load regulation.

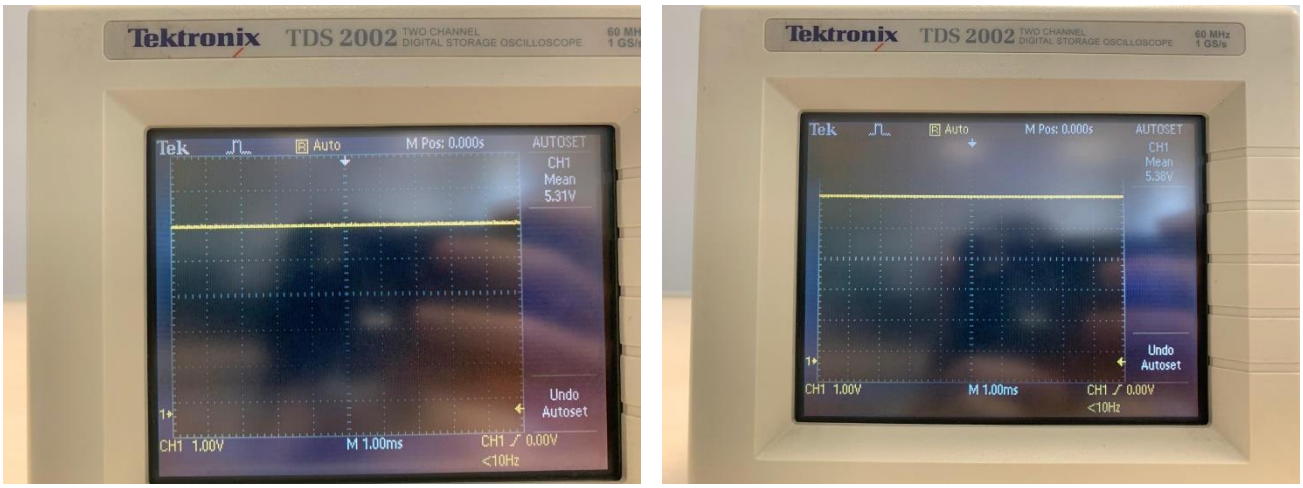

Figure 12: V_{out} graph for full load (left) and no load (right)

$$load\ regulation = \frac{V_{L,no\ load} - V_{L,full\ load}}{V_{L,full\ load}} 100\% = \frac{5.38 - 5.31}{5.31} 100\%$$

$$load\ regulation = \ 1.31\% \tag{11}$$

The result of equation (10) is different then equation (11). This is because the internal resistance of a Zener diode is dependent on the current through it and we make this measurement for 2 different currents through the diode. This will be discussed deeply in the discussion part of the report.

3. Discussion & Conclusion:

a. Discussion:

In part A we ignored a 3Ω difference between our load resistance of 497Ω and the desired load resistance of 500Ω. This 3Ω 's is not important because all the resistances we use in the lab already have a 5% error margin. This is way bigger than our 3Ω error which corresponds to a 0.6% error. The 5% inherent error margin means even if we connected an exact 500Ω resistor it would have a value between 475Ω and 525Ω. This same 5% error exists for the 120Ω resistor too. But these small errors do not hinder our experiment as there are imperfections in every real-life circuit so they add realism to the experiments if anything. To test if the current on the Zener diode stayed in the desired range, I tested the circuit on the border conditions and measured the current on the Zener diode. They were in the desired range so I was successful in my choice of the R resistance.

In part B I took a sin signal with 0.5 ampliated and 100Hz frequency as ΔV_{in}. ΔV_{in} is supposed to represent an infinitesimally small change in V_{in}. Choosing a big signal such as this is not ideal but for a signal with a smaller amplitude, the OPAMP would not trigger. Also, I could not connect the OPAMP to the signal generator with a sync cable because doing so also messes up the ground understanding of the OPAMP. So, I had to settle with a sub-optimal method. Doing

so made want to verify my result to do this I measured the voltage over the Zener diode with the OPAMP then I measured the current through the Zener diode using my multimeter. Then subtracted the breakdown voltage of the Zener diode from the voltage value and divided it with the current to find the internal resistance of the Zener diode. This method in itself has a lot of problems with it but it still gave the result of 3.28Ω which is close to 3.15Ω from our previous calculations. This gave me confidence my computations in part B are correct

In part C I computed 2 different load regulation values with 2 different methods. To understand why we first need to see load regulation depends on R_Z. As an example, if R_Z were to be 0 then the load regulation would also be 0%. In part B where we calculated the R_Z value for the analytic computation of load regulation, our R resistance is 170Ω compared to the 120Ω in part C where we did the measurements for the load regulation. So due to greater resistance in part B, there is less current through the Zener diode compared to part C. Normally higher current means less resistance but higher current also causes a greater power consumption which also means greater amount of heat production which overall increases the internal resistance. So, in short, in part C R_Z is greater due to higher current, and because R_Z is higher its load regulation is worse. But still, the difference between the two measurements are less than 1%. This means the difference is not too big and my computations from part B and C support each other. [1]

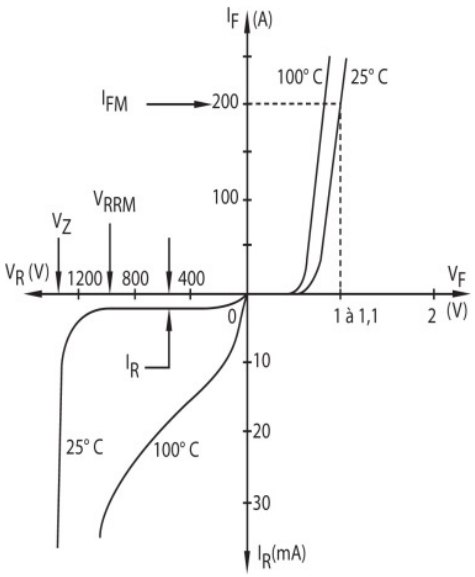

Figure 13: V-I graph of a Zener diode for 2 different temperatures.

b. Conclusion:

This lab's goal was for us to get familiarized with Zener diodes and concepts such as source regulation or load regulation. This lab was my first hands-on experience with a Zener diode. Before this lab, I thought using a Zener diode to regulate voltage was something almost only conceptual which wouldn't work in real life due to all the imperfections. Such as heat which the circuit generates in operation then that heat affects the internal resistance of the components. I thought this could only be overcome with a sophisticated design software. But in this lab, I learned that we can overcome these imperfections by designing our circuit in such a way that they work in an as broad as possible range of values instead of working in a single idealized value. Also, we give a rating to how much our circuits deviate from the ideal output relative to how imperfect of an input we give, source regulation and load regulation are just that conceptually. I also realized how imperfect all the circuit we built are, I have been using the EEE labs for more than a year and just now in this lab I realized how big an error 5% offset is on the resistors we use. But we never cared about them much because even though we didn't talk about them or calculate them specifically all the circuits we built are designed to work for a large range of imperfections. This made me understand why most circuits specify a range of compatible input signals. It is not because we are planning to use it in that range but because we know our input will be imperfect and have a range of possible values it can take centered around one point. Simply put our goal is not creating a perfect circuit; it is creating a circuit that works despite imperfections. I can easily say this lab, made me understand the EEE design philosophy a lot deeper.

References:

[1] ScienceDirect, "Zener Voltage ScienceDirect," Science Direct, [Online]. Available: https://www.sciencedirect.com/topics/engineering/zener-voltage. [Accessed 28 10 2020].