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EEE 313 Electronic Circuit Design – Lab Report 3

1. Introduction:

In this lab assignment, we were tasked with creating a 2 stage voltage amplifier using the schematic given to us in figure 1 in LTSpice. We are given the LTSpice code for a realistic NMOS and PMOS which we will use in this lab. We are asked to find (W/L) values of the transistors and resistance of R1 such that we will get |AV|=|Vout2/Vin|>30. First, I tested how the size (not their ratio) of w and L affected the channel length modulation effect (λ). Then I calculated the K_P, K_N, V_{tn}, and V_{tp} values of the given transistors by experimenting on them. Then using the values, I found from the previous part and the ideal mathematical formulas for transistors I calculated (W/L) ratios of the transistors and the resistance of R_1. Then I nudged these values with experimentation in to better values to finalize my design.

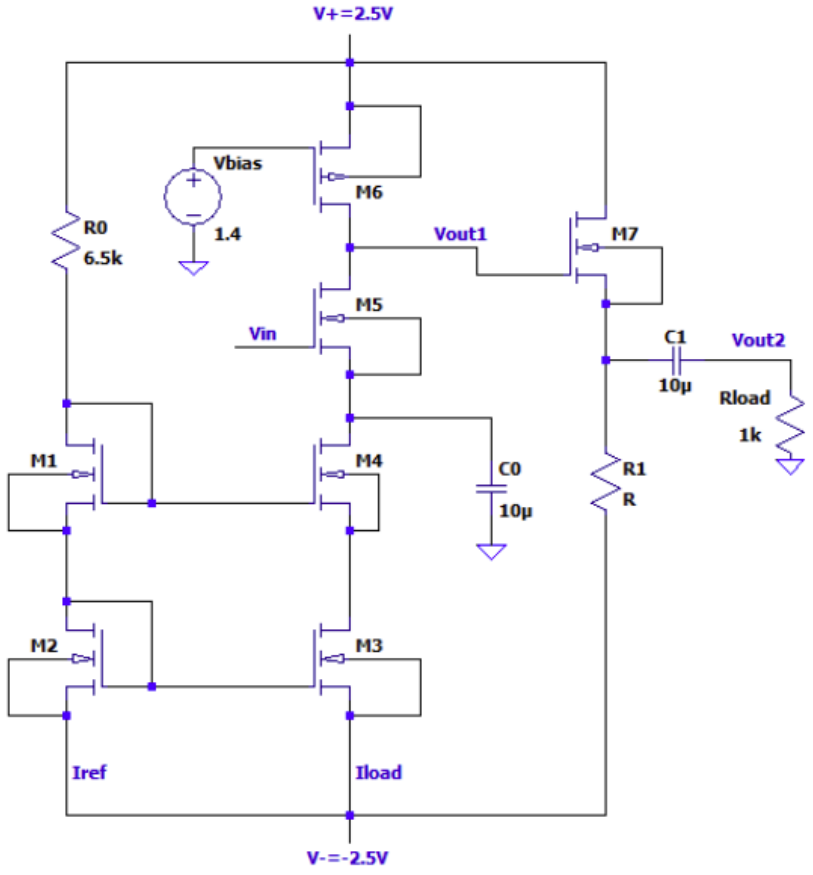

Figure 1: Circuit schematic we used in the lab

I pasted the code for transistors to LTSpice and build all my circuit using that code.

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2. Lab Work:

a. Part A:

In part A we are asked to find $V_{DS} - I_{DS}$ curves of the PMOS and NMOS devices for different V_{GS} voltages for the W/L values (25u/0.5u), (50u/1u), and (250u/5u). Then find a correlation between them and the channel length modulation effect (λ). After this, we are asked to find the K_P, K_N for the transistors and then find $V_{tn}$and V_{tp} for W/L = (50u/1u).

First, to find the $V_{DS} - I_{DS}$ curves of the NMOS device for different V_{GS} voltages, I built the circuit in figure 2 then used 2 source DC sweep. V2 is a DC sweep with a small step size which goes from 0 to 20 volts and V1 is a DC sweep with a step size of 2 volts which goes from 0 to 10 volts.

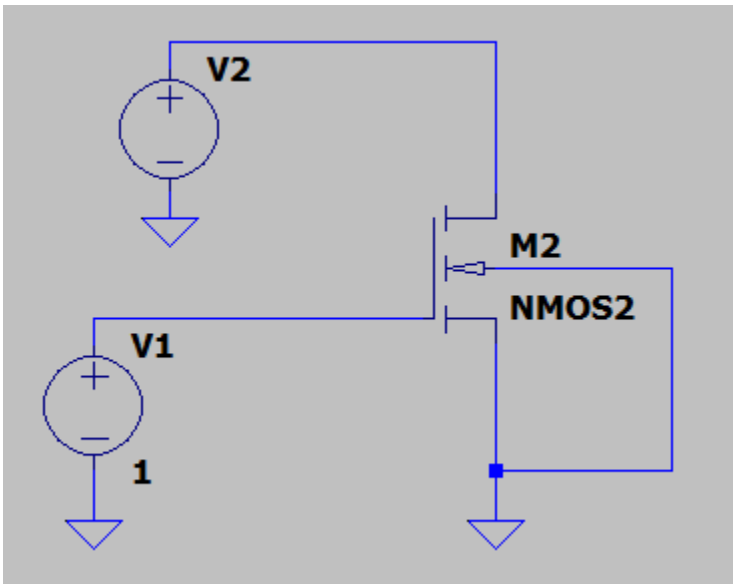

Figure 2: Schematic of the circuit used to calculate $V_{DS} - I_{DS}$ curves of the NMOS device for different V_{GS} voltages

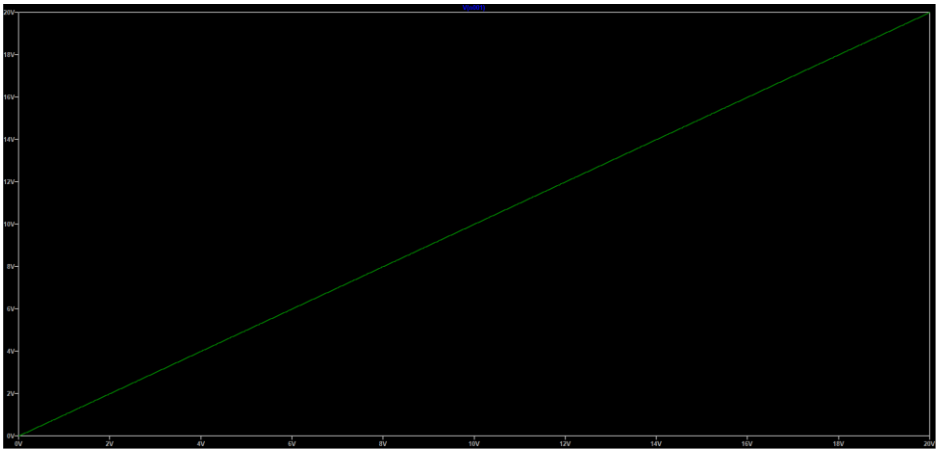

Figure 3: Graph of V_{DS} for the NMOS circuit.

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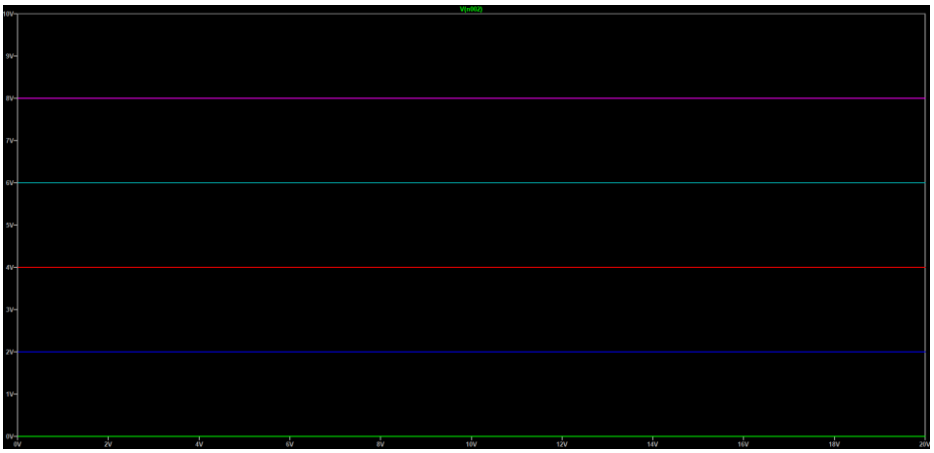

Figure 4: Graph of V_{GS} values of the NMOS circuit.

The color of the curves in figure 4 and the next 3 figures are consistent. So, the grey curve represents V_{GS} equals 10 volts, the pink curve represents V_{GS} equals 8 volts, and so forth.

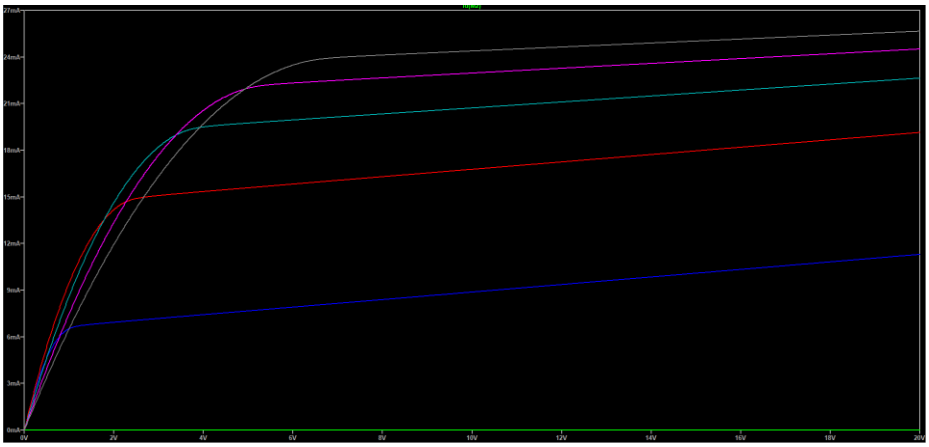

Figure 5: Graph of the $V_{DS} - I_{DS}$ curves of the NMOS device with (W/L) = 25µ/0.5µ for different V_{GS} voltages

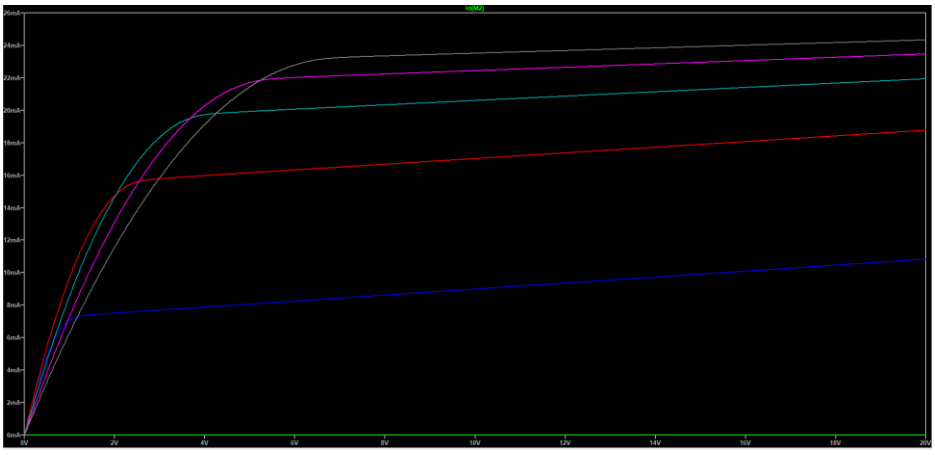

Figure 6: Graph of the $V_{DS} - I_{DS}$ curves of the NMOS device with (W/L) = 50µ/1µ for different V_{GS} voltages

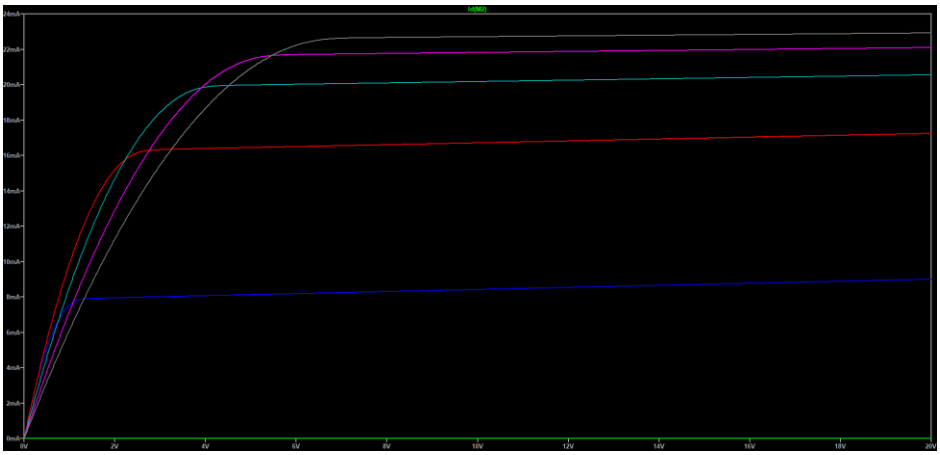

Figure 7: Graph of the $V_{DS} - I_{DS}$ curves of the NMOS device with (W/L) = 250µ/5µ for different V_{GS} voltages

Then to find the $V_{DS} - I_{DS}$ curves of the PMOS device for different V_{GS} voltages, I built the circuit in figure 8 then used 2 source DC sweep. V4 is a DC sweep with a small negative step size which goes from 0 to -20 volts and V1 is a DC sweep with a step size of -2 volts which goes from 0 to -10 volts.

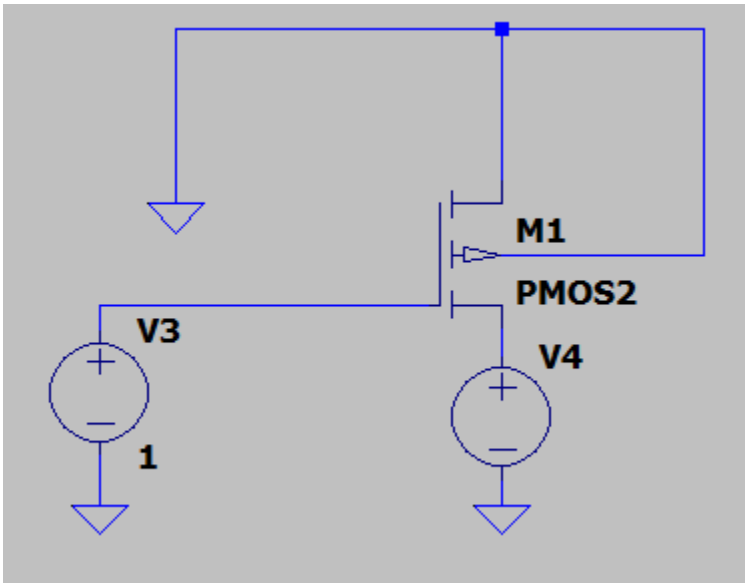

Figure 8: schematic of the circuit used to calculate $V_{DS} - I_{DS}$ curves of the PMOS device for different V_{GS} voltages

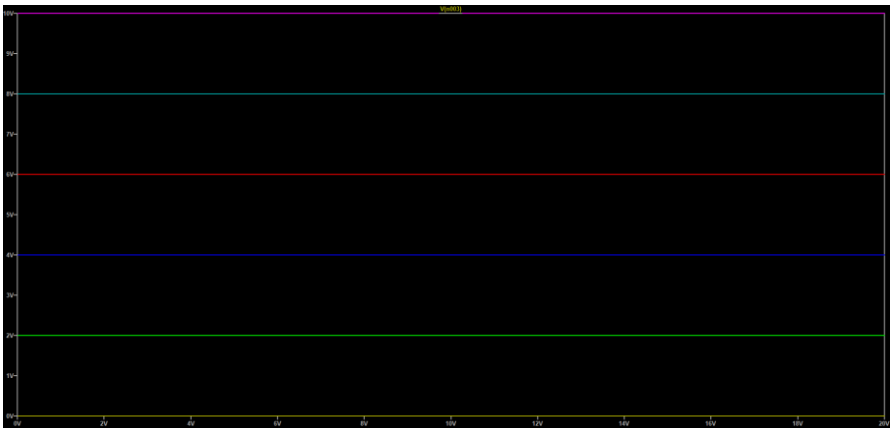

Figure 9: Graph of V_{SG} values of the NMOS circuit.

The color of the curves in figure 9 and the next 3 figures are again consistent. So, the pink curve represents V_{SG} equals 10 volts, the cyan curve represents V_{SG} equals 8 volts, and so forth.

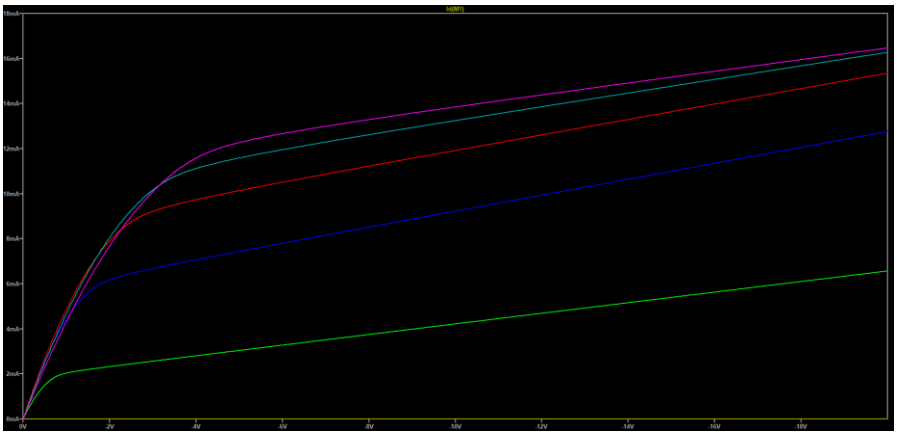

Figure 10: Graph of the $V_{DS} - I_{DS}$ curves of the NMOS device with (W/L) = 25µ/0.5µ for different V_{GS} voltages

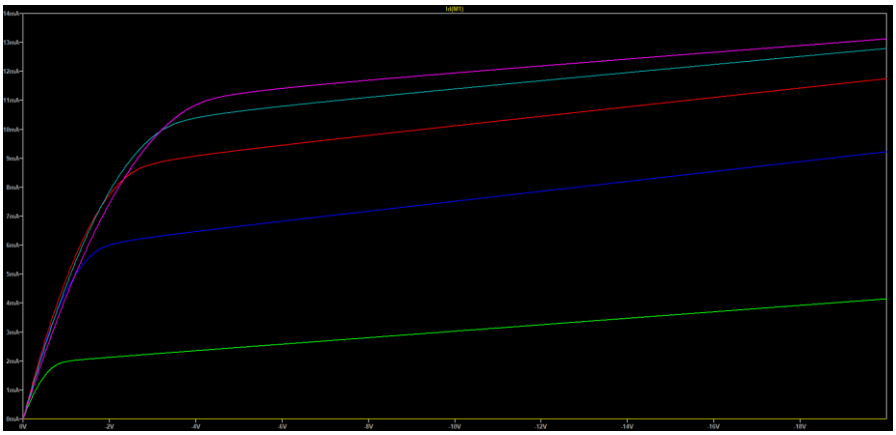

Figure 11: Graph of the $V_{DS} - I_{DS}$ curves of the NMOS device with (W/L) = 50µ/1µ for different V_{GS} voltages

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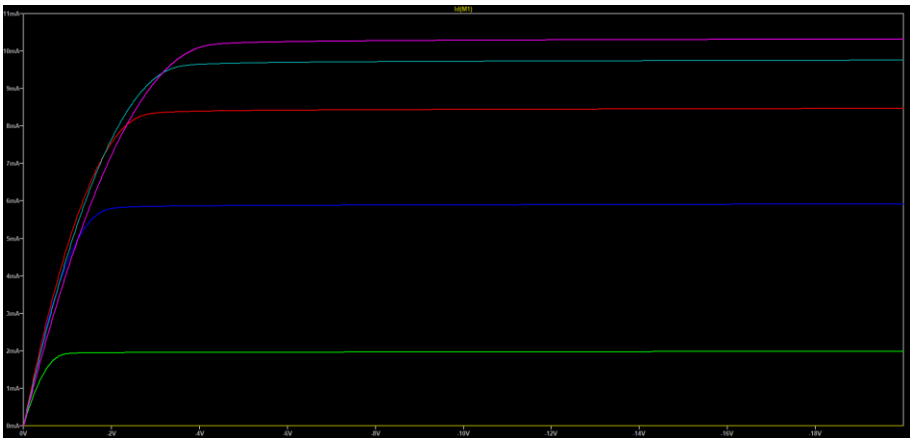

Figure 12: Graph of the $V_{DS} - I_{DS}$ curves of the NMOS device with (W/L) = 250µ/5µ for different V_{GS} voltages

In these graphs, we know the slope after saturation is λ. Because of this, I concluded channel length modulation effect (λ) decreases as W and L get bigger.

Then I used the current equation of an NMOS to find K_n:

$$I_D = K_N(V_{GS} - V_{tn})^2$$

$$\sqrt{I_D} = \sqrt{K_N}(V_{GS} - V_{tn})$$

From this, we can see slope of $\sqrt{I_D}\ vs\ V_{GS}$ is $\sqrt{K_N}$. Then to use this equation, I built the circuit in figure 13 and did a DC sweep over V5.

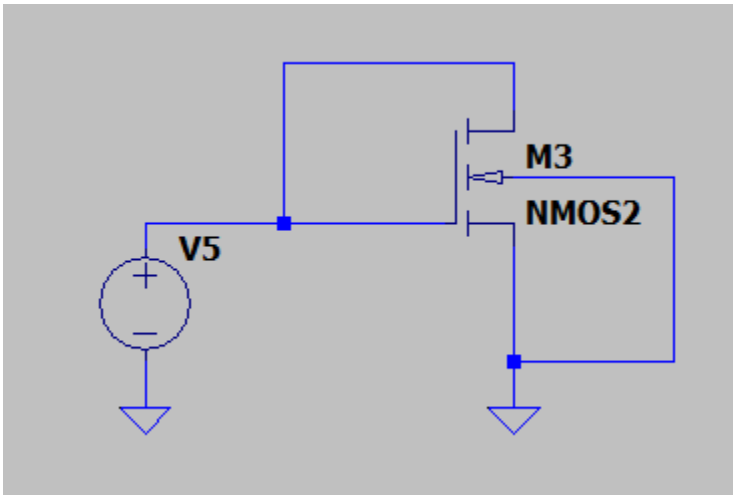

Figure 13: Schematic of the circuit used to find K_N

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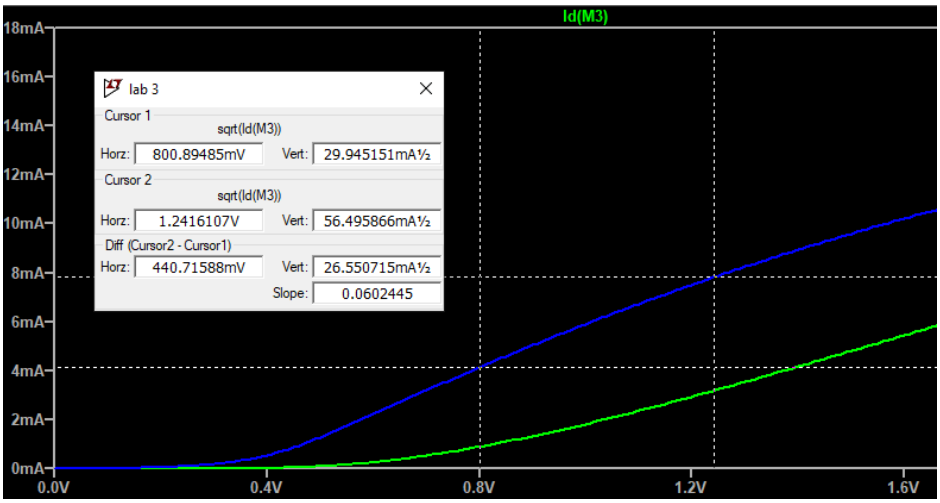

Figure 14: graph of $\sqrt{I_D}$ vs V_{GS} of NMOS

From figure 14 we can see the slope is 0.060 assuming our V_{GS} *and* V_{DS} values won't go to much over 1.25 volts. Then we can calculate K_N and K'_N as:

$$\sqrt{K_N} = 0.060$$

$$K_N = 3.629 mA/V^2$$

$$K_N = K'_N \frac{W}{2L} \quad , \quad \frac{W}{L} = 50$$

$$K'_N = 145.16\ \mu A/V^2$$

This time I used the current equation of a PMOS to find K_P:

$$I_D = K_P\left(V_{SG} - |V_{tp}|\right)^2$$

$$\sqrt{I_D} = \sqrt{K_P}(V_{SG} - |V_{tp}|)$$

From this, we can see slope of $\sqrt{I_D}$ *vs* V_{SG} is $\sqrt{K_P}$. Then to use this equation, I built the circuit in figure 15 and did a DC sweep over V6.

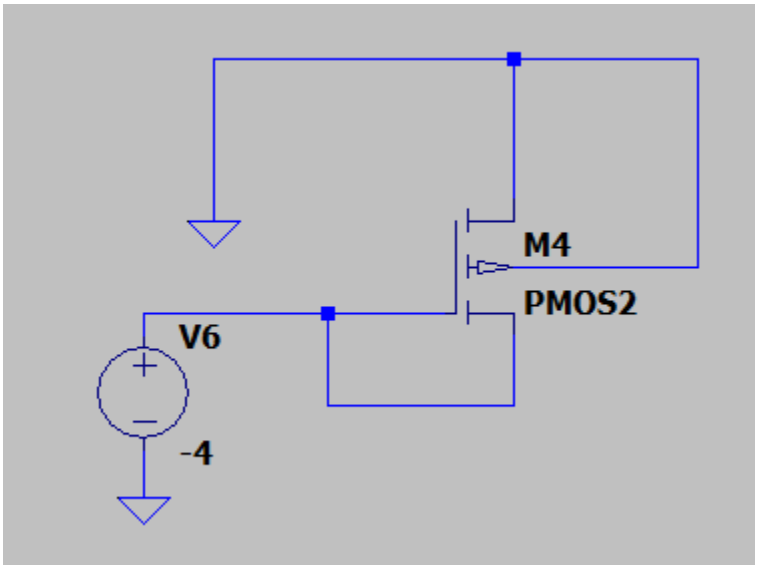

Figure 15: Schematic of the circuit used to find K_P

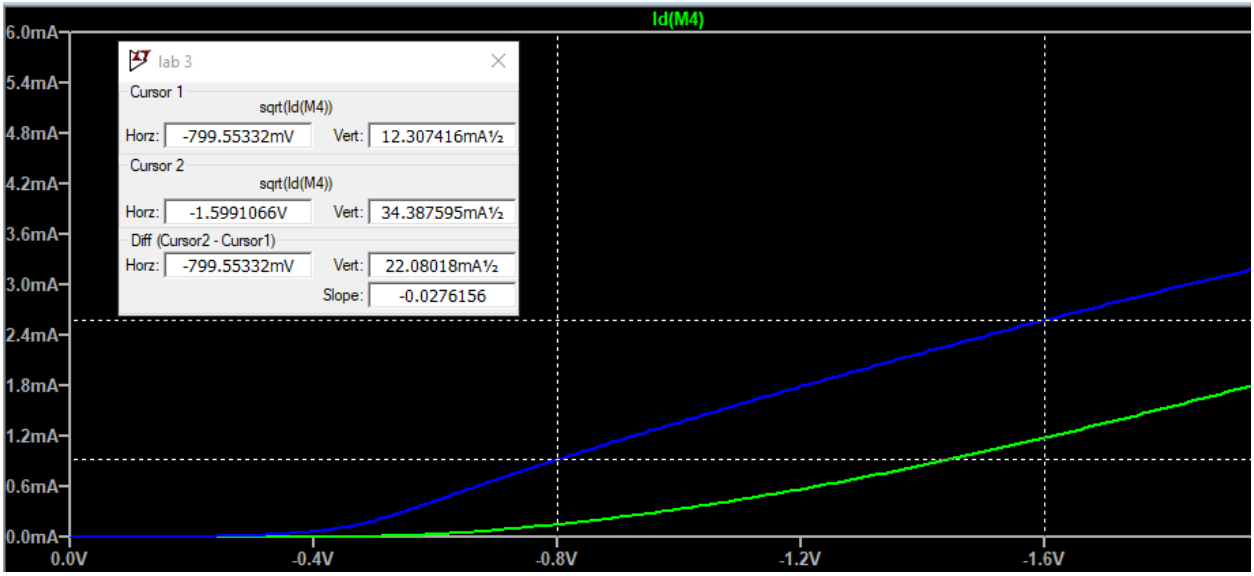

Figure 16: graph of $\sqrt{I_D}$ vs V_{GS} of PMOS

From figure 16 we can see the slope is -0.0276 assuming our V_{GS} *and* V_{DS} values won't go too much over 1.6 volts. Then we can calculate K_P and K_P' as:

$$\sqrt{K_P} = 0.0276$$

$$K_P = 0.729 mA/V^2$$

$$K_P = K_P' \frac{W}{2L} \quad , \quad \frac{W}{L} = 50$$

$$K_P' = 30.05\ \mu A/V^2$$

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To find V_{TN} and V_{TP} I will use the identity used in figure 17.

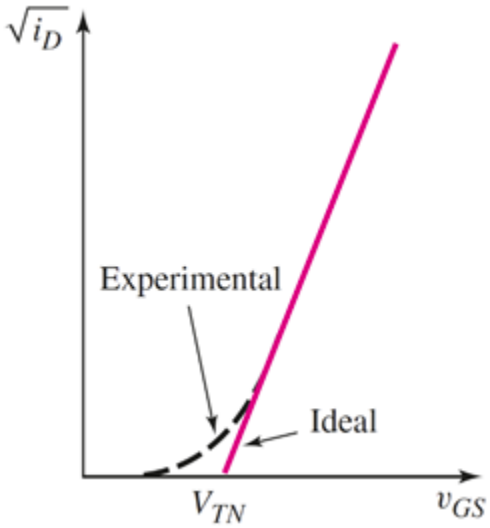

Figure 17: graph of $\sqrt{I_D}$ vs V_{GS} [1]

To get this graph I used the circuit in figure 13.

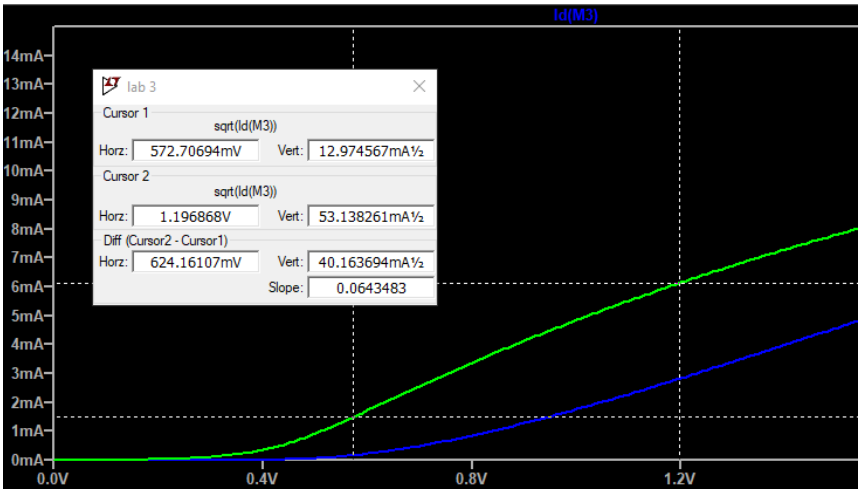

Figure 18: graph of $\sqrt{I_D}$ vs V_{GS} of NMOS

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To calculate V_{TN} I took the smallest point of the area we used to calculate the slope, $\sqrt{I_D} = 12.97mA^{1/2}$,and $V_{GS} = 572.7mV$ with a slope of 0.0643 then:

$$zero\ intercet = \frac{1}{slope} * \left(-\sqrt{I_D}\right) + V_{GS}$$

$$zero\ intercet = \frac{1}{0.0643} * (-12.97m) + 572.7m$$

$$V_{TN} = 0.371\ V$$

Then to calculate V_{TP} I used the same method but this time with the circuit in figure 15.

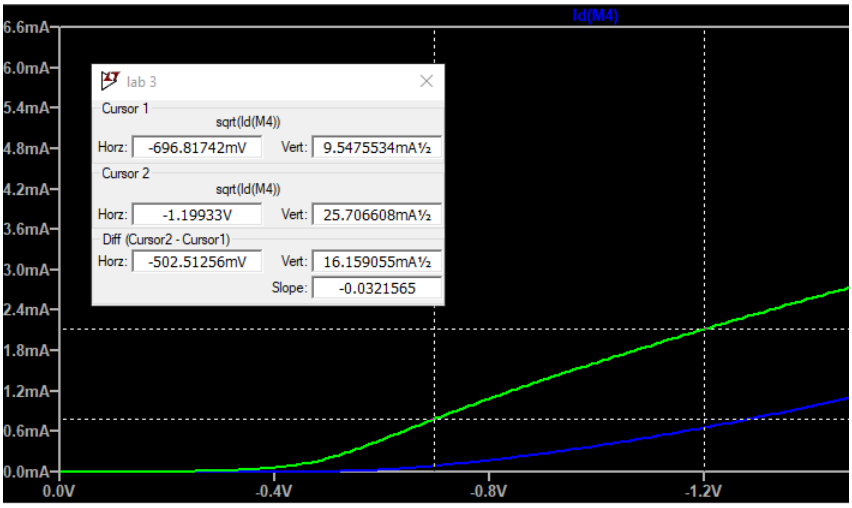

Figure 19: graph of $\sqrt{I_D}$ vs V_{GS} of NMOS

To calculate V_{TP} I took the smallest point of the area we used to calculate the slope. $\sqrt{I_D} = 9.55mA^{1/2}$ and $V_{GS} = 696.8mV$ with a slope of 0.0322 then:

$$zero\ intercet = \frac{1}{slope} * \left(-\sqrt{I_D}\right) + V_{SG}$$

$$zero\ intercet = \frac{1}{0.0322} * (-9.55m) + 696.8m$$

$$V_{TP} = -0.400\ V$$

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b. Part B:

In this part, we are asked to find the (W/L) values of the transistors M1 to M6 such that we get |Vout1/Vin|>34. Then look at why we need C_0 and what would happen if we didn't have C_0.

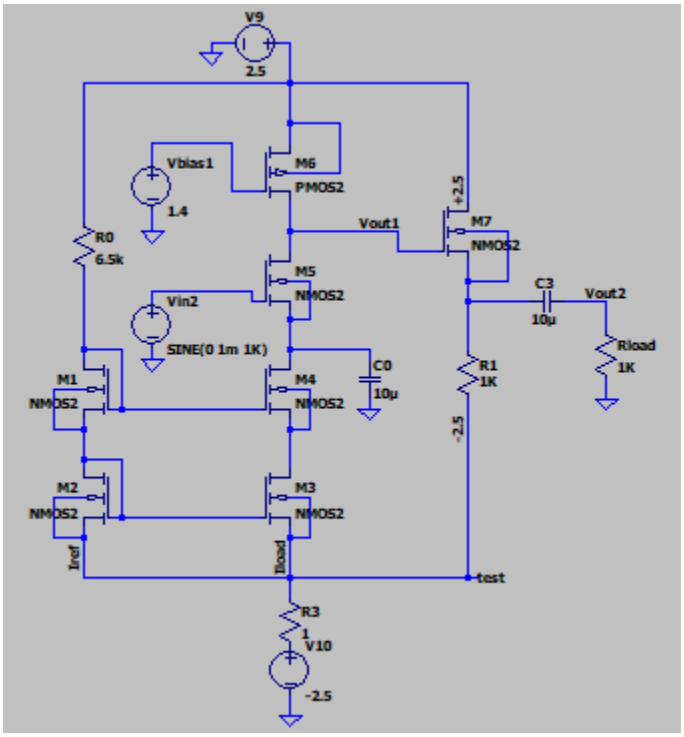

Figure 20: Schematic of the circuit I built in LTSpice.

$$I_{ref} = 0.5mA \; and \; I_{load} = 1.5mA$$

We are told to assume all the transistors are in saturation and try to satisfy that condition.

The leftmost side of the circuit is not affected by the rest of the circuit because of this I will first find $(W/L)_1$ and $(W/L)_2$. We know the current on that branch so we can calculate V_{D1}.

$$V_{D1} = V_+ - R_0 * I_{ref}$$

$$V_{D1} = 2.5 - 6.5K * 0.5m$$

$$V_{D1} = -0.75\,V$$

I will choose $(W/L)_1 = (W/L)_2$ to make the computations easier.

This means $V_{GS1} = V_{DS1} = V_{GS2} = V_{DS2}$ using this and the current equation of a saturated NMOS transistor I can calculate $(W/L)_1$ and $(W/L)_2$

$$V_{D1} - V_{-} = V_{DS1} + V_{DS2}$$

$$1.75 = 2V_{DS1}$$

$$V_{DS1} = 0.875$$

$$I_{ref} = K_{N1}(V_{DS1} - V_{TN})^2$$

$$0.5m = K_{N1}(0.875 - 0.371)^2$$

$$K_{N1} = \frac{0.5m}{(0.875 - 0.371)^2}$$

$$K_{N1} = \frac{0.5m}{(0.875 - 0.371)^2}$$

$$K_{N1} = 1.97m\ A/V^2$$

$$K_N' = 145.16\ \mu A/V^2$$

$$K_N = \frac{K_N' W}{2L}$$

$$1.97m = 145.16u \cdot \left(\frac{1}{2}\right) \cdot \left(\frac{W}{L}\right)_1$$

$$\left(\frac{W}{L}\right)_1 = 27.14 = 27$$

Then

$$\left(\frac{W}{L}\right)_2 = 27$$

After testing this result on the left side of the circuit. With $w = 27\mu$, $L = 1\mu$ I saw:

Figure 21: Graph of current I_{ref} for $w_1 = w_2 = 27\mu$, $L_1 = L_2 = 1\mu$

0.51 mA is really close to our desired current of 0.5mA but there is a small difference because of the ignored channel length modulation effect (λ). After this, I tried $w = 13.5\mu$, $L = 0.5\mu$:

Figure 22: Graph of current I_{ref} for $w_1 = w_2 = 13.5\mu$, $L_1 = L_2 = 0.5\mu$

Then I saw $I_{ref} = 0.4998\ mA$ which is closer to 0.5 mA so I used $w = 13.5\mu$, $L = 0.5\mu$ for M1 and M2.

Then we know $V_{GS2} = V_{GS3}$ because they are directly connected.

Now we will find $(W/L)_3$ and $(W/L)_4$. For this, I will again use the current equation of a saturated NMOS. $I_{load}\ is\ 1.5V\ and\ I_{ref}\ is\ 0.5V$ to satisfy these equations we need $(W/L)_3$ and $(W/L)_2$ to have the same ratio as $I_{load}\ and\ I_{ref}$. So:

$$(W/L)_3 = 3 \cdot (W/L)_2$$

$$(W/L)_3 = 81$$

Then I assumed V_{DS3} is really close to V_{DS2} so I can write: (this assumption requires I_{load} to not change much)

$$V_{GS1} = V_{GS4}$$

So, like the previous transistor M1 and M4 must hold the (W/L) ratio, so:

$$(W/L)_4 = 3 \cdot (W/L)_1$$

$$(W/L)_4 = 81$$

I chouse $w = 40.5\mu$, $L = 0.5\mu$ for M3 and M4

We also have all the needed information to find $(W/L)_6$, we use the saturated PMOS current equation.

$$I_{load} = K_{P6}(V_{SG} - |V_{TP}|)^2$$

$$1.5m = K_{P6}\big((2.5 - 1.4) - 0.4\big)^2$$

$$\frac{1.5m}{0.7^2} = K_{P6}$$

$$K_{P6} = 3.06m\ A/V^2$$

$$K_P' = 30.05\ \mu\ A/V^2$$

$$K_P = \frac{K_P' W}{2L}$$

$$3.06m = 30.05u \cdot \frac{1}{2} \cdot (W/L)_6$$

$$(W/L)_6 = 203$$

I chose $w = 203\mu$, $L = 1\mu$ for M6.

After this, I chose $w = 0.2m$, $L = 2\mu$ for M5 so I can test if my previous choices were correct. The amplitude of V_{in} is 0V. I can do this because the middle and left part of the circuit is not affected by the right side of the circuit.

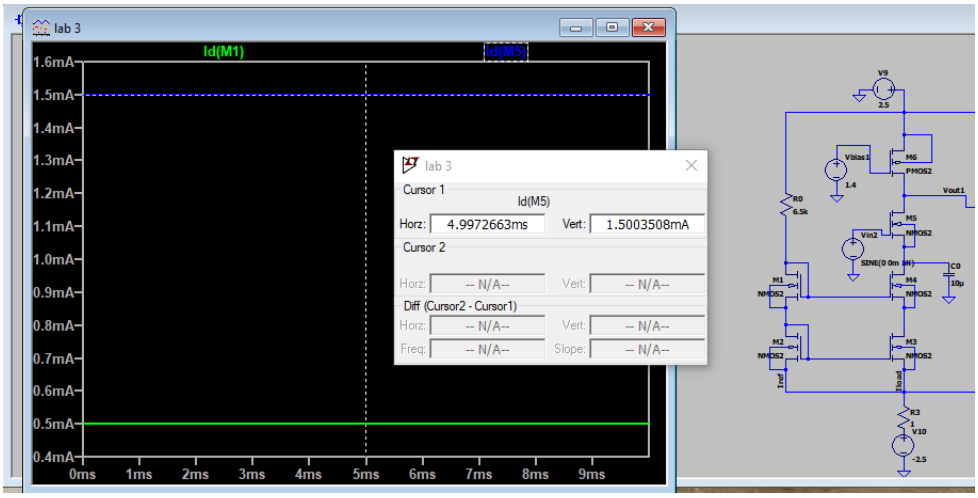

Figure 23: Graph of current I_{ref} for $w_3 = w_4 = 40.5\mu$, $L_3 = L_4 = 0.5\mu$ and $w_6 = 203\mu$, $L_6 = 1\mu$

I saw $I_{load} = 1.5\ mA$ which is what we wanted. Then I checked if all the transistors are in saturation. I saw all except M6 were in saturation. The voltage over M6 was 0.27V.

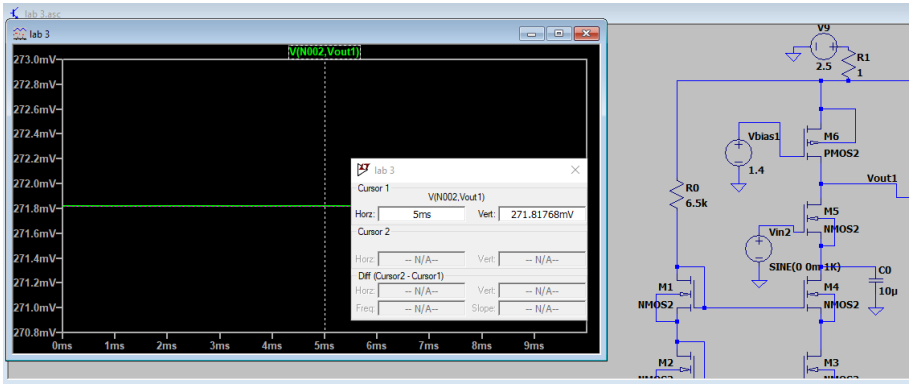

Figure 24: Graph of V_{SD6} for $w_3 = w_4 = 40.5\mu$, $L_3 = L_4 = 0.5\mu$ and $w_6 = 203\mu$, $L_6 = 1\mu$

To fix this I knew I needed to lower K_N because doing so would increase the voltage over the transistor. I lowered M6's (W/L) ratio to 153 and choose $w = 153\mu$, $L = 1\mu$

Then I saw I_{load} was 1.499 mA. Which is what we wanted.

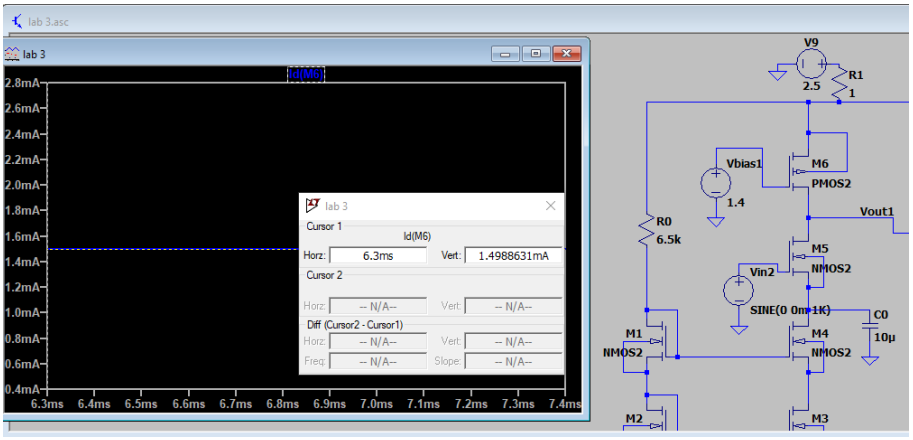

Figure 25: Graph of current I_{ref} for $w_3 = w_4 = 40.5\mu$, $L_3 = L_4 = 0.5\mu$ and $w_6 = 153\mu$, $L_6 = 1\mu$

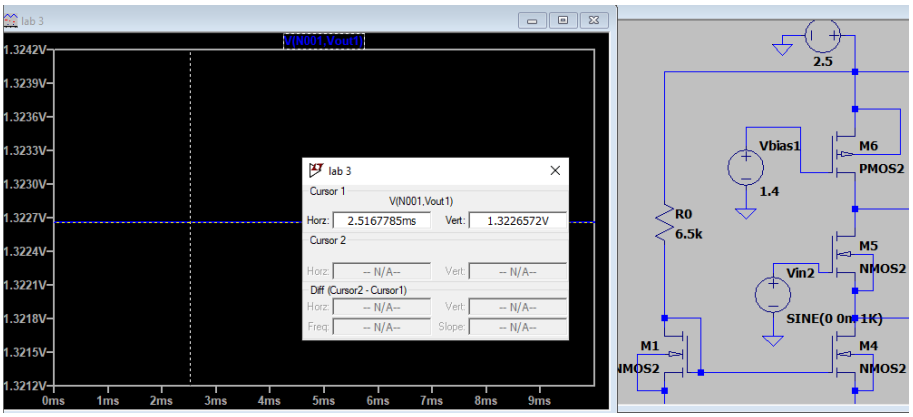

Figure 26: Graph of V_{SD6} for $w_3 = w_4 = 40.5\mu$, $L_3 = L_4 = 0.5\mu$ and $w_6 = 203\mu$, $L_6 = 1\mu$

We can see M6 is in saturation too. Now to find M5, we first need to look at the gain at V_{out1}. We only need $|A_{V1}| > 34$ but there is no limit to how big the gain should be. So, we will aim to get the biggest gain we can get and see if it is bigger than 34. To do this we first need to see what the gain depends on. For this, we can look at the small-signal model of M5.

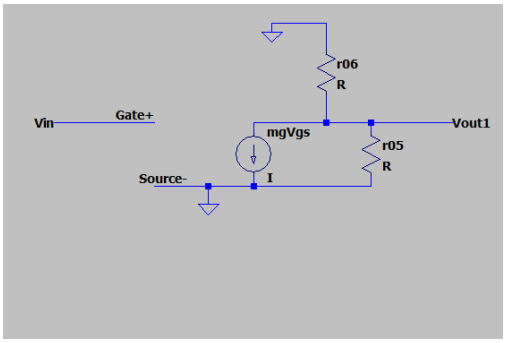

Figure 27: Small signal model of M5

Now if we calculate the gain.

$$KCL\ at\ V_{out1}: \frac{V_{out1}}{r_{05}} + mg(V_{in} - 0) + \frac{V_{out1}}{r_{06}} = 0$$

$$V_{out1}r_{06} + mgV_{in}r_{06}r_{05} + V_{out1}r_{05} = 0$$

$$V_{out1}(r_{06} + r_{05}) = -V_{in}mgr_{06}r_{05}$$

$$A_{V1} = \frac{V_{out1}}{V_{in}} = -\frac{mgr_{06}r_{05}}{(r_{06} + r_{05})}$$

We can see the gain is directly proportional to mg and increasing the value of r_{05} increases the gain. We won't be changing the M6's values so r_{06} can be seen as constant. We also know the formula mg for the idealistic case.

$$mg = 2\sqrt{K_N I_{DQ}}$$

We already know I_{DQ} is 1.5mA and it should be a constant. And the real-life version of this formula can't be too different than this so to increase mg we need to pick K_{N5} as big as possible. But we can not choose K_{N5} arbitrarily large because if K_{N5} is too large M5 won't be in saturation. So now I will find the smallest K_{N5} which will make M5 not in saturation and pick a value smaller than that.

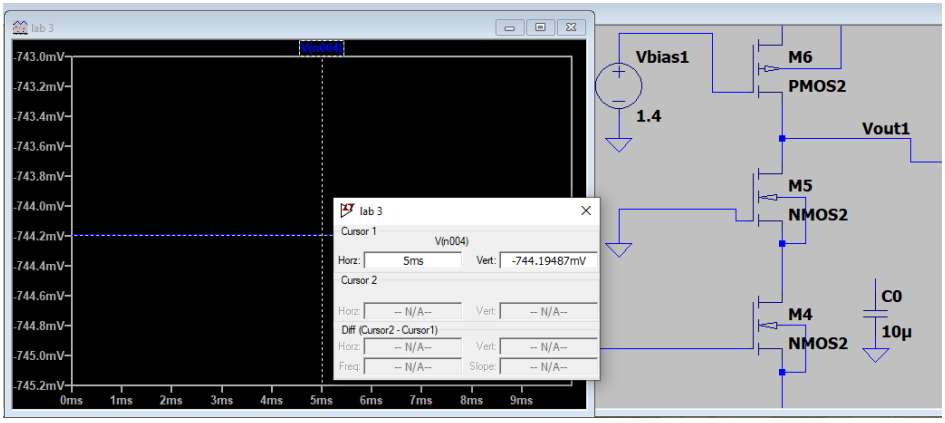

Figure 28: DC analyze schematic of M5 and the Voltage at V_{D4}

This measurement is done with an M5 value which doesn't put M5 out of saturation but we are trying to find the K_{N5} value which is just on the edge of the saturation so the current I_{load} and the voltage value of V_{D4} can not jump to a point far from this so we will take them as:

$$I_{load} = 1.5\ mA\ , V_{D4} = -0.744\ V$$

The condition for NMOS saturation is:

$$V_{DS} > V_{GS} - V_{tn}$$

To find the border case I will calculate :

$$V_{DS} = V_{GS} - V_{tn}$$

We calculated V_{tn} in part 1. $V_{tn} = \ 0.37\ V$ and V_{GS} can be calculated because we know V_{G5} and V_{S5}.

$$V_{GS5} = 0 - (-0.744) = 0.744\ V$$

$$V_{DS5} = 0.744 - 0.370 = 0.374$$

Now we can put our value inside of the triode region NMOS current equation.

$$I_{DQ} = K_{N5}(2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2)$$

$$1.5m = K_{N5}[2(0.744 - 0.370)0.374 - 0.374^2]$$

$$1.5m = K_{N5}0.374^2$$

$$K_{N5} = \frac{1.5m}{0.374^2}$$

$$K_{N5} = 10.72\ m\ A/V^2$$

$$K_N = K_N' \frac{W}{2L} \quad , \quad K_N' = 145.16 \frac{\mu A}{V^2}$$

$$10.72\ m = 145.16\mu \frac{(W/L)_5}{2}$$

$$(W/L)_5 = 147.8$$

We also know $r_0 = \frac{1}{\lambda I_{DQ}}$ so I will choose L as big as possible to make λ_5 smaller and r_{05} bigger. To make sure I am inside of the saturation range I choose $(W/L)_5 = 146$ and $w = 292\mu$ and $L = 2\mu$.

After this, I connected $V_{in} = 1\cos(2000\pi t)\, mV$ and looked at the gain of the circuit.

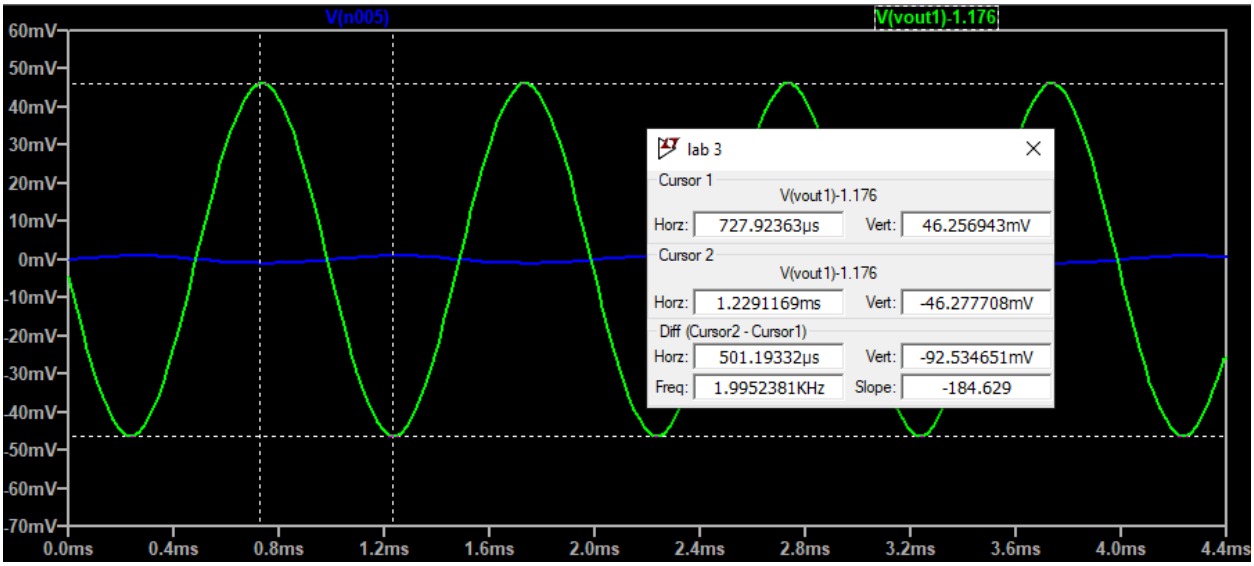

Figure 29: Graph of V_{in} and V_{out1} vs time

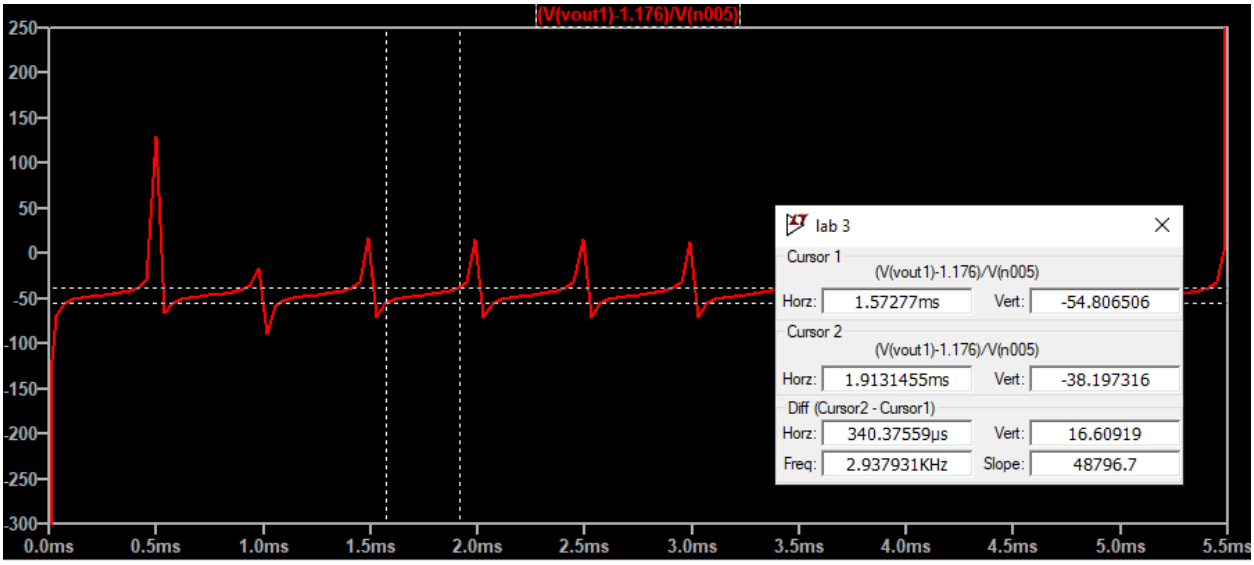

Figure 30: Graph of (V_{in} / V_{out}) vs time

The gain is around -46 which is over the needed 34 gain. It is not constant because the capacitor in the circuit is adding some delay to the circuit. This will be discussed further in the discussion part.

$$A_V = V_{out1}/V_{in} \cong -46$$

Also, the current I_{load} is still 1.5 mA.

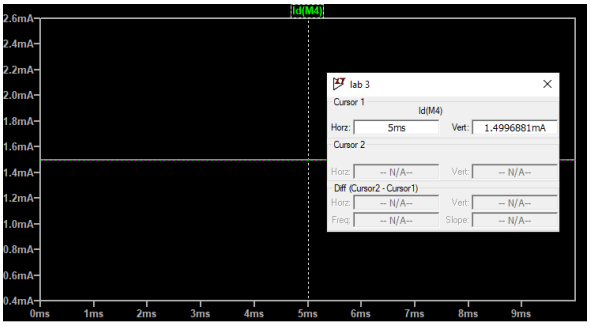

Figure 31: Graph of I_{load} vs time

Now I will put all the V_{DS} and V_{GS} values of the 6 transistors and prove they are in saturation. Using $V_{DS} > V_{GS} - V_{TN}$ for NMOS saturation condition and $V_{SD} > V_{SG} - |V_{TP}|$ for the PMOS saturation condition

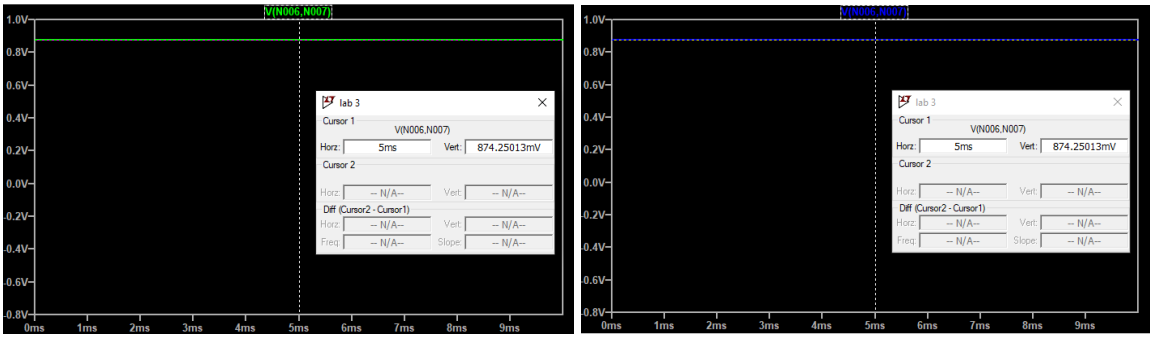

Figure 32: Graph of V_{DS1} vs time and Graph of V_{GS1} vs time

$$V_{DS1} = 0.874\,V, V_{GS1} = 0.874\,V\,, V_{TN} = 0.37\,V$$

$$0.874\ > 0.874 - 0.37$$

The saturation of M1 is proven.

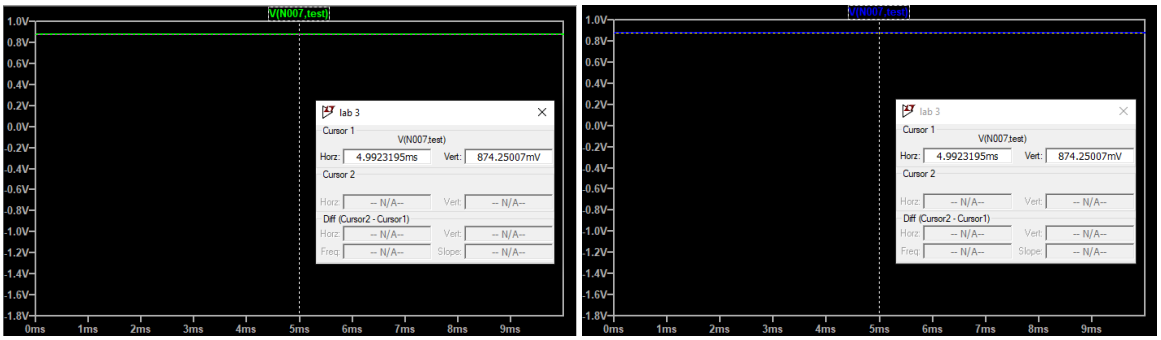

Figure 33: Graph of V_{DS2} vs time and Graph of V_{GS2} vs time

$$V_{DS2} = 0.8743\,V, V_{GS2} = 0.8743\,V\,, V_{TN} = 0.37\,V$$

$$0.8743\ > 0.8743 - 0.37$$

The saturation of M2 is proven.

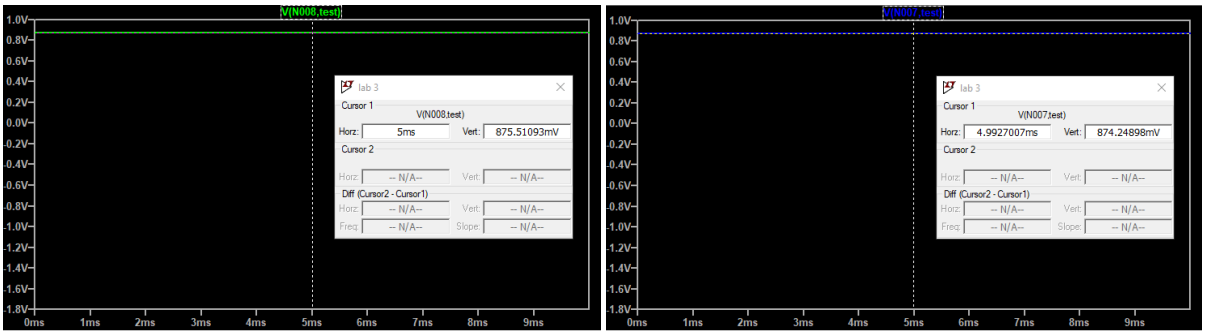

Figure 34: Graph of V_{DS3} vs time and Graph of V_{GS3} vs time

$$V_{DS3} = 0.8755\,V, V_{GS3} = 0.8742\,V\,, V_{TN} = 0.37\,V$$

$$0.8755\ > 0.8742 - 0.37$$

The saturation of M3 is proven.

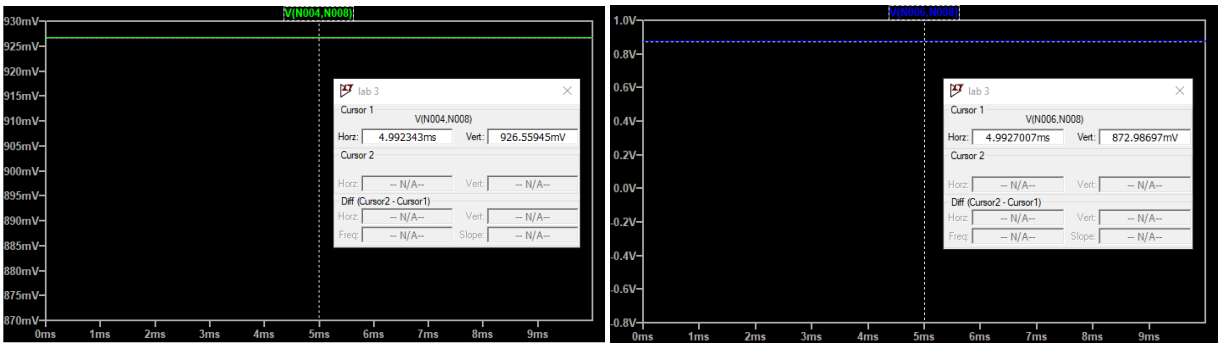

Figure 35: Graph of V_{DS4} vs time and Graph of V_{GS4} vs time

$$V_{DS4} = 0.9266\,V, V_{GS3} = 0.8730\,V\,, V_{TN} = 0.37\,V$$

$$0.9266\ > 0.8730 - 0.37$$

The saturation of M4 is proven.

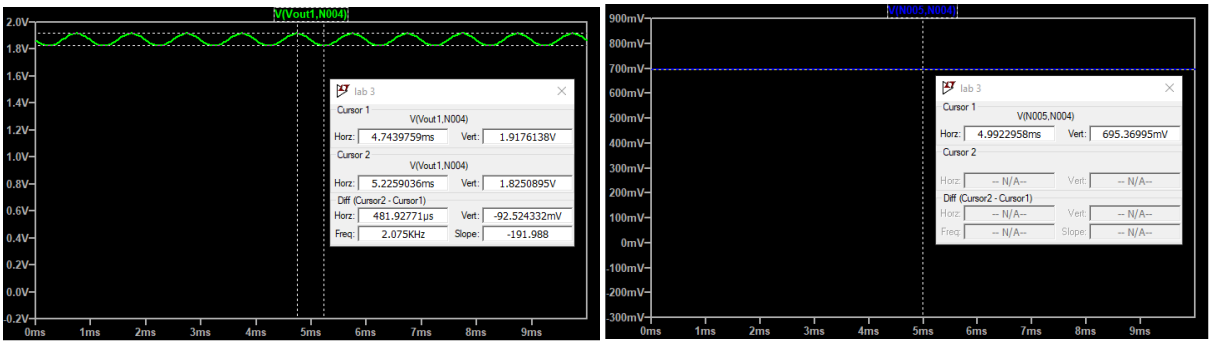

Figure 36: Graph of V_{DS5} vs time and Graph of V_{GS5} vs time

$$1.825\,V\ \leq V_{DS5}\ \leq\ 1.918\,V\,, V_{GS5} = 0.6954\,V\,, V_{TN} = 0.37\,V$$

$$1.882\ > 0.7442 - 0.37$$

The saturation of M5 is proven.

V_{DS5} will be discussed further in the discussion part.

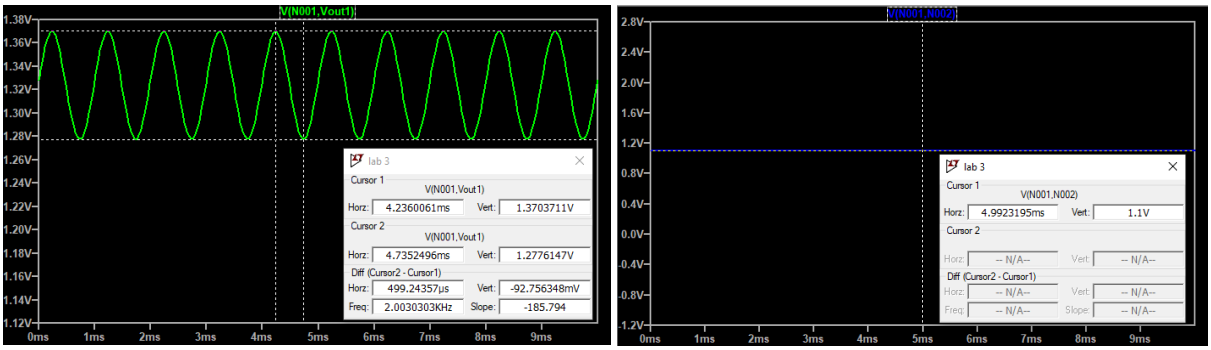

Figure 37: Graph of V_{DS6} vs time and Graph of V_{GS6} vs time

$$1.278\,V \leq V_{SD6} \leq 1.370\,V\,, V_{SG6} = 1.1\,V \quad , \quad V_{TP} = -0.4\,V$$

$$1.282 > 1.1 - 0.4$$

The saturation of M6 is proven.

Without C_0 the gain becomes next to nothing, 1666 times smaller than the original gain.

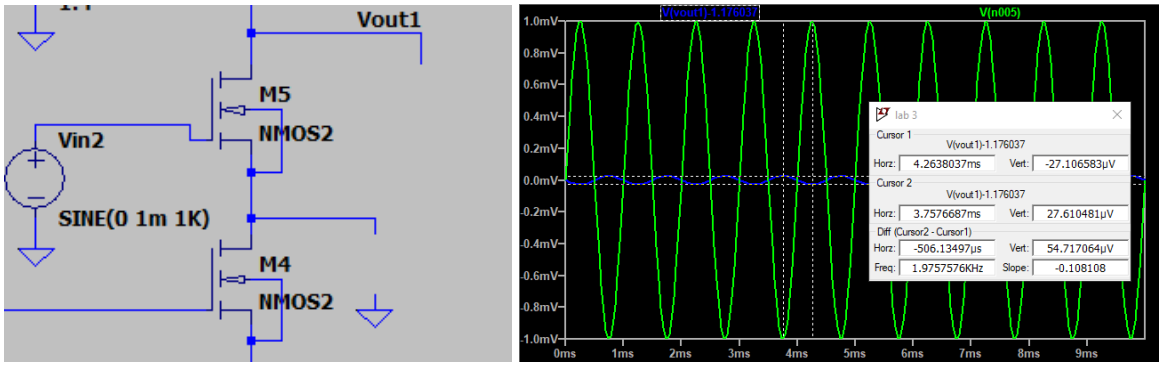

Figure 38: Circuit schematic without C_0 and V_{out1} vs time, V_{in} vs time for this circuit.

$$A_{VnoC_0} \cong -\frac{27\mu}{1m} = -0.027$$

To explain why this happens we need to look at the small signal-model of the M5.

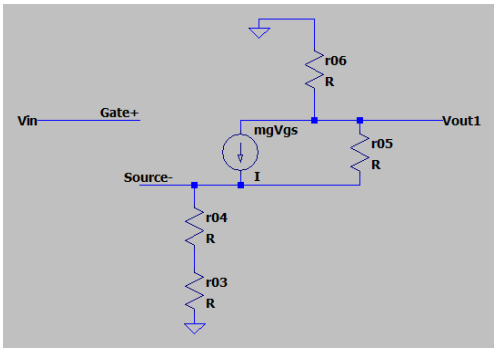

Figure 39: The small-signal model of M5 without C_0

Here $r_{03}, r_{04}, r_{05}, r_{06}$ represent small-signal output resistance of M3, M4, M5, M6 respectively.

If we write the symbolic equation for V_{out1} in terms of V_{in}

$$KCL\ at\ V_S: \frac{V_S}{r_{04}+r_{03}} - mg(V_{in}-V_S) + \frac{V_S - V_{out1}}{r_{05}} = 0$$

$$KCL\ at\ V_{out1}: \frac{V_{out1}-V_S}{r_{05}} + mg(V_{in}-V_S) + \frac{V_{out1}}{r_{06}} = 0$$

$$\frac{V_S}{r_{04}+r_{03}} + \frac{V_{out1}}{r_{06}} = 0$$

$$V_S = -\frac{V_{out1}}{r_{06}}(r_{04}+r_{03})$$

$$\frac{V_S}{r_{04}+r_{03}} - mg(V_{in}-V_S) + \frac{V_S - V_{out1}}{r_{05}} = 0$$

$$V_S r_{05} - mg(V_{in}-V_S)(r_{04}+r_{03})r_{05} + (V_S - V_{out1})(r_{04}+r_{03}) = 0$$

$$V_S[r_{05} + mg(r_{04}+r_{03})r_{05} + (r_{04}+r_{03})] - V_{out1}(r_{04}+r_{03}) = V_{in}(mg(r_{04}+r_{03})r_{05})$$

$$-\frac{V_{out1}}{r_{06}}(r_{04}+r_{03})[r_{05} + mg(r_{04}+r_{03})r_{05} + (r_{04}+r_{03})] - V_{out1}(r_{04}+r_{03}) = V_{in}(mg(r_{04}+r_{03})r_{05})$$

$$-V_{out1}(r_{04}+r_{03})[r_{05} + mg(r_{04}+r_{03})r_{05} + (r_{04}+r_{03}) + r_{06}] = V_{in}(r_{04}+r_{03})mgr_{05}$$

$$A_{VnoC_0} = \frac{V_{out1}}{V_{in}} = -\frac{mgr_{05}}{r_{05} + mg(r_{04}+r_{03})r_{05} + (r_{04}+r_{03}) + r_{06}}$$

All r_0 values are close to each other and roughly 4 KΩ. $r_0's$ will be further discussed in the discussion. If we compare A_{VnoC_0} with A_{V1} we can see A_{VnoC_0} is missing the r_{06} from its nominator and also its denominator is bigger because of the added terms with $(r_{04}+r_{03})$. If we look at it mathematically A_{VnoC_0}could be 10000 times smaller than A_{V1}. So, the 1666 times drop is more than justified.

If we look at the situation in a practical way the small-signal output resistance's of M3, M4 are drawing current and stealing most of our gain. To prevent this, we need C_0 to get them out of the small-signal model by grounding the terminal they are connected to the circuit.

As a side note if we ground V_{D4} without C_0 then V_{GS5} becomes 0 this closes M5. Then I_{load} becomes 0 and the circuit doesn't function at all.

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27.10.2020

c. Part C:

In this part, we are asked to Connect C_1 and R_{load} to V_{out1} directly without M7. Then look at the gain and find why we need M7.

If we Connect C_1 and R_{load} to V_{out1} directly without M7, we lose most of our gain from the initial part of the circuit and the gain drops down to around -8.

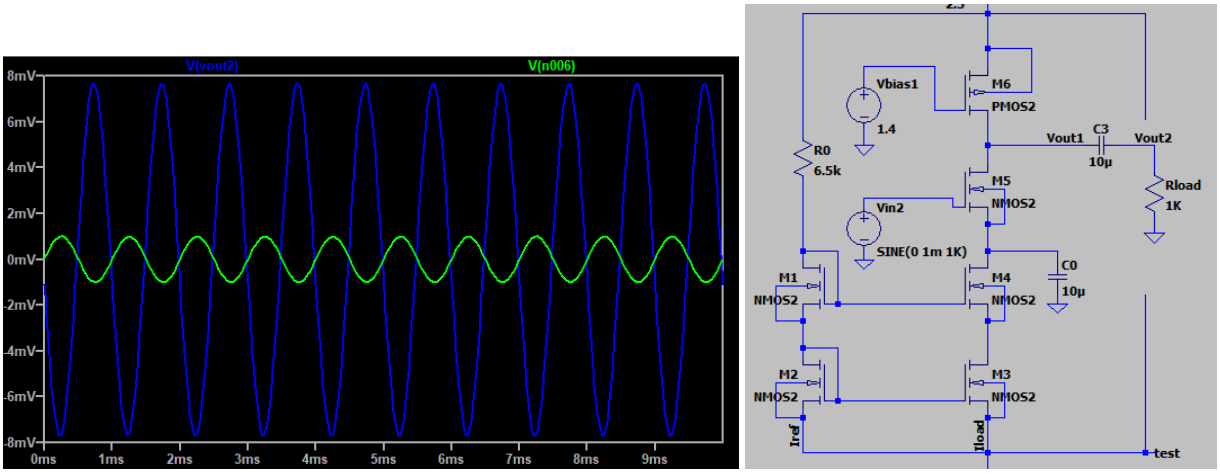

Figure 40: (V_{out2}/V_{in}) gain of the circuit without M7 and the circuit without M7

The reason for this can be seen if we look at the small-signal model of the circuit.

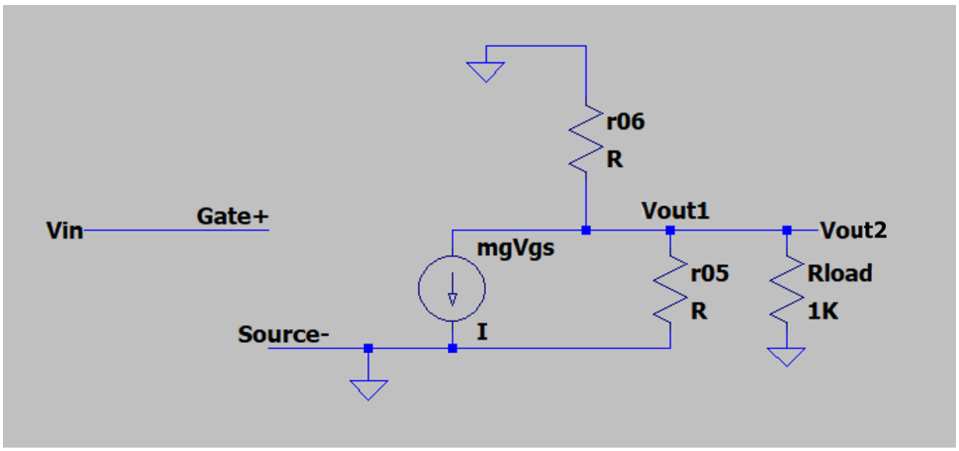

Figure 41: Small signal model of M5 without M7

$$KCL\ at\ V_{out2}: \frac{V_{out2}}{r_{06}} + \frac{V_{out2}}{r_{05}} + \frac{V_{out2}}{R_{load}} + gm(V_{in} - 0)$$

$$V_{out2}(r_{05}R_{load}) + V_{out2}\,(r_{06}R_{load}) + V_{out2}(r_{06}r_{05}) + r_{06}r_{05}R_{load}\ gmV_{in} = 0$$

$$V_{out2}[(r_{05}R_{load}) + (r_{06}R_{load}) + (r_{06}r_{05})] = -r_{06}r_{05}R_{load}\ gmV_{in}$$

$$A_{VnoM7} = \frac{V_{out2}}{V_{in}} = -\frac{r_{06}r_{05}R_{load}gm}{R_{load}(r_{06} + r_{05}) + (r_{06}r_{05})}$$

Compared to the gain from part 2 ($A_V = \frac{V_{out1}}{V_{in}} = -\frac{mgr_{06}r_{05}}{(r_{06}+r_{05})}$) A_{VnoM7} is smaller because its nominator has the extra R_{load} term which is 1K but the denominator also has the R_{load} term and on top of that it has +$(r_{06}r_{05})$ which is roughly 5 times of $R_{load}(r_{06}+r_{05})$. So, we can roughly write the gain as

$$A_{VnoM7} = \frac{V_{out2}}{V_{in}} \approx -\frac{r_{06}r_{05}R_{load}gm}{R_{load}(r_{06}+r_{05}) + 5R_{load}(r_{06}+r_{05})} = \frac{r_{06}r_{05}gm}{6(r_{06}+r_{05})} \approx \frac{1}{6}A_V$$

As we can see 1/6 of the previous gain for the circuit is really mathematically correlated.

If we think of the situation practically R_{load} decreases the overall resistance which we see the V_{out2} on. To prevent this, we need to put a buffer between V_{out1} and the load. M7 holds this purpose it is there so the load resistance doesn't lower the gain from the rest of the circuit.

d. Part D:

In this part, we are asked to find $(W/L)_7$ and R_1 such that we get $\left|V_{out2}/V_{in}\right| > 30$.

To find the W/L of M7 we first need to look at the small-signal model of M7.

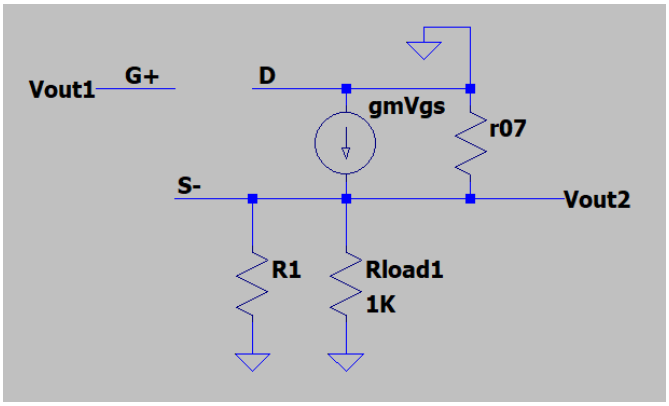

Figure 42: small signal model of M7

$$V_{GS} = V_{out1} - V_{out2}$$

Then we will write KCL at V_{out2}:

$$\frac{V_{out2}}{R_1} + \frac{V_{out2}}{1K} + \frac{V_{out2}}{r_{07}} - gm(V_{out1} - V_{out2}) = 0$$

$$V_{out2}r_{07}K + V_{out2}R_1r_{07} + V_{out2}R_1K - gm(V_{out1} - V_{out2})R_1r_{07}K = 0$$

$$V_{out2}(r_{07}K + R_1r_{07} + R_1K + gmR_1r_{07}K) = gmV_{out1}R_1r_{07}K$$

$$A_{V2} = \frac{V_{out2}}{V_{out1}} = \frac{gmR_1r_{07}K}{r_{07}K + R_1r_{07} + R_1K + gmR_1r_{07}K}$$

$$A_{V2} = \frac{V_{out2}}{V_{out1}} = \frac{1}{\frac{1}{gmR_1} + \frac{1}{gm1000} + \frac{1}{gmr_{07}} + 1}$$

To make A_{V2} as big as possible we need to make $\frac{1}{gmR_1} + \frac{1}{gm1000} + \frac{1}{gmr_{07}} + 1$ as small as possible. To do this we need to choose gm, R_1, r_{07} as big as possible.

We already know to make gm bigger we need to make K_N bigger and to make r_0 bigger we need to make λ bigger. So, I will choose $L = 2\mu$.

To find how big we can choose $(\mathrm{W/L})_7$ and R_1 we need to look at the DC analysis of M7 and look at its saturation conditions.

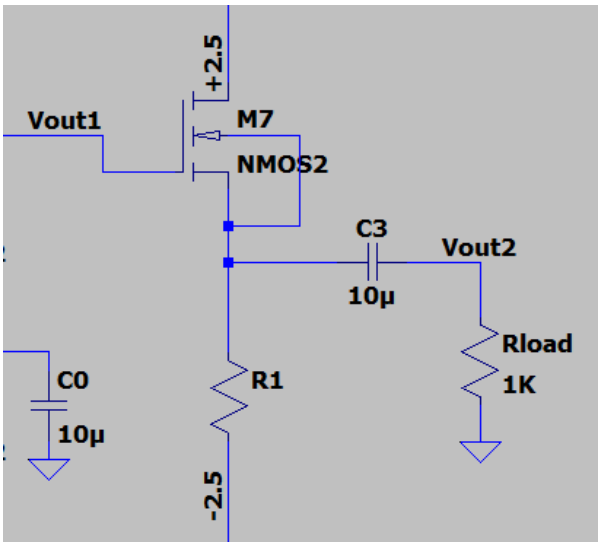

Figure 43: Schematic of the circuit which covers M7 and the load.

We know V_{D7} is 2.5 V and also $V_{G7} = V_{out1}$, from the previous part we know V_{out1}:

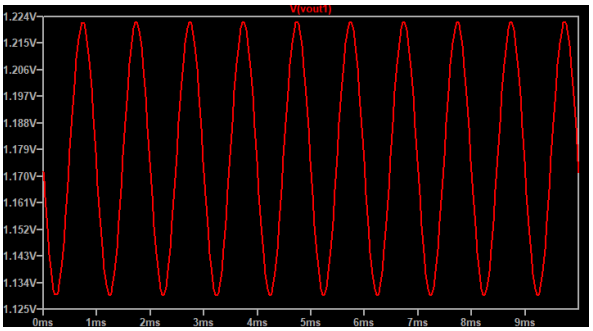

Figure 44: Graph of V_{out1}

$$V_{out1} = 1.175\ V$$

From these we can see if M7 is open, it is always in saturation using the NMOS saturation condition $V_{DS} > V_{GS} - V_{th}$

$$2.5 - V_{S7} > 1.175 - V_{S7} - 0.37$$

$$2.5 > 1.175 - 0.37$$

But an NMOS is open if $V_{GS} > V_{th}$, So:

$$1.175 - V_{S7} > 0.37$$

$$1.175 - V_{S7} > 0.37$$

$$0.805 > V_{S7}$$

We can write I_{DQ7} as V=IR equation and from M7's current equation.

$$I_{DQ7} = \frac{V_{S7} + 2.5}{R_1} = K_{N7}(1.175 - V_{S7} - 0.371)^2$$

$$K_{N7} = \frac{V_{S7} + 2.5}{R_1(0.804 - V_{S7})^2}$$

From looking at this equation we can see the closer we choose V_{S7} to 0.804 the bigger K_{N7} gets so I will choose $V_{S7} = 0.75$ to maximize my K_{N7}. I did not choose the maximum value to not accidentally close M7.

Then I can calculate I_{DQ7} and V_{GS7} as:

$$I_{DQ7} = \frac{0.75 + 2.5}{R_1} = \frac{3.25}{R_1}, V_{GS7} = 1.175 - 0.75 = 0.425$$

Now the current equation of M7 is:

$$\frac{3.2}{R_1} = K_{N7}(0.425 - 0.371)^2$$

$$\frac{1097}{K_{N7}} = R_1$$

We also know $gm = 2\sqrt{K_N I_{DQ}}$ is and from this, we can also calculate $gm = K_{N7}0.208$ but we can not calculate r_{07}. We know it depends on $(W/L)_7$ and we can experimentally calculate it for a given (W/L) value but we do not have the equation for it. So, we can not write $\frac{1}{gmR_1} + \frac{1}{gm1000} + \frac{1}{gmr_{07}} + 1$ in terms of K_N and find the K_N value which makes it the smallest. This means we have to guess a variable. we can guess $\frac{1}{gm1000}$ is going to be the largest term unless we choose R_1 smaller than it. And from $\frac{1097}{K_{N7}} = R_1$ we know K_{N7} and R_1 are inversely proportional. Using these we can say choosing $R_1 = 1K$ will make the largest term "$\frac{1}{gm1000}$" smallest. Because of this, I choose $R_1 = 1K\Omega$. Then:

$$\frac{1097}{K_{N7}} = 1000$$

$$K_{N7} = 1.097$$

$$K_N = K_N' \frac{W}{2L} \quad , \quad K_N' = 145.16\ \mu A/V^2$$

$$145.16\mu \frac{(W/L)_7}{2} = 1.097$$

$$(W/L)_7 = 15114$$

So, I choose w = 30228μ and L = 2μ for M7. Then for these values, I simulated my circuit.

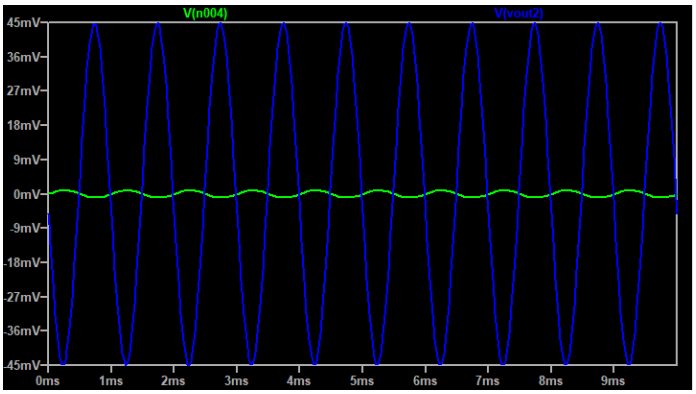

Figure 45: Graph of V_{in} vs time and V_{out2} vs time for $W_7 = 2\mu, L_7 = 30228\mu$

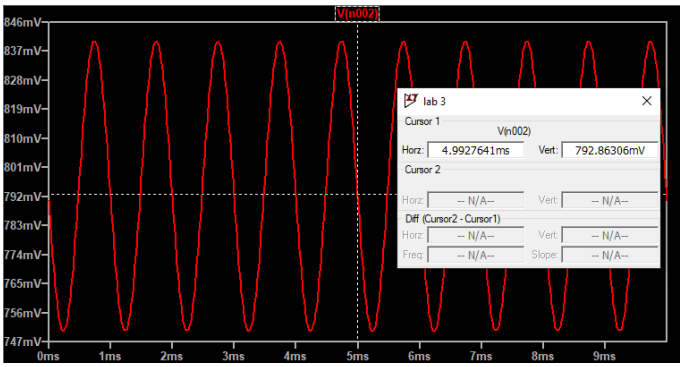

Figure 46: Graph of V_{S7} vs time for $W_7 = 2\mu, L_7 = 30228\mu$

The gain is around -45 which means on M7 we lost only 2% of our gain from the previous step and our choices for M7 are really successful. But W = 30228μ means 3cm which is not very realistic so I dropped that value to W = 302μ. I choose this value because M5 is also 292μm wide so it is a more realistic value. Then I repeated my simulation with this value.

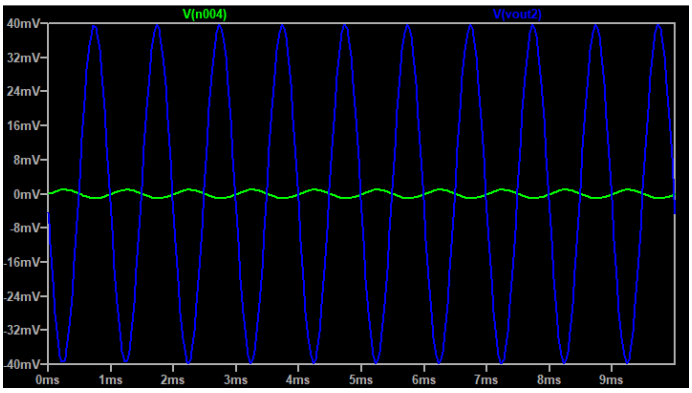

Figure 47: Graph of V_{in} vs time and V_{out2} vs time for W7 = 2µ,L7 = 302µ

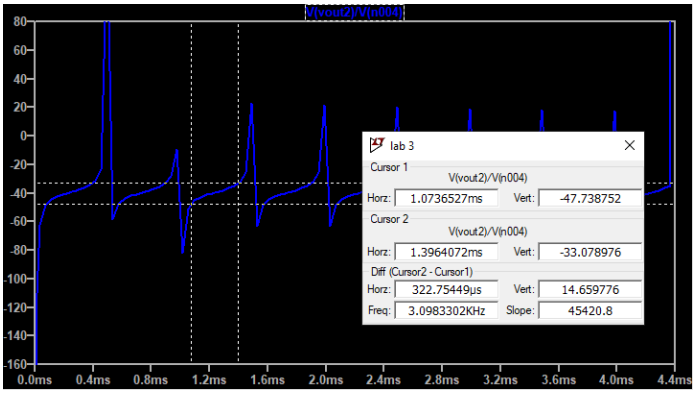

Figure 48: Graph of V_{out2}/V_{in} vs time for W7 = 2µ,L7 = 302µ

This time our gain dropped to around -40 and we were expecting a lower gain when we lowered w so this is expected. This gain is still bigger than the required gain of 30 and it is also achieved with a more realistic width for the M7 transistor. Because of this, I choose $L = 2\mu$, $w = 302\mu$ for M7, and 1KΩ for R_1.

3. Discussion & Conclusion:

a. Discussion:

As mentioned in part B the gain graph in figure 30 (also in figure 47) is not constant. This happens because the capacitors in the circuit are adding some small phase to the output. The amount of this phase can be lowered by picking a bigger capacitor but that won't stop gain from having periodic spikes which go to + and – infinity. But this is not a problem for us because these graphs are like this because of the phase of the output. Our gain doesn't actually go to positive and negative infinity it just looks like it does because the formula we use to calculate the gain V_{out} / V_{in} doesn't function properly with sin signal with phase. So, the only thing which could be seen as a problem here is drawing these graphs in the first place. I still draw them to talk about the phase and how it messes up the gain graph.

In part B I calculated the best value of M5 by assuming it would be on the edge of saturation yet when we looked at V_{DS5} it was around 1.85 V which is far from the 3.75 V which we took as the saturation point. This happened because we assumed V_{S5} wouldn't change much and it doesn't change much too but even a small change in V_{GS} affects the current on a transistor a great amount compared to a change in its V_{DS} constant. So actually, M5 never gets out of saturation because the more we increase its K_N the smaller its V_{GS} gets to compensate for that. Also, because its V_{tn} depends on its W and L lengths it never closes too. Even if I try choosing $W = 10$, $L = 2\mu$ and its V_{GS} value drop to 230 mV because its V_{tn} dropped to an even lower amount it doesn't close. And To top it off we are getting a gain of -200 at the end of the circuit too. So even if I didn't calculate the W/L value which produces the highest gain I couldn't do so because I do not know the formula for V_{tn} and even if I knew all the required formulas to calculate the exact W/L it will require an width length of 10 or more meters which is an extremely unrealistic value for a transistor. Because my choice of W/L satisfies the given condition and the value of the W/L which produces the highest gain is both impossible and impractical to calculate, my choice is satisfactory and correct.

In part B I talked about the resistance values of r_0's we do not know the exact equation for these but we know the idealistic mathematical equation for it, $r_0 = \frac{1}{\lambda I_{DQ}}$. But we also do not have an equation to calculate λ. We can calculate r_0 using the identity in figure 49.

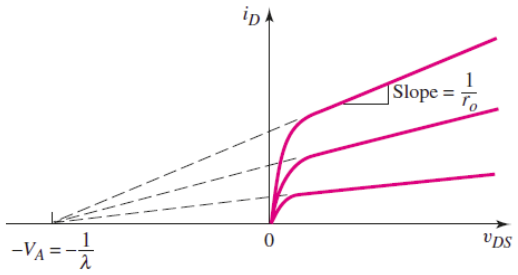

Figure 49: Graph of I_D vs V_{DS} it shows how to find r_0 [2]

I used that to calculate some of the r_0 values. As an example, r_{05} is 4.2KΩ, r_{04} is 4.0KΩ and r_{06} is 10KΩ. But these values are not important for as we can calculate them only when we know the W, L values of a transistor and we are trying to find the W, L values of the transistors. So, we cannot use these values in the calculation of W, L values of a transistor. Which makes them not useful for us.

In part D I said by making V_{S7} as close as possible to 0.804 V we would get the best possible gain. After choosing W/L as 15114 our gain $A_{V12} = V_{out2}/V_{out1}$ was around 0.98 which is really good for a current buffer with 1KΩ load. Also, its V_{S7} value was 0.793 V which shows my assumption of getting the best gain for a V_{S7} value close to 0.804 V was correct too. But creating a realistic circuit is more important than creating a perfect circuit, so I had to lower the W of M7 to 302μ. This still gave us a final absolute gain of 40 which is over the required 30. This makes my choice satisfactory and correct.

b. Conclusion:

This lab's goal was to make us use realistic transistors and get us familiarized with the design process of a realistic amplifier. This lab was my first experience with transistors. Even though they were not real transistors and only simulations their simulations still felt realistic and very new to me also calculating some of the parameters of the transistors experimentally made me understand them better. Design processes always seem impossibly hard to me, there is always a lot of unknowns without enough equations to solve them. But I realized this is not something I should fear but it is something I should like because there being not enough equations means I could add new constraints which lower the number of unknonws and makes my computations easier. I once again saw creating the best circuit is extremely hard and maybe impossible but creating a circuit that does what we want it to do is not so hard. Because when we are designing something, we usually need it to do something and that thing is usually modest and not hard to achieve. As an example, in this experiment, our goal was to create a circuit with an absolute gain higher than 30. Even though I did some not perfect assumption and ignored a lot of things I still created a circuit with 40 absolute gain. This gain is 33% bigger than the required one which is great. I also became a lot more acquainted with LTSpice. Before this, I thought of it as a software which we will just use in some courses than forget about but I understand it can be used for real design applications too. I learned how to use its graph function and its different forms of simulation such as DC sweep. I also saw it can become a lot more realistic if we use external codes for the components. This made me realize how versatile and important LTSpice is for us. Once again, I saw how important things, we are learning in this course will be for us after we graduate.

4. References:

[1] D. A. Neamen, "Mircoelectronics: Circuit Analysis and Design," in *Mircoelectronics: Circuit Analysis and Design*, New York, McGraw-Hill, 2010, p. 144.

[2] D. A. Neamen, "Mircoelectronics: Circuit Analysis and Design," in *Mircoelectronics: Circuit Analysis and Design*, New York, McGraw-Hill, 2010, p. 143.