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1/3/2021

EEE 313 Electronic Circuit Design – Lab Report 5

1. Introduction:

In this lab assignment, we are tasked with simulating a BJT amplifier circuit in LTspice. The circuit schematic is already provided to us in figure 1. We will first analytically calculate the values of R2, R3 and R4 for the given conditions. Then simulate the circuit and look at its gain at different frequencies and draw a logarithmic plot of the gain for different frequencies. Then we will find how each capacitor affects the gain and how the internal capacitance of the BJT affect the gain.

I_C=2mA
V_{out}/V_{in}=-5 @ 10kHz
R_{in}=27 kΩ
β = 300

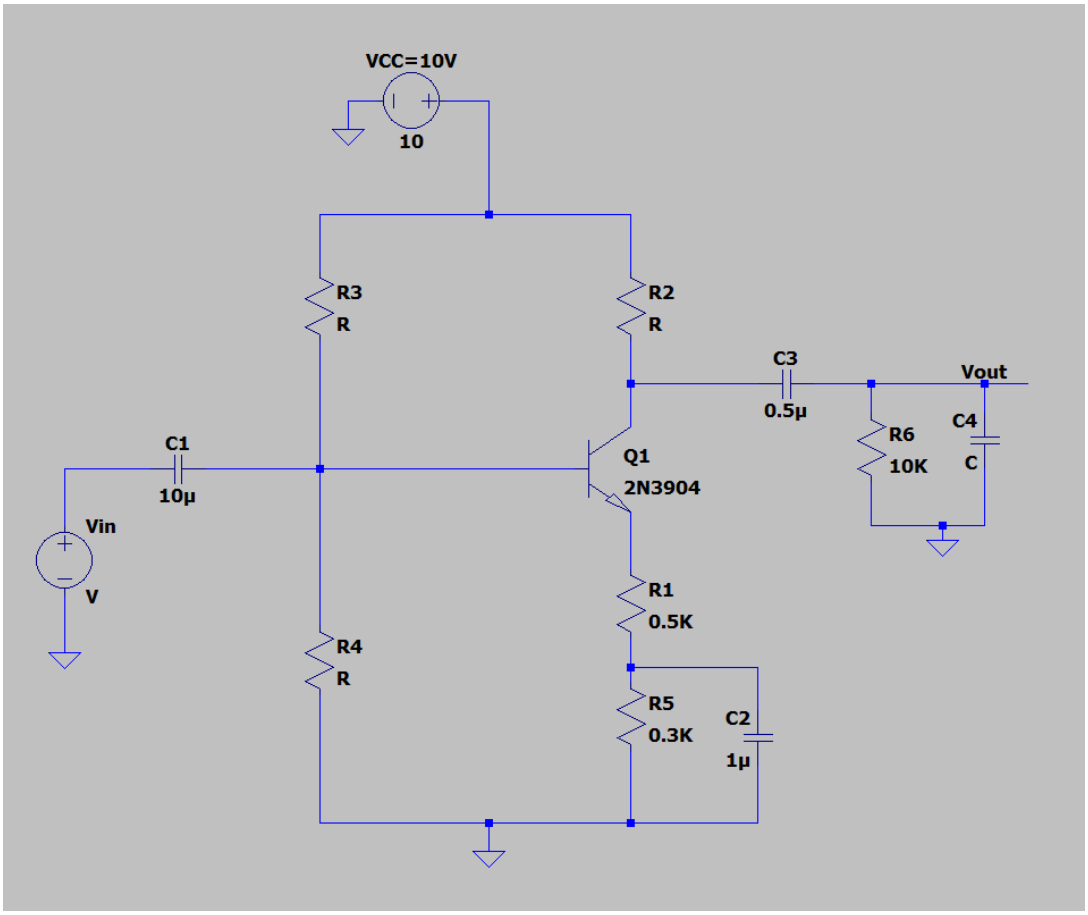

Figure 1: Circuit schematics we used in this lab

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2. Lab Work:

a. Part A:

In part A we are asked to analytically calculate the values of R2, R3 and R4 for the given conditions. To do this lets first consider DC analysis of the circuit assuming forward active region. In DC analysis all the capacitors are assumed to be open circuit.

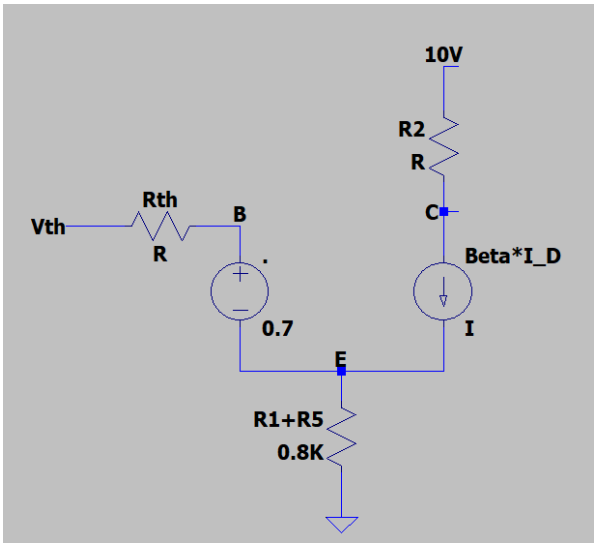

Figure 2: circuit schematic of the DC analysis circuit assuming forward active region.

Here the R_{TH} *and* V_{TH} are the Thevenin equivalent voltage and resistor the base of the transistor sees. So:

$$V_{TH} = \frac{10R_4}{R_3 + R_4} \qquad R_{TH} = \frac{R_3 R_4}{R_3 + R_4}$$

We are given I_C=2mA and we also know β = 300. from them we can calculate I_B and I_E

$$I_B = \frac{I_C}{\beta} = \frac{2mA}{300} = 0.006666\ mA$$

$$I_E = I_C + I_B = 2.006666\ mA$$

From them, we can calculate V_E *and* V_B.

$$V_E = I_E \cdot (R1 + R5) + 0$$

$$V_E = 2.006666\ mA \cdot 0.8K\Omega + 0$$

$$V_E = 1.605\ V$$

$$V_B = V_E + 0.7V = 1.605\ V + 0.7V = 2.305V$$

We can calculate r_π from $r_\pi = \frac{V_T}{I_{BQ}}$ because we know I_{BQ}

$$r_\pi = \frac{V_T}{I_{BQ}} = \frac{0.026}{0.006666mA} = 3.9K\Omega$$

Now let's look at the small-signal analysis of the circuit at the input frequency of 10 KHz. I assumed C1, C2 and C3 as short circuits and C4 as an open circuit. We will further discuss this in the discussion.

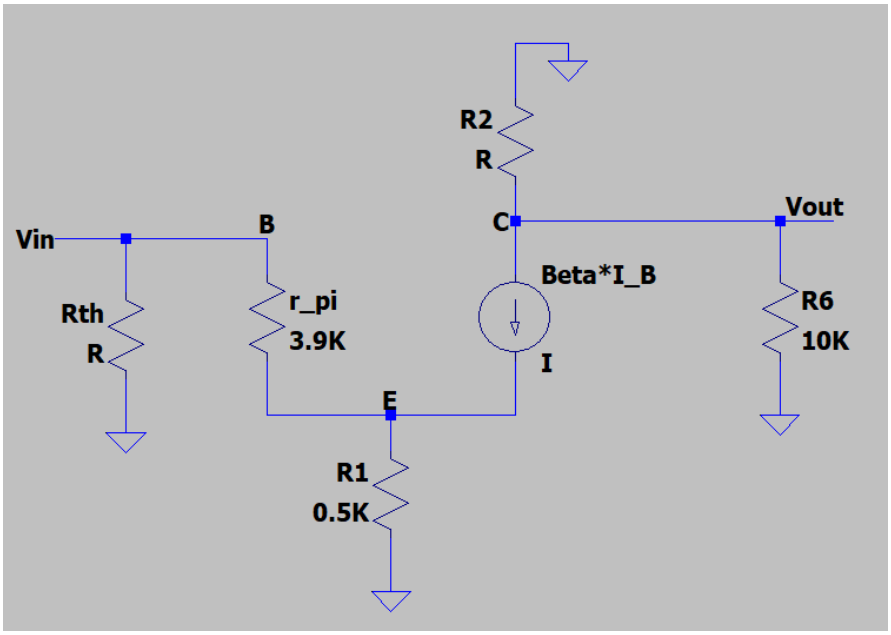

Figure 3: Small signal analysis circuit of the BJT circuit.

One of the conditions given to us is R_{in}=27 kΩ. We can write R_{in} from figure 3.

$$R_{in} = ((\beta + 1)R1 + r_\pi)//(R3//R4)$$

We multiply R1 with $(\beta + 1)$ because the current on R1 is $(\beta + 1)$ times bigger than it would be without the reactive current source. The current which reactive source supplies, have a similar effect to that resistance being $(\beta + 1)$ times bigger and the current source not existing. We can, instead of doing this solve KCL equations but that would take too long and we would be doing the same computations over and over again. So, I decided to just represent the effect of the current source by multiplying the resistance in the emitter side of the circuit with $(\beta + 1)$. I will again use this trick to show the effect of the reactive current source trough out the lab report. I will further explain why we multiply that resistance with $(\beta + 1)$ in the discussion.

$$R_{in} = ((301)0.5 + 3.9)//(R_3//R_4)$$

$$27 = \frac{154.4(R_3//R_4)}{154.4 + (R_3//R_4)}$$

$$4168.8 + 27(R_3//R_4) = 154.4(R_3//R_4)$$

$$127.4(R_3//R_4) = 4168.8$$

$$(R_3//R_4) = 32.72K\Omega$$

$$R_{TH} = 32.72K\Omega \quad (1)$$

Now we can look back to figure 2. We can calculate I_B as the current on the R_{TH} resistance.

$$I_B = \frac{V_{TH} - V_B}{R_{TH}} \quad (2)$$

We know everything in equation 2 other then V_{TH}. So, we can find V_{TH} from it.

$$0.006666\,mA = \frac{V_{TH} - 2.305V}{32.72K\Omega}$$

$$V_{TH} = 2.523V \quad (3)$$

We also know:

$$V_{TH} = \frac{10R_4}{R_3 + R_4} \qquad R_{TH} = \frac{R_3R_4}{R_3 + R_4} \quad (4)$$

By putting equation 1 and 3 inside of equation 4 we can find:

$$R3 = 129.6K\Omega \qquad R4 = 43.8K$$

Then to find R2 we can calculate i_B easily from $I = \frac{V}{R}$:

$$i_B = \frac{v_{in}}{R1(\beta + 1) + r_\pi}$$

$$i_B = \frac{v_{in}}{154K}$$

Then we can write V_{out} in terms of I_B

$$V_{out} = -\beta i_B(R_2//R_6)$$

$$V_{out} = -\frac{\beta(R_2//R_6)}{R1(\beta + 1) + r_\pi}V_{in}$$

$$A_v = -\frac{\beta(R_2//R_6)}{R1(\beta + 1) + r_\pi}$$

One of the conditions was the gain being -5 at 10 KHz. We can use this to calculate R2.

$$5 = \frac{300\,\frac{R_2 \cdot 10}{R_2 + 10}}{154}$$

$$770 \cdot (R_2 + 10) = 3000 \cdot R_2$$

$$2230 \cdot R_2 = 7700$$

$$R_2 = 3.45\ K\Omega$$

The I put in all the calculated resistances in to the simulation in LTspice. To cheek if I satisfy the given conditions.

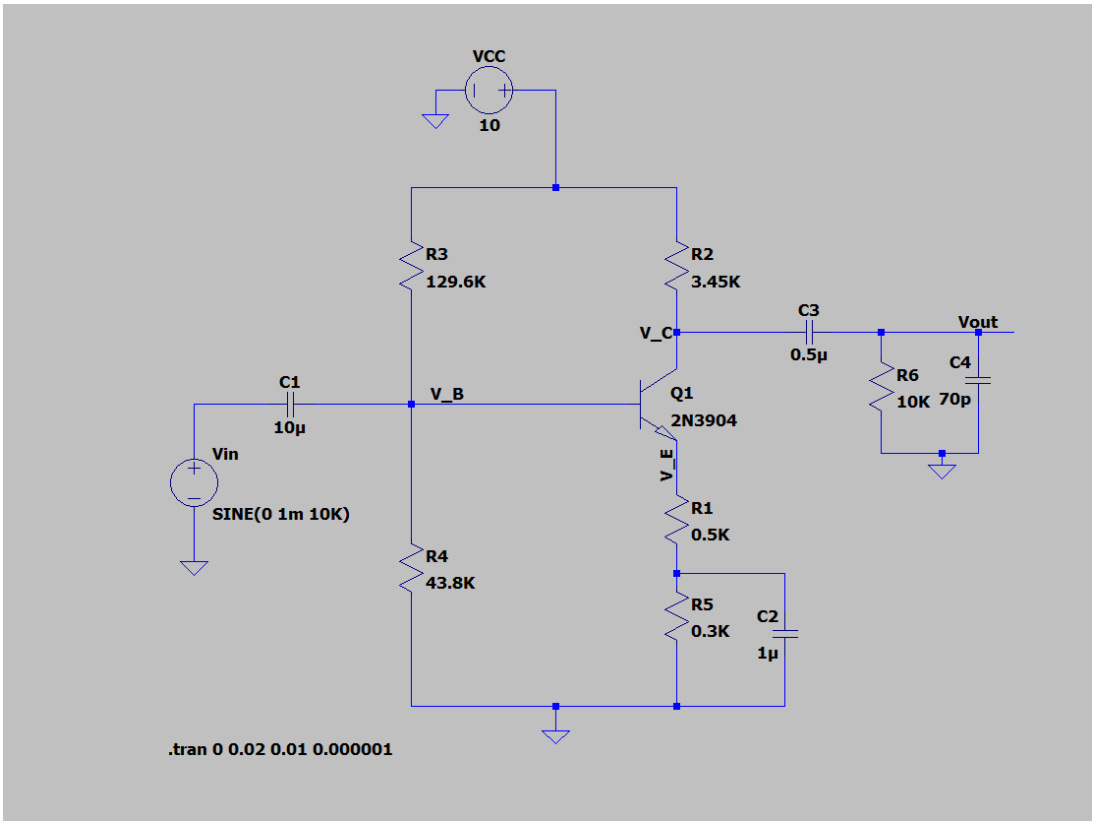

Figure 4: circuit schematic in LTspice with the calculated resistance values.

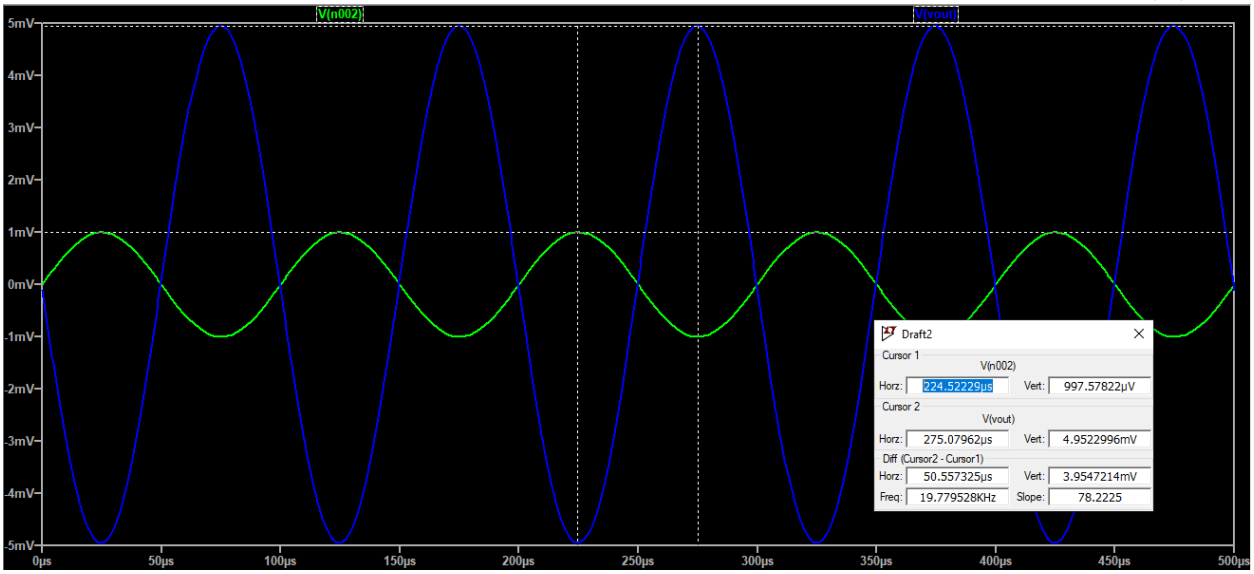

Figure 5: the gain of the circuit at 10KHz input signal.

We can see the gain is almost exactly -5 which is great. It also shows our computations are very accurate and all the assumptions we made were logical and correct.

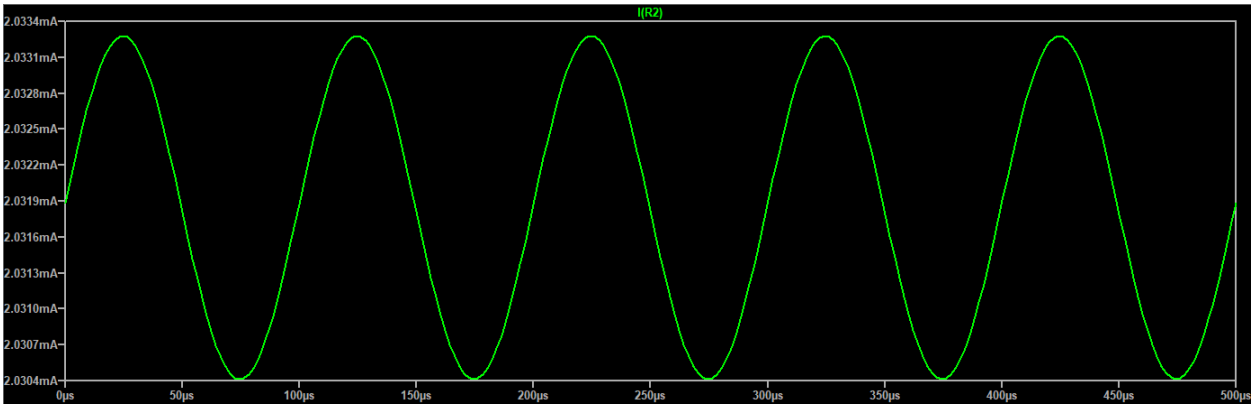

Figure 6: graph of the I_C current from the simulation of the circuit.

Again the I_C current is just like we were expecting it 2mA. Because we satisfy the given conditions in the simulation our choice of R2, R3 and R4 are correct and satisfactory.

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b. Part B:

In this part, we are asked to do AC analysis for the frequency range of 10mHz-1GHz. While doing this it is recommended to use that we choose AC amplitude as 1 and AC phase as 0 for the small-signal source. Then the V_{out} plot will be the gain of our circuit. We will use the logarithmic sweep function of the LTspice to simulate the circuit to get the desired effect.

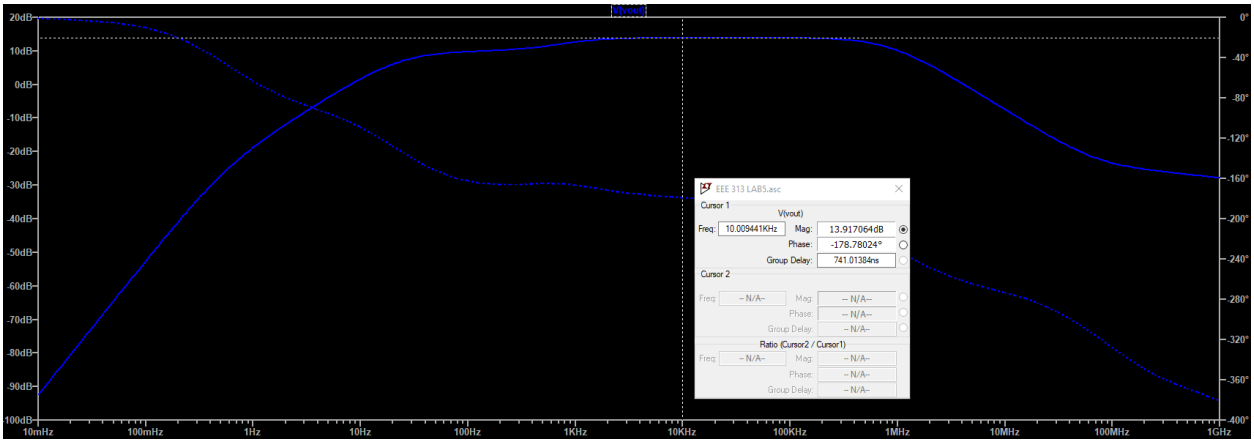

Figure 7: the gain of the circuit for the logarithmic sweep.

c. Part C:

In this part, we are asked to analyze the graph we got in part B and explain each cutoff frequency.

First to understand which cut off frequency is caused by which capacitor. I doubled the capacitance of C1 then looked at how the cut of frequencies changed. Then I gave C1 half of its original capacitance value then looked how the cut of frequencies changed. I did this so I can see which cut of frequencies are mostly affected by C1. I repeated this process for all the capacitors. I found the first decrease in slope is caused by C1. The second decrease in slope is caused by C3. The first increase in the slope and the third decrease in the slope are both caused by the capacitor C2. The fourth decrease in slope is caused of C4. The second increase in slope is caused by the internal capacitances and they will be further discussed in part 5.

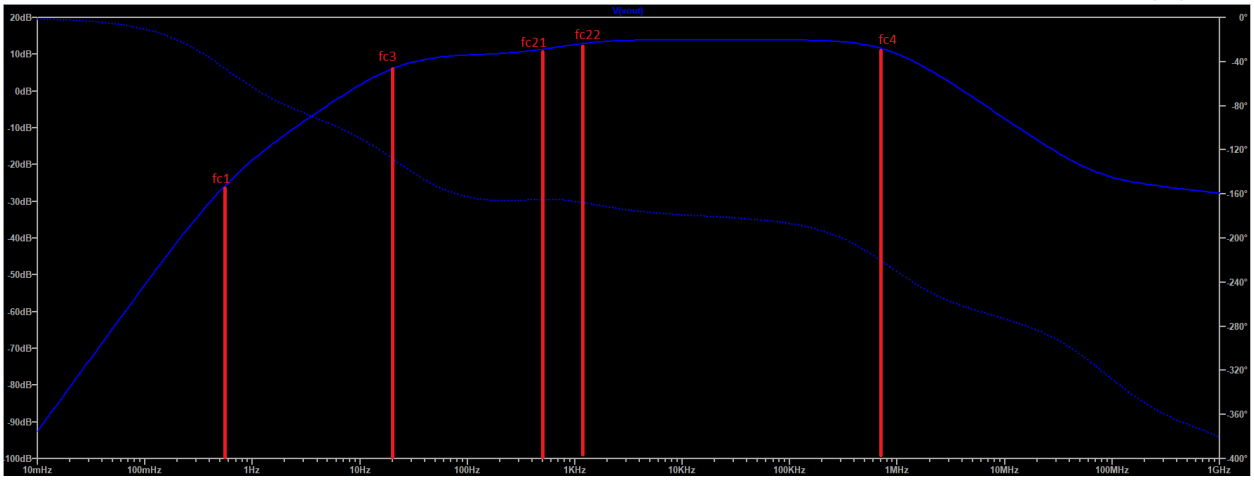

Figure 8: frequency response of the circuit which shows who causes each cut of frequency.

Now I will calculate each capacitance cut off frequency analytically.

The capacitor C1 doesn't get affected by C3 or C4 as those 2 are connected to the collector of the circuit. From figure 8 we can see C2's operational region is almost 1000 times higher than C1's so C2 will simply act as an open circuit at the operational region of C1. This assumption will be further discussed in the discussion. So, we can calculate the effect of C1 separately using figure 9.

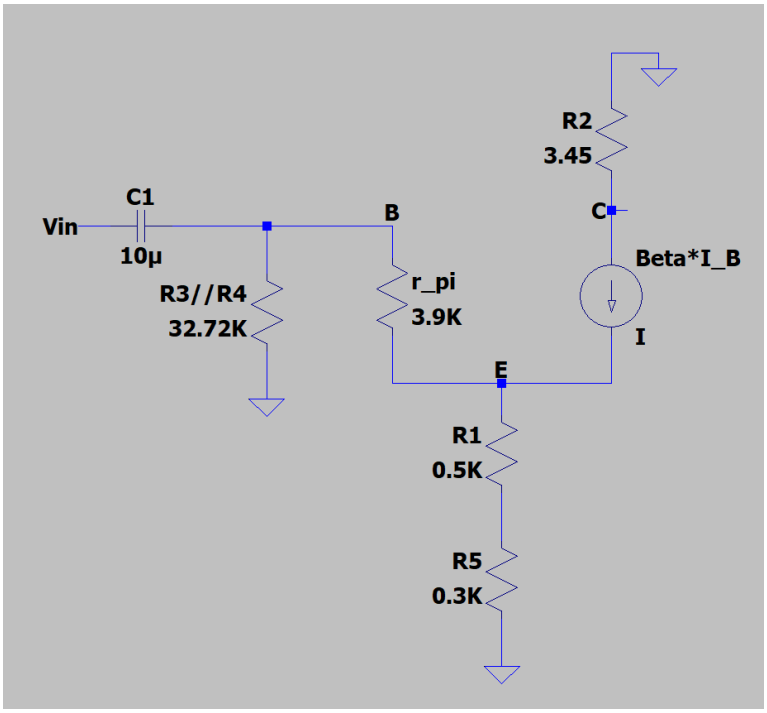

Figure 9: small signal model of the circuit for a frequency which is around the active region of C1.

Around the lowest frequencies only on C1 current can pass and all the other capacitors act like an open circuit. Here we will calculate the gain at the collector terminal. The cut-off frequency of C1 for this circuit and its effect on the gain will the same for the larger circuit with all the transistors. This is the trick we are using in this part. We can do this because these simplified circuits are how the circuit will actually act around that frequency range. By looking at the circuit at specified frequencies we can solve much easier equations. This will be further discussed in the discussion.

We can write V_B from a voltage divider as.

$$V_{B=}\frac{[r_\pi + (R_1 + R_5)(\beta + 1)]//(R_3//R_4)}{\frac{1}{j\omega C_1} + [r_\pi + (R_1 + R_5)(\beta + 1)]//(R_3//R_4)} v_{in} \quad (5)$$

Then we can simply write i_B from $I = \frac{V}{R}$:

$$i_B = \frac{V_B}{r_\pi + (R_1 + R_5)(\beta + 1)} \quad (6)$$

Then we can write V_{out} as i_B:

$$v_{out} = -\beta i_B R_2 \quad (7)$$

Then the gain is just the combination of equation 7, 6 and 5:

$$A_{v1} = -\beta \frac{R_2[r_\pi + (R_1 + R_5)(\beta + 1)]//(R_1 + R_5)}{r_\pi + (R_1 + R_5)(\beta + 1)} \frac{1}{\frac{1}{j\omega c_1} + [r_\pi + (R_1 + R_5)(\beta + 1)]//(R_3//R_4)} \quad (8)$$

Left side of equation 8 is related to the amplitude of the gain and we only care about the phase and its cut of frequency so we will only look at the right side of equation 8.

$$\frac{j\omega c_1}{1 + [r_\pi + (R_1 + R_5)(\beta + 1)]//(R_3//R_4)j\omega c_1} \quad (9)$$

Equation 9 has a zero at 0 this is one of the reasons why we have such a high slop at the start. The other one is a pole and it causes the first cut of frequency. That frequency can be written as.

$$Z_1 = [r_\pi + (R_1 + R_5)(\beta + 1)]//(R_3//R_4)c_1$$

$$f_{C1} = \frac{1}{2\pi Z_1} = \frac{1}{2\pi[r_\pi + (R_1 + R_5)(\beta + 1)]//(R_3//R_4)c_1} \quad (10)$$

$$f_{C1} = \frac{1}{2\pi[244.7K]//(32.72K)10^{-5}}$$

$$f_{C1} = 0.55Hz$$

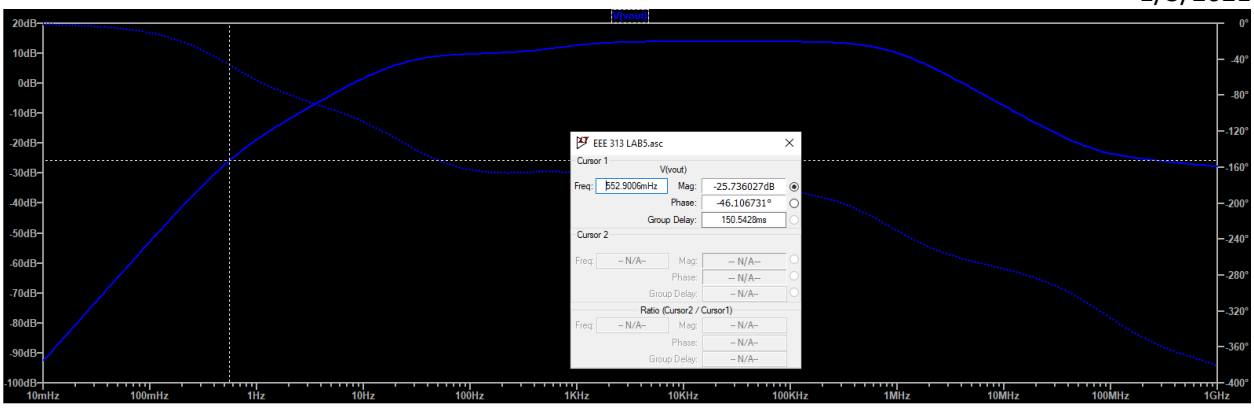

Figure 10: frequency response of the circuit.

If we look at the frequency response of the circuit from figure 10 the 0.55 Hz frequency correlates with the first cut of frequency.

Now we will look at the effect of C3. The capacitor C3 doesn't get affected by C1 or C2 as those 2 are not directly connected to the collector of the circuit. From figure 8 we can see C4's operational region is almost 100000 times higher than C3's so C4 will simply act as an open circuit at the operational region of C3. This assumption will be further discussed in the discussion. So, we can calculate the effect of C3 separately using figure 11.

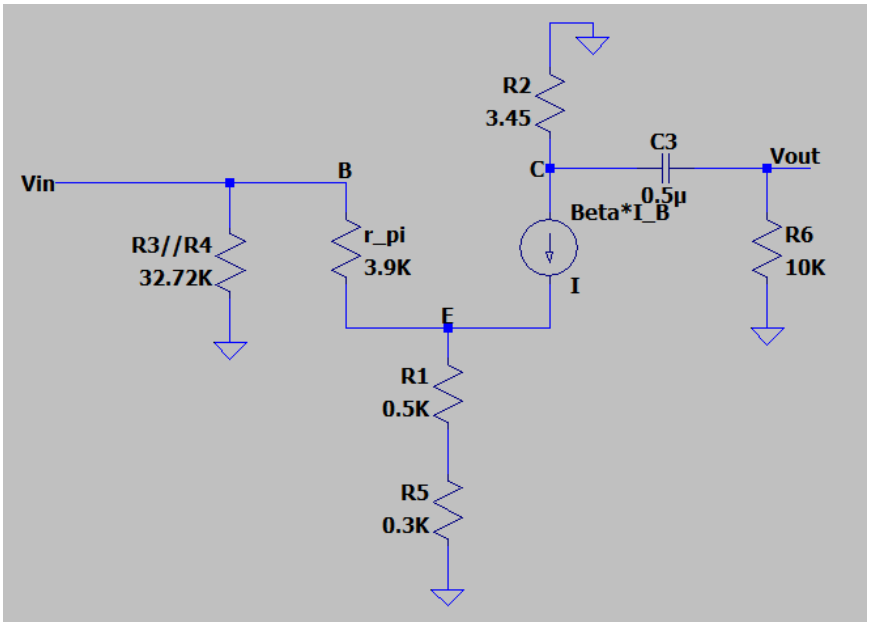

Figure 11: small signal model of the circuit for a frequency which is around the active region of C3.

The gain of the circuit in figure can be written by first finding V_C then applying a voltage devider.

$$V_C = -\beta i_b (R_2 // \left(\frac{1}{j\omega C_3} + R_6\right)$$

$$V_{out} = V_C(\frac{R_6}{\frac{1}{j\omega C_3} + R_6})$$

$$V_{out} = -\beta i_b (R_2 // \left(\frac{1}{j\omega C_3} + R_6\right)(\frac{R_6}{\frac{1}{j\omega C_3} + R_6})$$

$$V_{out} = -\beta i_B R_2 \left(\frac{R_6 j\omega c_3}{R_6 j\omega c_3 + 1}\right)\frac{R_6 j\omega c_3 + 1}{(R_2 + R_6)j\omega c_3 + 1}$$

$$V_{out} = -\beta * i_b * \frac{R_2}{R_2 + R_6}\frac{(R_2 + R_6)j\omega c_3}{(R_2 + R_6)j\omega c_3 + 1} \quad (11)$$

Again, we only care about the part with $j\omega$ as it is the part which effects the phase in equation 11.

$$\frac{(R_2 + R_6)j\omega c_3}{(R_2 + R_6)j\omega c_3 + 1} \quad (12)$$

Equation 12 has a zero at 0 this is one of the reasons why we have such a high slop at the start. The other one is a pole and it causes the second cut of frequency. That frequency can be written as.

$$Z_3 = (R_2 + R_6)j\omega c_3$$

$$f_{C3} = \frac{1}{2\pi Z_3} = \frac{1}{2\pi(R_2 + R_6)c_3} \quad (13)$$

$$f_{C3} = 23.57Hz$$

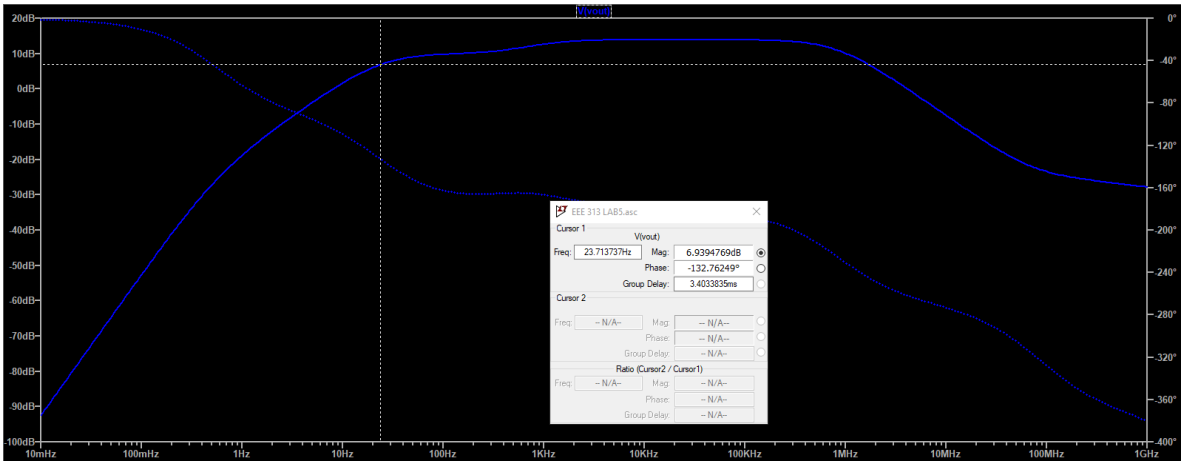

Figure 12: frequency response of the circuit.

If we look at the frequency response of the circuit from figure 12 the 23.67 Hz frequency correlates with the second cut of frequency which is also the second decrease in the slope.

Now we will look at the effect of C2. Just like C1, it is not affected by C3 and C4. Our assumption of C2 not affecting C1 also means C2 doesn't get affected by C1. And we can calculate the cut off frequencies of C2 from figure 12.

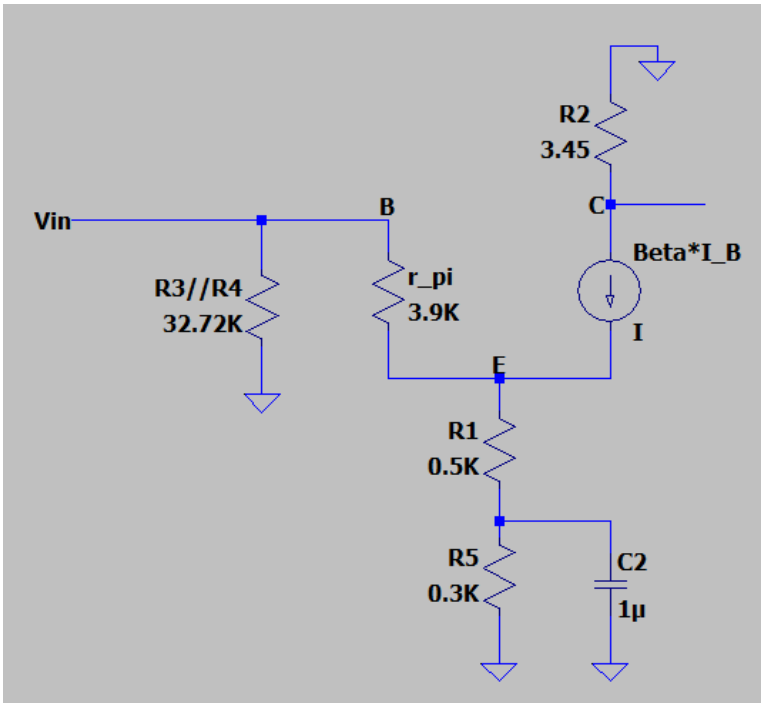

Figure 13: Small signal model of the circuit for a frequency which is around the active region of C2.

We can write i_B from $I = \frac{V}{R}$:

$$i_B = \frac{v_{in}}{r_\pi + (\beta+1)(R_1 + \left(R_5 // \frac{1}{j\omega C_2}\right))}$$

$$i_B = \frac{v_{in}}{r_\pi + (\beta+1)(R_1 + \left(\frac{R_5}{j\omega R_5 C_2 + 1}\right))}$$

$$i_B = \frac{v_{in}}{r_\pi + (\beta+1)R_1 + \left(\frac{R_5(\beta+1)}{j\omega R_5 C_2 + 1}\right)}$$

$$i_B = \frac{v_{in}(j\omega R_5 C_2 + 1)}{(r_\pi + (\beta+1)R_1)(j\omega R_5 C_2 + 1) + R_5(\beta+1)}$$

$$i_B = \frac{v_{in}(j\omega R_5 C_2 + 1)}{(r_\pi + (\beta+1)R_1)(j\omega R_5 C_2) + (r_\pi + (\beta+1)R_1) + R_5(\beta+1)}$$

$$i_B = \frac{v_{in}(j\omega R_5 C_2 + 1)}{(r_\pi + (\beta+1)R_1)(j\omega R_5 C_2) + r_\pi + (\beta+1)(R_1 + R_5)}$$

$$i_B = \frac{1}{r_\pi + (\beta+1)(R_1+R_5)} \frac{v_{in}(j\omega R_5 C_2 + 1)}{1 + \frac{(r_\pi + (\beta+1)R_1)R_5 C_2}{r_\pi + (\beta+1)(R_1+R_5)} j\omega} \quad (14)$$

Left side of equation 13 is related to the amplitude of the gain and we only care about the phase and its cut of frequency so we will only look at the right-side equation 13.

$$\frac{v_{in}(j\omega R_5 C_2 + 1)}{1 + \frac{(r_\pi + (\beta+1)R_1)R_5 C_2}{r_\pi + (\beta+1)(R_1+R_5)} j\omega} \quad (15)$$

Equation 15 has two cut off frequencies one of them is a poll and the other one is a zero. Let's first calculate the value of the zero.

$$Z_{21} = R_5 C_2$$

$$f_{C21} = \frac{1}{2\pi Z_{21}} = \frac{1}{2\pi R_5 C_2} \quad (16)$$

$$f_{C21} = 530.5Hz$$

This f_C is the first increase in the slope.

Then let's calculate the pole now.

$$Z_{22} = \frac{(r_\pi + (\beta+1)R_1)R_5 C_2}{r_\pi + (\beta+1)(R_1+R_5)}$$

$$f_{C22} = \frac{1}{2\pi Z_{22}} = \frac{1}{2\pi \frac{(r_\pi + (\beta+1)R_1)R_5 C_2}{r_\pi + (\beta+1)(R_1+R_5)}} \quad (17)$$

$$f_{C22} = 851Hz$$

This f_C is the third decrease in the slope.

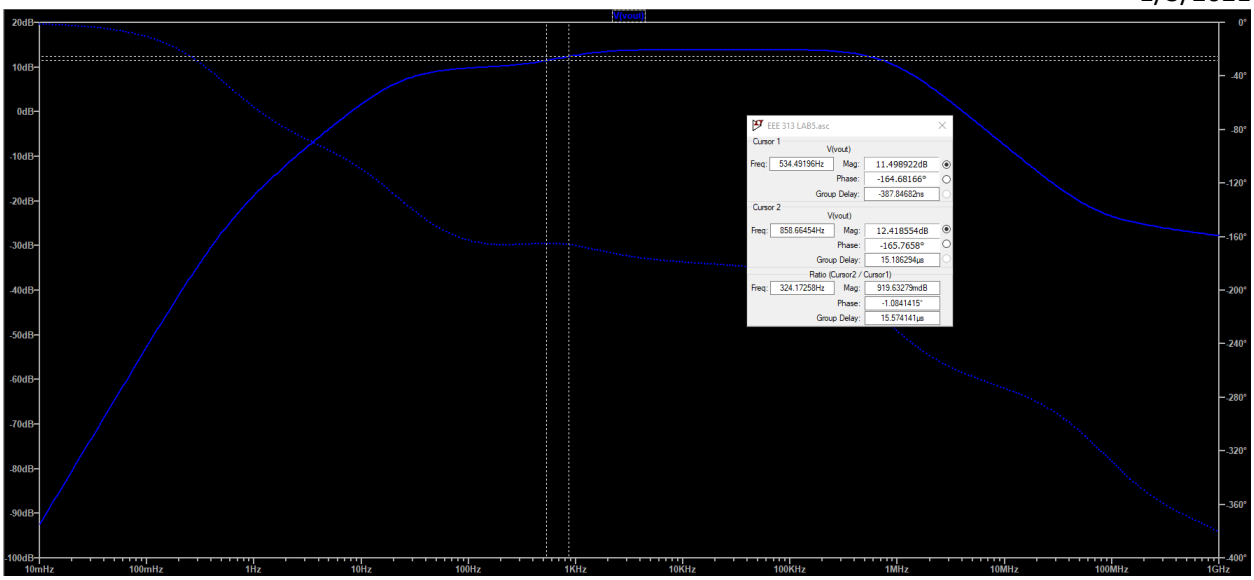

Figure 14: frequency response of the circuit.

If we look at the frequency response of the circuit from figure 14 the 530.5 Hz frequency correlates with the third cut of frequency which is also the first increase in the slope and the 851 Hz frequency correlates with the third cut of frequency which is also the third decrease in the slope.

Now let's look at the effect of C4. Just like C3, C4 doesn't get affected by C1 and C2. And just like C4 didn't affect C3, C3 wont affect C4. So, we can use the circuit in figure 14.

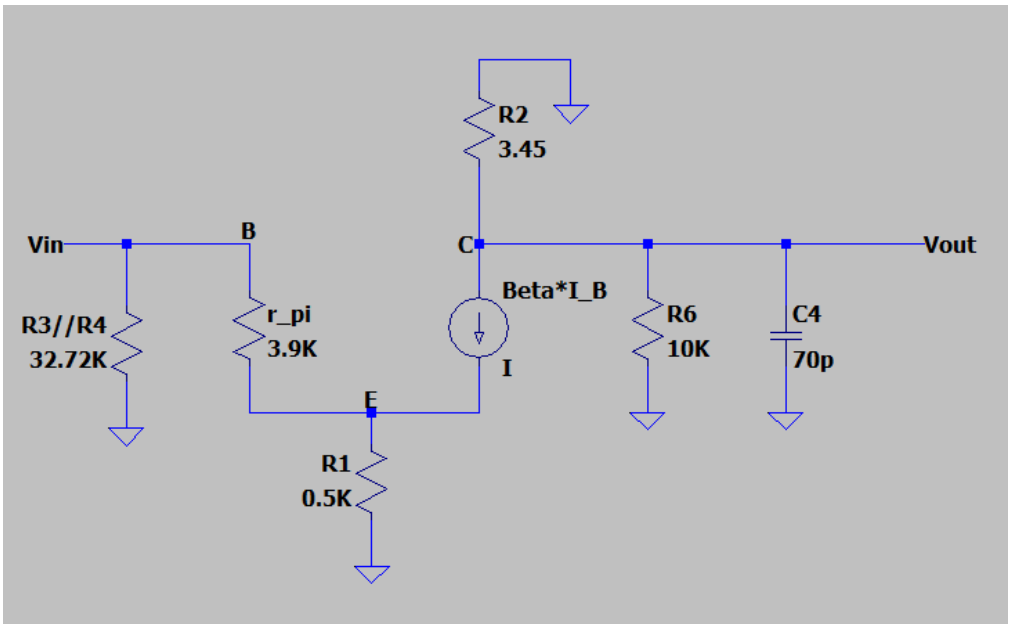

Figure 15: Small signal model of the circuit for a frequency which is around the active region of C4.

We can write V_{out} in terms of i_B as:

$$v_{out} = -\beta i_B (R_2 // R_6 // \frac{1}{j\omega C_4})$$

$$v_{out} = -\beta i_B \frac{(R_2 // R_6)}{(R_2 // R_6) C_4 j\omega + 1}$$

$$v_{out} = -\beta i_B (R_2 // R_6) \frac{1}{1 + (R_2 // R_6) C_4 j\omega} \quad (18)$$

Left side of equation 18 is related to the amplitude of the gain and we only care about the phase and its cut of frequency so we will only look at the right-side of equation 18.

$$\frac{1}{1 + (R_2 // R_6) C_4 j\omega} \quad (19)$$

Equation 19 has a pole and it causes the fifth cut of frequency which is the fourth decrease in the slope. That frequency can be written as.

$$Z_4 = (R_2 // R_6) C_4$$

$$f_{C4} = \frac{1}{2\pi Z_4} = \frac{1}{2\pi (R_2 // R_6) C_4} \quad (20)$$

$$f_{C4} = 884.4\ KHz$$

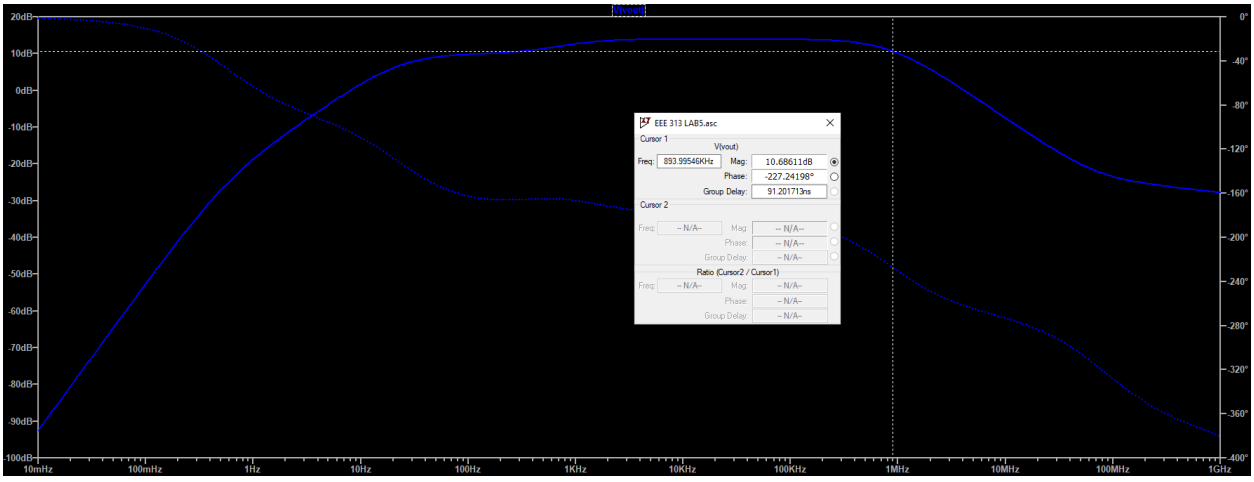

Figure 16: Frequency response of the circuit.

If we look at the frequency response of the circuit from figure 16 the $884.4\ KHz$ frequency correlates with the fifth cut of frequency which is also the fourth decrease in the slope. All this

frequency's correlating with the simulation graph shows me my computations are sound and represent the behavior of the circuit correctly.

d. Part D:

In this part, we are asked to increase the bandpass of our BFT amplifier by changing the capacitance values of the capacitors.

In part C we already identified which capacitor creates which cut of frequency and also the equation for each of the cut of frequencies. We found Equation 10 for f_1, equation 13 for f_3, Equation 16 for f_{21}, Equation 17 for f_{22} and Equation 20 for f_4. We can look at figure 8 and see to increase the bandpass of the circuit we need to move $f_1, f_3, f_{21}\ and\ f_{22}$ to lower frequencies and move f_4 to higher frequencies. I looked at the equations for the cut of frequencies and decided to double the capacitance values of C_1, C_2, C_3 and half the value of C_4.

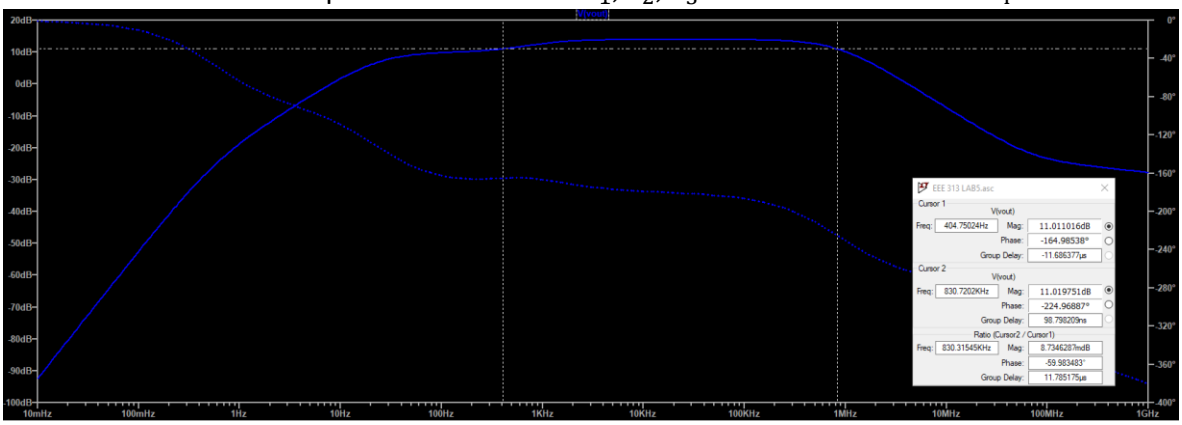

Figure 17: Bandpass of the original amplifier.

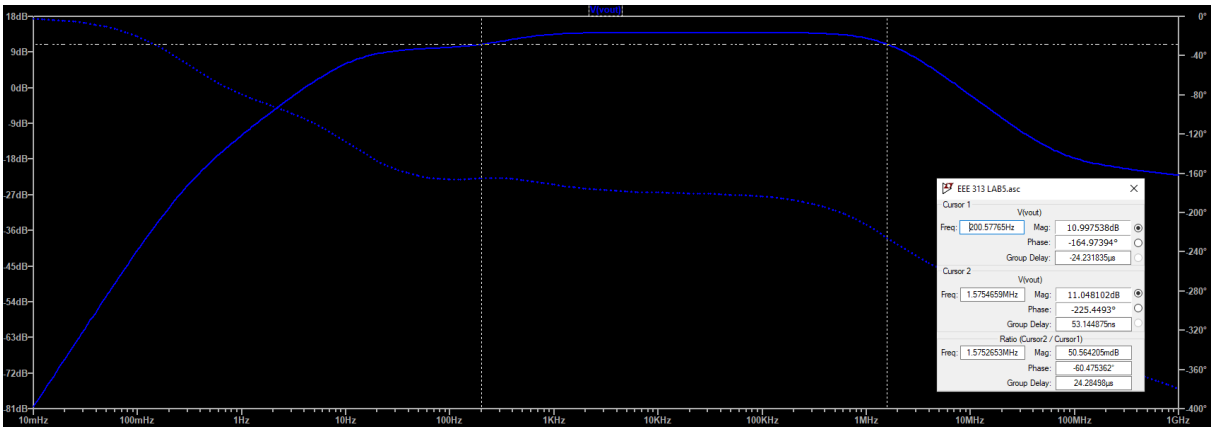

Figure 18: Bandpass of the circuit which was modified to increase the bandpass.

From figure 17 and 18 we can see all the cut of frequencies moved in a direction we wanted and the band pass increased.

e. Part E:

In this part, we are asked to remove C4 from the circuit and run the AC analysis of the circuit again. Then comment on the effect of the internal capacitances.

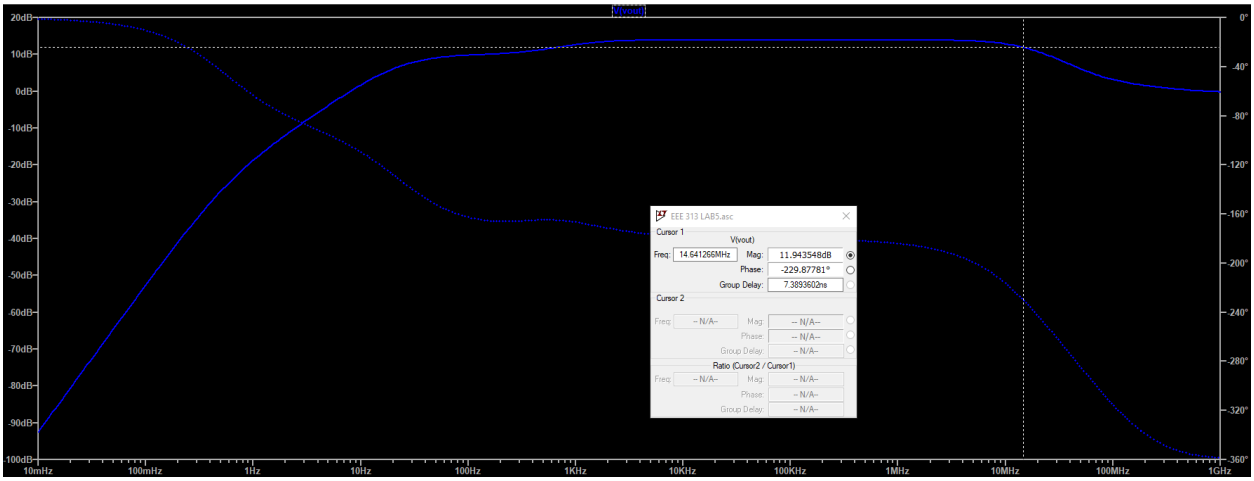

Figure 19: frequency response of the circuit without C4.

This is the frequency response of the circuit without C4. To understand this we need to look at the small-signal model of the circuit with the internal capacitors and C4. At a frequency high enough for the internal capacitors to have any effect, C_1, C_2, C_3 will act as short circuits so they won't be drawn in figure 20.

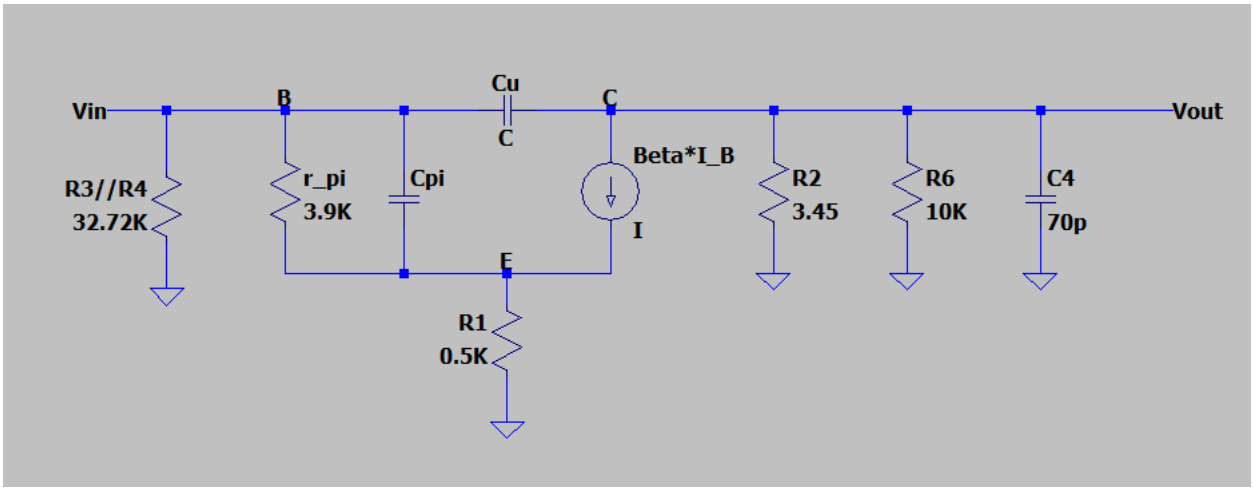

Figure 20: small signal model of the circuit with the internal capacitors.

We can split C_μ to the emitter and base sides using miller effect.

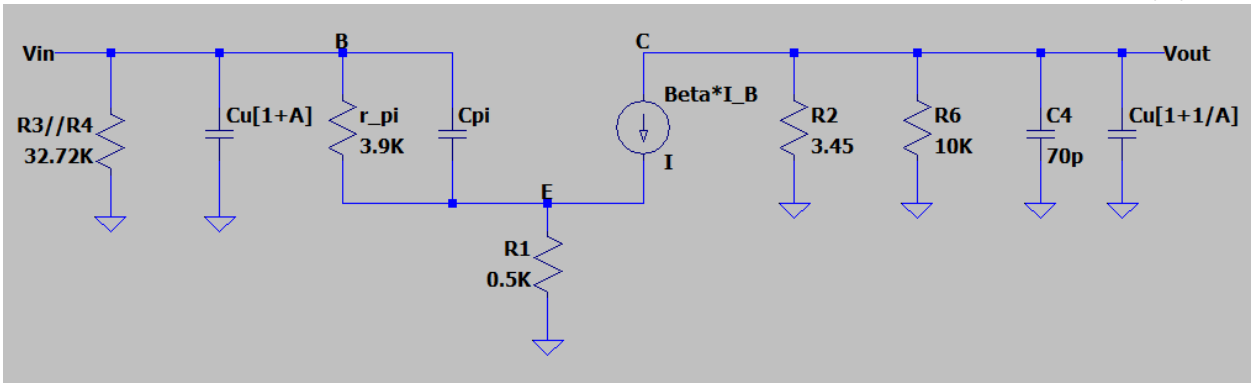

Figure 21: small signal model of the circuit with the internal capacitors with Miller effect.

From figure 21 we can see throughout the lab when we were talking about the value of C_{4our} (I use this to demote the C_4 we did the analytic computations for) and calculating the effect of C_{4our} we were actually calculating the effect of $C_{4our} = C_4 + C_\mu(1 + \frac{1}{A})$ we just ignored the value of $C_\mu(1 + \frac{1}{A})$ because it was so small. Because of this when we remove C_4 it has an effect similar to lowering the value of C_{4our} very much. Because even if we removed C_4 , C_{4our} doesn't become 0, its effect and cut off frequency from the graph don't disappear. Instead, its cut off frequency will just move to higher frequencies.

Also, we can see at very high frequencies C_π will short r_π, which will increase the current i_B. i_B directly effects the gain so at high frequencies C_π will increase our gain. We can see this effect in all the frequency response graphics. This is the last cut of frequency which we have been seeing in all of the graphs.

3. Discussion & Conclusion:

a. Discussion:

In part A while doing the small-signal analysis of the circuit. I assumed C1, C2, C3 to be short circuit and C4 to be open circuit. I did this because we were told in the report 10 KHz would be in the mid-band of the circuit. Then I chose the ideal state for each of the capacitors for the maximum possible gain. Now after doing the simulation of the circuit, we can see from figure 7 the 10 KHz is in the mid-band. It is great that our assumption is correct. But we could have done the same computations with a generic frequency which we assumed to be in the mid-band because the computations in part A don't actually include any frequency in them.

In part A while solving the circuit in figure 3, we multiplied R1 with $(\beta + 1)$ while calculating the current I_B. What we are doing there is we are separating the reactive current source and the r_π resistance. When we do that, we also need to put new R1 resistances to both sides that keep this new circuit and the old one equivalent. The current on the new R1 with the side with r_π has $\frac{1}{(\beta+1)}$ times less current on it. to keep the voltage on the new R1 and the old R1 the same which

keeps the node voltage the same, we multiply the new R1's resistance value with $(\beta + 1)$. This can be done for a Z1 too and we are doing it in the later part of the lab too. It is the same principle we split the Z1 and increase its impedance to keep the node voltages the same. Also, from how accurate our simulation results are from the end of part A, we can see doing this trick is not only analytically sound it also matches with the simulation results.

In part C we assumed that on the operational region of C2, C1 will act as a short circuit. If we calculate the impedance of C1 at 20 KHz which is around the center of the operational region of C2. $Z_1 = \frac{1}{j \cdot 20000 \cdot 2\pi \cdot 10^{-5}} = -j \cdot 0.796$, if we look at the schematic in figure 9 which is the circuit which we did this assumption. The smallest resistance in that circuit is 800 Ω. Which is 1000 bigger than the impedance of Z_1 in that frequency. Also, the cut of frequencies which we calculated with that assumption correlate with the graphs the simulation drew. This means this assumption and the formulas I found for the cut of frequencies are sound both analytically and simulation wise.

In part C we assumed C4 will act as an open circuit in the operational region of C3. The center of the operational region of C3 is 20 Hz we can calculate the impedance of C4 at that frequency. $Z_4 = \frac{1}{j \cdot 20 \cdot 2\pi \cdot 70 \cdot 10^{-12}} =$113.7M, if we look at figure 11, we can see the largest resistance next to C4 is 10KΩ. This means Z_4 impendence is 1000 times larger than the largest resistance next to it. which means it is a safe assumption to assume C4 as an open circuit. the cut of frequencies which we calculated with that assumption correlates with the graphs the simulation drew. This means this assumption and the formulas I found for the cut of frequencies are sound both analytically and simulation wise. Another thing which is important to mention is without these assumptions in part C the equation we got for the frequency response would be really complex and it would be extremely hard to get a clean cut off frequency from them.

Something which is really interesting is almost no matter what we do we get unity gain at really high frequencies. This can be explained by looking at figure 20. At really high frequencies C_μ shorts V_{in} and V_{out}. When this happens, we get unity gain no matter what because all the other parts of the circuit became redundant so they can't affect the gain in any way. We can stop this by putting any source resistance. In reality there will be always some source resistance no matter how small so this behavior is not something we would see in real life normally.

b. Conclusion:

This lab's goal was for us to simulate a BJT amplifier circuit and find its frequency response. This was the first time I used a BJT transistor and the first time I calculated an amplifier's frequency response. I was surprised by how accurate the values I calculated were. In part A we were told to calculate first calculate the resistance values analytically then fine tune them experimentally. But my values were so accurate I didn't even need to change them at all. I also didn't know about the logarithmic sweep function of LTspice, it was extremely useful.

During this course, my respect for LTspice only grew. I started seeing it as an actual engineering tool and not just as a free simulation tool we used in some courses. I wasn't sure if the Miller effect or splitting a resistance to 2 sides like I talked about in the discussion were safe or realistic when I first learned of them in the course. But now I understand that they are completely safe because a circuit is not characterized by its components but rather by its node voltages and the currents between those nodes. As long as those 2 are the same for 2 circuits they are equivalent circuits. And the Miller effect or that resistor splitting is just that, we are creating easier to solve circuits while keeping its node voltages and node currents the same. Also, before this lab I saw the cut off frequencies and the frequency response of a circuit as something which we cannot or didn't manipulate or care about. I thought we would normally just pick the biggest and cheapest capacitor possible in a small signal amplifier. But after doing this lab I see we can easily compute the capacitor values for the specific cut off frequencies we want and in normal life, we will be probably doing that.