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1/3/2021

EEE 313 Electronic Circuit Design – Lab Report 4

1. Introduction:

In this lab assignment, we are tasked with first characterizing an nMOS transistor (ZVN2110) and then designing a single-stage voltage amplifier using our characterization results. We used DC sweep too characterize the nMOS transistor on circuits a and b in figure 1. Then calculated the component values of the amplifier circuit analytically, c from figure 1. Then looked at our gain.

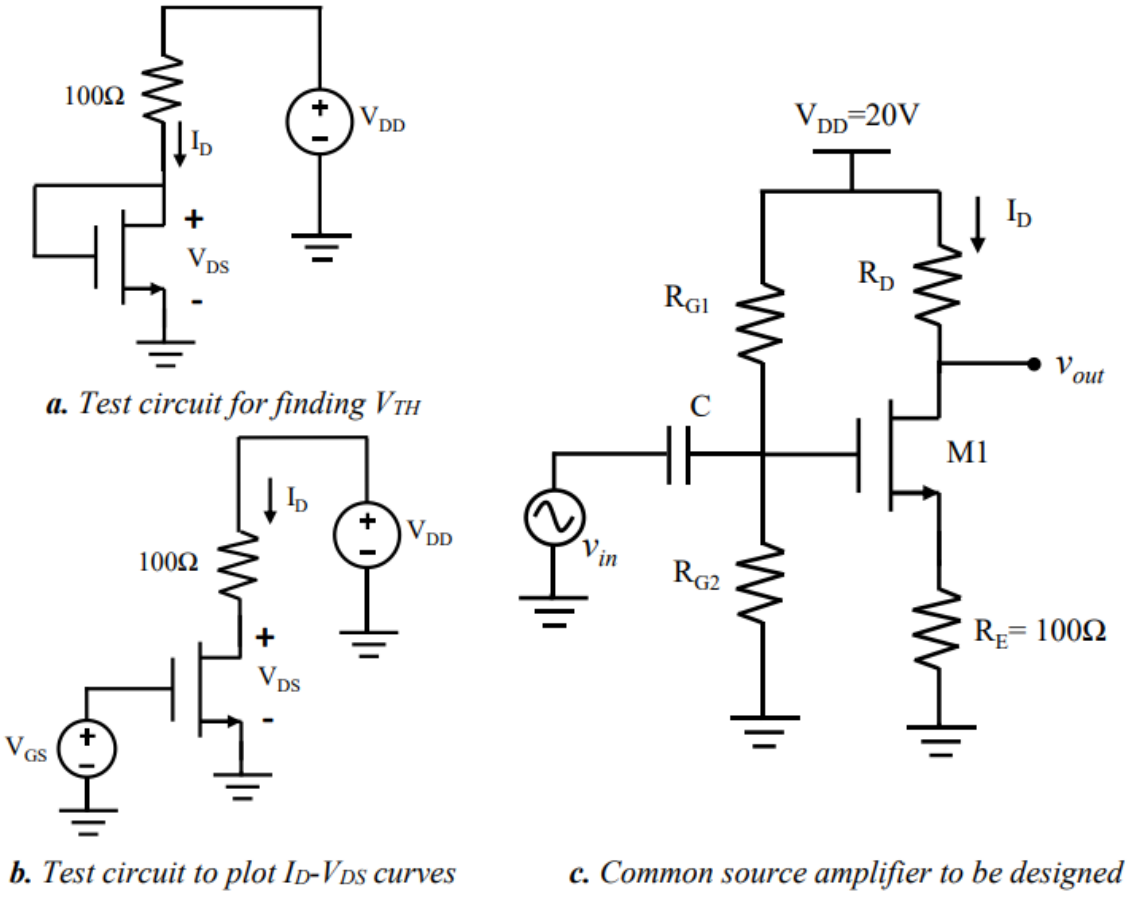

Figure 1: Circuit schematics we used in this lab

We set up these circuits in the lab on a breadboard. Then took the measurement using an oscilloscope.

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2. Lab Work:

a. Part A:

In part A we are asked to find the V_{TH} of the NMOS transistor by giving different V_{DD} voltages to the circuit figure 2. Then finding the point when the transistor opens by looking at $I_D = 1mA$.

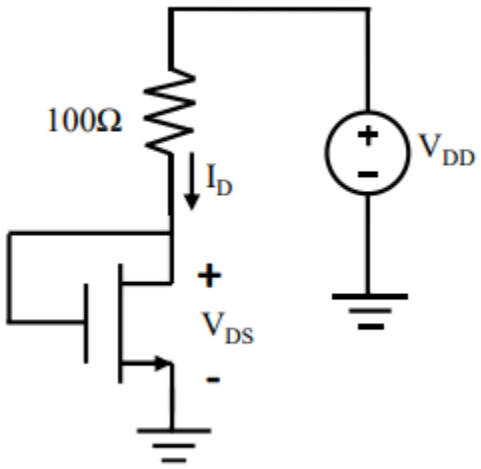


Figure 2: circuit schematic of the circuit which was used to find V_{TH}.

We built this circuit on a breadboard in the lab. Used a signal generator to give the DC sweep and used an oscilloscope to take the measurements. Here we do not need to care about the internal resistance of the signal generator because we do not care about the DC sweep values placed in it but the rate, we experimentally measure the voltage the circuit receives from the signal source. So, we do not care about what happens inside of the signal generate and only see it as the signal in figure 5.

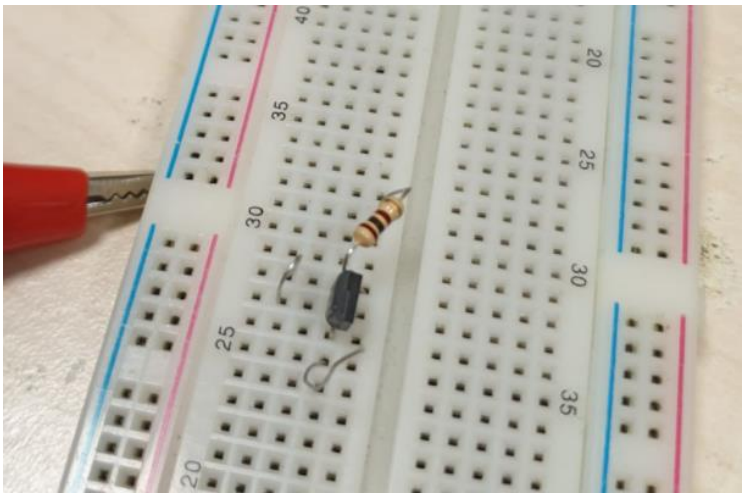


Figure 3: Picture of the circuit built on a breadboard.

Figure 4: Picture of the signal generator.

I gave the circuit a DC sweep signal and because I didn't trust the signal generator would actually supply a linear signal, I measured the signal it supplied.

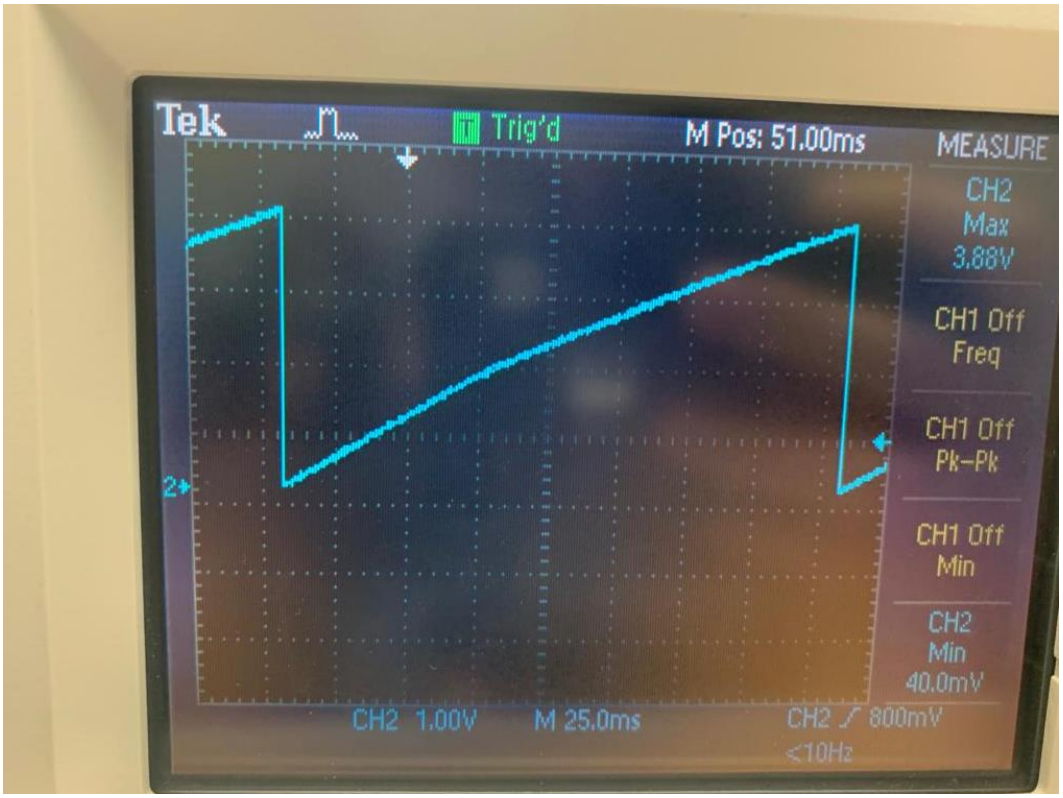


Figure 5: V_{DD} sweep signal over a period of its input to the circuit.

Like we were expecting it is not linear. Because of this to find the V_{DD} value of any measurement point we will not only multiply its measurement time with the linear increase rate of the V_{DD} signal. Instead, we will look at its measurement time and look at the V_{DD}'s value at that time point from this graph.

Then for that DC sweep, I measured the voltage over the 100Ω resistor.

Figure 6: graph of voltage over the 100Ω resistor for the DC sweep.

I found the point where the $V_R = 100\ mV$ then looked at its time of measurement then found V_{DD}'s value at that time. Which is 1.86V so we can say.

$$V_{TH} = 1.86\ V$$

Because this method didn't feel safe enough, I also wanted to calculate V_{TH} using the method shown in figure 7.

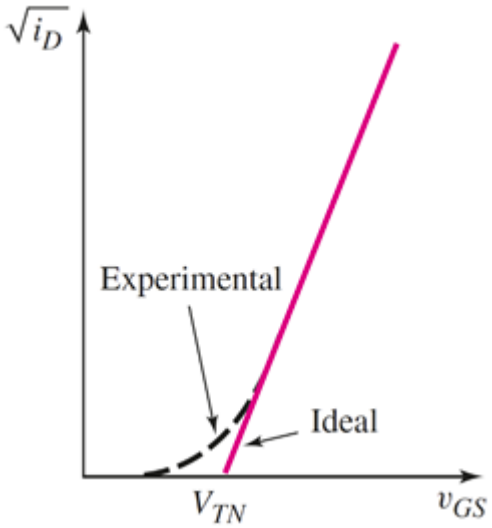
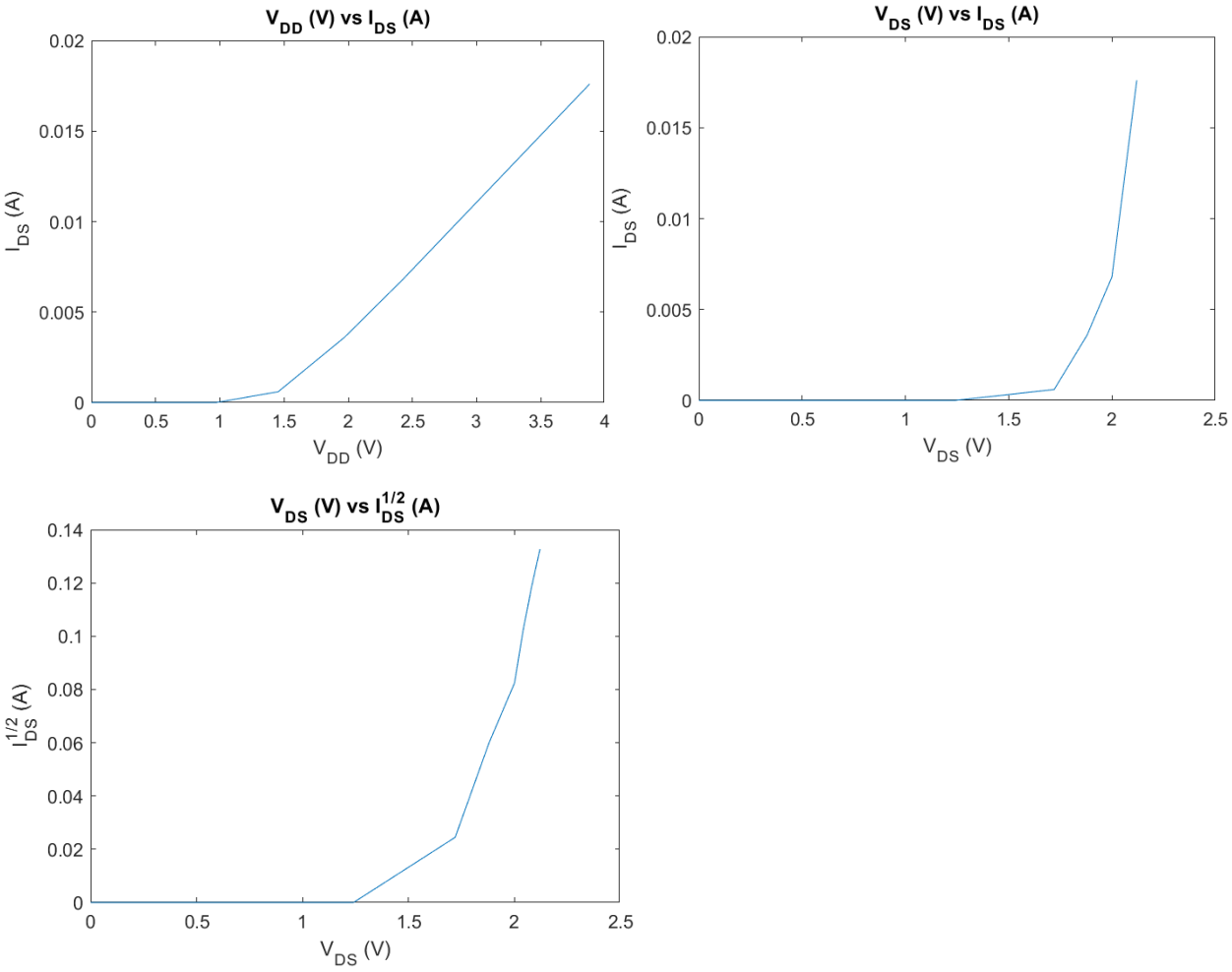


Figure 7: $\sqrt{I_D}$ vs V_{GS} graph.

I took measurements of V_{DS} over one period too.

Figure 8: graph of V_{DS} for the DC sweep.

Then I took equally spaced measurements from figures 5, 6, 8 then plotted them on MATLAB. Finally, I drew the graph of the identity given in figure 7 and calculated V_{TH} from it.



I took 2 points from the long linear part of the V_{DS} vs $\sqrt{I_{DS}}$ graph. $(2.0\ V\ , 0.082\ A)$ and $(2.04\ V\ , 0.102\ A)$ and we know the NMOS saturation current equation:

$$I_D = K_N(V_{GS} - V_{TH})^2$$

$$\sqrt{I_D} = \sqrt{K_N}(V_{GS} - V_{TH})$$

So, we can write:

$$\sqrt{I_{D1}} - \sqrt{I_{D2}} = \sqrt{K_N}((V_{GS1} - V_{TH}) - (V_{GS2} - V_{TH}))$$

$$\frac{\sqrt{I_{D1}} - \sqrt{I_{D2}}}{(V_{GS1} - V_{TH}) - (V_{GS2} - V_{TH})} = \sqrt{K_N} \quad (1)$$

We plug in the values we know in to equation 1.

$$\frac{0.102 - 0.082}{2.04 - 2} = \sqrt{K_N}$$

$$0.5 = \sqrt{K_N}$$

Then we can find V_{TH} using the linear equation given in figure 7:

$$I_{DS} = \sqrt{K_N}(V_{DS} - V_{TN}) \quad (2)$$

Put the point $2.0\ V$, $0.082\ A$ in equation 2.

$$0.082 = 0.5(2 - V_{TH})$$

$$0.164 = (2 - V_{TH})$$

$$V_{TH} = 1.836\ V$$

This is really close to our find of V_{TH} from the other method which gives me confidence for both of them. I will be using $V_{TH} = 1.836\ V$ for the rest of the experiments because it is found with the more scientific method. In the manual, we are told to take the measurement of the current between 0 and 30 mV in this part. We only did between 0 and 18 mV because the point which is most important for our measurements is at 1 mV also, we can see all the different states of a transistor for a measurement between 0 and 18 mV. I also asked Erdinç Tatar if this measurement is enough and correct and he told me that it is. He also told me to write in my report that he approves of this measurement method.

b. **Part B:**

In this part, we are asked to do 3 DC sweeps over the V_{DD} for 3 different V_{GS} voltages, $\mathrm{V_{GS}} = V_{TH} + 0.3$, $\mathrm{V_{GS}} = V_{TH} + 0.4$ *and* $\mathrm{V_{GS}} = V_{TH} + 0.5$ for the circuit given in figure 9. Then we are asked to find the K_N and λ of the given transistor.

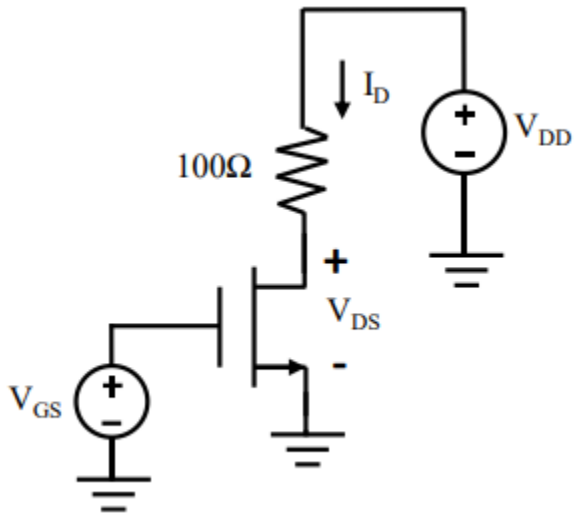


Figure 9: Schematic of the circuit used in part B.

First, I built this circuit on the breadboard using a DC voltage source for the V_{GS} and a signal generator for the DC sweep for the V_{DD}. Then made my measurements with an oscilloscope.

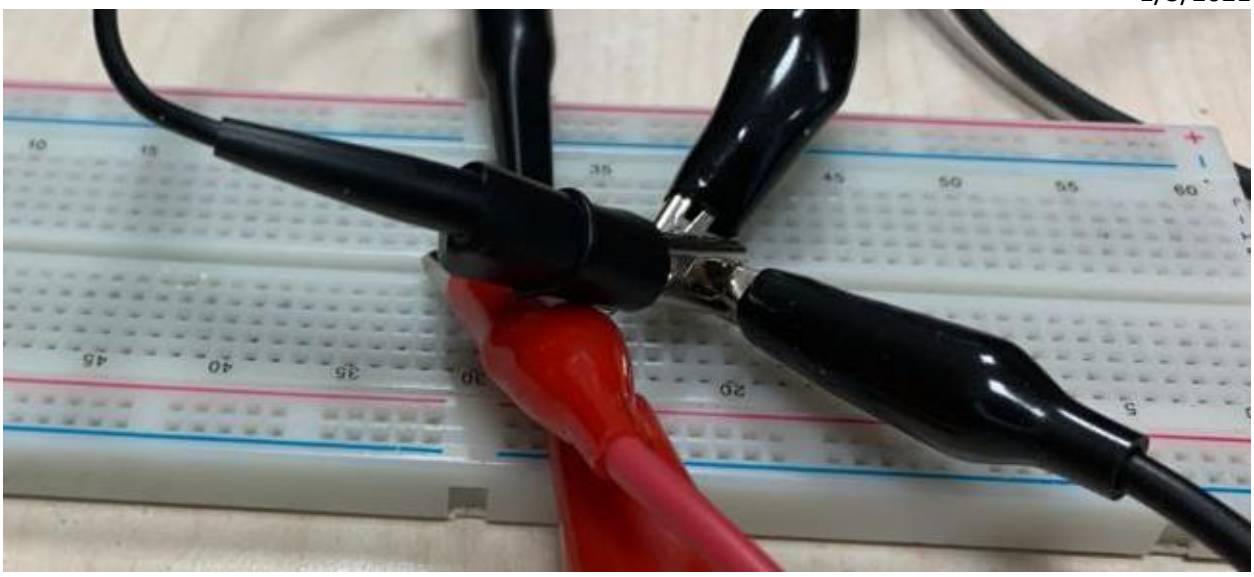


Figure 10: assembled circuit on the breedboard.

Then with this setup I got these results.

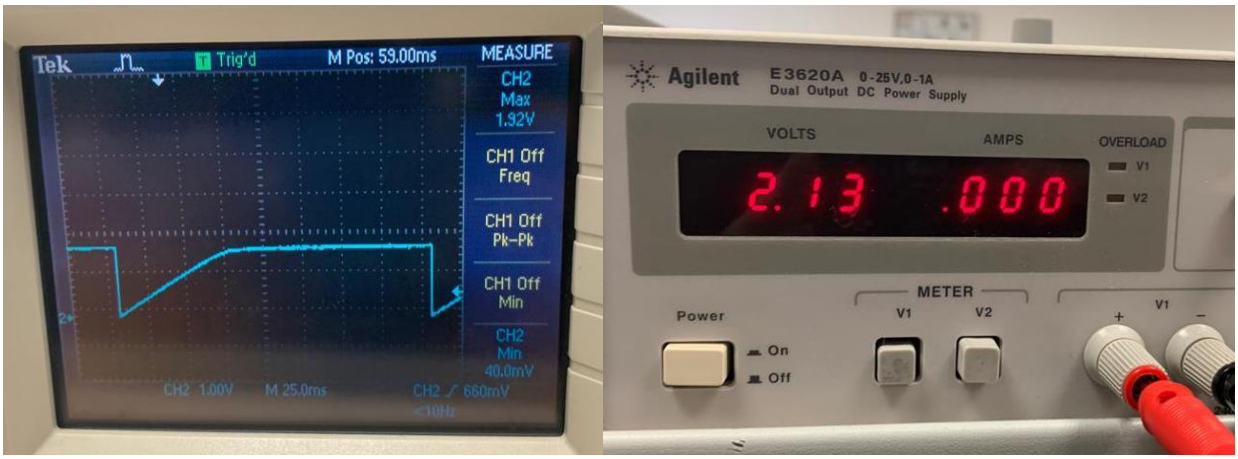


Figure 11: time vs $100I_D$ graph for V_{GS} = 2.14.

Figure 12: time vs $100I_D$ graph for V_{GS} = 2.24.

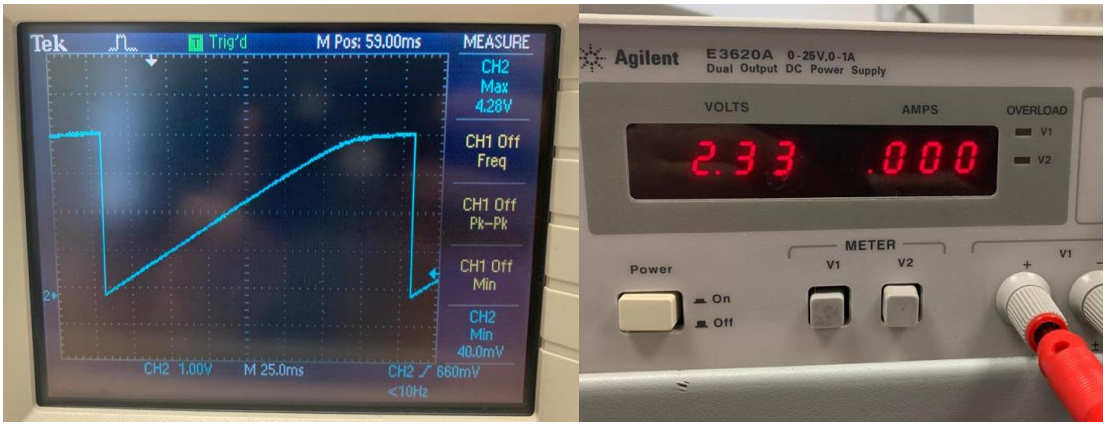


Figure 13: time vs $100I_D$ graph for V_{GS} = 2.34.

Then I manually took sample points from these measurements to calculate their $V_{DS}'s$ using the equation given in the lab manual: $V_{DS} = V_{DD} - I_D 100$. Then I put these values in MATLAB to plot these graphs. I used a different V_{DD} signal range for this part so I am putting this one here too. I used it to find the V_{DD} values of the different measurement points.

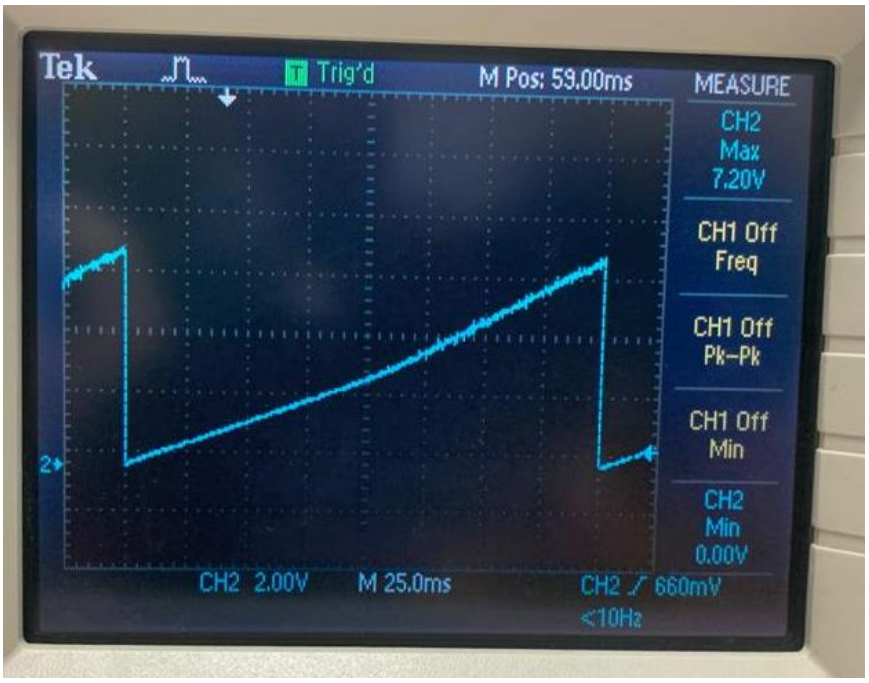
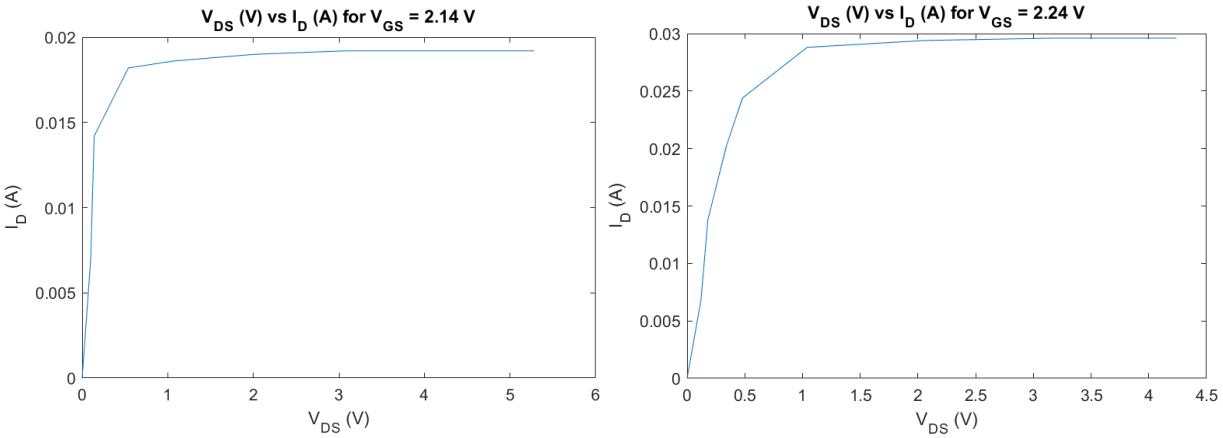
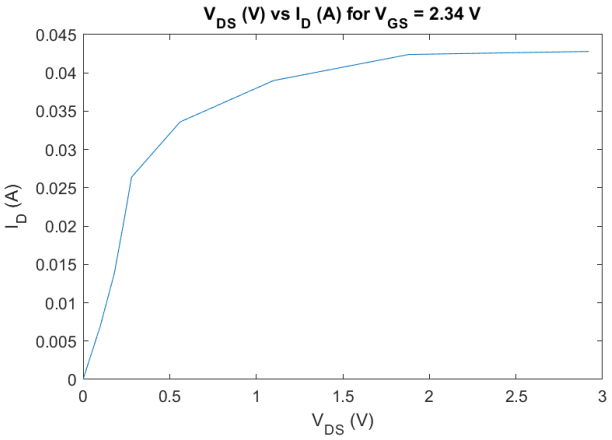


Figure 14: V_{DS} graph for one sweep period in part 2

I got these MATLAB graphs:





To find the λ of the transistor I used the identity shown in figure 15 and $r_0 = \frac{1}{I_{DQ}\lambda}$ equation.

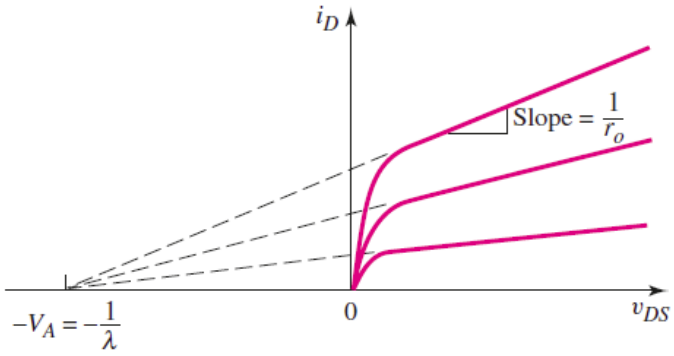


Figure 15: identity used to find r_0.

To do this we can zoom in to the linear part of one of the I_D vs V_{DS} graphs. Then look at an equivalent time interval of both graphs then from them calculate V_{DS} and using that find the slop of I_D vs V_{DS} graph.

Figure 16: zoomed in I_D to calculate r_0

Figure 17: zoomed in V_{DS} to calculate r_0

At the sample point 1 $V_{DD1} = 6.40\ V$, $V_{R1} = 100I_{D1} = 4.04\ V$ so its $V_{DS1} = 2.36\ V$ and at the sample point 2 $V_{DD2} = 8.80\ V$, $V_R = 100I_D = 4.40\ V$ so its $V_{DS2} = 4.40\ V$. Using these we can calculate r_0 as:

$$\frac{I_{D2} - I_{D1}}{V_{DS2} - V_{DS1}} = \frac{1}{r_0}$$

$$\frac{0.0440 - 0.0404}{4.40 - 2.36} = \frac{1}{r_0}$$

$$\frac{0.0036}{2.04} = \frac{1}{r_0}$$

$$\frac{1}{r_0} = 1.76\ m\Omega^{-1}$$

We can rewrite $r_0 = \frac{1}{I_{DQ}\lambda}$ as $\lambda = \frac{1}{I_{DQ}r_0}$ for or sample point the average current is $I_{DQ} = \frac{I_{D2}+I_{D1}}{2}$

$$I_{DQ} = \frac{0.0440 + 0.0404}{2}$$

$$I_{DQ} = 0.0422\ A$$

$$\lambda = \frac{1}{I_{DQ}r_0}$$

$$\lambda = \frac{1.76\ m}{0.0422}$$

$$\lambda = 0.042\ V^{-1}$$

Now to calculate K_N we can use the saturated NMOS current equation.

$$I_D = K_N(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \qquad (3)$$

To find the best value I could find I will use the end point of the 3 I_D vs V_{DS} graphs and calculate the K_N for each of them using equation 3.

For $V_{GS} = 0.3 + V_{TH}$:

$$0.0192 = K_{N1}(0.3)^2(1 + 0.042 \cdot 5.28)$$

$$0.0192 = K_{N1} \cdot 0.09 \cdot 1.22$$

$$K_{N1} = \frac{0.0192}{0.1098} = 0.175$$

For $V_{GS} = 0.4 + V_{TH}$:

$$0.0296 = K_{N2}(0.4)^2(1 + 0.042 \cdot 4.24)$$

$$0.0296 = K_{N2} \cdot 0.16 \cdot 1.178$$

$$K_{N2} = \frac{0.0296}{0.1885} = 0.157$$

For $V_{GS} = 0.5 + V_{TH}$:

$$0.0428 = K_{N3}(0.5)^2(1 + 0.042 \cdot 2.92)$$

$$0.0428 = K_{N3} \cdot 0.25 \cdot 1.123$$

$$K_{N1} = \frac{0.0428}{0.2807} = 0.152$$

Then finally, we can say:

$$K_N = \frac{K_{N1} + K_{N2} + K_{N3}}{3}$$

$$K_N = \frac{0.175 + 0.157 + 0.152}{3}$$

$$K_N = 0.16$$

c. Part C:

In this part, we are asked to design a common source amplifier like the one shown in figure 18 which gives an absolute gain higher than 9. We also want it to do this with a drain current between 10 mA and 15 mA with an input signal of 100mV V_{PP} with 10 KHz frequency. Also, we want R_{in} to be more than 30 KΩ and R_{out} to be less than 2 KΩ. Then we are asked to increase the V_{in} voltage value until we get a saturated output.

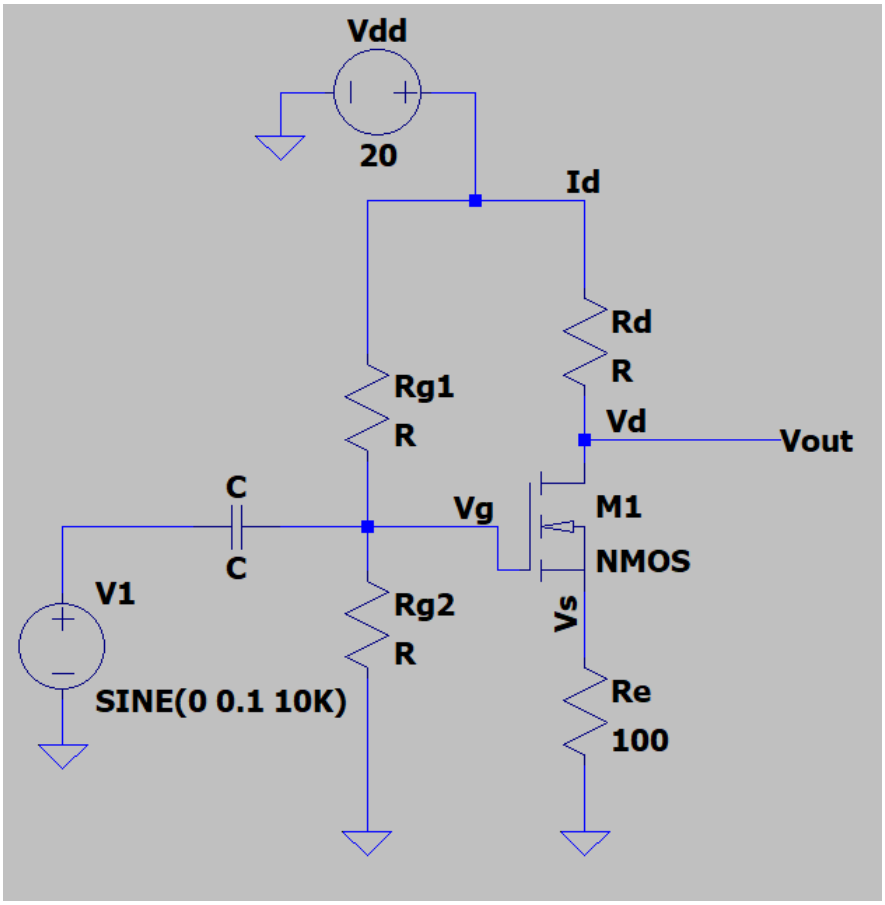


Figure 18: Circuit schematic of the amplifier circuit

I first assumed the transistor is in saturation. Then we know the current equation of a saturated transistor.

$$I_D = K_N(V_{GS} - V_{TN})^2(1 + \lambda V_{DS}) \quad (4)$$

Then because we are given a range of desired I_D values I choose I_D as 14 mA. then I plugged in all the values I know to equation 4.

$$0.014 = 0.16(V_G - 1.4 - 1.836)^2(1 + 0.042V_{DS})$$

$$\frac{0.0875}{(1 + 0.042V_{DS})} = (V_G - 1.4 - 1.836)^2$$

$$\frac{0.296}{(1 + 0.042V_{DS})^{\frac{1}{2}}} = (V_G - 1.4 - 1.836)$$

$$V_G = 3.236 + \frac{0.296}{(1 + 0.042V_{DS})^{\frac{1}{2}}} \quad (5)$$

In equation 5 the effect of λV_{DS} is minimal. So, I am going to ignore it. This will be further discussed in the discussion. Then we know V_G.

$$V_G = 3.532$$

We know V_G gets it value from a voltage divider between $R_{G1}\ and\ R_{G2}$. We can use this to find the ratio between R_{G2}, R_{G1}. To do this we write it as:

$$V_G = V_{DD}\frac{R_{G2}}{R_{G1} + R_{G2}}$$

$$3.532 = 20\frac{R_{G2}}{R_{G1} + R_{G2}}$$

$$R_{G2} = 7R\ , R_{G1} = 33R$$

Now we know the ratio between R_{G2}, R_{G1}. We only need to choose sufficiently large while the fit in to the ratio. For this I choose.

$$R_{G2} = 39\ K\Omega\ , R_{G1} = 200\ K\Omega$$

Why I choose them the way I did will be further discussed in the discussion.

Then we will look at the small signal model of the circuit for the small signal gain.

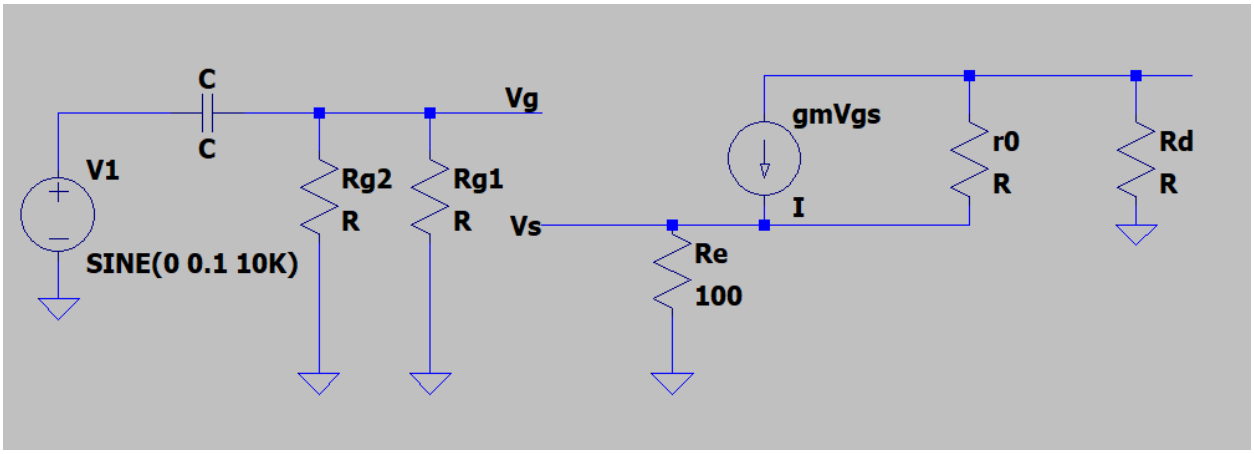


Figure 19: small signal model of the circuit.

From this we can see without calculating that the higher we make R_D the higher the gain will be and because there isn't any upper limit to how high the gain should be, we will just calculate the R_D value for the highest gain. But we cannot arbitrarily increase R_D because as we can see from figure 18, we the higher we make R_D the smaller V_D will get and if it gets too small the transistor will get out of the linear region. From this, we can get a limit to R_D.

We know the equation for the saturation condition of an NMOS transistor.

$$V_{DS} > V_{GS} - V_{TN}$$

$$V_D - V_S > V_G - V_S - V_{TN}$$

$$20 - I_D R_D - (0 - I_D R_E) > V_G - (0 - I_D R_E) - V_{TN}$$

$$20 - 0.014R_D - (0 - 0.014 \cdot 100) > 3.532 - (0 - 0.014 \cdot 100) - \ 1.836$$

$$20 + 1.4 - 0.014R_D > 3.532 + 1.4 - 1.836$$

$$-0.014R_D > -18.304$$

$$0.014R_D < 18.304$$

$$R_D < 1307\Omega$$

From this, I choose R_D as 1.2 KΩ. I will further discuss this in the discussion part.

From these values, I built my circuit on a breadboard. I used a DC voltage source the V_{DD} and used a signal generator for the input small signal and took my measurements with an oscilloscope. I used a 400 mF capacitor for the capacitor. This will be further discussed in the discussion.

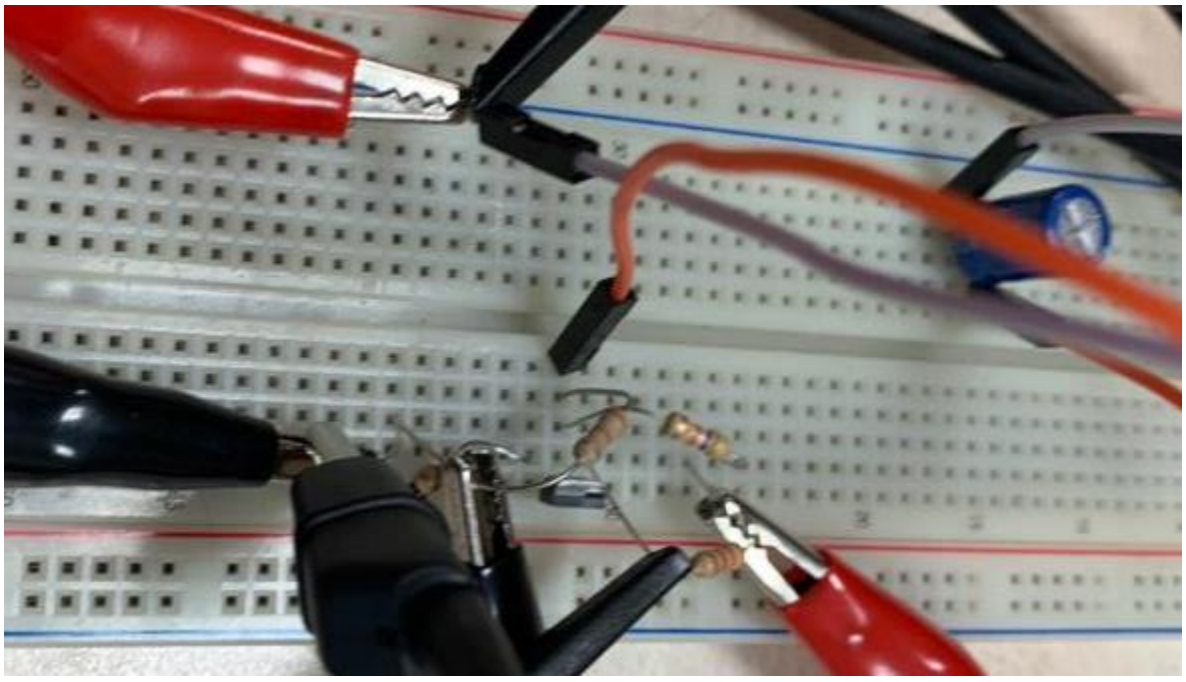


Figure 20: the circuit in part c on the breadboard

After giving the input signal to the circuit and taking the measurements of the input and out put signal at the same time I got.

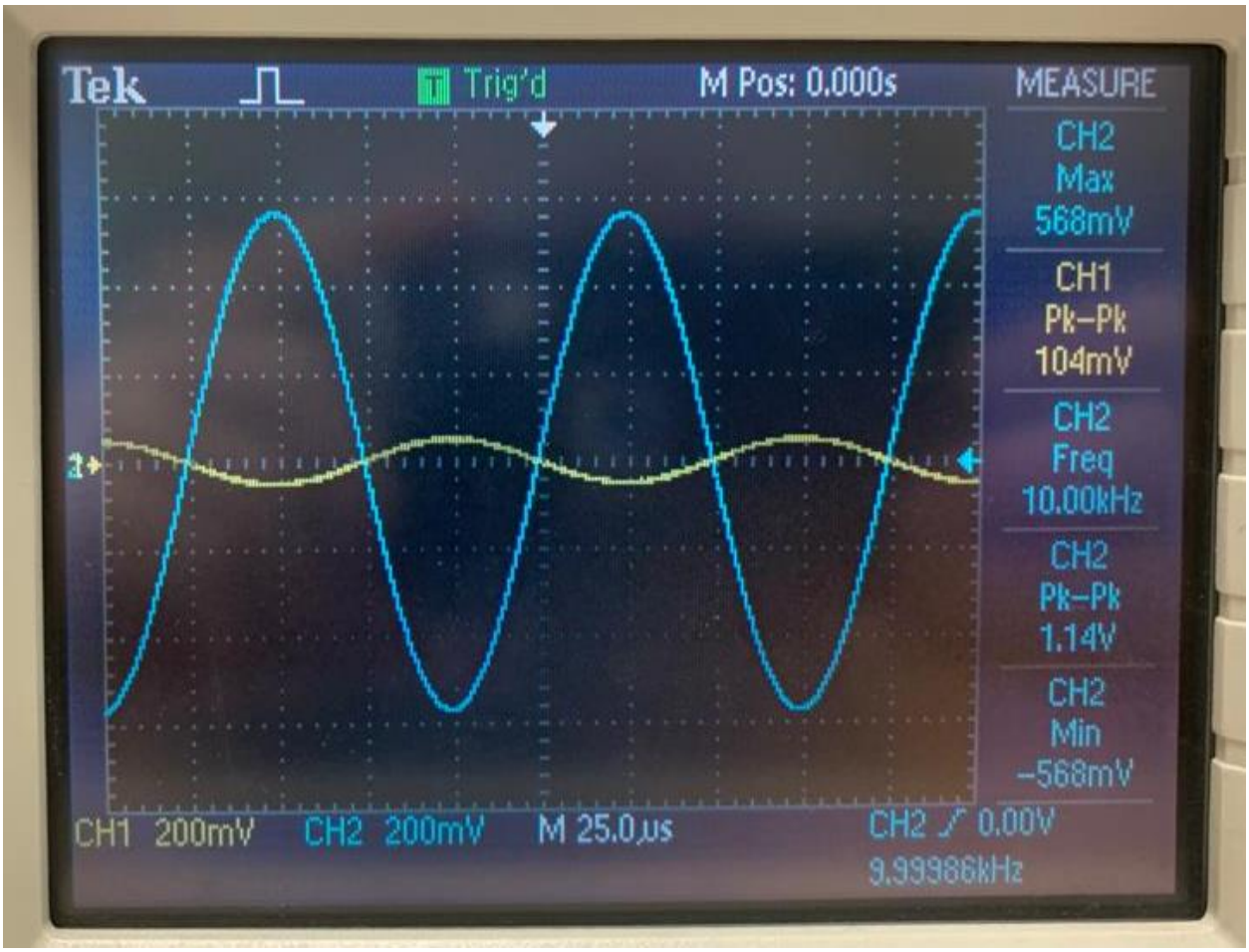


Figure 21:Graph of the input output voltages from the amplifier circuit.

The gain is here is $A_V = -\frac{1.14}{0.104}$ which means $|A_V| = 11 > 9$ so this satisfies the given condition. Also while giving is this gain the current the DC voltage supply supplies is 0.015 A which is the sum the two currents on the two branches of the circuit and the current on the R_{G1}, R_{G2} is very small so the current on the transistor "I_D" is very close to 0.015 A. which is between 10 mA and 15 mA. If we calculate R_{in}

$$R_{in} = R_{G1}//R_{G2}$$

$$R_{in} = 200K//39K$$

$$R_{in} = 32.64\ K\Omega$$

Which is bigger than 30 KΩ.

Then if we calculate R_{out} we know $r_0 = \frac{1}{I_{DQ}\lambda} = \frac{1}{0.014 \cdot 0.042} = 1700\ \Omega$

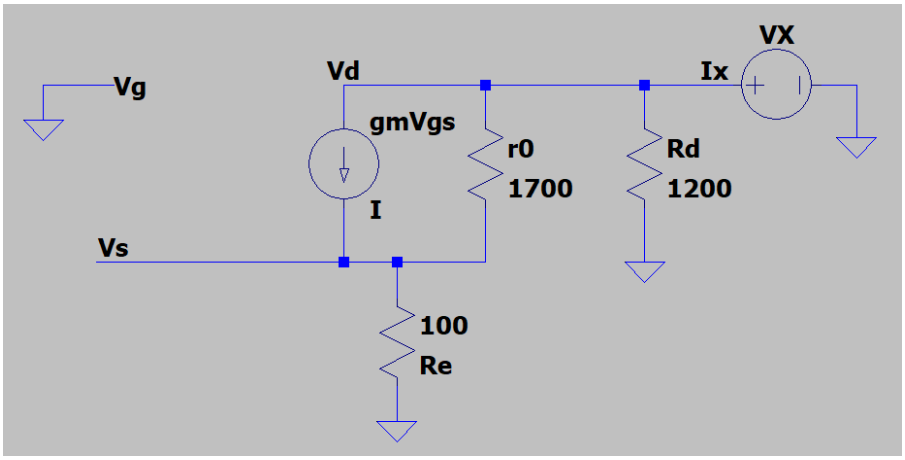


Figure 22: circuit schematic of the circuit to calculate the Rout

From figure 22 we can write:

$$I_X = \frac{V_X}{R_D // r_0 + R_e}$$

$$I_X = \frac{V_X}{1200 // 1800}$$

$$I_X = \frac{V_X}{720}$$

$$R_{out} = \frac{V_X}{I_X} = 720\Omega$$

$R_{out} = 720\Omega < 2000\Omega$ so, we have achieved all of our conditions for the amplifier circuit.

Then I increased the V_{in} voltage value until I get a saturated output.

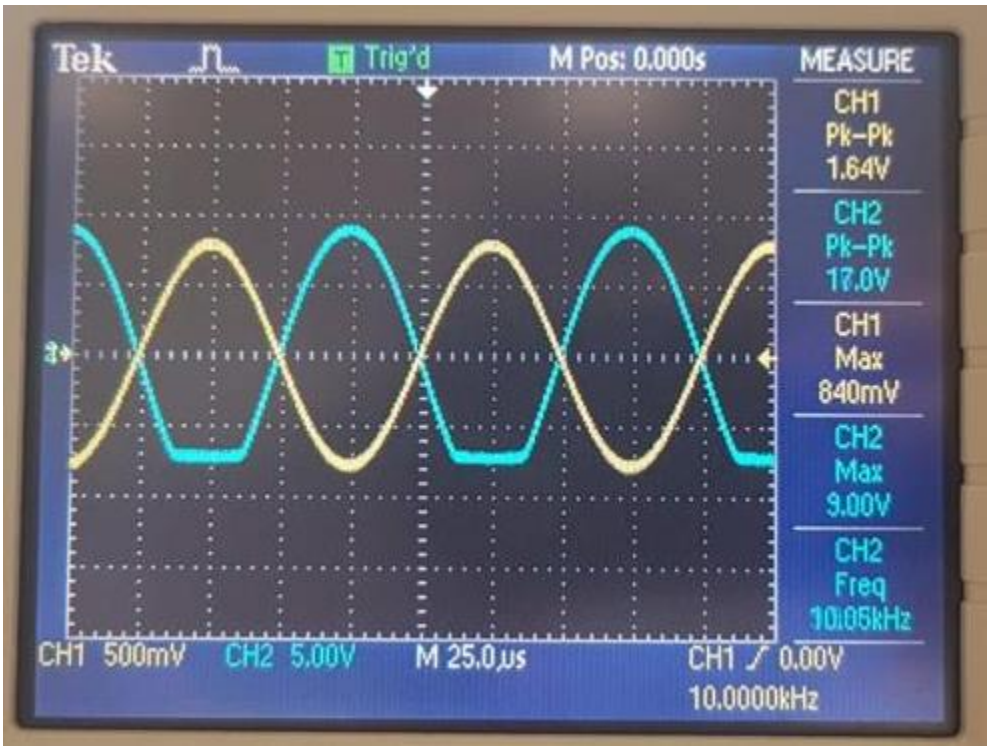


Figure 23: Graph of increased Input voltage with the saturated output voltage.

This happens because if we increase the input voltage too much the transistor gets out of the saturation region. We can see this better if we write the NMOS saturation condition formula.

$$V_{DS} > V_{GS} - V_{TN}$$

$$V_D - V_S > V_G - V_S - V_{TN} \quad (6)$$

In equation 6; V_D , V_S and V_{TN} are constant in the saturation region so:

$$V_D > V_G - V_{TN}$$

$$V_G < V_D - V_{TN}$$

So, the maximum input voltage is determined $V_D - V_{TN}$. For our values

$$V_G < 20 - 0.014 \cdot 1200 - 1.836$$

$$V_G < 1.364$$

On the figure 23 the saturation occurs at lower voltage level the calculated one. This will be further discussed in the discussion.

d. Part D:

In this part, we are asked to connect a parallel capacitor to R_e and report our gain. Then explain the change in our gain.

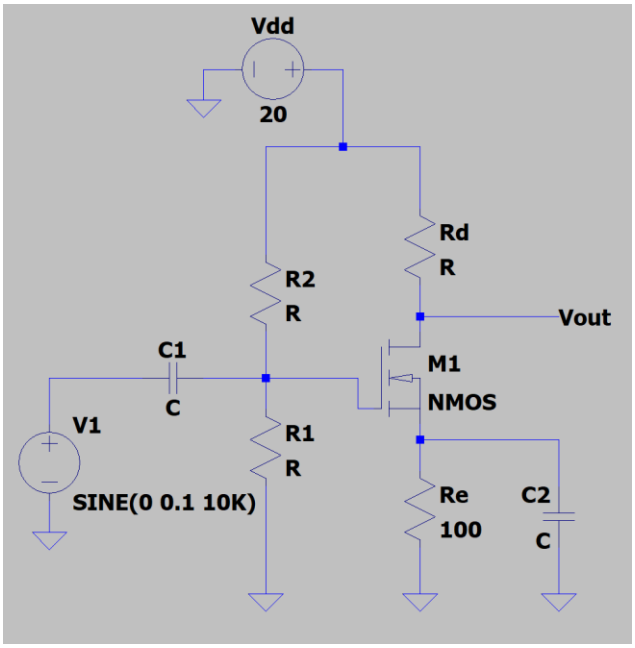


Figure 24: Circuit schematic of amplifier circuit in part D.

I once again built this circuit on a breadboard. I used a DC voltage source for the V_{DD} and used a signal generator for the input small signal and took my measurements with an oscilloscope. I used a 400 mF capacitor for both of the capacitors.

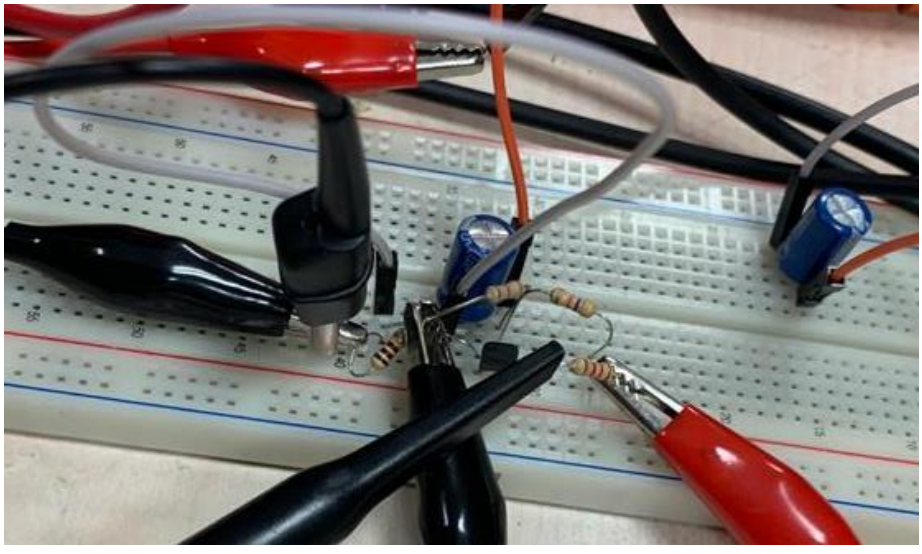


Figure 25: Picture of the amplifier circuit in part D.

After building it I gave it the input signal and recorded the input output signals.

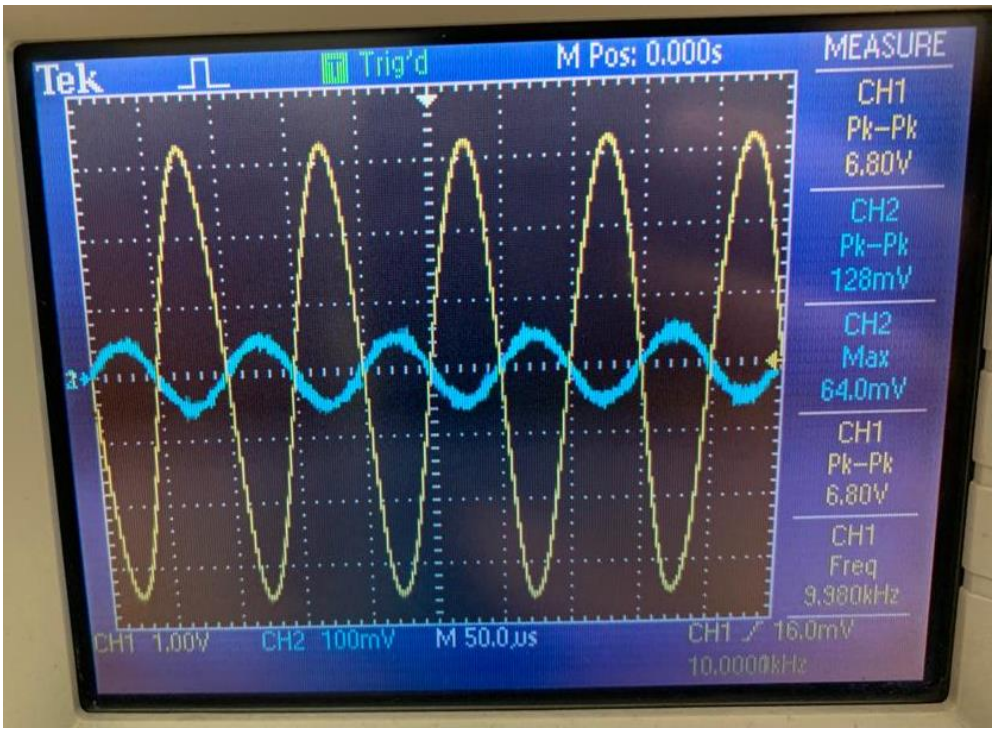


Figure 26: Graph of the input output voltages of the amplifier circuit in part D.

We can see the gain almost increased by 7 times. This is expected and can be explained by doing the circuit analysis of the circuit. The capacitor acts like open circuit for DC voltage so we only need to do the analysis on the Small signal model.

Lets first calculate the gain for the circuit in part C, the one without the extra capacitor.

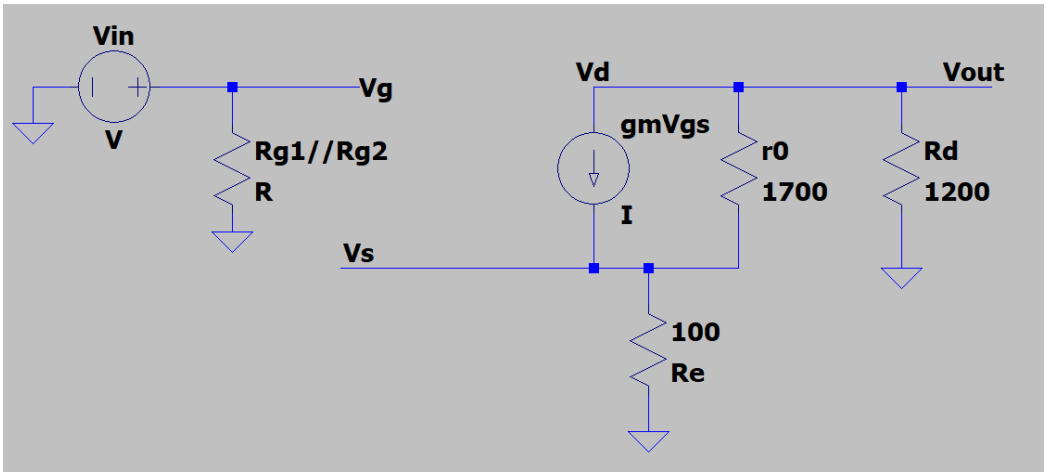


Figure 27: The small signal model of the amplifier from part C.

We know $V_{GS} = V_{in} - V_s$

We write KCL at V_{out}:

$$\frac{V_{out}}{R_d} + \frac{V_{out} - V_S}{r_0} + g_m V_{GS} = 0 \quad (7)$$

We write KCL at V_S:

$$-\frac{V_{out} - V_S}{r_0} - g_m V_{GS} + \frac{V_S}{R_e} = 0 \quad (8)$$

We sum equation 7 and 8:

$$\frac{V_{out}}{R_d} + \frac{V_S}{R_e} = 0$$

$$V_S = -\frac{V_{out} R_e}{R_d} \quad (9)$$

Put equation 9 back into equation 7:

$$V_{out}\left(\frac{1}{R_d} + \frac{1}{r_0}\right) - \frac{V_S}{r_0} + g_m(V_{in} - V_s) = 0$$

$$V_{out}\left(\frac{1}{R_d} + \frac{1}{r_0}\right) - V_S\left(g_m + \frac{1}{r_0}\right) + g_m V_{in} = 0$$

$$V_{out}\left(\frac{1}{R_d} + \frac{1}{r_0}\right) + \frac{V_{out} R_e}{R_d}\left(g_m + \frac{1}{r_0}\right) + g_m V_{in} = 0$$

$$V_{out}\left(\frac{1}{R_d} + \frac{1}{r_0} + \frac{R_e}{R_d} g_m + \frac{R_e}{R_d r_0}\right) + g_m V_{in} = 0$$

$$V_{out}\left(\frac{1}{R_d} + \frac{1}{r_0} + \frac{R_e}{R_d} g_m + \frac{R_e}{R_d r_0}\right) = -g_m V_{in}$$

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{\left(\frac{1}{R_d} + \frac{1}{r_0} + \frac{R_e}{R_d} g_m + \frac{R_e}{R_d r_0}\right)} \quad (10)$$

To put in our values. We need to know gm first

$$g_m = 2\sqrt{K_N * I_{DQ}}$$

$$g_m = 2\sqrt{0.16 * 0.014}$$

$$g_m = 0.095\ (\frac{A}{V})$$

Put all the values we know into equation 10.

$$\frac{V_{out}}{V_{in}} = A_V = \frac{0.095}{\frac{1}{1200} + \frac{1}{1700} + \frac{100}{1200}0.095 + \frac{100}{1200 \cdot 1700}}$$

$$A_V = 10.12$$

This is just like what we were expecting so this is nice.

Then we calculate the gain of the amplifier in this part:

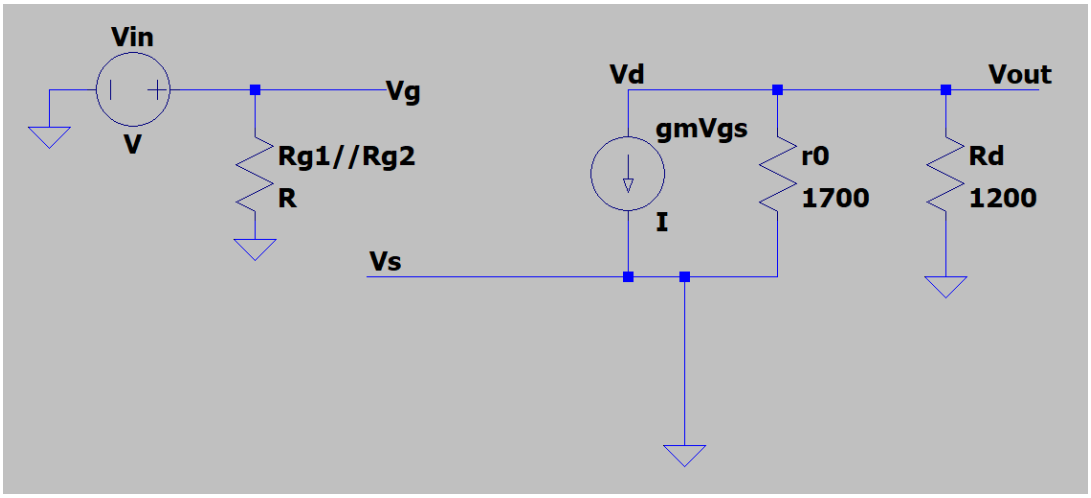


Figure 28: The small signal model of the amplifier from part D.

In AC the capacitor will act like a short circuit which will short the source terminal of the transistor. Then the gain can be easily calculated as:

$$V_{GS} = V_{in} - 0$$

$$V_{out} = -g_m V_{GS} \cdot r_0 // R_d$$

$$V_{out} = -g_m V_{in} \cdot r_0 // R_d$$

$$\frac{V_{out}}{V_{in}} = A_V = -g_m \cdot r_0 // R_d \quad (11)$$

Then we can put in our values in this circuit into equation 11:

$$A_V = -0.095 \cdot 700$$

$$A_V = -0.095 \cdot 700$$

$$A_V = -66.8$$

Once again this is just like the voltage value in figure 26, which means our computations represent the reality.

From these computations we can see why connecting a capacitor to the source terminal increased the gain almost 7-fold.

3. Discussion & Conclusion:

a. Discussion:

In part C while calculating V_G we ignored the effect of the λ. This was not very important because we know the V_{DS} from our experiments was 1.8 volts but to be even more robust we will assume it was 2 volts. Even if V_{DS} was 2 volts then the value of V_G is 3.52 volts. This is only 0.01 volts smaller than the V_G calculated without the λ. And on top of the difference being very small, I didn't even choose exact resistance values for the resistance which determine V_G.

Just as I mentioned it, I did not choose the exact resistance values for the resistors which determine V_G. I choose the values I did because those resistors were available in the lab and I didn't want to combine multiple resistances to create the exact resistances I needed. This has 2 reasons, first, all the resistances we use in the lab already has 5% error margins so to get the exact resistance values I would need to combine multiple resistances and then measure its resistance with a multimeter and change the resistance in it until I find ones with the right amount of error. Second, is we choosing those resistances to get a specific V_G voltage which will create a I_D current between 2 values. So, V_G has a range of values it can take and there is a range of values $R_{G1}\ and\ R_{G2}$ can take and we only need our choice of $R_{G1}\ and\ R_{G2}$ to fall in that range. We can check if they fell in that range by experimenting and measuring the I_D voltage. If we measured an I_D current out of the desired range we would have chosen more precise resistance values. But we didn't so our crude choice of R_{G1} and R_{G2} is correct and sufficient.

Once again in part C, I chose R_D as 1.2 KΩ just like I explained above we don't want an exact gain we only need our gain to be bigger than a specified amount which was 9 to be precise. I didn't want to choose R_D to big fearing I would get the NMOS out of saturation. So, I choose R_D as 1.2 KΩ which is modestly big but still relatively far from the maximum amount. This choice gave us an absolute gain of almost 11 which is greater than 9 so my choice is correct and sufficient.

I choose all my capacitors as 400 mF capacitors because that was the biggest one available in the laboratory. I choose their capacitance as big as possible because the bigger their capacitance is the lower their impedance will be at the frequency of the small signal. And we want them to have as low as possible impedance because their impedance negatively affects our gain.

On Part C our calculated maximum V_{in} voltage until V_{out} saturates is higher than the one we experimentally measured. This is something to be expected because we did the computations for the experimental maximum V_{in} voltage until V_{out} saturates by assuming I_D current as 14 mA. But during experimentation, we saw it was a value close to 15 mA. I_D effects V_D linearly and at a great rate. Increasing I_D by 1 mA decreases V_D by 1.2 volts. The experimental value of 0.600 volts is only 0.764 volts which is smaller than the analytic value of 1.364 volts. This can accrue because our experimental I_D value is 0.637 mA higher than the assumed one. This correlates with out measurements of the I_D in the experiment. This means my calculation correlate with the behavior of the circuit. Also, I successfully found what determines maximum V_{in} voltage until V_{out} saturates. Because the amplifier satisfies all the conditions given in the lab and I found what determines the maximum voltage V_{in} could take until V_{out} saturates, my work in this part was successful and sufficient.

b. Conclusion:

This lab's goal was for us to use a real NMOS transistor and find some of its characteristics and using them to build a real small-signal amplifier. This was the first time I used a real NMOS transistor. I was extremely surprised by how well the formulas we were learning in the course. Before in courses, I have taken I would almost always write how the formulas we are using for the experiment do not represent reality and how the thing which we were ignoring were affecting our measurements in an uncalculatable way. But in this experiment, the experimental measurements almost perfectly correlate with the analytic computations and the things which we ignored actually weren't affecting our results in a meaningful way or we can compute their effect analytically. This is really exciting for me because this is the first time, I am not explaining how the things we are ignoring are causing an uncalculatable error in a lab like this. Because of this, I realized how close to reality things that we are learning in this course are. The other reason for the almost nonexistent error is all the requirement for the amplifier circuit were not exact so, we didn't need to calculate exact values so it is a lot easier to find component values which satisfy them. This approach to a system requirement is a lot more realistic because in real life we really need an exact voltage value instead we usually need a voltage between two thresholds. Seeing the formulas, we learned working so correctly in a realistic task, gave me the confidence I could actually design and implement a circuit which could really work in realistic setting using the thing I learned in this course.