LabWork 7
FSM Design
Batu Arda Düzgün
06.12.2019

Gates:

- One 74 LS/HC 08 (Quad 2-input AND gate)
- One 74 LS/HC 32 (Quad 2-input OR gate)
- One 74 LS/HC 86N (Quad 2-input XOR gate)
- One 74 LS/HC 74 (ON Semiconductor - Dual D Flip−Flop)

Abstract / Objective:

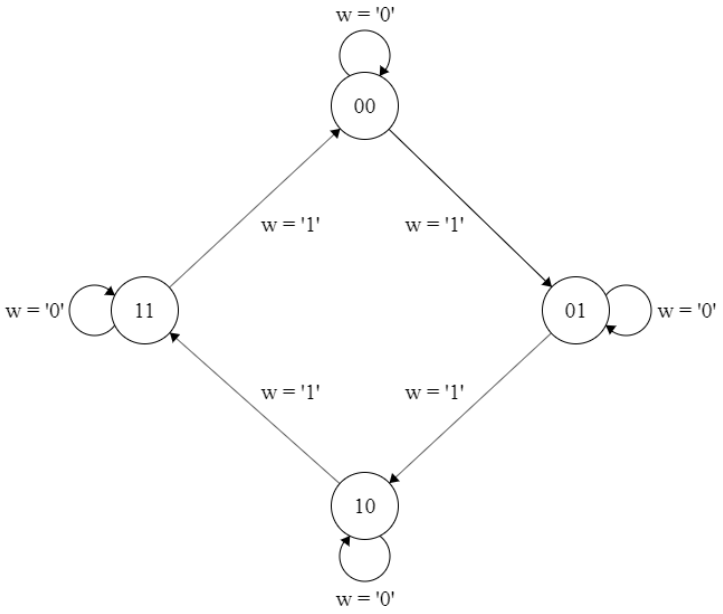
In this Lab we are expected create a FSM on our breadboards using circuit components from 74 LS/HC family. We already created circuits using this components so the purpose of this lab is to broaden our understanding of FSM's and for us to design our own FSM circuits. To do this I will draw FSM graph of my design. Then using that I will draw the truth table of my design then draw K maps of my outputs then finally using the K maps I will find the Logic equations of my design and finalize my design.

Design Specification Plan:

I will take my FSM's inputs from a sound censors. I will use a sound censor for input because I am making a project that uses sound censors in it. So I am used to using them and I like using them. I will just connect my D flip flops out puts to Leds because if I do it that way it is easier to see if the FSM is working as intended. Also I thought it would be almost classical to make a light that would light on and off by clapping.

Proposed Design Methodology:

I will be using a 2 bit FSM so it will have 4 different states. I want it to change between those 4 states when I give it a '1' signal and I also want it to stay the same way when I give it a '0' signal. So first I will draw the FSM graph of my circuit.



w is my input from the sound censor

Then from the FSM graph I will write the truth table of my design.

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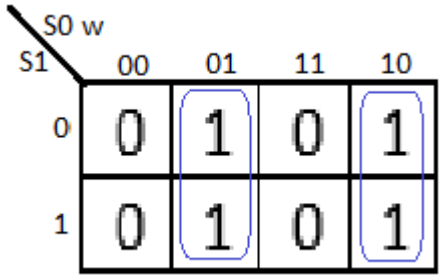
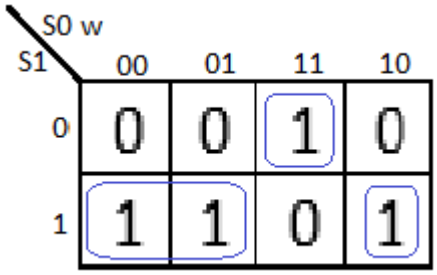
S1	S0	w	NS1	NS0
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

S1 and S0 are the current state of my D flip flops and NS1 and NS0 are the nest state of my D flip flops.

Then from truth table I will draw the K maps for NS1 And NS0.



NS0 = (S0 xor w)



NS1 = (S1 and S0') or ((S1 xor w) and S0)

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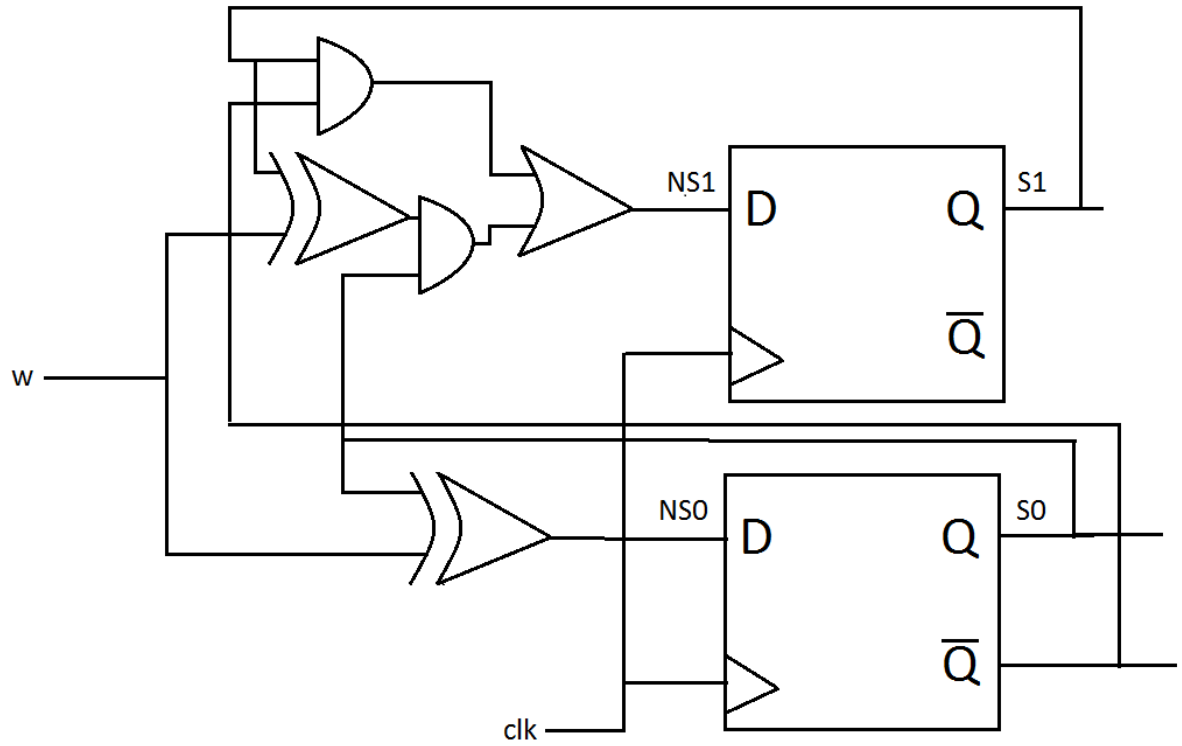
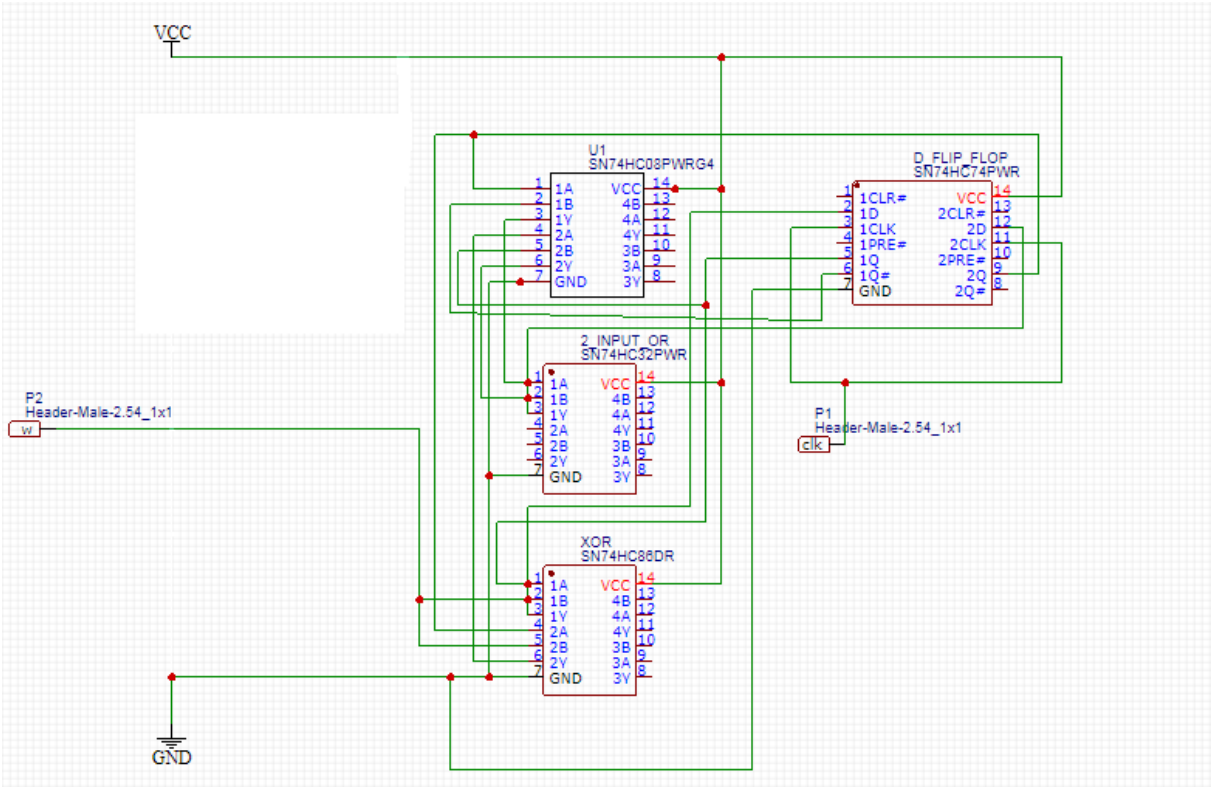


This is a basic diagram of my FSM circuit (my actual circuit will be way different than this.)



This is a schematic of my circuit.