Lab3 Combinational circuit Design
Preliminary Report
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Objective:

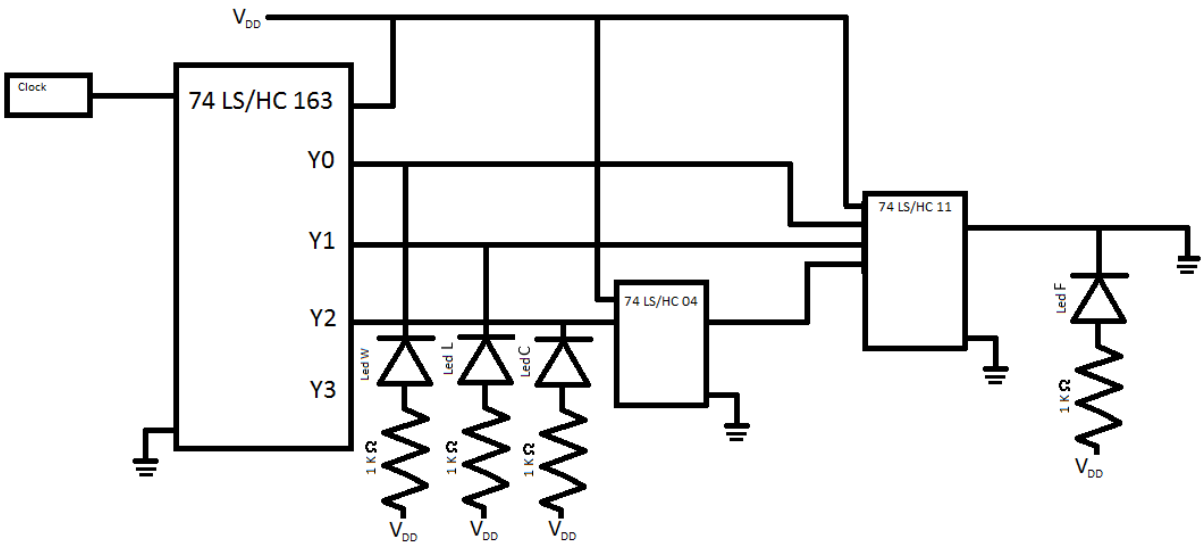
In this lab session we will create a logic equation and then implement it on a breadboard. We will feed the inputs of this circuit from a 74HC163 4-bit counter. This counter has 4 outputs based on its clock. For gates we will use other circuit components from 74 LS/HC family this are the gates used in early electronics in 70s. Finally we will connect the outputs to led lights. Doing this experiment will help us understand the inner workings of a digital circuit such as our BAYSY 3 better and give us an understanding to how people created circuits in 70s.

Design Specification Plan:

In my scenario I will be looking if a plant has right conditions to grow in a simplistic way. It needs water, light and it must not be cold. I will use "W" for the input signal of water, "L" for the input signal of the light, "C" for the input signal of the cold and "F" for the output signal. So my logic equation is $WL\bar{C}$ = F .This is great because to realize this I only need a 3 input AND gate and an inverter.

Proposed Design Methodology:

Like I said before I will be using a 74HC163 4-bit counter. This counter has 4 outputs based on its internal clock. This outputs are named Y0, Y1, Y2 and Y3. I will take Y0 for W, Y1 for L and Y2 for C. I will not be using the fourth output Y3. I will connect 1 led to each of the 3 inputs first to see when they are on clearly. Then I will connect C the 74 LS/HC 04 which is a hex inverter. A Hex inverter is just 6 inverters bundled together. I will be only using one of them. Then I will connect the now inverted C signal and the other two signals to the 74 LS/HC 11 which is a triple 3-input AND gate. Again I will be only using one of them. Then I will have my output signal F coming out of the AND gate. To finish the circuit I will connect 1 final led F then connect F to the ground. Then I will connect 74 LS/HC 11 and 74 LS/HC 04 to VDD and the ground because they need to be connected to them to function because inside they are PMOS and NMOS transistor gates.



This is a representation of the circuit I will build. Some parts have more complex connections than what I showed.

Y0	Y1	Y2	W	L	C	$\bar{C}$	F	Led_W	LED_L	Led_C	Led_F
0	0	0	0	0	0	1	0	1	1	1	1
1	0	0	1	0	0	1	0	0	1	1	1
0	1	0	0	1	0	1	0	1	0	1	1
1	1	0	1	1	0	1	1	0	0	1	0
0	0	1	0	0	1	0	0	1	1	0	1
1	0	1	1	0	1	0	0	0	1	0	1
0	1	1	0	1	1	0	0	1	0	0	1
1	1	1	1	1	1	0	0	0	0	0	1

This is the expected truth table.

As expected it is correct for $WL\bar{C}$ = F

But the Led lights light when the current on the wires they are attached to are low.

Y2 \ Y1Y0	00	01	11	10
0	0	0	1	0
1	0	0	0	0

This is the K map of the logic equation for F nothing ground breaking could be understud form it because its SOP is just $WL\bar{C}$ = F