System Description

Project: PF517-105
Customer: Özyegin University

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Creation - Modification			
	Author		Changes Log Book
	Name	Date	Modification subject
1	Andy Yen	2017/04/19	Initial Release
2			
3			
4			
5			

Contents

OVERVIEW

PROJECT: PF517-105

CUSTOMER: Özyegin University

SYSTEM S/N: PF517105S01

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Section B	**Mapping I/O blocks to signal conditioning**

SECTION A – SYSTEM SUMMARY

OP4200 IO SYSTEM

SIMULATOR GENERAL OVERVIEW

The OP4200 is part of the OPAL-RT line of simulation systems. It contains a SoC (system on chip) integrating an ARM CPU and a Kintex™-7 FPGA, signal conditioning for up to 128 I/O lines and 2 high-speed fiber-optic SFP ports. The design provides four slots for signal conditioning cassettes. The design makes it easy to use with standard connectors (DB37, DB9).

The target computer delivered includes the features listed in Table 1.

Table 1: List of features

Items	Quantity	Description
Operating System	1	Petalinux (ARMv7-based) version 4.0.0-xilinx
Chassis Type	1	OP4200
CPU	1	666 MHz
Total Core #	2	
Memory		1024MB DDR3L SDRAM
Motherboard		SoC (system on chip) integrating an ARM CPU and a Kintex™-7 FPGA
IP Addresses		192.168.10.101 (eth 0 – see Figure 1 for identification)
DC Input		24 VDC

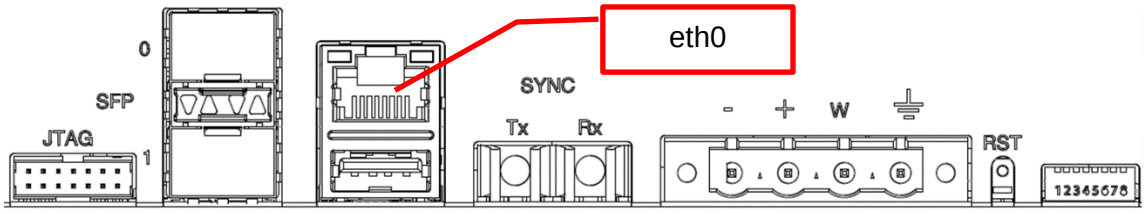


Figure 1: Computer connectors on OP4200

For more information on the OP4200 simulator, please consult the OP4200 RCP/HIL SYSTEM USER MANUAL which is provided on the delivery CD.

The credentials to log on to the real-time simulator are

Username: ***root***
Password: ***oprt935$***

SIGNAL CONDITIONING MODULE CONFIGURATION

The OP4200 is an entry-level simulator that can accept up to 4 signal conditioning cassettes, which provides greater signal conditioning flexibility. (see Figure 2).

There are 4 cassettes slots, labeled 1 to 4, slots in the OP4200. Digital cassettes have two DB37 connectors (one for channels 00-15 and one for channels 16-31), and analog cassettes have one DB37 connector (for channels 00-15).

Similarly to other OPAL-RT products, the I/O location is identified by a cassette number.

Table 2 lists the conditioning modules provided in the delivered system

Table 2: Signal conditioning module location

Slot	Cassette	Module inside
1A	OP4240-1, 16 analog input	OP5340
2A	OP4230-1, 16 analog output	OP5330-3
3A	OP4250-1, 32 digital input	OP5353
4A	OP4260-1, 32 digital output	OP5360-2

SYSTEM OVERVIEW

The following image is a diagram showing the layout of the delivered system. It is a top view and is meant to show the component placement and interconnection.

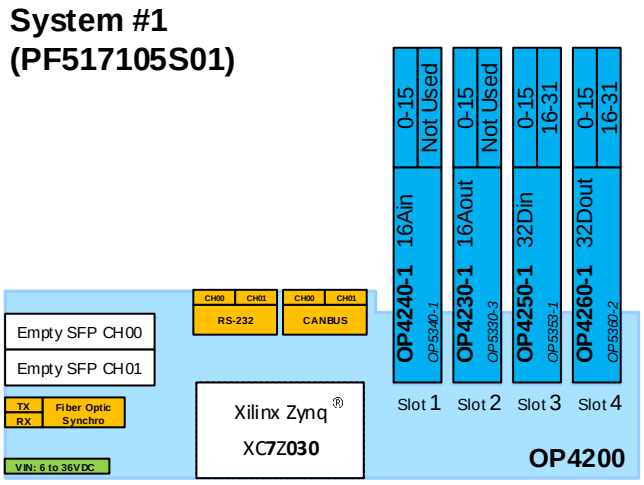


Figure 2: Block diagram of the OP4200 simulator

I/O BITSTREAM NAME AND CONFIGURATION

The bitstream (configuration data) loaded into the FPGA and its IO content are listed in Table 3.

Table 3: bitstream name and IO configuration

I/O Bitstream	IO Configuration
Bitstream Name: `MEZX5-AX-0001-3_1_2_360-eHSgen3_with_IOs-21-17.bin`	• 16 Static Digital Inputs and Outputs • 16 Pulse-Width Modulated (PWM) Digital Inputs and Outputs • 16 Analog Inputs and Outputs

Bitstream configuration can be checked from RT-LAB, via the OP4200_fpgaUtility command. The following lines are displayed:

```
# OP4200_fpgaUtility -b

Opal-RT Board: AXI board detection in progress...
        FPGA board ID:          ZX
        FPGA board minor ID:    5
        Bitstream revision ID:  23
        Bitstream minor ID:     33
        Carrier revision ID:    3

Opal-RT Board: AXI communication initialized
 Slot | Side |       Category        |         Card          |   More Information    |
  1   |   A  |          AIN          |        OP5340         |          --           |
  2   |   A  |         AOUT          |       OP5330-3        |          --           |
  3   |   A  |          DIN          |        OP5353         |          --           |
  4   |   A  |         DOUT          |       OP5360-2        |          --           |
```

.

SECTION B – MAPPING I/O BLOCKS TO SIGNAL CONDITIONING

The following section shows the relation between the I/O configuration in the RT-LAB workspace and the signal conditioning modules available, also named cassettes, on the OP4200 simulator.

The illustration below shows the arrangement of the 4 conditioning cassettes assigned specific slots, labeled 1 to 4, in the OP4200.

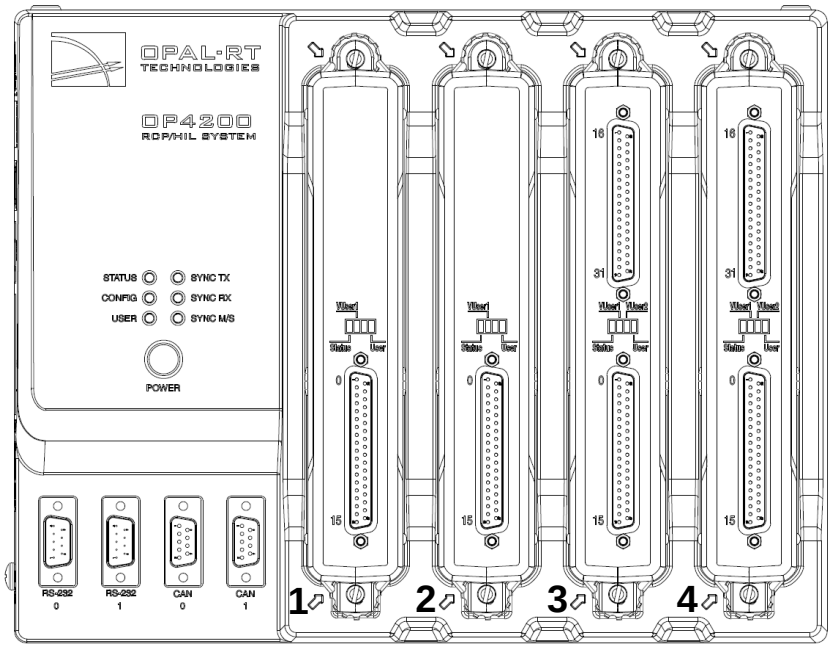


Figure 3: OP4200 connector panel

Digital cassettes have two DB37 connectors (one for channels 00-15 and one for channels 16-31), and analog cassettes have one DB37 connector (for channels 00-15). These connectors respect OPAL-RT's standard DB37 pinout, as shown in the table below.
Note that Vuser is available on Digital Outputs only.

Ch. 00-15				Ch. 16-31			
DB37	**Module pin assignment**	**DB37**	**Module pin Assignment**	**DB37**	**Module pin Assignment**	**DB37**	**Module pin assignment**
1	+CH00	20	-CH00	1	+CH16	20	-CH16
2	+CH01	21	-CH01	2	+CH17	21	-CH17
3	+CH02	22	-CH02	3	+CH18	22	-CH18
4	+CH03	23	-CH03	4	+CH19	23	-CH19
5	+CH04	24	-CH04	5	+CH20	24	-CH20
6	+CH05	25	-CH05	6	+CH21	25	-CH21
7	+CH06	26	-CH06	7	+CH22	26	-CH22
8	+CH07	27	-CH07	8	+CH23	27	-CH23
9	+CH08	28	-CH08	9	+CH24	28	-CH24
10	+CH09	29	-CH09	10	+CH25	29	-CH25
11	+CH10	30	-CH10	11	+CH26	30	-CH26
12	+CH11	31	-CH11	12	+CH27	31	-CH27
13	+CH12	32	-CH12	13	+CH28	32	-CH28
14	+CH13	33	-CH13	14	+CH29	33	-CH29
15	+CH14	34	-CH14	15	+CH30	34	-CH30
16	+CH15	35	-CH15	16	+CH31	35	-CH31
17		36		17		36	
18	Vuser 1 A*	37	Vrtn 1 A*	18	Vuser 2 A*	37	Vrtn 2 A*
19				19			

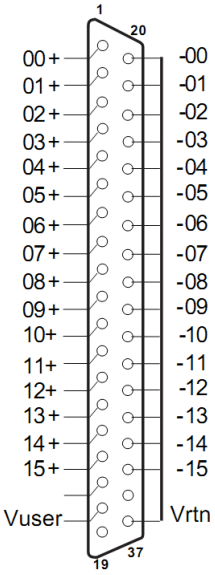


Figure 4: General pin assignments

The following I/O configuration mapping is applicable for the hardware test model which is used to validate the hardware functionality and which is provided on the delivery CD.

For details on the generic pin assignments of the OP4200, please consult the OP4200 RCP/HIL SYSTEM USER MANUAL which is provided on the delivery CD. The following is intended to show the specific pin assignment on standard DB37 and DB9 connectors for the system and bitstream delivered.

OPAL-RT Board Interface Configuration

OPAL-RT Board interface configuration shows the OP4200 hardware configuration associated with the bitstream of the project. It displays the expected conditioning cassettes and their corresponding settings.

By default, all available IO are enabled to be used by the model.

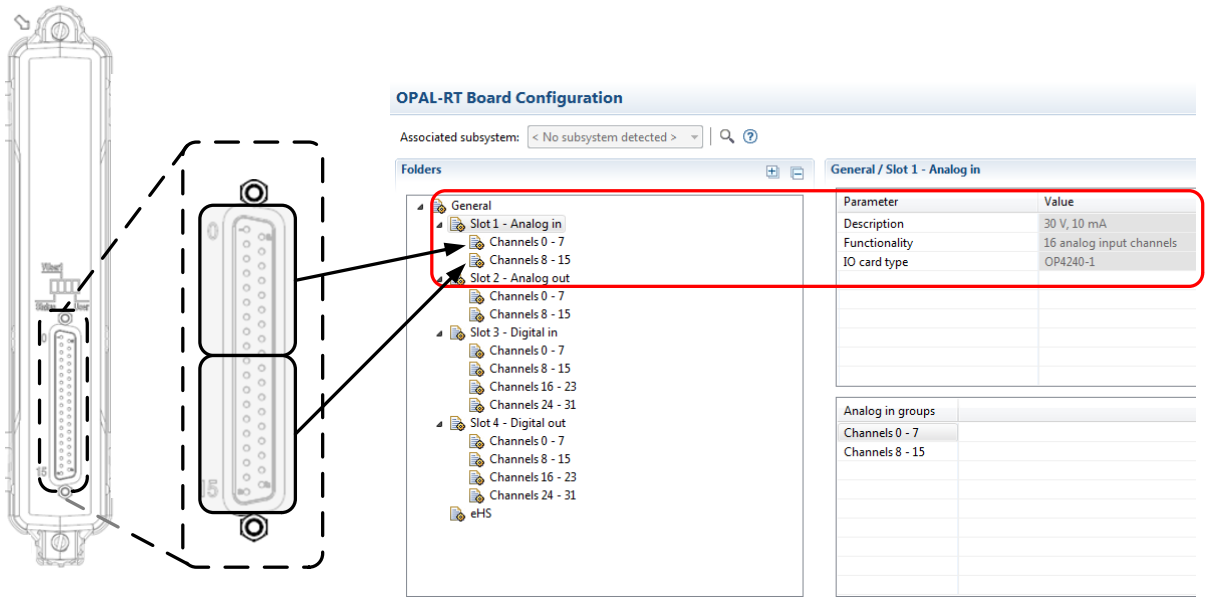


Figure 5: Example of OPAL-RT Board interface configuration vs OP4200 Connectors

PROJECT & MODEL CONFIGURATION

Once the configuration of the OPAL-RT Board interface is set, the enabled inputs/outputs are shown in the I/O section of the Project configuration.

The I/Os / OPAL-RT Board section of the configuration panel of the RT-LAB project lists the hardware inputs/outputs available to be mapped to the Simulink models inputs/outputs labels.

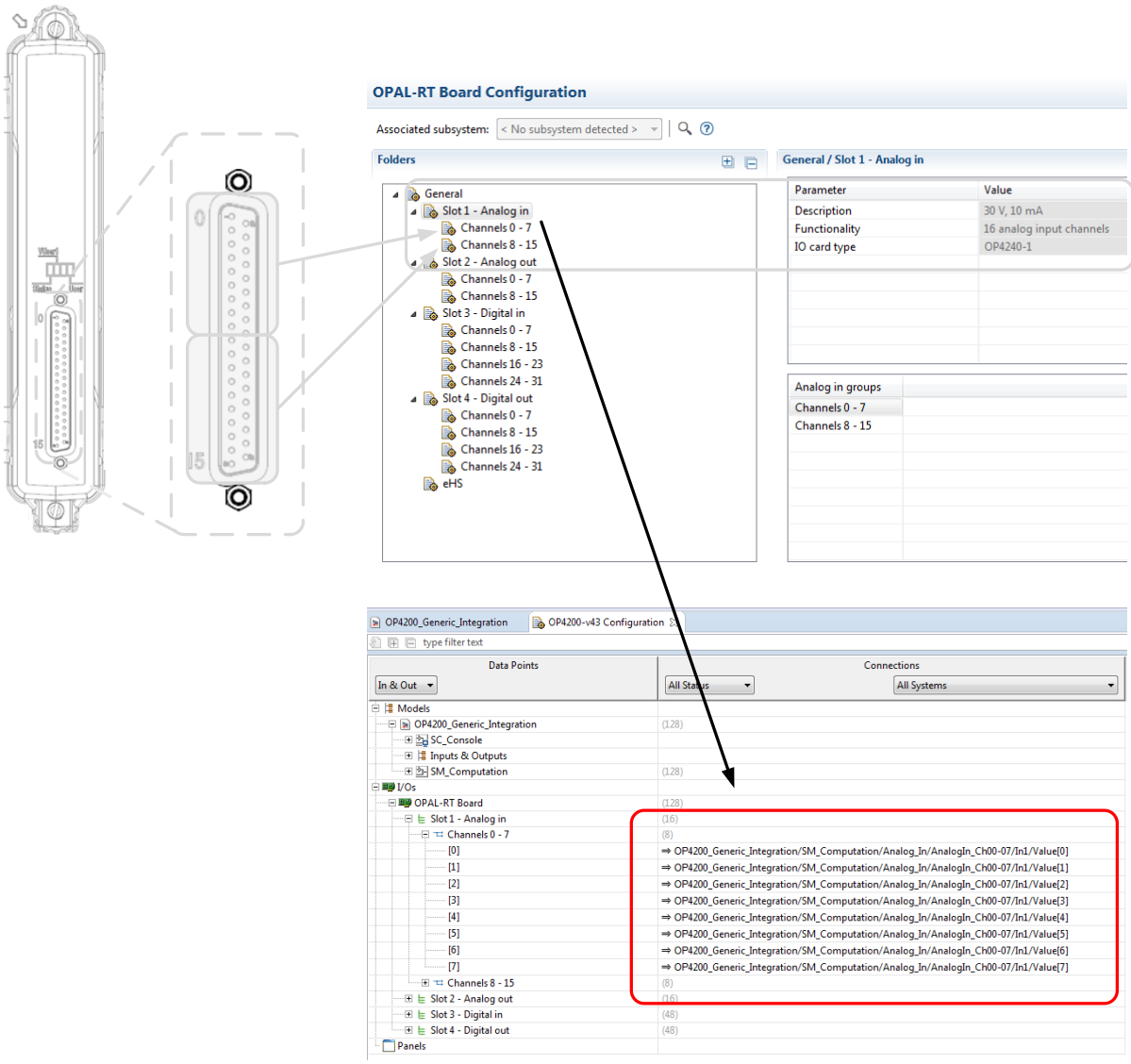
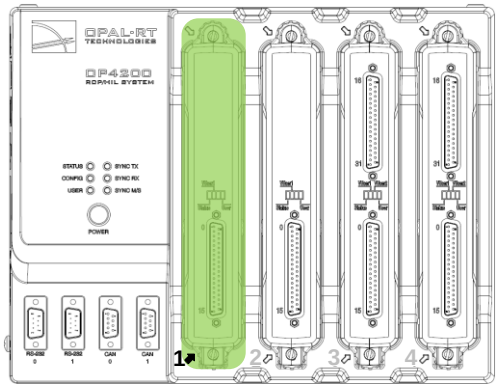


Figure 6: Example of OPAL-RT Board I/O, mapped to OpInput blocks found in the model

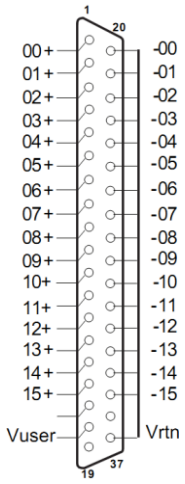
I/O CHANNELS ASSIGNMENT

The following sections will show the mapped signals of the model delivered with your system.

SLOT 1 (CH 00-15): ANALOG INPUTS

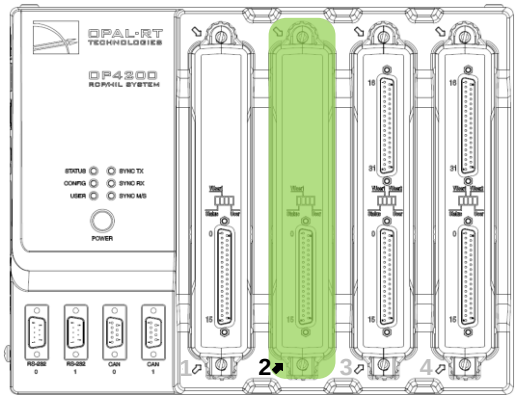


Connector 1A Ch. 00-15			
DB37	Module pin assignment	DB37	Module pin Assignment
1	+AIN00	20	-AIN00
2	+AIN01	21	-AIN01
3	+AIN02	22	-AIN02
4	+AIN03	23	-AIN03
5	+AIN04	24	-AIN04
6	+AIN05	25	-AIN05
7	+AIN06	26	-AIN06
8	+AIN07	27	-AIN07
9	+AIN08	28	-AIN08
10	+AIN09	29	-AIN09
11	+AIN10	30	-AIN10
12	+AIN11	31	-AIN11
13	+AIN12	32	-AIN12
14	+AIN13	33	-AIN13
15	+AIN14	34	-AIN14
16	+AIN15	35	-AIN15
17		36	DGND
18		37	
19			

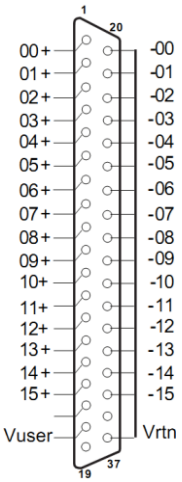


I/Os	
OPAL-RT Board	(128)
Slot 1 - Analog in	(16)
Channels 0 - 7	(8)
[0]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch00-07/In1/Value[0]
[1]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch00-07/In1/Value[1]
[2]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch00-07/In1/Value[2]
[3]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch00-07/In1/Value[3]
[4]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch00-07/In1/Value[4]
[5]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch00-07/In1/Value[5]
[6]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch00-07/In1/Value[6]
[7]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch00-07/In1/Value[7]
Channels 8 - 15	(8)
[0]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch08-15/In1/Value[0]
[1]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch08-15/In1/Value[1]
[2]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch08-15/In1/Value[2]
[3]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch08-15/In1/Value[3]
[4]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch08-15/In1/Value[4]
[5]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch08-15/In1/Value[5]
[6]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch08-15/In1/Value[6]
[7]	⇒ OP4200_Generic_Integration/SM_Computation/Analog_In/AnalogIn_Ch08-15/In1/Value[7]

SLOT 2 (CH 00-15): ANALOG OUTPUTS

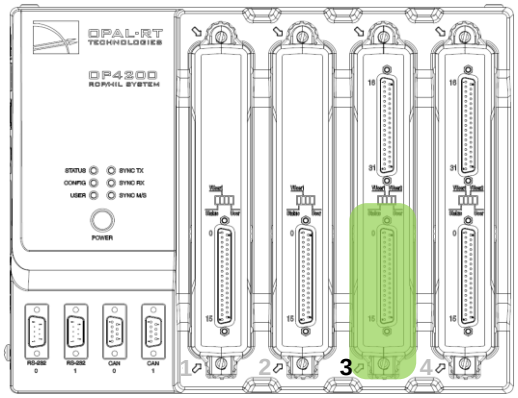


Connector 1A Ch. 00-15			
DB37	**Module pin assignment**	**DB37**	**Module pin Assignment**
1	+AOUT00	20	-AOUT00
2	+AOUT01	21	-AOUT01
3	+AOUT02	22	-AOUT02
4	+AOUT03	23	-AOUT03
5	+AOUT04	24	-AOUT04
6	+AOUT05	25	-AOUT05
7	+AOUT06	26	-AOUT06
8	+AOUT07	27	-AOUT07
9	+AOUT08	28	-AOUT08
10	+AOUT09	29	-AOUT09
11	+AOUT10	30	-AOUT10
12	+AOUT11	31	-AOUT11
13	+AOUT12	32	-AOUT12
14	+AOUT13	33	-AOUT13
15	+AOUT14	34	-AOUT14
16	+AOUT15	35	-AOUT15
17		36	DGND
18		37	
19			

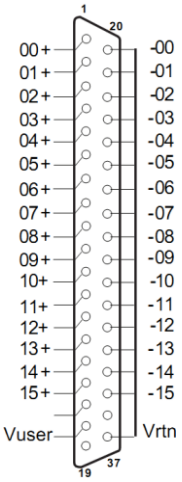


I/Os	
OPAL-RT Board	(128)
Slot 1 - Analog in	(16)
Slot 2 - Analog out	(16)
Channels 8 - 15	(8)
Channel 8	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch08-15/OpOutput/port1[0]
Channel 9	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch08-15/OpOutput/port1[1]
Channel 10	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch08-15/OpOutput/port1[2]
Channel 11	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch08-15/OpOutput/port1[3]
Channel 12	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch08-15/OpOutput/port1[4]
Channel 13	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch08-15/OpOutput/port1[5]
Channel 14	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch08-15/OpOutput/port1[6]
Channel 15	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch08-15/OpOutput/port1[7]
Channels 0 - 7	(8)
Channel 0	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch00-07/OpOutput/port1[0]
Channel 1	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch00-07/OpOutput/port1[1]
Channel 2	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch00-07/OpOutput/port1[2]
Channel 3	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch00-07/OpOutput/port1[3]
Channel 4	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch00-07/OpOutput/port1[4]
Channel 5	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch00-07/OpOutput/port1[5]
Channel 6	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch00-07/OpOutput/port1[6]
Channel 7	⇐ OP4200_Generic_Integration/SM_Computation/Analog_Out/AnalogOut_Ch00-07/OpOutput/port1[7]

SLOT 3 (CH 00-15): DIGITAL INPUTS

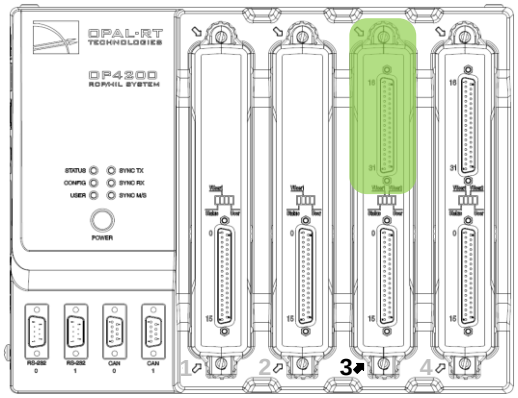


Connector 1A Ch. 00-15			
DB37	**Module pin assignment**	**DB37**	**Module pin Assignment**
1	+DIN00	20	-DIN00
2	+DIN01	21	-DIN01
3	+DIN02	22	-DIN02
4	+DIN03	23	-DIN03
5	+DIN04	24	-DIN04
6	+DIN05	25	-DIN05
7	+DIN06	26	-DIN06
8	+DIN07	27	-DIN07
9	+DIN08	28	-DIN08
10	+DIN09	29	-DIN09
11	+DIN10	30	-DIN10
12	+DIN11	31	-DIN11
13	+DIN12	32	-DIN12
14	+DIN13	33	-DIN13
15	+DIN14	34	-DIN14
16	+DIN15	35	-DIN15
17		36	DGND
18		37	
19			

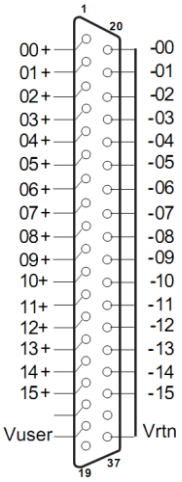


Slot 3 - Digital in	(48)
Channels 16 - 23 (Pulse width modulated)	(16)
Channels 24 - 31 (Pulse width modulated)	(16)
Channels 0 - 7 (Static)	(8)
[0]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch00-07/In1/Value[0]
[1]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch00-07/In1/Value[1]
[2]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch00-07/In1/Value[2]
[3]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch00-07/In1/Value[3]
[4]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch00-07/In1/Value[4]
[5]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch00-07/In1/Value[5]
[6]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch00-07/In1/Value[6]
[7]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch00-07/In1/Value[7]
Channels 8 - 15 (Static)	(8)
[0]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch08-15/In1/Value[0]
[1]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch08-15/In1/Value[1]
[2]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch08-15/In1/Value[2]
[3]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch08-15/In1/Value[3]
[4]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch08-15/In1/Value[4]
[5]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch08-15/In1/Value[5]
[6]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch08-15/In1/Value[6]
[7]	⇒ OP4200_Generic_Integration/SM_Computation/Digital_In/DigitalIn_Ch08-15/In1/Value[7]

SLOT 3 (CH 16-31): DIGITAL INPUTS

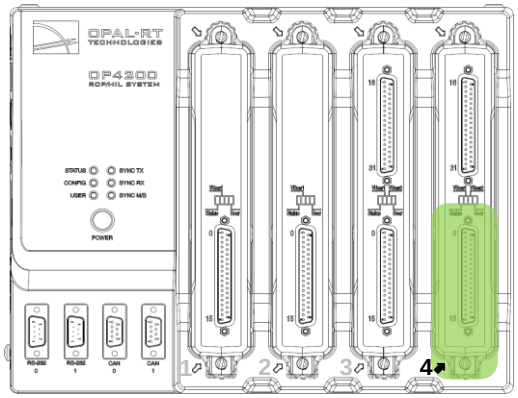


Connector 1A Ch. 16-31			
DB37	**Module pin Assignment**	**DB37**	**Module pin assignment**
1	+DIN16	20	-DIN16
2	+DIN17	21	-DIN17
3	+DIN18	22	-DIN18
4	+DIN19	23	-DIN19
5	+DIN20	24	-DIN20
6	+DIN21	25	-DIN21
7	+DIN22	26	-DIN22
8	+DIN23	27	-DIN23
9	+DIN24	28	-DIN24
10	+DIN25	29	-DIN25
11	+DIN26	30	-DIN26
12	+DIN27	31	-DIN27
13	+DIN28	32	-DIN28
14	+DIN29	33	-DIN29
15	+DIN30	34	-DIN30
16	+DIN31	35	-DIN31
17		36	
18		37	
19			

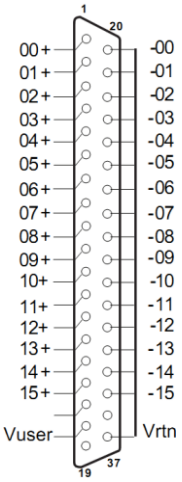


Slot 3 - Digital in	(48)
Channels 16 - 23 (Pulse width modulated)	(16)
Channel 16	(2)
Frequency	⇒ OP4200_Generic_Integration/SM_Computation/PWM_In/PWMIn_Ch00/In1/Value[0]
Duty cycle	⇒ OP4200_Generic_Integration/SM_Computation/PWM_In/PWMIn_Ch00/In1/Value[1]
Channel 17	(2)
Channel 18	(2)
Channel 19	(2)
Channel 20	(2)
Channel 21	(2)
Channel 22	(2)
Channel 23	(2)
Channels 24 - 31 (Pulse width modulated)	(16)
Channel 24	(2)
Channel 25	(2)
Channel 26	(2)
Channel 27	(2)
Channel 28	(2)
Channel 29	(2)
Channel 30	(2)
Channel 31	(2)

SLOT 4 (CH 00-15): DIGITAL OUTPUTS



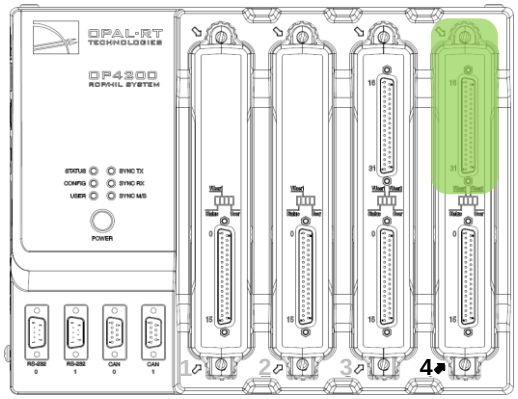
Connector 1A Ch. 00-15			
DB37	**Module pin assignment**	**DB37**	**Module pin Assignment**
1	+DOUT00	20	Vrtn 1
2	+DOUT01	21	Vrtn 1
3	+DOUT02	22	Vrtn 1
4	+DOUT03	23	Vrtn 1
5	+DOUT04	24	Vrtn 1
6	+DOUT05	25	Vrtn 1
7	+DOUT06	26	Vrtn 1
8	+DOUT07	27	Vrtn 1
9	+DOUT08	28	Vrtn 1
10	+DOUT09	29	Vrtn 1
11	+DOUT10	30	Vrtn 1
12	+DOUT11	31	Vrtn 1
13	+DOUT12	32	Vrtn 1
14	+DOUT13	33	Vrtn 1
15	+DOUT14	34	Vrtn 1
16	+DOUT15	35	Vrtn 1
17		36	
18	Vuser 1	37	Vrtn 1
19			



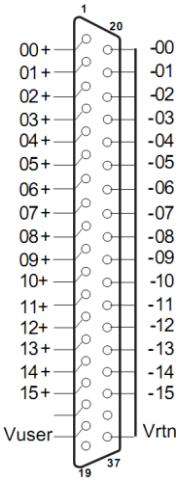
Digital Output channels require a Vuser reference voltage, which is provided through the DB37 connector pin 18 and referenced to Vrtn pin 37.

Slot 4 - Digital out	(48)
Channels 16 - 23 (Pulse width modulated)	(16)
Channels 24 - 31 (Pulse width modulated)	(16)
Channels 0 - 7 (Static)	(8)
[0]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch00-07/OpOutput/port1[0]
[1]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch00-07/OpOutput/port1[1]
[2]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch00-07/OpOutput/port1[2]
[3]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch00-07/OpOutput/port1[3]
[4]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch00-07/OpOutput/port1[4]
[5]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch00-07/OpOutput/port1[5]
[6]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch00-07/OpOutput/port1[6]
[7]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch00-07/OpOutput/port1[7]
Channels 8 - 15 (Static)	(8)
[0]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch08-15/OpOutput/port1[0]
[1]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch08-15/OpOutput/port1[1]
[2]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch08-15/OpOutput/port1[2]
[3]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch08-15/OpOutput/port1[3]
[4]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch08-15/OpOutput/port1[4]
[5]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch08-15/OpOutput/port1[5]
[6]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch08-15/OpOutput/port1[6]
[7]	⇐ OP4200_Generic_Integration/SM_Computation/Digital_Out/DigitalOut_Ch08-15/OpOutput/port1[7]

SLOT 4 (CH 16-31): DIGITAL OUTPUTS



Connector 1A Ch. 16-31			
DB37	**Module pin Assignment**	**DB37**	**Module pin assignment**
1	+DOUT16	20	Vrtn 2
2	+DOUT17	21	Vrtn 2
3	+DOUT18	22	Vrtn 2
4	+DOUT19	23	Vrtn 2
5	+DOUT20	24	Vrtn 2
6	+DOUT21	25	Vrtn 2
7	+DOUT22	26	Vrtn 2
8	+DOUT23	27	Vrtn 2
9	+DOUT24	28	Vrtn 2
10	+DOUT25	29	Vrtn 2
11	+DOUT26	30	Vrtn 2
12	+DOUT27	31	Vrtn 2
13	+DOUT28	32	Vrtn 2
14	+DOUT29	33	Vrtn 2
15	+DOUT30	34	Vrtn 2
16	+DOUT31	35	Vrtn 2
17		36	DGND
18	Vuser 2	37	Vrtn 2
19			



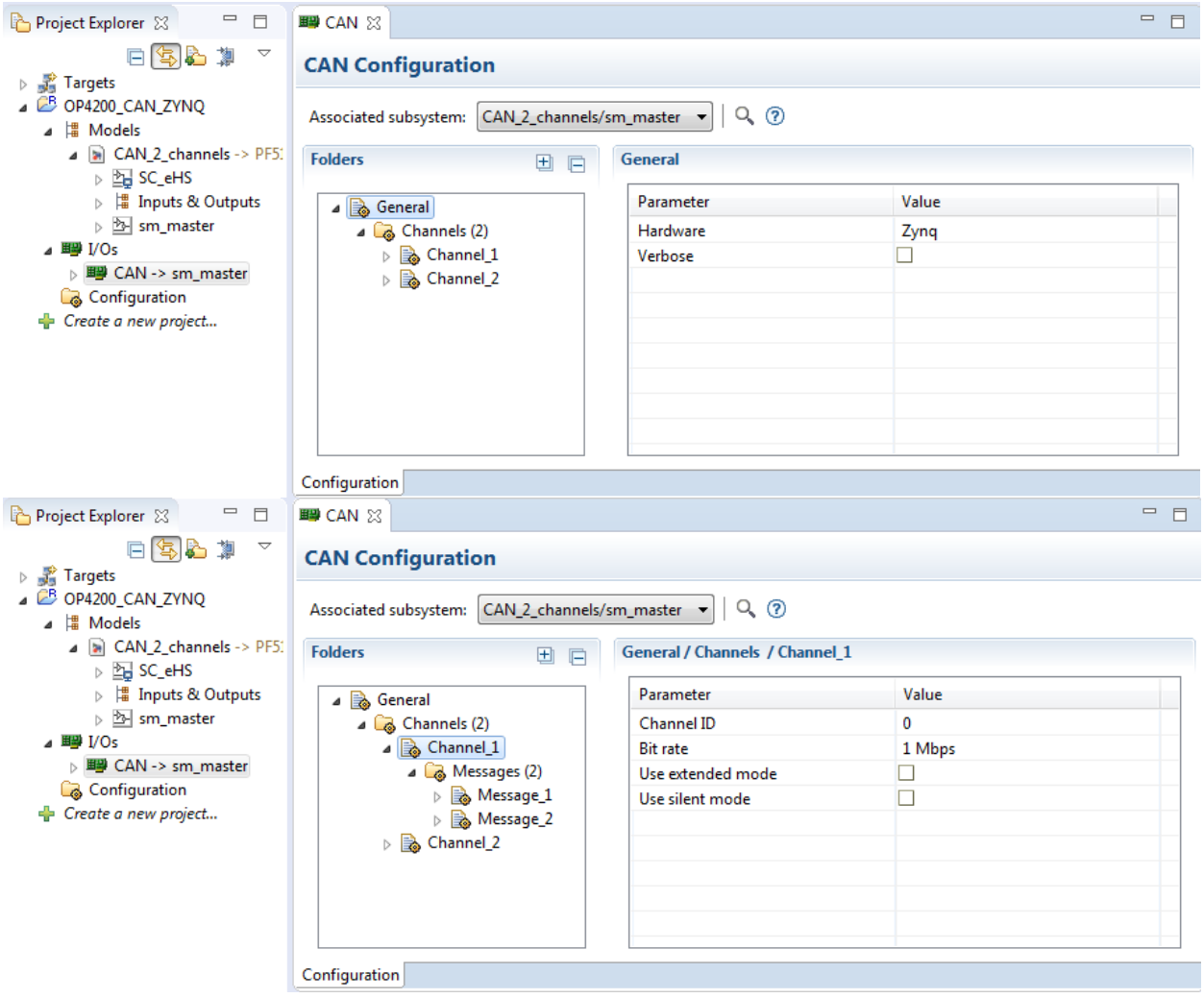
Digital Output channels require a Vuser reference voltage, which is provided through the DB37 connector pin 18 and referenced to Vrtn pin 37.

Slot 4 - Digital out	(48)
Channels 16 - 23 (Pulse width modulated)	(16)
Channel 16	(2)
Frequency	⇐ OP4200_Generic_Integration/SM_Computation/PWM_Out/PWMOut_Ch00/OpOutput/port1[0]
Duty cycle	⇐ OP4200_Generic_Integration/SM_Computation/PWM_Out/PWMOut_Ch00/OpOutput/port1[1]
Channel 17	(2)
Channel 18	(2)
Channel 19	(2)
Channel 20	(2)
Channel 21	(2)
Channel 22	(2)
Channel 23	(2)
Channels 24 - 31 (Pulse width modulated)	(16)
Channel 24	(2)
Channel 25	(2)
Channel 26	(2)
Channel 27	(2)
Channel 28	(2)
Channel 29	(2)
Channel 30	(2)
Channel 31	(2)

CAN INTERFACE CONFIGURATION

OPAL-RT Board interface configuration shows the CAN hardware configuration associated with the project. It lists the expected channels and their corresponding settings.

In the example model, four channels are enabled to be used by the model.



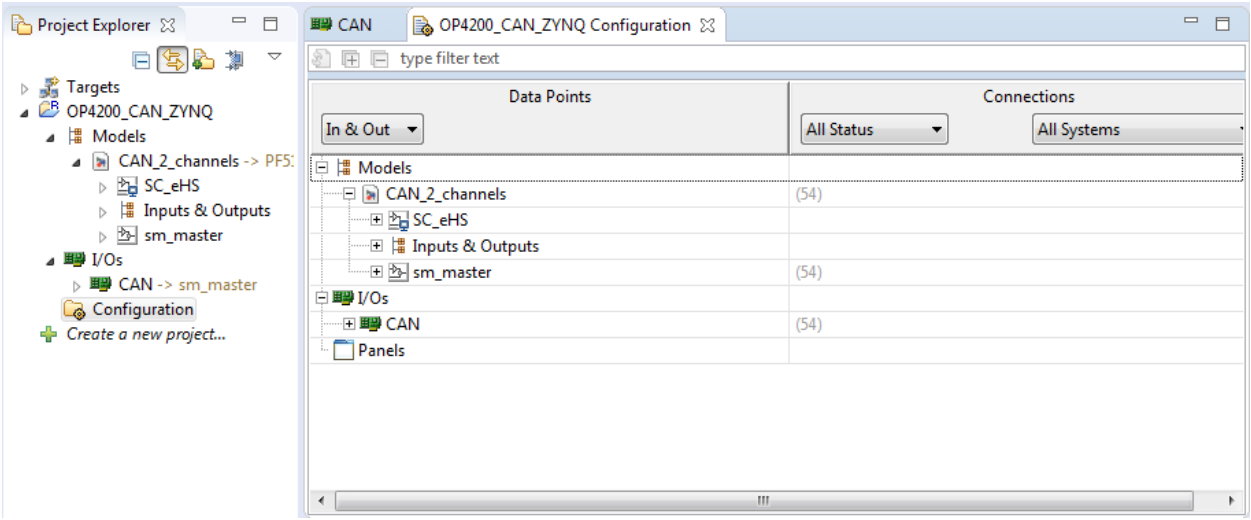


Figure 7: Example of OPAL-RT Board interface configuration

PROJECT & MODEL CONFIGURATION

Once the configuration of the OPAL-RT Board interface is set, the enabled inputs/outputs are shown in the I/O section of the Project configuration.

The I/Os / OPAL-RT Board section of the configuration panel of the RT-LAB project lists the hardware inputs/outputs available to be mapped to the Simulink models inputs/outputs labels.

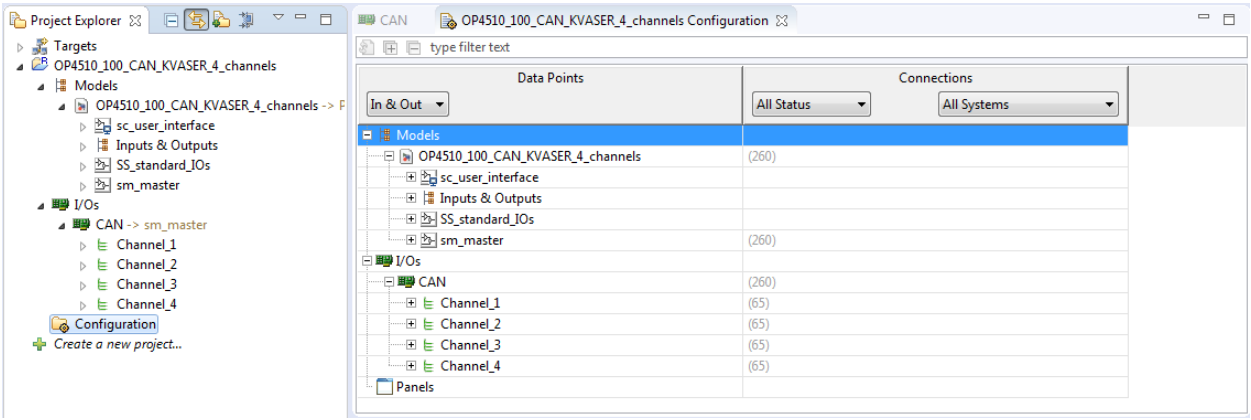


Figure 8: Example of OPAL-RT Board I/O, mapped to OpInput blocks found in the model

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Note: