**Lab Report for Lab Assignment 3**

In the ripple-carry 15-bit adder/subtractor, we first constructed a full adder to be instantiated in the design. After creating that building block, we used it 15 times and implemented an overflow detector V. The overall design was similar to the one explained in class. The design successfully added and subtracted two binary numbers even when there is an overflow. Below are screenshots of schema for a full adder and ripple-carry 15-bit adder/subtractor, in addition the operations.

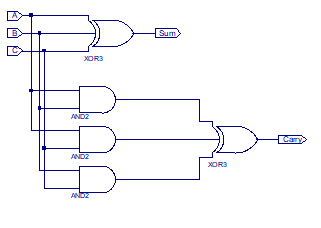


Figure 1 FullAdder

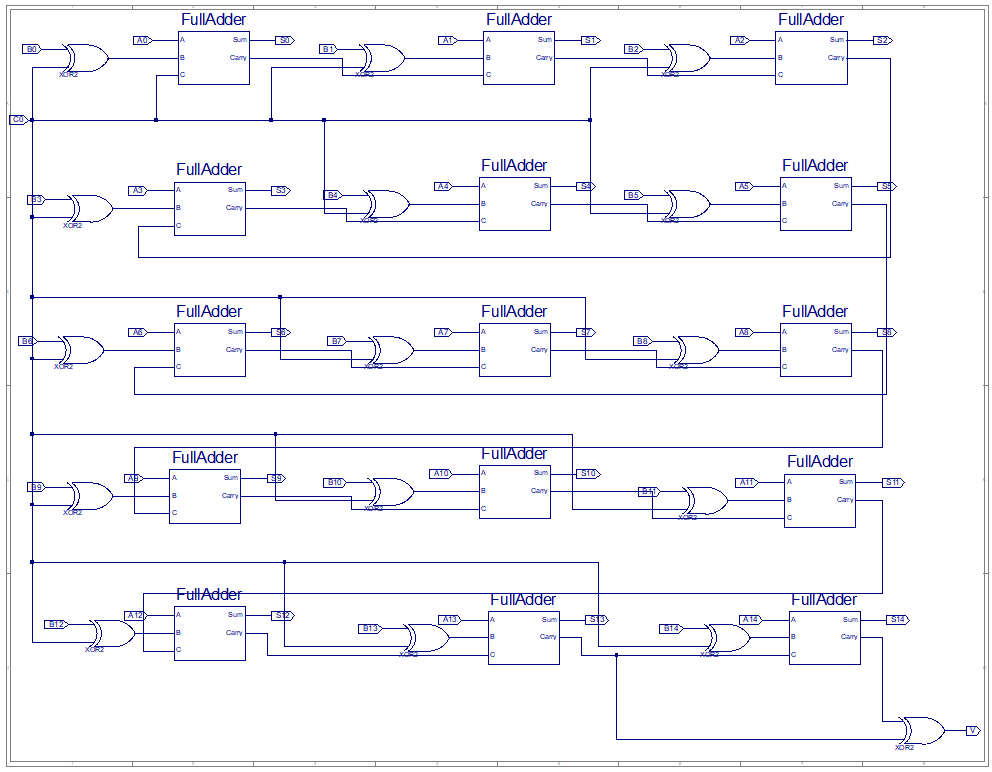
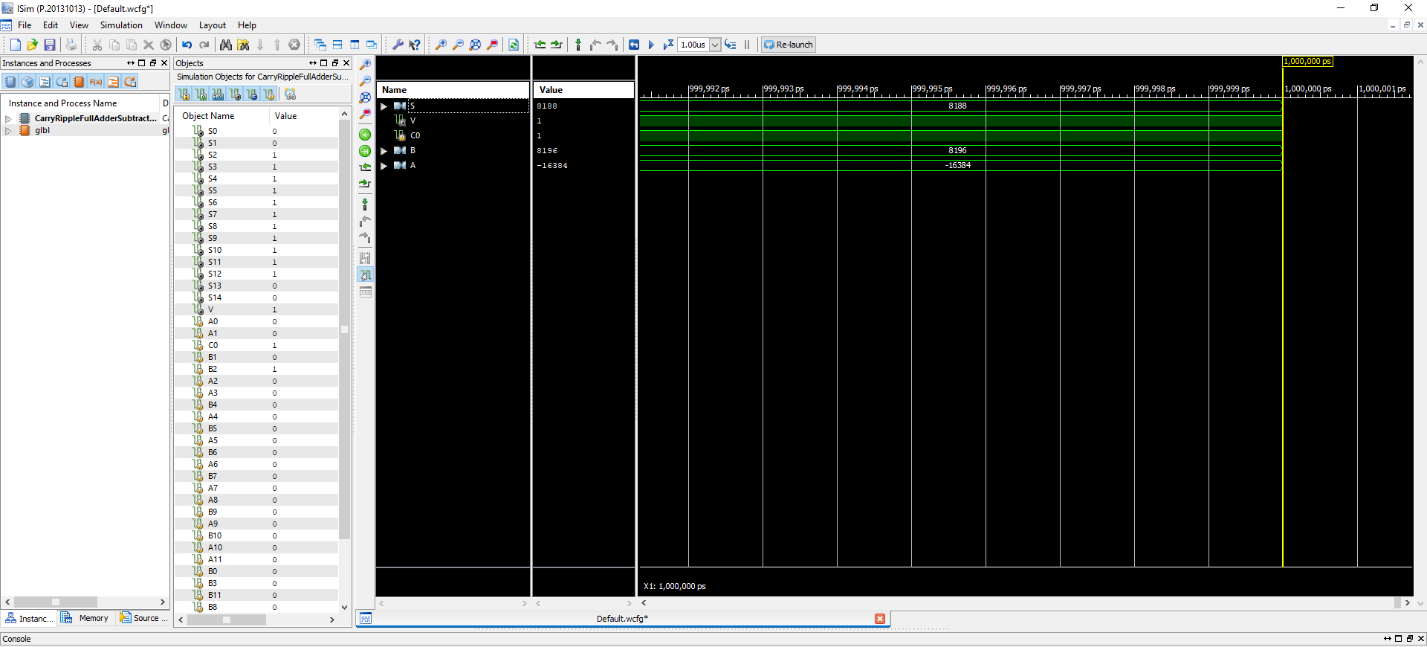
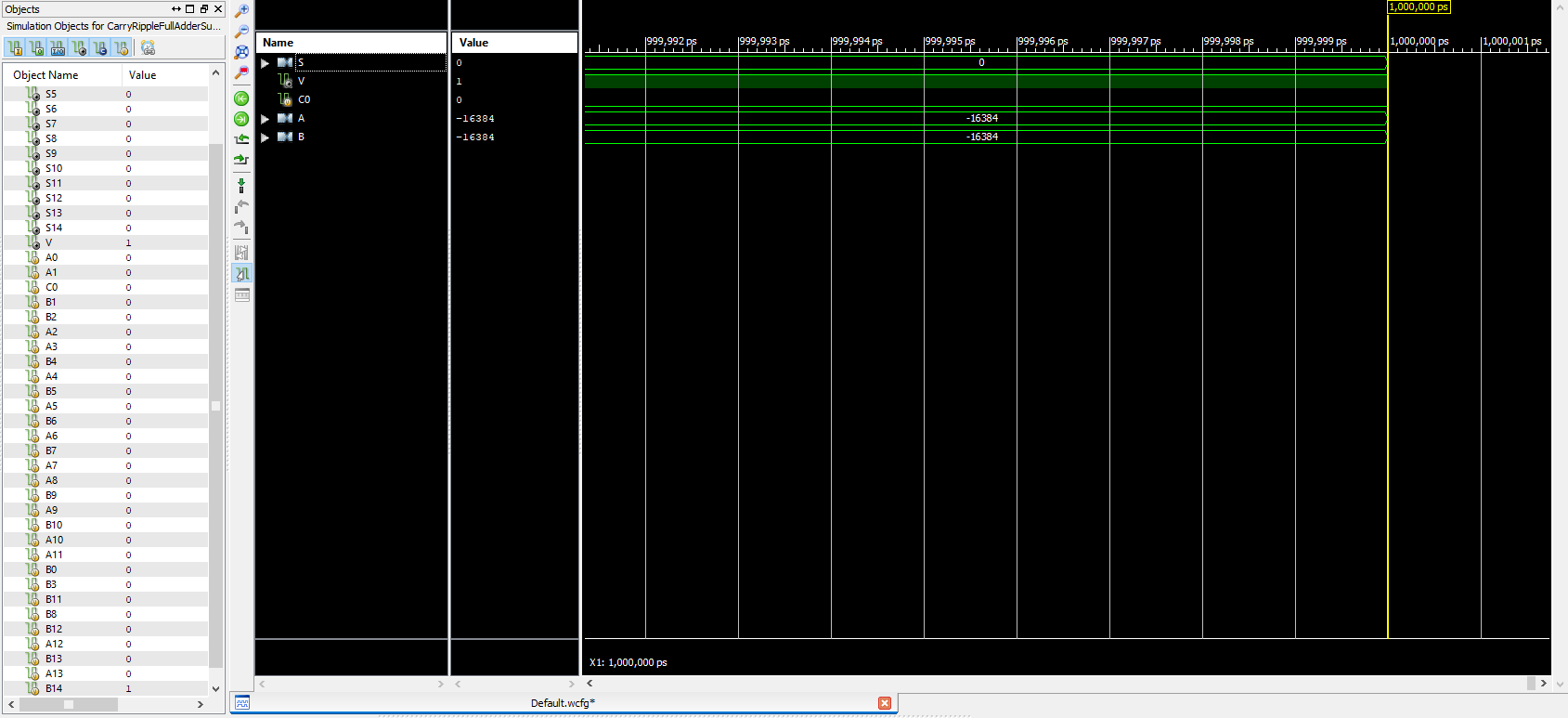
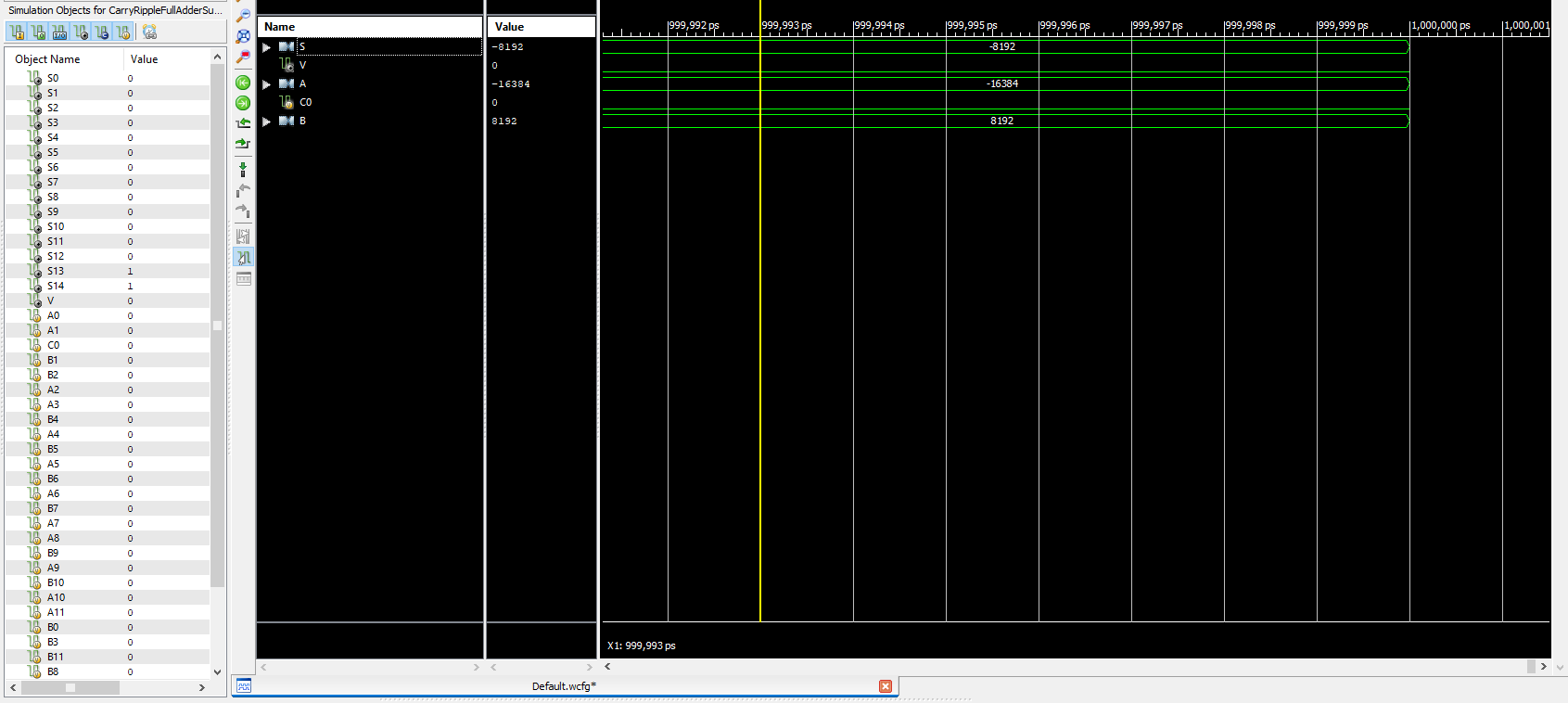
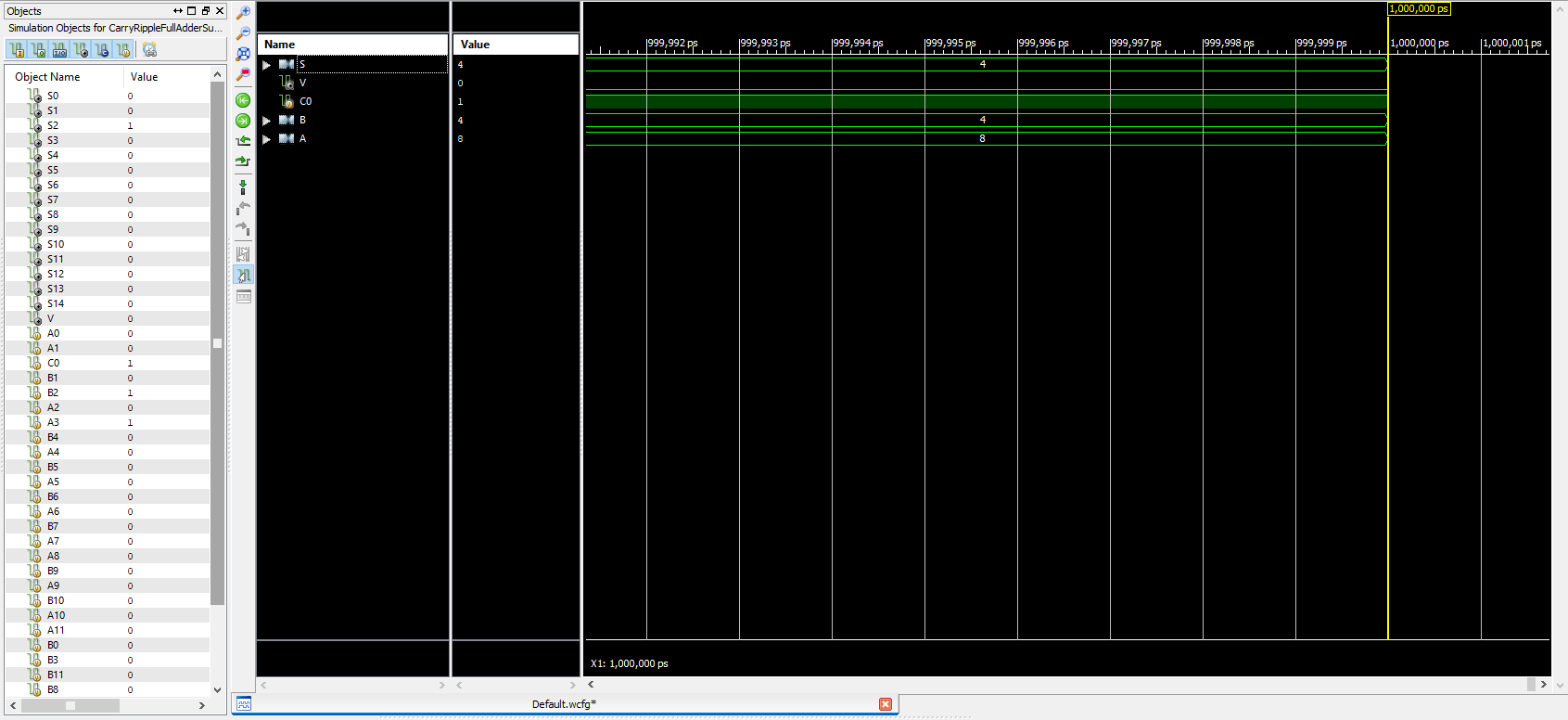


Figure 2 ripple-carry 15-bit adder/subtractor

In the hybrid adder/subtractor, we used five 3-bit carry-lookahead adders in order to make a complete 15-bit adder and GP generators. Again, we implemented an overflow detector and successfully made addition and subtraction operations. Below are screenshots of schema for a 3-bit carry-lookahead adder, a GP generator and 15-bit hybrid carry-lookahead adder/subtractor, in addition the operations.

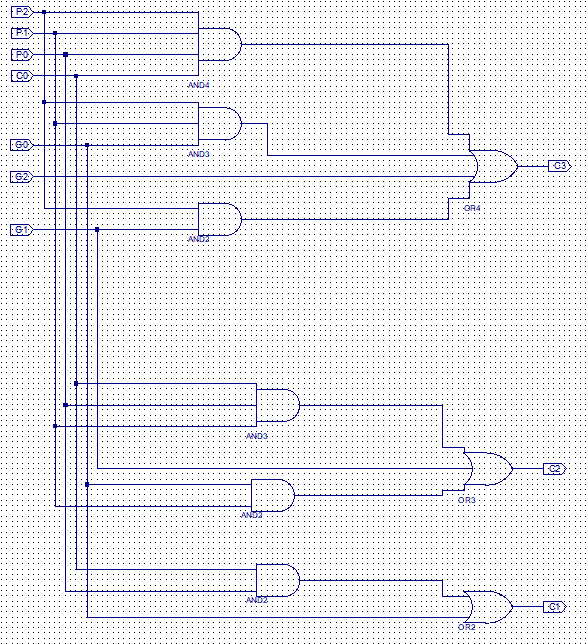


Figure 3 3-bit carry-lookahead adder

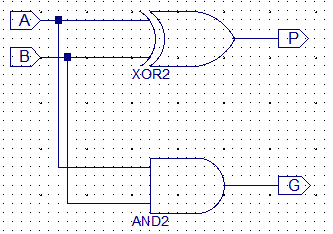


Figure 4 GP Generator

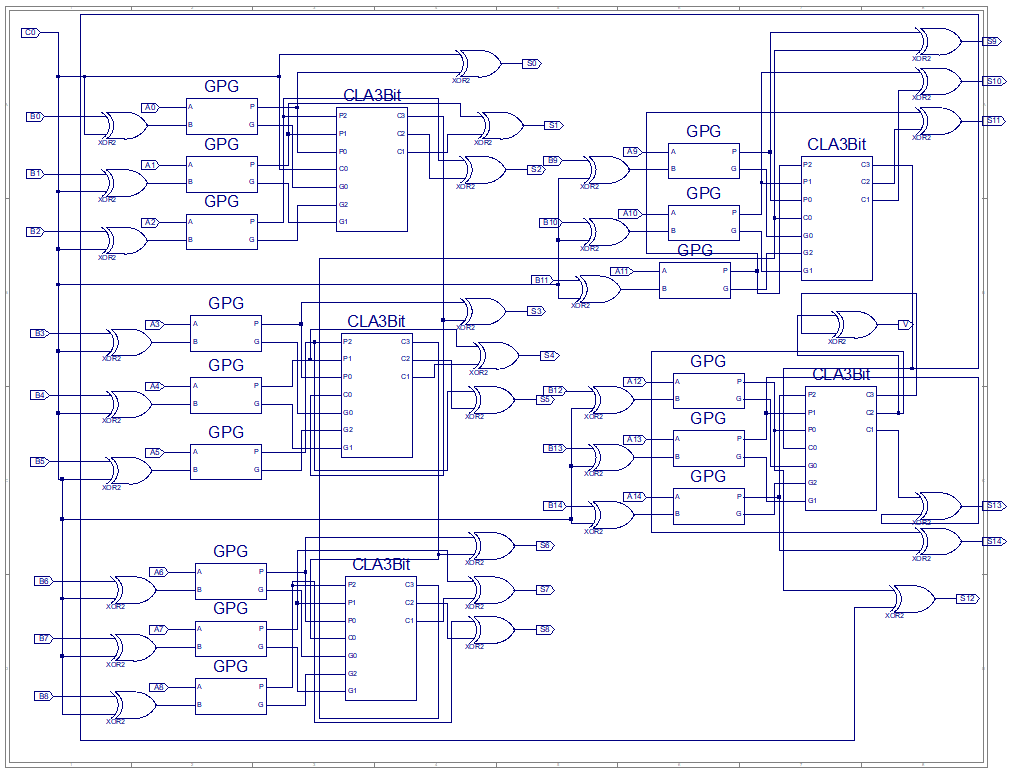
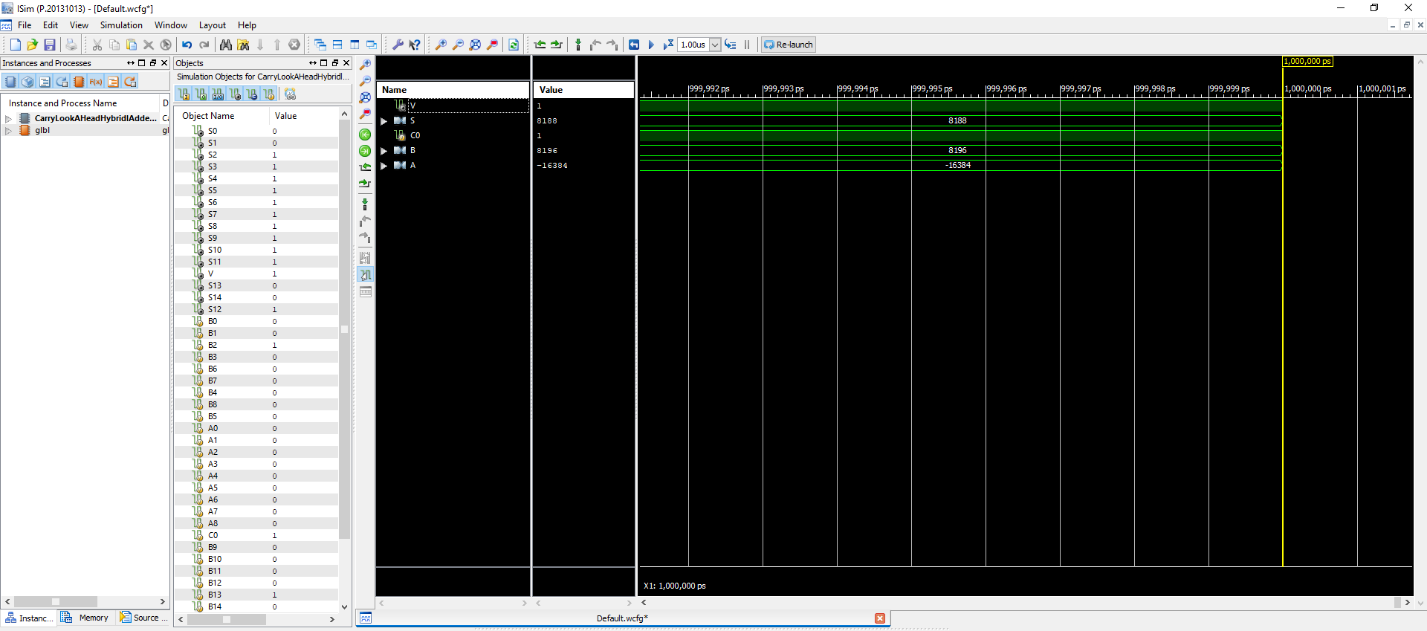
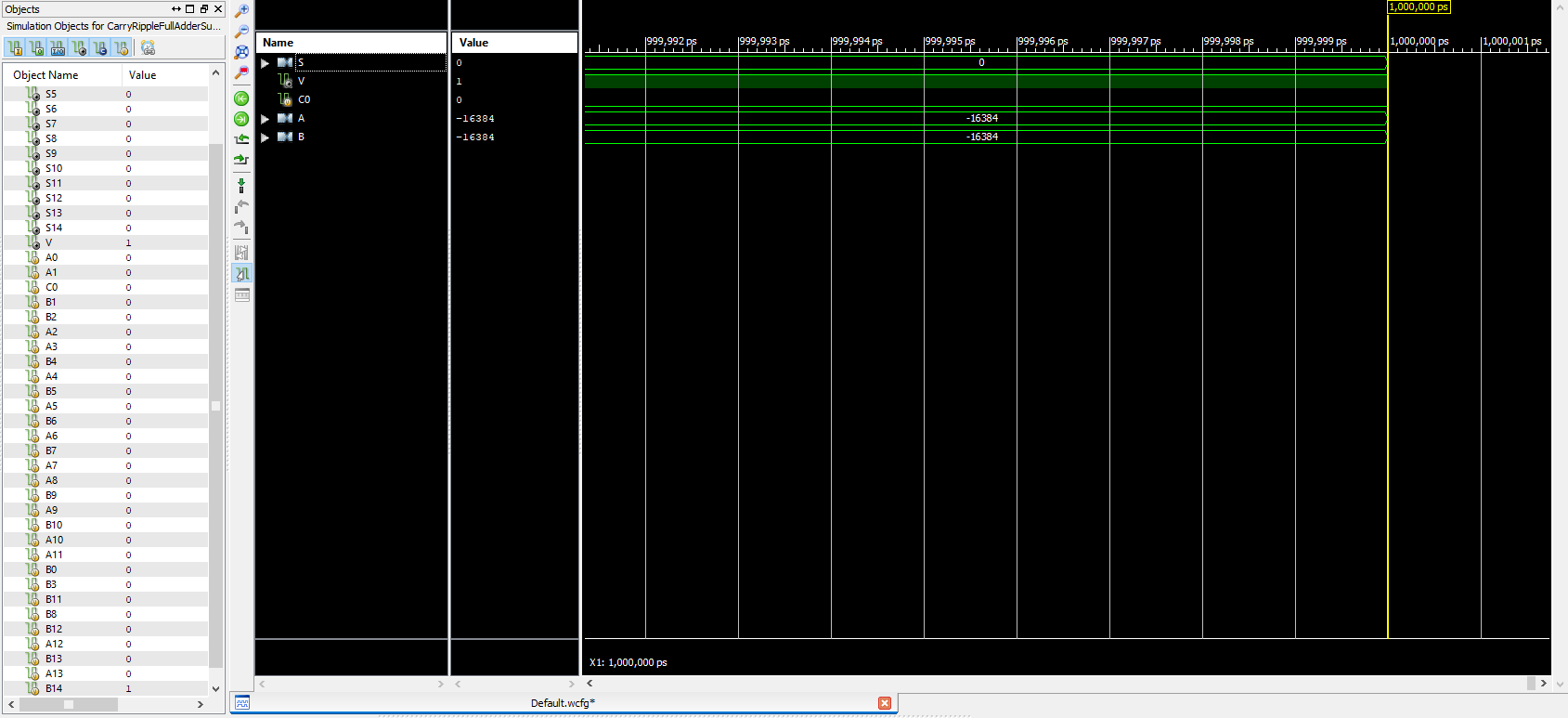
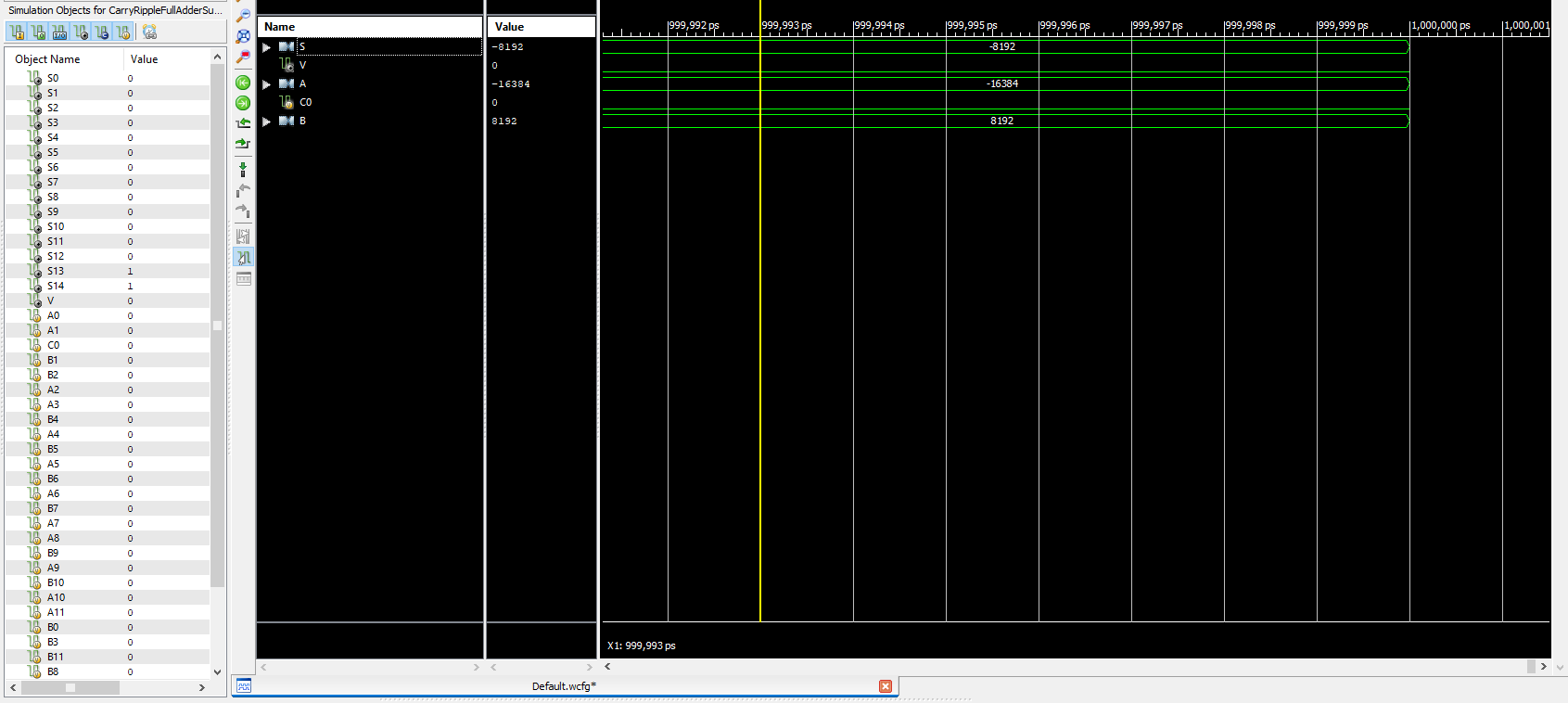
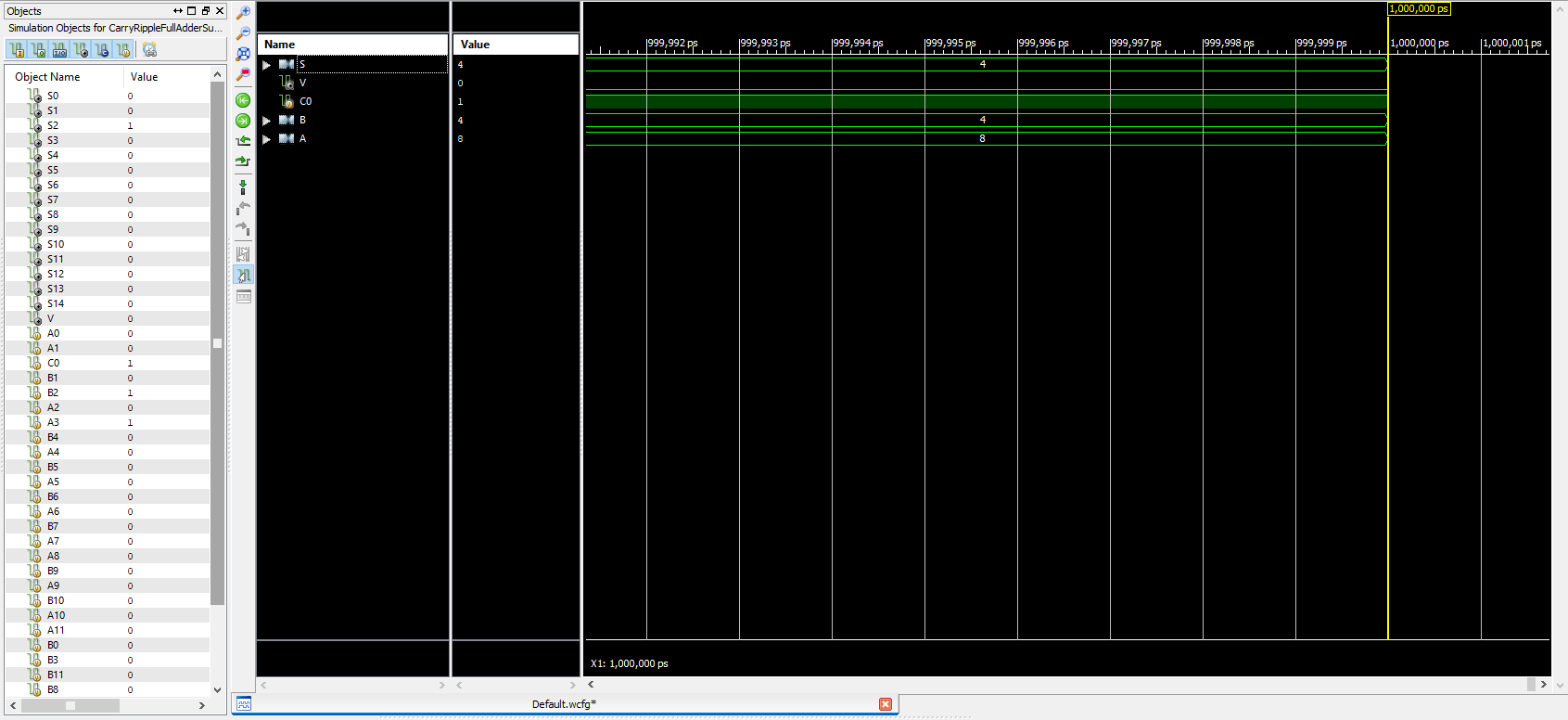


Figure 5 15-bit carry-lookahead adder/subtractor



The delay times and LUT counts are provided below. Although we expected to see less delay time in the hybrid adder, it was higher than the ripple-carry. But as the hybrid design is more complex, the LUT count is higher than the ripple-carry.

Ripple-Carry

Number of 4 input LUTs: 37

Delay: 26.846ns

Hybrid

Number of 4 input LUTs: 46

Delay: 27.033ns