**CS 303 21/12/2019**

**Term Project Report**

The main purpose of the project is to create an ATM module that will perform on a FPGA Board. The preparation of the project has been done in three steps.

1. The first step was the preparation of an ASM Chart that shows all states and respective operations that would take place on respective states. ASM Chart also symbolizes the flow of the whole module.
2. In the second step, the Verilog commend file created according the ASM Chart provided, the Verilog file is a file that includes the required codes to proceed between states and perform actions that take place in the flow such as locking the system for a while.
3. In the last step, the TopModule Verilog and UCF files are created, TopModule Verilog file gives ability to perform operations that are represented in the Verilog file that created in the second step and UCF file initialize the LEDs and buttons which are on FPGA Board.

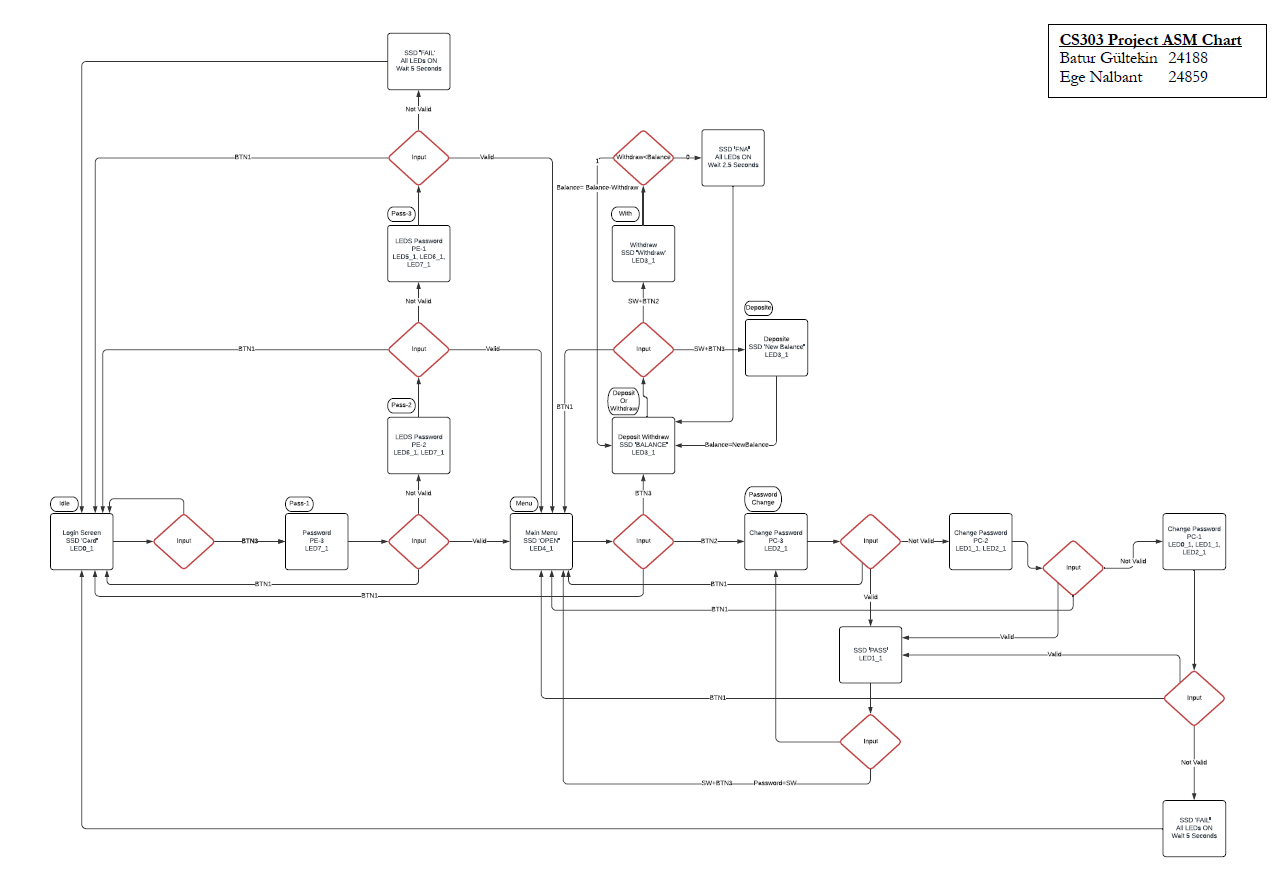


Figure 1 The ASM Chart that we prepared for the first step.

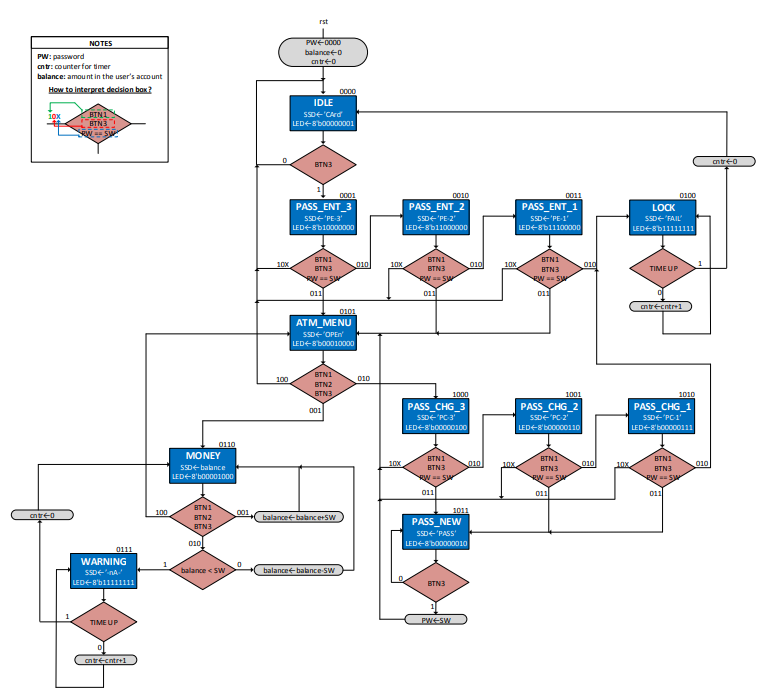


Figure 2 The provided ASM Chart which taken reference while creating Verilog file.

**Verilog File and TopModule:**

The Verilog file is an implementation of the provided ASM Chart. It contains combinational and sequential parts.

* In the combinational part: the possible outcomes and the required condition to perform operations such as state change by using buttons are implemented.
* In the sequential part: reset button and states of LEDs are implemented.

In the TopModule, the verilog file is used as a function to be able to iterate repeatedly with out the need of another function. In addition, the buttons and LEDs of the FGPA Board are initialized by creating UCF file.

**Total Number of 4 input LUTs:** 328, Utilization 17%

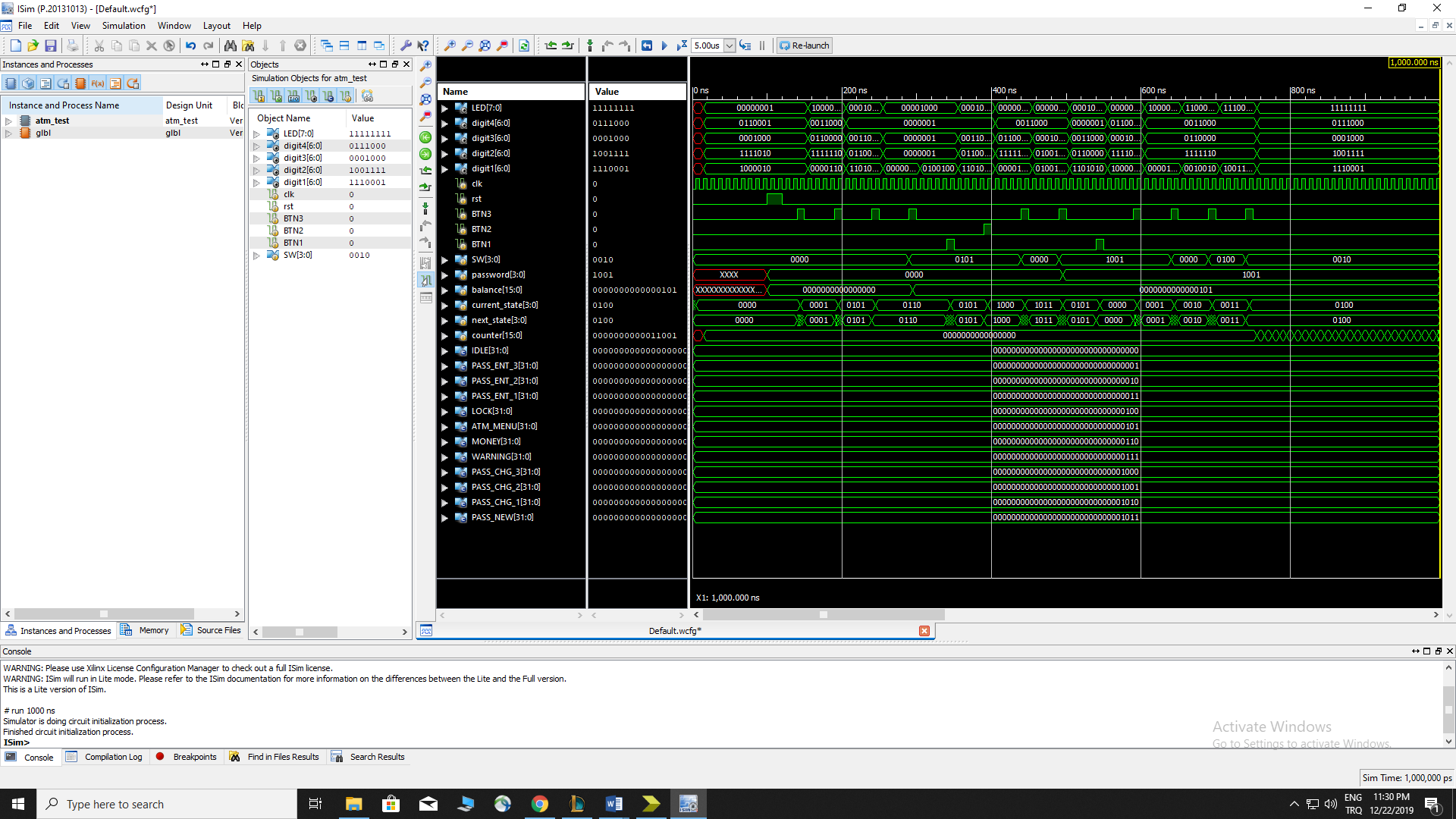


Figure 3 A screenshot of the simulation