

Lesson 3 - LAB 2 – Report

Makefile:

*This Makefile compatible with CPU: Cortex-M3

```
1  #@copyright : Bavly-Mansour
2  CC=arm-none-eabi-
3  CFLAGS= -mcpu=cortex-m3 -gdwarf-2
4  INCS= -I .
5  LIBS=
6  SRC= $(wildcard *.c)
7  OBJ= $(SRC:.c=.o)
8  As = $(wildcard *.s)
9  AsOBJ = $(As:.s=.o)
10 Project_name=learn_in_depth_cortex_m3
11
12 all: $(Project_name).bin
13     @echo "=====
14     @echo "=====DONE=====
15     @echo "=====
16
17 %.o: %.c
18     $(CC)gcc.exe -c $(CFLAGS) $(INCS) $< -o $@
19     @echo "=====Compiler gcc DONE=====
20
21
22 %.o: %.s
23     $(CC)as.exe $(CFLAGS) $(INCS) $< -o $@
24     @echo "=====STARTUP DONE=====
25
26 $(Project_name).elf: $(OBJ) $(AsOBJ)
27     $(CC)ld.exe -T linker_script.ld -Map=app.map $(OBJ) $(AsOBJ) -o $@
28     @echo "=====linker DONE=====
29
30 $(Project_name).bin: $(Project_name).elf
31     $(CC)objcopy.exe -O binary $(Project_name).elf $(Project_name).bin
32     @echo "=====File.bin DONE=====
33
34 $(Project_name).hex: $(Project_name).elf
35     $(CC)objcopy.exe -O binary $< $@
36     @echo "=====File.hex DONE=====
37
38 clean:
39     rm *.elf *.bin
40     @echo "=====CLEAN=====
41
42 clean_all:
43     rm *.elf *.bin *.o
44     @echo "=====CLEAN ALL=====
```

* -gdwarf-2 instead of -g with Cortex-M3.

* \$@ is for target, \$< for dependency.

* % is a generalization means all of.

Output of Makefile:

```
Bavly@DESKTOP-CNE79H4 MINGW64 /d/Embedded system diploma/Embedded System Diploma
/Diploma Assignmets/First_Term/Unit_3_Embedded_C/Lesson 3/Lab 2 (master)
$ make clean_all
rm *.elf *.bin *.o
=====CLEAN ALL=====

Bavly@DESKTOP-CNE79H4 MINGW64 /d/Embedded system diploma/Embedded System Diploma
/Diploma Assignmets/First_Term/Unit_3_Embedded_C/Lesson 3/Lab 2 (master)
$ make
arm-none-eabi-gcc.exe -c -mcpu=cortex-m3 -gdwarf-2 -I . main.c -o main.o
=====Compiler gcc DONE=====
arm-none-eabi-gcc.exe -c -mcpu=cortex-m3 -gdwarf-2 -I . startup.c -o startup.o
=====Compiler gcc DONE=====
arm-none-eabi-ld.exe -T linker_script.ld -Map=app.map main.o startup.o -o learn
_in_depth_cortex_m3.elf
=====linker DONE=====
arm-none-eabi-objcopy.exe -O binary learn_in_depth_cortex_m3.elf learn_in_depth_
cortex_m3.bin
=====File.bin DONE=====
=====
=====DONE=====
=====
```

Main.c file :

```
1  /**
2  ****
3  * @file      : main.c
4  * @author    : Eng Bavly Mansour
5  * @brief     : Main program body
6  ****
7  */
8
9  #include <stdint.h>
10 #include <platform_Types.h>
11
12
13 #define RCC_BASE      0x40021000
14 #define GPIOA_BASE    0x40010800
15 #define RCC_APB2ENR   *(volatile uint32_t*) (RCC_BASE + 0x18)
16 // 0x18 is the offset of base memory address
17 #define GPIOA_CHR     *(volatile uint32_t*) (GPIOA_BASE + 0x04)
18 // general purpose input output port A
19 #define GPIOA_ODR     *(volatile uint32_t*) (RCC_BASE + 0x0c)
20 // output data register
21
22 // #if !defined(__SOFT_FP__) && defined(__ARM_FP)
23 // #warning "FPU is not initialized, but the project is compiling for an FPU. Please initialize the FPU before use."
24 // #endif
25
26 unsigned char g_variable[3] = {1,2,3};
27 unsigned char const const_var[3] = {1,2,3};
28 unsigned char bss_var[3] ;
29
30 /*g_variable : global variable
31 const_var   : constant variable
32 bss_var     : uninitialized variable*/
33
34 int main(void)
35 {
36     /* Loop forever */
37     int i;
38     RCC_APB2ENR |= (1<<2);
39     GPIOA_CHR &= 0xff0ffff;
40     GPIOA_CHR |= 0x00200000;
41     while (1){
42
43         GPIOA_ODR |= 1<<13;
44         // set 1 to a bit |= 1<<n
45         for (i = 0 ; i < 5000 ; i++)
46             GPIOA_ODR &= ~(1<<13);
47         // clear a bit &= ~(1<<n)
48         for (i = 0; i < 5000 ; i++);
49
50     }
51     return 0;
52 }
53
```

Startup.s file for Cortex-M3:

```
startup.s-org  x startup.c  x main.c  x Makefile  x
1  /* startup_cortexM3.s By: Bavly Mansour*/
2
3  /*SRAM 0x20000000 */
4
5  .section .vectors
6
7  .word 0x20001000      /*stack top address*/
8  .word _reset         /*1 reset */
9  .word Vector_handler /*2 NMI*/
10 .word Vector_handler /*3 hard fault*/
11 .word Vector_handler /*4 MM fault*/
12 .word Vector_handler /*5 Bus fault*/
13 .word Vector_handler /*6 Usage fault*/
14 .word Vector_handler /*7 Reserved*/
15 .word Vector_handler /*8 Reserved*/
16 .word Vector_handler /*9 Reserved*/
17 .word Vector_handler /*10 Reserved*/
18 .word Vector_handler /*11 SV call*/
19 .word Vector_handler /*12 Debug reserve*/
20 .word Vector_handler /*13 Reserved*/
21 .word Vector_handler /*14 PendSV*/
22 .word Vector_handler /*15 SysTick*/
23 .word Vector_handler /*16 TRQ0*/
24 .word Vector_handler /*17 TRQ1*/
25 .word Vector_handler /*18 TRQ2*/
26 .word Vector_handler /*19 ... */
27
28 /* on to IRQ67*/
29
30 .section .text
31
32 _reset:
33     bl main
34     b .
35
36 .thumb_func      /* dealing with 16 and 32 bits*/
37
38 Vector_handler :
39     b _reset
40
```

- .word is for enabling memory alignment.
- .thumb_func dealing with 16 and 32 bits instructions.

Startup.c file for Cortex-M3:

```
startup.s-org x startup.c x main.c x Makefile x linker_script.ld x
1  /*
2  ****
3  ****
4  learn-in-depth
5  By:Bavly Mansour
6  ****
7  ****
8  */
9
10 #include <stdint.h>
11 #define STACK_Start_SP 0x20001000 //txt replacement of STACK_Start_SP "stack pointer" to address 0x20001000
12 extern int main (void); // define external int main (void)
13 void Rest_Handler (void); //define rest_handler function
14
15
16 /*Copying data from flash to SRAM and allocate space
17 for bss and stack according to the memory bounders */
18
19
20 void NMI_Handler() __attribute__((weak,alias("Default_Handler")));
21 void H_Fault_Handler() __attribute__((weak,alias("Default_Handler")));
22 void MM_Fault_Handler() __attribute__((weak,alias("Default_Handler")));
23 void Bus_Fault() __attribute__((weak,alias("Default_Handler")));
24 void Usage_Fault_Handler() __attribute__((weak,alias("Default_Handler")));
25
26
27 extern unsigned int _E_text;
28 extern unsigned int _S_DATA;
29 extern unsigned int _E_DATA;
30 extern unsigned int _S_bss;
31 extern unsigned int _E_bss;
32 extern unsigned int _stack_top;
33
34 void Default_Handler ()
35 {
36     Rest_Handler();
37 }
38
39 void Rest_Handler (void)
40 {
41     // copying data from ROM to RAM
42     unsigned int DATA_size = (unsigned char*)&_E_DATA - (unsigned char*)&_S_DATA;
43     unsigned char* P_src = (unsigned char*)&_E_text ;
44     unsigned char* P_dst = (unsigned char*)&_S_DATA ;
45
46     for (int i =0 ; i < DATA_size ; i++){
47         *((unsigned char *)P_dst++) = *((unsigned char*)P_src++);
48     }
49 }
```

- Alias attribute causes the declaration to be emitted as an alias for another symbol.
- Weak attribute causes the declaration to be emitted as a weak symbol rather than a global.

- **Handler functions in MapFile :**

```
.text          0x08000000      0x137
*(.vectors*)
.vectors       0x08000000      0x1c  startup.o
               0x08000000      vectors
*(.text*)
.text          0x0800001c      0x80  main.o
               0x0800001c      main
.text          0x0800009c      0x98  startup.o
               0x0800009c      H_Fault_Handler
               0x0800009c      MM_Fault_Handler
               0x0800009c      Bus_Fault
               0x0800009c      Default_Handler
               0x0800009c      Usage_Fault_Handler
               0x0800009c      NMI_Handler
               0x080000a8      Rest_Handler
*(.rodata)
.rodata        0x08000134      0x3   main.o
               0x08000134      const_var
               0x08000137      _E_text = .
```

- Main at 0x0800001c
- And all Handler functions at the same address of the default address due to the alias. Default_Handler at 0x0800009c, while the Rest_handler has a different address at 0x080000a8.

Linker script for Cortex-M3:

```
startup.s-org x startup.c x main.c x Makefile x linker_script.ld
1  /*This is linker script for LAB2 CPU=CORTEx-M3 ,by : ENG_BAVLY*/
2
3  MEMORY
4  {
5      flash(RX) : ORIGIN = 0X08000000 , LENGTH = 128K
6      /*flash memory origin and length , flash: read and execute*/
7      sram(RwX) : ORIGIN = 0X20000000 , LENGTH = 20K
8      /*sRAM origin and length , sram : read write execute*/
9
10 }
11 /*sections*/
12 SECTIONS {
13     .text :{
14         *(.vectors*)
15         *(.text*)
16         *(.rodata)
17         _E_text = .;          /*end of text section in flash @ 0x08000b3*/
18     }> flash
19
20     /*everything inside .text put it in flash */
21
22     .data :{
23         _S_DATA = .;          /*start of data section @ 0x08000b3 the same address of end text section */
24         *(.data)
25         . = ALIGN(4) ;
26         _E_DATA = .;          /*end of data section */
27     }>sram AT > flash        /*virtual memory :sram */
28
29     .bss :{
30         _S_bss = . ;          /*start of bss section */
31         *(.bss*)
32         . = ALIGN(4);
33         _E_bss = . ;
34         . = ALIGN(4);          /*end of bss section */
35         . = . + 0x1000 ;
36         _stack_top = . ;
37     }>sram
38     /* bss are the uninitialized variables = zeros so ignore them from the flash */
39
40 }
```

- According to memory borders:
 - _E_text is the end of .text section
 - _S_DATA is the start of .data section
 - _S_bss is the start of .bss section
- .text section includes .rodata section.
- ALIGN(4) is for memory alignment.

- Memory configuration according to linker script memory borders:

```

6
7  Memory Configuration
8
9  Name          Origin          Length          Attributes
10 flash         0x08000000      0x00020000      xr
11 sram          0x20000000      0x00005000      xrw
12 *default*     0x00000000      0xffffffff
13

```

- Linker script memory map:

```

55 ▼ .data          0x20000000      0x4 load address 0x08000137
56          0x20000000      _S_DATA = .
57  *(.data)
58 ▼ .data          0x20000000      0x3 main.o
59          0x20000000      g_variable
60 ▼ .data          0x20000003      0x0 startup.o
61          0x20000004      . = ALIGN (0x4)
62 ▼ *fill*         0x20000003      0x1
63          0x20000004      _E_DATA = .
64
65 ▼ .igot.plt      0x20000004      0x0 load address 0x0800013b
66 .igot.plt      0x20000004      0x0 main.o
67
68 ▼ .bss           0x20000004      0x1003 load address 0x0800013b
69          0x20000004      _S_bss = .
70  *(.bss*)
71 .bss           0x20000004      0x0 main.o
72 ▼ .bss           0x20000004      0x0 startup.o
73          0x20000004      . = ALIGN (0x4)
74          0x20000004      _E_bss = .
75          0x20000004      . = ALIGN (0x4)
76          0x20001004      . = (. + 0x1000)
77 ▼ *fill*         0x20000004      0x1000
78          0x20001004      _stack_top = .
79 ▼ COMMON         0x20001004      0x3 main.o
80          0x20001004      bss_var

```

- The start of .bss section is the same address of the end of .data section
 $\&_E_DATA = \&_S_bss = 0x20000004$
- $_stack_top$ is at $0x20001004 = _E_bss + 0x1000$