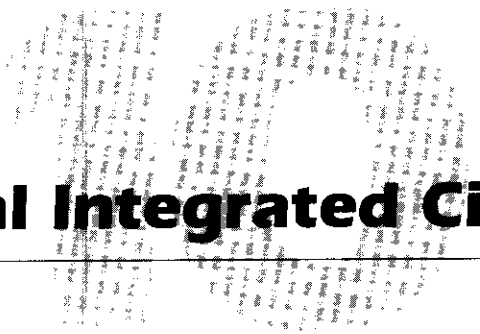


Digital Integrated Circuits

10-1 INTRODUCTION

The integrated circuit (IC) and the digital logic families were introduced in Section 2-8. This chapter presents the electronic circuits in each IC digital logic family and analyzes their electrical operation. A basic knowledge of electrical circuits is assumed.

The IC digital logic families to be considered here are

RTL	Resistor-transistor logic
DTL	Diode-transistor logic
TTL	Transistor-transistor logic
ECL	Emitter-coupled logic
MOS	Metal-oxide semiconductor
CMOS	Complementary metal-oxide semiconductor

The first two, RTL and DTL, have only historical significance since they are no longer used in the design of digital systems. RTL was the first commercial family to have been used extensively. It is included here because it represents a useful starting point for explaining the basic operation of digital gates. DTL circuits have been replaced by TTL. In fact, TTL is a modification of the DTL gate. The operation of the TTL gate will be easier to understand after the DTL gate is analyzed. TTL, ECL, and CMOS have a large number of SSI circuits, as well as MSI, LSI, and VLSI components. MOS is mostly used for LSI and VLSI components.

The basic circuit in each IC digital logic family is either a NAND or NOR gate. This basic circuit is the primary building block from which all other more complex digital components are obtained. Each IC logic family has available a data book that lists all the integrated circuits in that family. The differences in the logic functions available from each logic family are not so much in the functions that they achieve as in the specific electrical characteristics of the basic gate from which the circuit is constructed.

NAND and NOR gates are usually defined by the Boolean functions that they implement in terms of binary variables. When analyzing them as electronic circuits, it is necessary to investigate their input–output relationships in terms of two voltage levels: a *high* level designated by *H* and a *low* level designated by *L*. As mentioned in Section 2-8, the assignment of binary 1 to *H* results in a positive logic system and the assignment of binary 1 to *L* results in a negative logic system. The truth table in terms of *H* and *L* of a positive logic NAND gate is shown in Fig. 10-1. We notice that the output of the gate is high as long as one or more inputs are low. The output is low only when both inputs are high. The behavior of a positive logic NAND gate in terms of high and low signals can be stated as follows:

If *any* input of a NAND gate is low, the output is high.

If *all* inputs of a NAND gate are high, the output is low.

The corresponding truth table for a positive logic NOR gate is shown in Fig. 10-2. The output of the NOR gate is low when one or more inputs are high. The output is high when both inputs are low. The behavior of a positive logic NOR gate in terms of high and low signals can be stated as follows:

If *any* input of a NOR gate is high, the output is low.

If *all* inputs of a NOR gate are low, the output is high.

These statements for NAND and NOR gates must be remembered because they will be used during the analysis of the electronic gates in this chapter.

A bipolar junction transistor (BJT) can be either an *npn* or a *pnp* junction transistor. In contrast, the field-effect transistor (FET) is said to be unipolar. The operation of a bipolar transistor depends on the flow of two types of carriers: electrons and holes. A unipolar transistor depends on the flow of only one type of majority carrier, which may be electrons (n-channel) or holes (p-channel). The first four digital logic families listed, RTL, DTL, TTL, and ECL, use bipolar transistors. The last two families, MOS and

Inputs		Output
x	*y*	*z*
L	*L*	*H*
L	*H*	*H*
H	*L*	*H*
H	*H*	*L*

FIGURE 10-1
Positive logic NAND gate

Inputs		Output
x	y	z
L	L	H
L	H	L
H	L	L
H	H	L

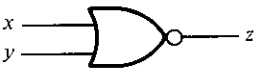


FIGURE 10-2
Positive logic NOR gate

CMOS, employ a type of unipolar transistor called a metal-oxide-semiconductor field-effect transistor, abbreviated MOSFET or MOS for short.

In this chapter, we first introduce the most common characteristics by which the digital logic families are compared. We then describe the properties of the bipolar transistor and analyze the basic gates in the bipolar logic families. We then explain the operation of the MOS transistor and introduce the basic gates of its two logic families.

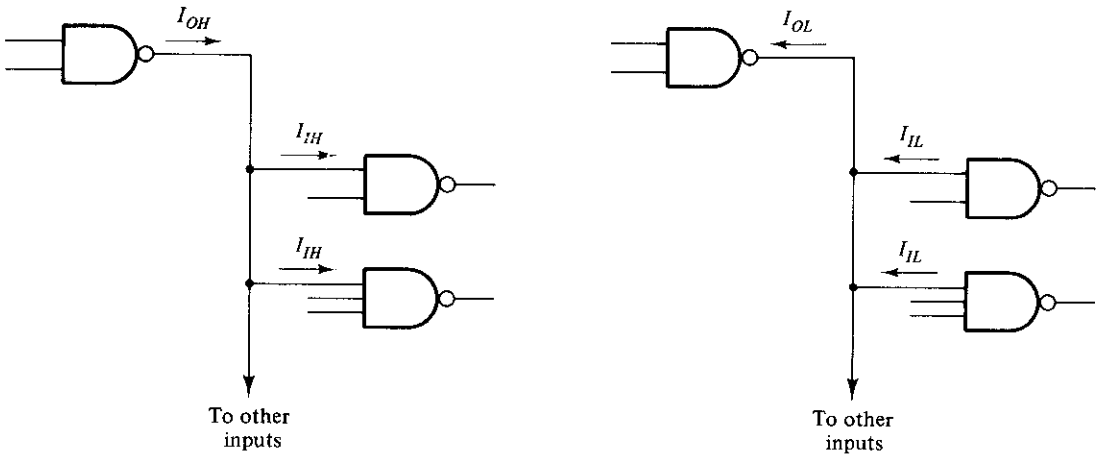
10-2 SPECIAL CHARACTERISTICS

The characteristics of IC digital logic families are usually compared by analyzing the circuit of the basic gate in each family. The most important parameters that are evaluated and compared are fan-out, power dissipation, propagation delay, and noise margin. We first explain the properties of these parameters and then use them to compare the IC logic families.

Fan-Out

The fan-out of a gate specifies the number of standard loads that can be connected to the output of the gate without degrading its normal operation. A standard load is usually defined as the amount of current needed by an input of another gate in the same logic family. Sometimes the term *loading* is used instead of fan-out. This term is derived because the output of a gate can supply a limited amount of current, above which it ceases to operate properly and is said to be overloaded. The output of a gate is usually connected to the inputs of other gates. Each input consumes a certain amount of current from the gate output, so that each additional connection adds to the load of the gate. Loading rules are sometimes specified for a family of digital circuits. These rules give the maximum amount of loading allowed for each output of each circuit in the family. Exceeding the specified maximum load may cause a malfunction because the circuit cannot supply the power demanded from it. The fan-out is the maximum number of inputs that can be connected to the output of a gate, and is expressed by a number.

The fan-out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of a gate. Consider the connections shown in Fig. 10-3. The output of one gate is connected to one or more inputs of other gates. The output of the gate is in the high voltage level in Fig. 10-3(a). It provides a



(a) High-level output

(b) Low-level output

FIGURE 10-3
Fan-out computation

current source I_{OH} to all the gate inputs connected to it. Each gate input requires a current I_{IH} for proper operation. Similarly, the output of the gate is in the low voltage level in Fig. 10-3(b). It provides a current sink I_{OL} for all the gate inputs connected to it. Each gate input supplies a current I_{IL}. The fan-out of the gate is calculated from the ratio I_{OH}/I_{IH} or I_{OL}/I_{IL}, whichever is smaller. For example, the standard TTL gates have the following values for the currents:

$$I_{OH} = 400\ \mu A$$
$$I_{IH} = 40\ \mu A$$
$$I_{OL} = 16\ mA$$
$$I_{IL} = 1.6\ mA$$

The two ratios give the same number in this case:

$$\frac{400\ \mu A}{40\ \mu A} = \frac{16\ mA}{1.6\ mA} = 10$$

Therefore, the fan-out of standard TTL is 10. This means that the output of a TTL gate can be connected to no more than ten inputs of other gates in the same logic family. Otherwise, the gate may not be able to drive or sink the amount of current needed from the inputs that are connected to it.

Power Dissipation

Every electronic circuit requires a certain amount of power to operate. The power dissipation is a parameter expressed in milliwatts (mW) and represents the amount of power needed by the gate. The number that represents this parameter does not include the

power delivered from another gate; rather, it represents the power delivered to the gate from the power supply. An IC with four gates will require, from its power supply, four times the power dissipated in each gate.

The amount of power that is dissipated in a gate is calculated from the supply voltage V_{CC} and the current I_{CC} that is drawn by the circuit. The power is the product $V_{CC} \times I_{CC}$. The current drain from the power supply depends on the logic state of the gate. The current drawn from the power supply when the output of the gate is in the high-voltage level is termed I_{CCH}. When the output is in the low-voltage level, the current is I_{CCL}. The average current is

$$I_{CC}(\text{avg}) = \frac{I_{CCH} + I_{CCL}}{2}$$

and is used to calculate the average power dissipation:

$$P_D(\text{avg}) = I_{CC}(\text{avg}) \times V_{CC}$$

For example, a standard TTL NAND gate uses a supply voltage V_{CC} of 5 V and has current drains $I_{CCH} = 1$ mA and $I_{CCL} = 3$ mA. The average current is $(3 + 1)/2 = 2$ mA. The average power dissipation is $5 \times 2 = 10$ mW. An IC that has four NAND gates dissipates a total of $10 \times 4 = 40$ mW. In a typical digital system there will be many ICs, and the power required by each IC must be considered. The total power dissipation in the system is the sum total of the power dissipated in all ICs.

Propagation Delay

The propagation delay of a gate is the average transition-delay time for the signal to propagate from input to output when the binary signal changes in value. The signals through a gate take a certain amount of time to propagate from the inputs to the output. This interval of time is defined as the propagation delay of the gate. Propagation delay is measured in nanoseconds (ns). 1 ns is equal to 10^{-9} of a second.

The signals that travel from the inputs of a digital circuit to its outputs pass through a series of gates. The sum of the propagation delays through the gates is the total delay of the circuit. When speed of operation is important, each gate must have a short propagation delay and the digital circuit must have a minimum number of gates between inputs and outputs.

The average propagation delay time of a gate is calculated from the input and output waveforms, as shown in Fig. 10-4. The signal-delay time between the input and output when the output changes from the high to the low level is referred to as t_{PHL}. Similarly, when the output goes from the low to the high level, the delay is t_{PLH}. It is customary to measure the time between the 50 percent point on the input and output transitions. In general, the two delays are not the same, and both will vary with loading conditions. The average propagation-delay time is calculated as the average of the two delays.

As an example, the delays for a standard TTL gate are $t_{PHL} = 7$ ns and $t_{PLH} = 11$ ns. These quantities are given in the TTL data book and are measured with a load resistance of 400 ohms and a load capacitance of 15 pF. The average propagation delay of the TTL gate is $(11 + 7)/2 = 9$ ns.

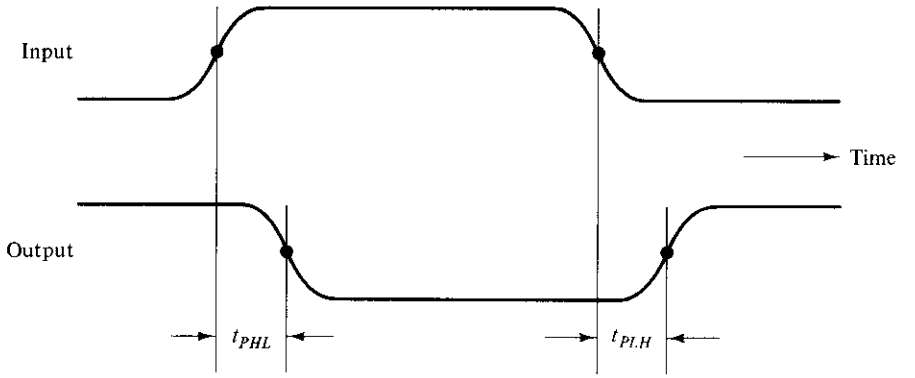


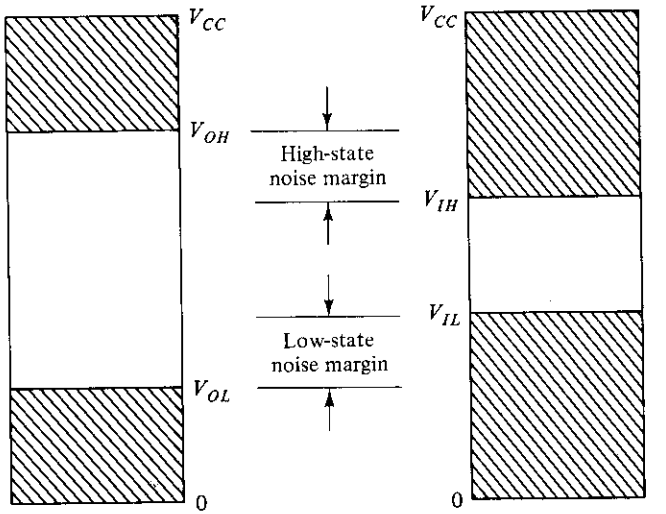
FIGURE 10-4
Measurement of propagation delay

Under certain conditions, it is more important to know the maximum delay time of a gate rather than the average value. The TTL data book lists the following maximum propagation delays for a standard NAND gate: t_{PHL} = 15 ns and t_{PLH} = 22 ns. When speed of operation is critical, it is necessary to take into account the maximum delay to ensure proper operation.

The input signals in most digital circuits are applied simultaneously to more than one gate. All the gates that are connected to external inputs constitute the first logic level of the circuit. Gates that receive at least one input from an output of a first-level gate are considered to be in the second logic level, and similarly for the third and higher logic levels. The total propagation delay of the circuit is equal to the propagation delay of a gate times the number of logic levels in the circuit. Thus, a reduction in the number of logic levels results in a reduction of signal delay and faster circuits. The reduction of the propagation delay in circuits may be more important than the reduction of the total number of gates if speed of operation is a major factor.

Noise Margin

Spurious electrical signals from industrial and other similar sources can induce undesirable voltages on the connecting wires between logic circuits. These unwanted signals are referred to as *noise*. There are two types of noise to be considered. DC noise is caused by a drift in the voltage levels of a signal. AC noise is a random pulse that may be created by other switching signals. Thus, noise is a term used to denote an undesirable signal that is superimposed upon the normal operating signal. *Noise margin* is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. The ability of circuits to operate reliably in a noise environment is important in many applications. Noise margin is expressed in volts and represents the maximum noise signal that can be tolerated by the gate.



(a) Output voltage range (b) Input voltage range

FIGURE 10-5
Signals for evaluating noise margin

The noise margin is calculated from knowledge of the voltage signal available in the output of the gate and the voltage signal required in the input of the gate. Figure 10-5 illustrates the signals for computing noise margin. Part (a) shows the range of output voltages that can occur in a typical gate. Any voltage in the gate output between V_{CC} and V_{OH} is considered as the high-level state and any voltage between 0 and V_{OL} in the gate output is considered as the low-level state. Voltages between V_{OL} and V_{OH} are indeterminate and do not appear under normal operating conditions except during transition between the two levels. The corresponding two voltage ranges that are recognized by the input of the gate are indicated in Fig. 10-5(b). In order to compensate for any noise signal, the circuit must be designed so that V_{IL} is greater than V_{OL} and V_{IH} is less than V_{OH}. The noise margin is the difference $V_{OH} - V_{IH}$ or $V_{IL} - V_{OL}$, whichever is smaller.

As illustrated in Fig. 10-5, V_{OL} is the maximum voltage that the output can be when in the low-level state. The circuit can tolerate any noise signal that is less than the noise margin ($V_{IL} - V_{OL}$) because the input will recognize the signal as being in the low-level state. Any signal greater than V_{OL} plus the noise-margin figure will send the input voltage into the indeterminate range, which may cause an error in the output of the gate. In a similar fashion, a negative-voltage noise greater than $V_{OH} - V_{IH}$ will send the input voltage into the indeterminate range.

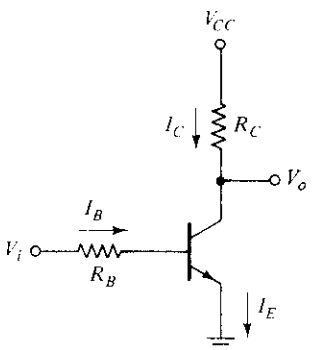
The parameters for the noise margin in a standard TTL NAND gate are $V_{OH} = 2.4$ V, $V_{OL} = 0.4$ V, $V_{IH} = 2$ V, and $V_{IL} = 0.8$ V. The high-state noise margin is $2.4 - 2 = 0.4$ V, and the low-state noise margin is $0.8 - 0.4 = 0.4$ V. In this case, both values are the same.

10-3 BIPOLAR-TRANSISTOR CHARACTERISTICS

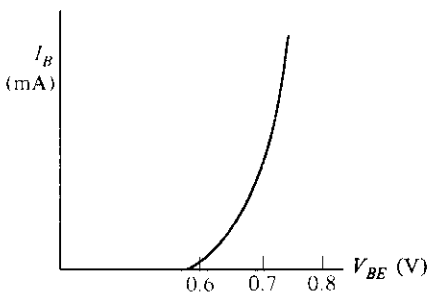
This section is devoted to a review of the bipolar transistor as applied to digital circuits. This information will be used for the analysis of the basic circuit in the four bipolar logic families. Bipolar transistors may be of the *npn* or *pnp* type. Moreover, they are constructed either with germanium or silicon semiconductor material. IC transistors, however, are made with silicon and are usually of the *npn* type.

The basic data needed for the analysis of digital circuits may be obtained from inspection of the typical characteristic curves of a common-emitter *npn* silicon transistor, shown in Fig. 10-6. The circuit in (a) is a simple inverter with two resistors and a transistor. The current marked I_C flows through resistor R_C and the collector of the transistor. Current I_B flows through resistor R_B and the base of the transistor. The emitter is connected to ground and its current $I_E = I_C + I_B$. The supply voltage is between V_{CC} and ground. The input is between V_i and ground, and the output is between V_o and ground.

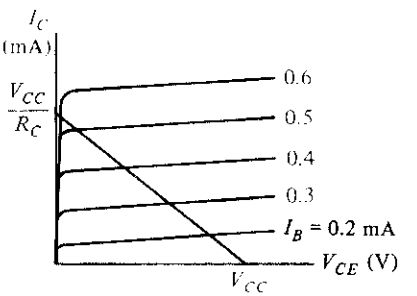
We have assumed a positive direction for the currents as indicated. These are the directions in which the currents normally flow in an *npn* transistor. Collector and base currents, I_C and I_B, respectively, are positive when they flow into the transistor. Emit-



(a) Inverter circuit



(b) Transistor-base characteristic



(c) Transistor-collector characteristic

FIGURE 10-6
Silicon *npn* transistor characteristics

ter current I_E is positive when it flows out of the transistor, as indicated by the arrow in the emitter terminal. The symbol V_{CE} stands for the voltage drop from collector to emitter and is always positive. Correspondingly, V_{BE} is the voltage drop across the base-to-emitter junction. This junction is forward biased when V_{BE} is positive. It is reverse biased when V_{BE} is negative.

The base–emitter graphical characteristic is shown in Fig. 10-6(b). This is a plot of V_{BE} versus I_B. If the base–emitter voltage is less than 0.6 V, the transistor is said to be *cut off* and no base current flows. When the base–emitter junction is forward biased with a voltage greater than 0.6 V, the transistor conducts and I_B starts rising very fast whereas V_{BE} changes very little. The voltage V_{BE} across a conducting transistor seldom exceeds 0.8 V.

The graphical collector–emitter characteristics, together with the load line, are shown in Fig. 10-6(c). When V_{BE} is less than 0.6 V, the transistor is cut off with $I_B = 0$ and a negligible current flows in the collector. The collector-to-emitter circuit then behaves like an open circuit. In the *active* region, collector voltage V_{CE} may be anywhere from about 0.8 V up to V_{CC}. Collector current I_C in this region can be calculated to be approximately equal to $I_B h_{FE}$, where h_{FE} is a transistor parameter called the *dc current gain*. The maximum collector current depends not on I_B, but rather on the external circuit connected to the collector. This is because V_{CE} is always positive and its lowest possible value is 0 V. For example, in the inverter shown, the maximum I_C is obtained by making $V_{CE} = 0$ to obtain $I_C = V_{CC}/R_C$.

It was stated that $I_C = h_{FE} I_B$ in the active region. The parameter h_{FE} varies widely over the operating range of the transistor, but still it is useful to employ an average value for the purpose of analysis. In a typical operating range, h_{FE} is about 50, but under certain conditions, it could go down to as low as 20. It must be realized that the base current I_B may be increased to any desirable value, but the collector current I_C is limited by external circuit parameters. As a consequence, a situation can be reached where $h_{FE} I_B$ is greater than I_C. If this condition exists, then the transistor is said to be in the *saturation* region. Thus, the condition for saturation is determined from the relationship

$$I_B \geq \frac{I_{CS}}{h_{FE}}$$

where I_{CS} is the maximum collector current flowing during saturation. V_{CE} is not exactly zero in the saturation region, but is normally about 0.2 V.

The basic data needed for analyzing bipolar transistor digital circuits are listed in Table 10-1. In the cutoff region, V_{BE} is less than 0.6 V, V_{CE} is considered as an open circuit, and both currents are negligible. In the active region, V_{BE} is about 0.7 V, V_{CE} may vary over a wide range, and I_C can be calculated as a function of I_B. In the saturation region, V_{BE} hardly changes, but V_{CE} drops to 0.2 V. The base current must be large enough to satisfy the inequality listed. To simplify the analysis, we will assume that $V_{BE} = 0.7$ V if the transistor is conducting, whether in the active or saturation region.

The analysis of digital circuits may be undertaken using a prescribed procedure: For each transistor in the circuit, determine if its V_{BE} is less than 0.6 V. If so, then the tran-

TABLE 10-1
Typical *npn* Silicon Transistor Parameters

Region	V_{BE} (V)*	V_{CE} (V)	Current Relationship
Cutoff	< 0.6	Open circuit	$I_B = I_C = 0$
Active	0.6–0.7	> 0.8	$I_C = h_{FE} I_B$
Saturation	0.7–0.8	0.2	$I_B \geq I_{CS}/h_{FE}$

*V_{BE} will be assumed to be 0.7 V if the transistor is conducting, whether in the active or saturation region.

sistor is cut off and the collector-to-emitter circuit is considered an open circuit. If V_{BE} is greater than 0.6 V, the transistor may be in the active or saturation region. Calculate the base current, assuming that $V_{BE} = 0.7$ V. Then calculate the maximum possible value of collector current I_{CS}, assuming $V_{CE} = 0.2$ V. These calculations will be in terms of voltages applied and resistor values. Then, if the base current is large enough that $I_B \geq I_{CS}/h_{FE}$, we deduce that the transistor is in the saturation region with $V_{CE} = 0.2$ V. However, if the base current is smaller and the above relationship is not satisfied, the transistor is in the active region and we recalculate collector current I_C using the equation $I_C = h_{FE} I_B$.

To demonstrate with an example, consider the inverter circuit of Fig. 10-6(a) with the following parameters:

$$R_C = 1 \text{ k}\Omega \qquad V_{CC} = 5 \text{ V (voltage supply)}$$
$$R_B = 22 \text{ k}\Omega \qquad H = 5 \text{ V (high-level voltage)}$$
$$h_{FE} = 50 \qquad L = 0.2 \text{ V (low-level voltage)}$$

With input voltage $V_i = L = 0.2$ V, we have that $V_{BE} < 0.6$ V and the transistor is cut off. The collector–emitter circuit behaves like an open circuit; so output voltage $V_o = 5 \text{ V} = H$.

With input voltage $V_i = H = 5$ V, we deduce that $V_{BE} > 0.6$ V. Assuming that $V_{BE} = 0.7$, we calculate the base current:

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{5 - 0.7}{22 \text{ k}\Omega} = 0.195 \text{ mA}$$

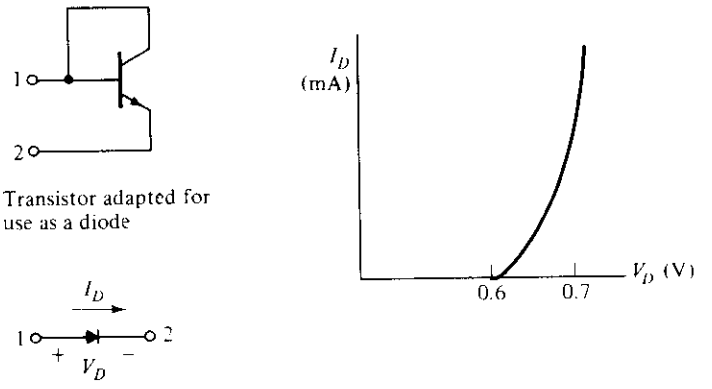
The maximum collector current, assuming $V_{CE} = 0.2$ V, is

$$I_{CS} = \frac{V_{CC} - V_{CE}}{R_C} = \frac{5 - 0.2}{1 \text{ k}\Omega} = 4.8 \text{ mA}$$

We then check for saturation:

$$0.195 = I_B \geq \frac{I_{CS}}{h_{FE}} = \frac{4.8}{50} = 0.096 \text{ mA}$$

and find that the inequality is satisfied since $0.195 > 0.096$. We conclude that the transistor is saturated and output voltage $V_o = V_{CE} = 0.2 \text{ V} = L$. Thus, the circuit behaves as an inverter.



(a) Transistor adapted for use as a diode

(b) Diode graphic symbol

(c) Diode characteristic

FIGURE 10-7
Silicon diode symbol and characteristic

The procedure just described will be used extensively during the analysis of the circuits in the following sections. This will be done by means of a qualitative analysis, i.e., without writing down the specific numerical equations. The quantitative analysis and specific calculations will be left as exercises in the Problems section at the end of the chapter.

There are occasions where not only transistors but also diodes are used in digital circuits. An IC diode is usually constructed from a transistor with its collector connected to the base, as shown in Fig. 10-7(a). The graphic symbol employed for a diode is shown in Fig. 10-7(b). The diode behaves essentially like the base–emitter junction of a transistor. Its graphical characteristic, shown in Fig. 10-7(c), is similar to the base–emitter characteristic of a transistor. We can then conclude that a diode is off and nonconducting when its forward voltage, V_D, is less than 0.6 V. When the diode conducts, current I_D flows in the direction shown in Fig. 10-7(b), and V_D stays at about 0.7 V. One must always provide an external resistor to limit the current in a conducting diode, since its voltage remains fairly constant at a fraction of a volt.

10-4 RTL AND DTL CIRCUITS

RTL Basic Gate

The basic circuit of the RTL digital logic family is the NOR gate shown in Fig. 10-8. Each input is associated with one resistor and one transistor. The collectors of the transistors are tied together at the output. The voltage levels for the circuit are 0.2 V for the low level and from 1 to 3.6 V for the high level.

The analysis of the RTL gate is very simple and follows the procedure outlined in the previous section. If any input of the RTL gate is high, the corresponding transistor is

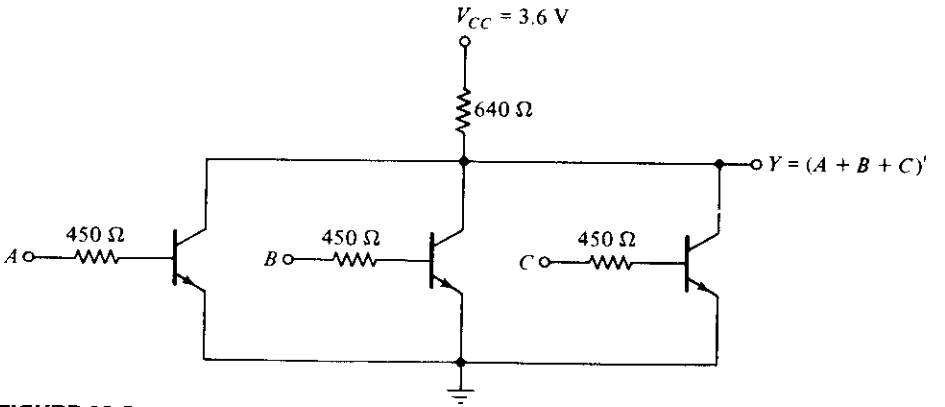


FIGURE 10-8
RTL basic NOR gate

driven into saturation. This causes the output to be low, regardless of the states of the other transistors. If all inputs are low at 0.2 V, all transistors are cut off because $V_{BE} < 0.6$ V. This causes the output of the circuit to be high, approaching the value of supply voltage V_{CC}. This confirms the conditions stated in Fig. 10-2 for the NOR gate. Note that the noise margin for low signal input is $0.6 - 0.2 = 0.4$ V.

The fan-out of the RTL gate is limited by the value of the output voltage when high. As the output is loaded with inputs of other gates, more current is consumed by the load. This current must flow through the 640-Ω resistor. A simple calculation (see Problem 10-2) will show that if h_{FE} drops to 20, the output voltage drops to about 1 V when the fan-out is 5. Any voltage below 1 V in the output may not drive the next transistor into saturation as required. The power dissipation of the RTL gate is about 12 mW and the propagation delay averages 25 ns.

DTL Basic Gates

The basic circuit in the DTL digital logic family is the NAND gate shown in Fig. 10-9. Each input is associated with one diode. The diodes and the 5-kΩ resistor form an AND gate. The transistor serves as a current amplifier while inverting the digital signal. The two voltage levels are 0.2 V for the low level and between 4 and 5 V for the high level.

The analysis of the DTL gate should conform to the conditions listed in Fig. 10-1 for the NAND gate. If any input of the gate is low at 0.2 V, the corresponding input diode conducts current through V_{CC} and the 5-kΩ resistor into the input node. The voltage at point P is equal to the input voltage of 0.2 V plus a diode drop of 0.7 V, for a total of 0.9 V. In order for the transistor to start conducting, the voltage at point P must overcome a potential of one V_{BE} drop in $Q1$ plus two diode drops across $D1$ and $D2$, or $3 \times 0.6 = 1.8$ V. Since the voltage at P is maintained at 0.9 V by the input conducting diode, the transistor is cut off and the output voltage is high at 5 V.

If all inputs of the gate are high, the transistor is driven into the saturation region.

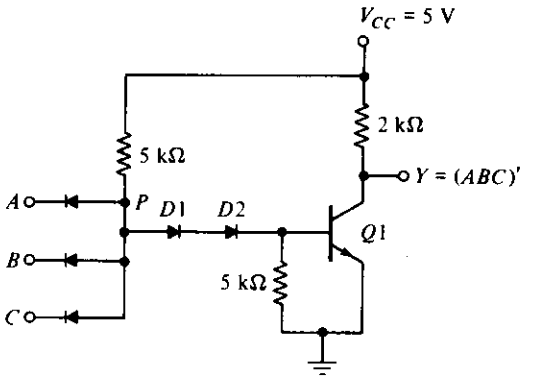


FIGURE 10-9
DTL basic NAND gate

The voltage at P now is equal to V_{BE} plus the two diode drops across $D1$ and $D2$, or $0.7 \times 3 = 2.1$ V. Since all inputs are high at 5 V and $V_P = 2.1$ V, the input diodes are reverse biased and off. The base current is equal to the difference of currents flowing in the two 5-kΩ resistors and is sufficient to drive the transistor into saturation (see Problem 10-3). With the transistor saturated, the output drops to V_{CE} of 0.2 V, which is the low level for the gate.

The power dissipation of a DTL gate is about 12 mW and the propagation delay averages 30 ns. The noise margin is about 1 V and a fan-out as high as 8 is possible. The fan-out of the DTL gate is limited by the maximum current that can flow in the collector of the saturated transistor (see Problem 10-4).

The fan-out of a DTL gate may be increased by replacing one of the diodes in the base circuit with a transistor, as shown in Fig. 10-10. Transistor $Q1$ is maintained in

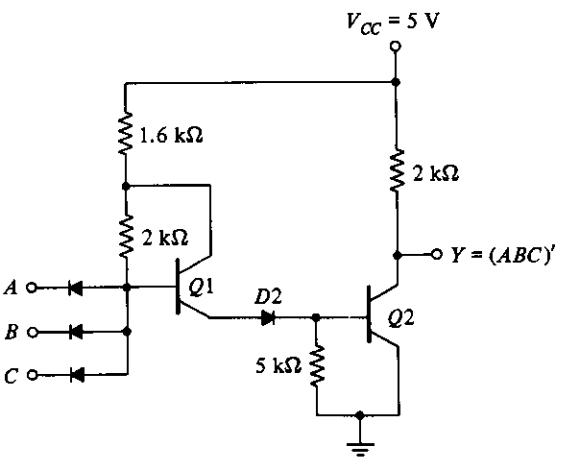


FIGURE 10-10
Modified DTL gate

the active region when output transistor $Q2$ is saturated. As a consequence, the modified circuit can supply a larger amount of base current to the output transistor. The output transistor can now draw a larger amount of collector current before it goes out of saturation. Part of the collector current comes from the conducting diodes in the loading gates when $Q2$ is saturated. Thus, an increase in allowable collector saturated current allows more loads to be connected to the output, which increases the fan-out capability of the gate.

10-5 TRANSISTOR-TRANSISTOR LOGIC (TTL)

The original basic TTL gate was a slight improvement over the DTL gate. As the TTL technology progressed, additional improvements were added to the point where this logic family became the most widely used family in the design of digital systems. There are several subfamilies or series of the TTL technology. The names and characteristics of seven TTL series appear in Table 10-2. Commercial TTL ICs have a number designation that starts with 74 and follows with a suffix that identifies the series type. Examples are 7404, 74S86, and 74ALS161. Fan-out, power dissipation and propagation delay were defined in Section 10-2. The speed–power product is an important parameter for comparing the various TTL series. This is the product of the propagation delay and power dissipation and is measured in picojoules (pJ). A low value for this parameter is desirable, because it indicates that a given propagation delay can be achieved without excessive power dissipation, and vice versa.

The standard TTL gate was the first version in the TTL family. This basic gate was then designed with different resistor values to produce gates with lower power dissipation or with higher speed. The propagation delay of a transistor circuit that goes into saturation depends mostly on two factors: storage time and *RC* time constants. Reducing the storage time decreases the propagation delay. Reducing resistor values in the circuit reduces the *RC* time constants and decreases the propagation delay. Of course, the trade-off is higher power dissipation because lower resistances draw more current

TABLE 10-2
TTL Series and Their Characteristics

TTL Series Name	Prefix	Fan-out	Power Dissipation (mW)	Propagation Delay (ns)	Speed–Power Product (pJ)
Standard	74	10	10	9	90
Low-power	74L	20	1	33	33
High-speed	74H	10	22	6	132
Schottky	74S	10	19	3	57
Low-power Schottky	74LS	20	2	9.5	19
Advanced Schottky	74AS	40	10	1.5	15
Advanced low-power Schottky	74ALS	20	1	4	4

from the power supply. The speed of the gate is inversely proportional to the propagation delay.

In the low-power TTL gate, the resistor values are higher than in the standard gate to reduce the power dissipation, but the propagation delay is increased. In the high-speed TTL gate, resistor values are lowered to reduce the propagation delay, but the power dissipation is increased. The Schottky TTL gate was the next improvement in the technology. The effect of the Schottky transistor is to remove the storage time delay by preventing the transistor from going into saturation. This series increases the speed of operation without an excessive increase in power dissipation. The low-power Schottky TTL sacrifices some speed for reduced power dissipation. It is equal to the standard TTL in propagation delay, but has only one-fifth the power dissipation. Recent innovations have led to the development of the advanced Schottky series. It provides an improvement in propagation delay over the Schottky series and also lowers the power dissipation. The advanced low-power Schottky has the lowest speed–power product and is the most efficient series. It is replacing all other low-power versions in new designs.

All TTL series are available in SSI and in more complex forms as MSI and LSI components. The differences in the TTL series are not in the digital logic that they perform, but rather in the internal construction of the basic NAND gate. In any case, TTL gates in all the available series come in three different types of output configuration:

1. Open-collector output
2. Totem-pole output
3. Three-state (or tristate) output

These three types of outputs will be considered in conjunction with the circuit description of the basic TTL gate.

Open-Collector Output Gate

The basic TTL gate shown in Fig. 10-11 is a modified circuit of the DTL gate. The multiple emitters in transistor $Q1$ are connected to the inputs. These emitters behave most of the time like the input diodes in the DTL gate since they form a *pn* junction with their common base. The base–collector junction of $Q1$ acts as another *pn* junction diode corresponding to $D1$ in the DTL gate (see Fig. 10-5). Transistor $Q2$ replaces the second diode, $D2$, in the DTL gate. The output of the TTL gate is taken from the open collector of $Q3$. A resistor connected to V_{CC} must be inserted external to the IC package for the output to "pull up" to the high voltage level when $Q3$ is off; otherwise, the output acts as an open circuit. The reason for not providing the resistor internally will be discussed later.

The two voltage levels of the TTL gate are 0.2 V for the low level and from 2.4 to 5 V for the high level. The basic circuit is a NAND gate. If any input is low, the corresponding base–emitter junction in $Q1$ is forward biased. The voltage at the base of $Q1$ is equal to the input voltage of 0.2 V plus a V_{BE} drop of 0.7 or 0.9 V. In order for $Q3$ to start conducting, the path from $Q1$ to $Q3$ must overcome a potential of one diode drop

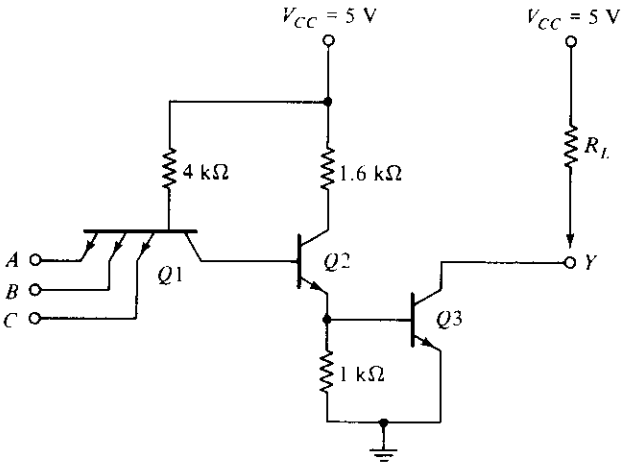


FIGURE 10-11
Open-collector TTL gate

in the base–collector *pn* junction of $Q1$ and two V_{BE} drops in $Q2$ and $Q3$, or $3 \times 0.6 = 1.8$ V. Since the base of $Q1$ is maintained at 0.9 V by the input signal, the output transistor cannot conduct and is cut off. The output level will be high if an external resistor is connected between the output and V_{CC} (or an open circuit if a resistor is not used).

If all inputs are high, both $Q2$ and $Q3$ conduct and saturate. The base voltage of $Q1$ is equal to the voltage across its base–collector *pn* junction plus two V_{BE} drops in $Q2$ and $Q3$, or about $0.7 \times 3 = 2.1$ V. Since all inputs are high and greater than 2.4 V, the base–emitter junctions of $Q1$ are all reverse biased. When output transistor $Q3$ saturates (provided it has a current path), the output voltage goes low to 0.2 V. This confirms the conditions of a NAND operation.

In this analysis, we said that the base–collector junction of $Q1$ acts like a *pn* diode junction. This is true in the steady-state condition. However, during the turn-off transition, $Q1$ does exhibit transistor action, resulting in a reduction in propagation delay. When all inputs are high and then one of the inputs is brought to a low level, both $Q2$ and $Q3$ start turning off. At this time, the collector junction of $Q1$ is reverse biased and the emitter is forward biased; so transistor $Q1$ goes momentarily into the active region. The collector current of $Q1$ comes from the base of $Q2$ and quickly removes the excess charge stored in $Q2$ during its previous saturation state. This causes a reduction in the storage time of the circuit as compared to the DTL type of input. The result is a reduction of the turn-off time of the gate.

The open-collector TTL gate will operate without the external resistor when connected to inputs of other TTL gates, although this is not recommended because of the low noise immunity encountered. Without an external resistor, the output of the gate will be an open circuit when $Q3$ is off. An open circuit to an input of a TTL gate behaves as if it has a high-level input (but a small amount of noise can change this to a

low level). When $Q3$ conducts, its collector will have a current path supplied by the input of the loading gate through V_{CC}, the 4-kΩ resistor, and the forward-biased base-emitter junction.

Open-collector gates are used in three major applications: driving a lamp or relay, performing wired logic, and for the construction of a common-bus system. An open-collector output can drive a lamp placed in its output through a limiting resistor. When the output is low, the saturated transistor $Q3$ forms a path for the current that turns the lamp on. When the output transistor is off, the lamp turns off because there is no path for the current.

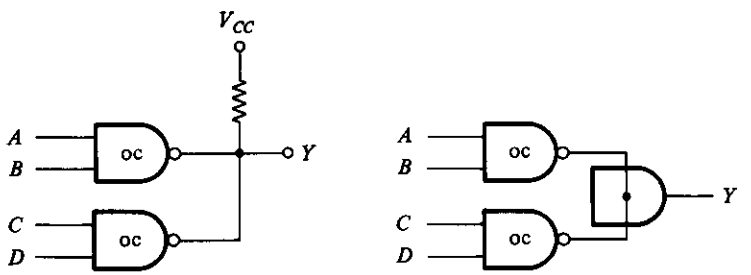
If the outputs of several open-collector TTL gates are tied together with a single external resistor, a wired-AND logic is performed. Remember that a positive-logic AND function gives a high level only if all variables are high; otherwise, the function is low. With outputs of open-collector gates connected together, the common output is high only when all output transistors are off (or high). If an output transistor conducts, it forces the output to the low state.

The wired logic performed with open-collector TTL gates is depicted in Fig. 10-12. The physical wiring in (a) shows how the outputs must be connected to a common resistor. The graphic symbol for such a connection is demonstrated in (b). The AND function formed by connecting together the two outputs is called a wired-AND function. The AND gate is drawn with the lines going through the center of the gate to distinguish it from a conventional gate. The wired-AND gate is not a physical gate, but only a symbol to designate the function obtained from the indicated connection. The Boolean function obtained from the circuit of Fig. 10-12 is the AND operation between the outputs of the two NAND gates:

$$Y = (AB)' \cdot (CD)' = (AB + CD)'$$

The second expression is preferred since it shows an operation commonly referred to as an AND-OR-INVERT function (see Section 3-7).

Open-collector gates can be tied together to form a common bus. At any time, all gate outputs tied to the bus, except one, must be maintained in their high state. The se-



(a) Physical connection (b) Wired-logic graphic symbol

FIGURE 10-12
Wired-AND of two open-collector (oc) gates, $Y = (AB + CD)'$

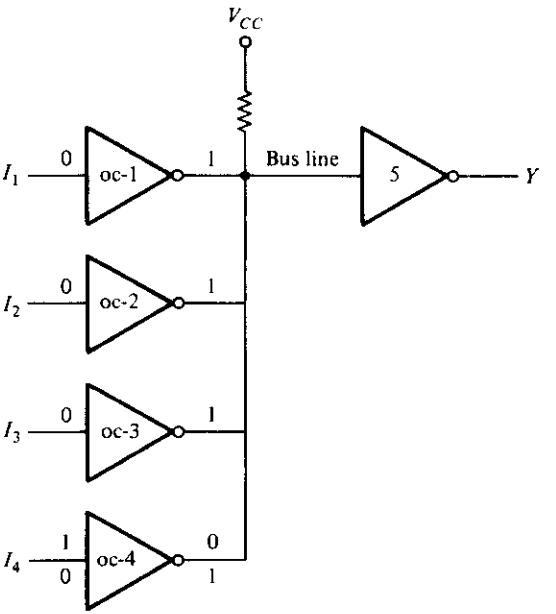


FIGURE 10-13
Open-collector gates forming a common bus line

lected gate may be either in the high or low state, depending on whether we want to transmit a 1 or 0 on the bus. Control circuits must be used to select the particular gate that drives the bus at any given time.

Figure 10-13 demonstrates the connection of four sources tied to a common bus line. Each of the four inputs drives an open-collector inverter, and the outputs of the inverters are tied together to form a single bus line. The figure shows that three of the inputs are 0, which produces a 1 or high level on the bus. The fourth input, I_4, can now transmit information through the common-bus line into inverter 5. Remember that an AND operation is performed in the wired logic. If $I_4 = 1$, the output of gate 4 is 0 and the wired-AND operation produces a 0. If $I_4 = 0$, the output of gate 4 is 1 and the wired-AND operation produces a 1. Thus, if all other outputs are maintained at 1, the selected gate can transmit its value through the bus. The value transmitted is the complement of I_4, but inverter 5 in the receiving end can easily invert this signal again to make $Y = I_4$.

Totem-Pole Output

The output impedance of a gate is normally a resistive plus a capacitive load. The capacitive load consists of the capacitance of the output transistor, the capacitance of the fan-out gates, and any stray wiring capacitance. When the output changes from the low to the high state, the output transistor of the gate goes from saturation to cutoff and the

total load capacitance, C, charges exponentially from the low to the high voltage level with a time constant equal to RC. For the open-collector gate, R is the external resistor marked R_L. For a typical operating value of $C = 15$ pF and $R_L = 4$ kΩ, the propagation delay of a TTL open-collector gate during the turn-off time is 35 ns. With an *active pull-up* circuit replacing the passive pull-up resistor R_L, the propagation delay is reduced to 10 ns. This configuration, shown in Fig. 10-14, is called a *totem-pole* output because transistor $Q4$ "sits" upon $Q3$.

The TTL gate with the totem-pole output is the same as the open-collector gate, except for the output transistor $Q4$ and the diode $D1$. When the output Y is in the low state, $Q2$ and $Q3$ are driven into saturation as in the open-collector gate. The voltage in the collector of $Q2$ is $V_{BE}(Q3) + V_{CE}(Q2)$ or $0.7 + 0.2 = 0.9$ V. The output $Y = V_{CE}(Q3) = 0.2$ V. Transistor $Q4$ is cutoff because its base must be one V_{BE} drop plus one diode drop, or $2 \times 0.6 = 1.2$ V, to start conducting. Since the collector of $Q2$ is connected to the base of $Q4$, the latter's voltage is only 0.9 V instead of the required 1.2 V, and so $Q4$ is cut off. The reason for placing the diode in the circuit is to provide a diode drop in the output path and thus ensure that $Q4$ is cut off when $Q3$ is saturated.

When the output changes to the high state because one of the inputs drops to the low state, transistors $Q2$ and $Q3$ go into cutoff. However, the output remains momentarily low because the voltages across the load capacitance cannot change instantaneously. As soon as $Q2$ turns off, $Q4$ conducts because its base is connected to V_{CC} through the 1.6-kΩ resistor. The current needed to charge the load capacitance causes $Q4$ to momentarily saturate, and the output voltage rises with a time constant RC. But R in this case is equal to 130 Ω, plus the saturation resistance of $Q4$, plus the resistance of the diode, for a total of approximately 150 Ω. This value of R is much smaller than the

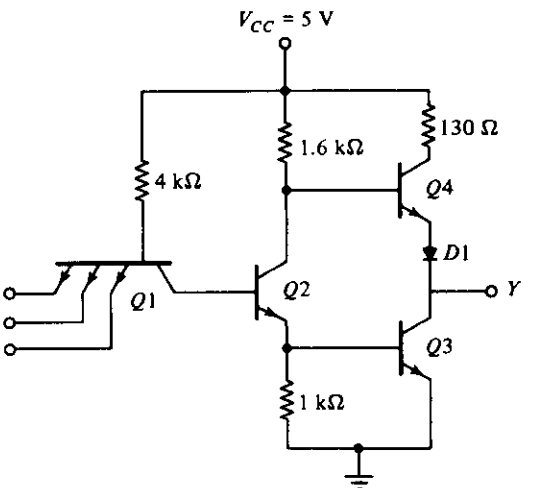


FIGURE 10-14
TTL gate with totem-pole output

passive pull-up resistance used in the open-collector circuit. As a consequence, the transition from the low to high level is much faster.

As the capacitive load charges, the output voltage rises and the current in $Q4$ decreases, bringing the transistor into the active region. Thus, in contrast to the other transistors, $Q4$ is in the *active* region when in a steady-state condition. The final value of the output voltage is then 5 V, minus a V_{BE} drop in $Q4$, minus a diode drop in $D1$ to about 3.6 V. Transistor $Q3$ goes into cutoff very fast, but during the initial transition time, both $Q3$ and $Q4$ are on and a peak current is drawn from the power supply. This current spike generates noise in the power-supply distribution system. When the change of state is frequent, the transient-current spikes increase the power-supply current requirement and the average power dissipation of the circuit increases.

The wired-logic connection is not allowed with totem-pole output circuits. When two totem-poles are wired together with the output of one gate high and the output of the second gate low, the excessive amount of current drawn can produce enough heat to damage the transistors in the circuit (see Problem 10-7). Some TTL gates are constructed to withstand the amount of current that flows under this condition. In any case, the collector current in the low gate may be high enough to move the transistor into the active region and produce an output voltage in the wired connection greater than 0.8 V, which is not a valid binary signal for TTL gates.

Schottky TTL Gate

As mentioned before, a reduction in storage time results in a reduction of propagation delay. This is because the time needed for a transistor to come out of saturation delays the switching of the transistor from the on condition to the off condition. Saturation can be eliminated by placing a Schottky diode between the base and collector of each saturated transistor in the circuit. The Schottky diode is formed by the junction of a metal and semiconductor, in contrast to a conventional diode, which is formed by the junction of p-type and n-type semiconductor material. The voltage across a conducting Schottky diode is only 0.4 V, as compared to 0.7 V in a conventional diode. The presence of a Schottky diode between the base and collector prevents the transistor from going into saturation. The resulting transistor is called a *Schottky transistor*. The use of Schottky transistors in a TTL decreases the propagation delay without a sacrifice of power dissipation.

The Schottky TTL gate is shown in Fig. 10-15. Note the special symbol used for the Schottky transistors and diodes. The diagram shows all transistors to be of the Schottky type except $Q4$. An exception is made of $Q4$ since it does not saturate, but stays in the active region. Note also that resistor values have been reduced to further decrease the propagation delay.

In addition to using Schottky transistors and lower resistor values, the circuit of Fig. 10-15 includes other modifications not available in the standard gate of Fig. 10-14. Two new transistors, $Q5$ and $Q6$ have been added, and Schottky diodes are inserted between each input terminal and ground. There is no diode in the totem-pole circuit.

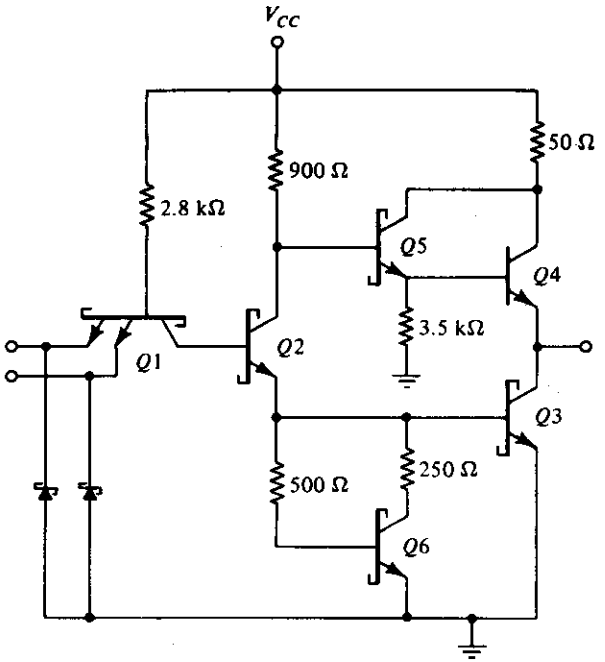


FIGURE 10-15
Schottky TTL gate

However, the new combination of $Q5$ and $Q4$ still gives the two V_{BE} drops necessary to prevent $Q4$ from conducting when the output is low. This combination comprises a double emitter-follower called a *Darlington pair*. The Darlington pair provides a very high current gain and extremely low resistance. This is exactly what is needed during the low-to-high swing of the output, resulting in a decrease of propagation delay.

The diodes in each input shown in the circuit help clamp any ringing that may occur in the input lines. Under transient switching conditions, signal lines appear inductive; this, along with stray capacitance, causes signals to oscillate or "ring." When the output of a gate switches from the high to the low state, the ringing waveform at the input may have excursions below ground as great as 2–3 V, depending on line length. The diodes connected to ground help clamp this ringing since they conduct as soon as the negative voltage exceeds 0.4 V. When the negative excursion is limited, the positive swing is also reduced. The success of the clamp diodes in limiting line effects has been so successful that all versions of TTL gates use them.

The emitter resistor of $Q2$ in Fig. 10-14 has been replaced in Fig. 10-15 by a circuit consisting of transistor $Q6$ and two resistors. The effect of this circuit is to reduce the turn-off current spikes discussed previously. The analysis of this circuit, which helps to reduce the propagation time of the gate, is too involved to present in this brief discussion.

Three-State Gate

As mentioned earlier, the outputs of two TTL gates with totem-pole structures cannot be connected together as in open-collector outputs. There is, however, a special type of totem-pole gate that allows the wired connection of outputs for the purpose of forming a common-bus system. When a totem-pole output TTL gate has this property, it is called a *three-state* (or tristate) gate.

A three-state gate exhibits three output states: (1) a low-level state when the lower transistor in the totem-pole is on and the upper transistor is off, (2) a high-level state when the upper transistor in the totem-pole is on and the lower transistor is off, and (3) a third state when both transistors in the totem-pole are off. The third state provides an open circuit or high-impedance state that allows a direct wire connection of many outputs to a common line. Three-state gates eliminate the need for open-collector gates in bus configurations.

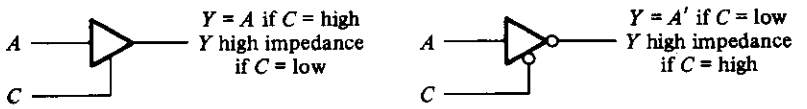
Figure 10-16(a) shows the graphic symbol of a three-state buffer gate. When the control input C is high, the gate is enabled and behaves like a normal buffer with the output equal to the input binary value. When the control input is low, the output is an open circuit, which gives a high impedance (the third state) regardless of the value of input A. Some three-state gates produce a high-impedance state when the control input is high. This is shown symbolically in Fig. 10-16(b). Here we have two small circles, one for the inverter output and the other to indicate that the gate is enabled when C is low.

The circuit diagram of the three-state inverter is shown in Fig. 10-16(c). Transistors $Q6$, $Q7$, and $Q8$ associated with the control input form a circuit similar to the open-collector gate. Transistors $Q1$–$Q5$, associated with the data input, form a totem-pole TTL circuit. The two circuits are connected together through diode $D1$. As in an open-collector circuit, transistor $Q8$ turns off when the control input at C is in the low-level state. This prevents diode $D1$ from conducting, and also, the emitter in $Q1$ connected to $Q8$ has no conduction path. Under this condition, transistor $Q8$ has no effect on the operation of the gate and the output in Y depends only on the data input at A.

When the control input is high, transistor $Q8$ turns on, and the current flowing from V_{CC} through diode $D1$ causes transistor $Q8$ to saturate. The voltage at the base of $Q5$ is now equal to the voltage across the saturated transistor, $Q8$, plus one diode drop, or 0.9 V. This voltage turns off $Q5$ and $Q4$ since it is less than two V_{BE} drops. At the same time, the low input to one of the emitters of $Q1$ forces transistor $Q3$ (and $Q2$) to turn off. Thus, both $Q3$ and $Q4$ in the totem-pole are turned off and the output of the circuit behaves like an open circuit with a very high output impedance.

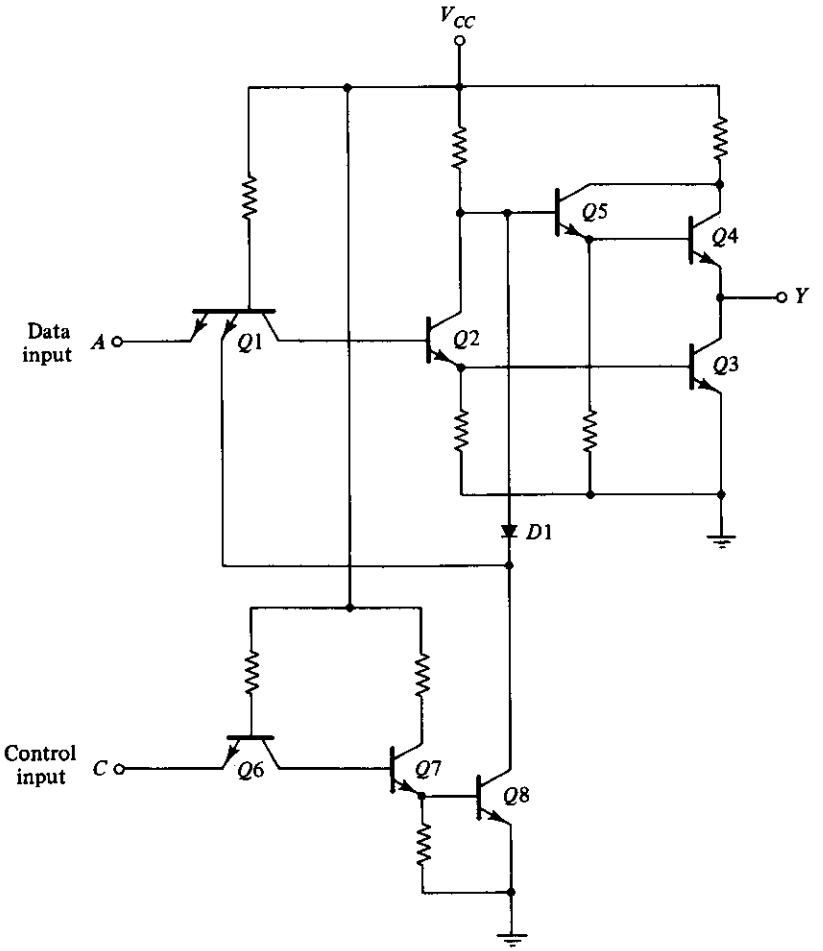
A three-state bus is created by wiring several three-state outputs together. At any given time, only one control input is enabled while all other outputs are in the high-impedance state. The single gate not in a high-impedance state can transmit binary information through the common bus. Extreme care must be taken that all except one of the outputs are in the third state; otherwise, we have the undesirable condition of having two active totem-pole outputs connected together.

An important feature of most three-state gates is that the output enable delay is longer than the output disable delay. If a control circuit enables one gate and disables



(a) Three-state buffer gate

(b) Three-state inverter gate



(c) Circuit diagram for the three-state inverter of (b)

FIGURE 10-16
Three-state TTL gate

another at the same time, the disabled gate enters the high-impedance state before the other gate is enabled. This eliminates the situation of both gates being active at the same time.

There is a very small leakage current associated with the high-impedance condition in a three-state gate. Nevertheless, this current is so small that as many as 100 three-state outputs can be connected together to form a common-bus line.

10-6 EMITTER-COUPLED LOGIC (ECL)

Emitter-coupled logic (ECL) is a nonsaturated digital logic family. Since transistors do not saturate, it is possible to achieve propagation delays of 2 ns and even below 1 ns. This logic family has the lowest propagation delay of any family and is used mostly in systems requiring very high-speed operation. Its noise immunity and power dissipation, however, are the worst of all the logic families available.

A typical basic circuit of the ECL family is shown in Fig. 10-17. The outputs

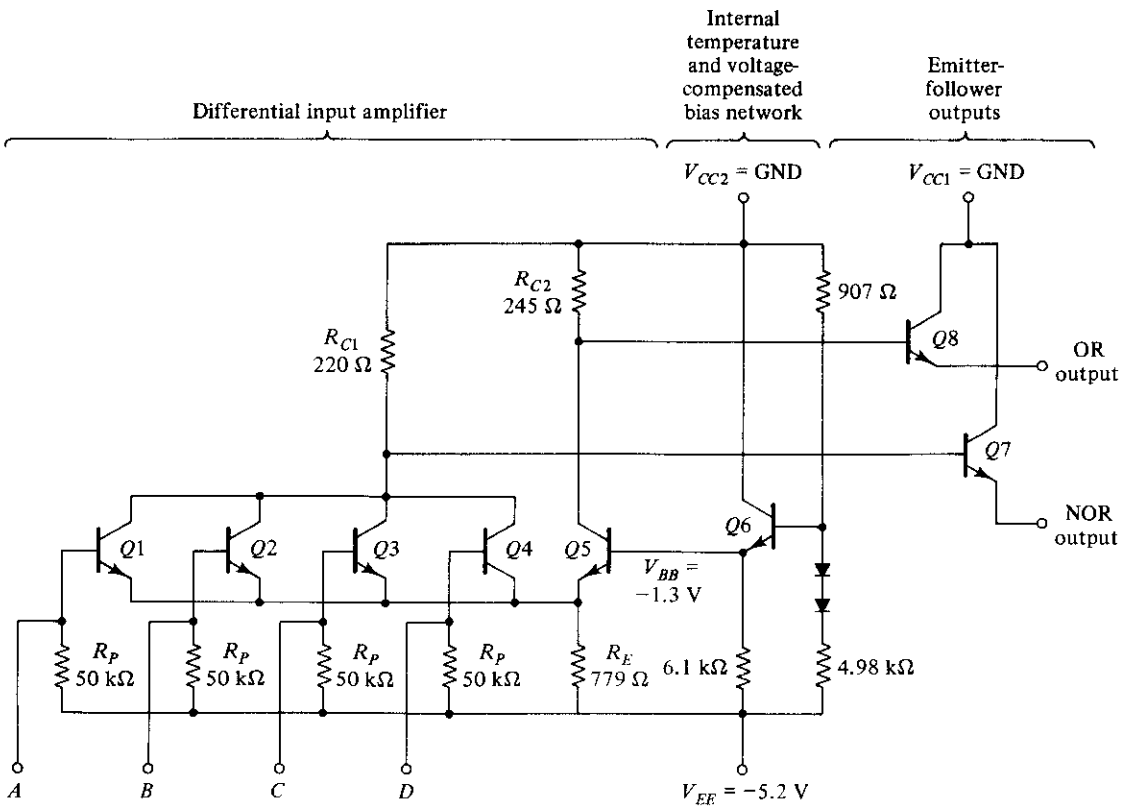


FIGURE 10-17
ECL basic gate

provide both the OR and NOR functions. Each input is connected to the base of a transistor. The two voltage levels are about -0.8 V for the high state and about -1.8 V for the low state. The circuit consists of a differential amplifier, a temperature- and voltage-compensated bias network, and an emitter-follower output. The emitter outputs require a pull-down resistor for current to flow. This is obtained from the input resistor, R_P, of another similar gate or from an external resistor connected to a negative voltage supply.

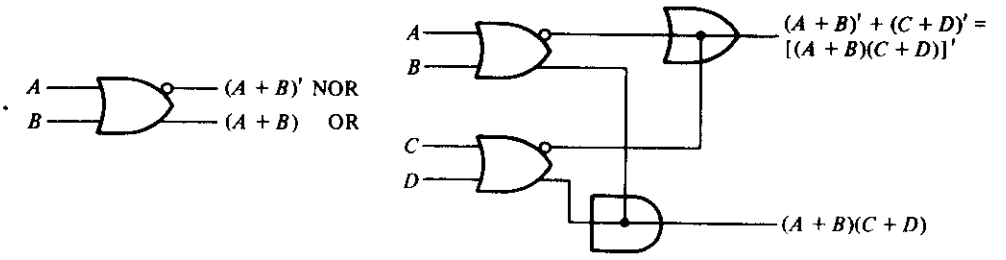
The internal temperature- and voltage-compensated bias circuit supplies a reference voltage to the differential amplifier. Bias voltage V_{BB} is set at -1.3 V, which is the midpoint of the signal logic swing. The diodes in the voltage divider, together with $Q6$, provide a circuit that maintains a constant V_{BB} value despite changes in temperature or supply voltage. Any one of the power supply inputs could be used as ground. However, the use of the V_{CC} node as ground and V_{EE} at -5.2 V results in best noise immunity.

If any input in the ECL gate is high, the corresponding transistor is turned on and $Q5$ is turned off. An input of -0.8 V causes the transistor to conduct and places -1.6 V on the emitters of all transistors (V_{BE} drop in ECL transistors is 0.8 V). Since $V_{BB} = -1.3$ V, the base voltage of $Q5$ is only 0.3 V more positive than its emitter. $Q5$ is cut off because its V_{BE} voltage needs at least 0.6 V to start conducting. The current in resistor R_{C2} flows into the base of $Q8$ (provided there is a load resistor). This current is so small that only a negligible voltage drop occurs across R_{C2}. The OR output of the gate is one V_{BE} drop below ground, or -0.8 V, which is the high state. The current flowing through R_{C1} and the conducting transistor causes a drop of about 1 V below ground (see Problem 10-9). The NOR output is one V_{BE} drop below this level, or at -1.8 V, which is the low state.

If all inputs are at the low level, all input transistors turn off and $Q5$ conducts. The voltage in the common-emitter node is one V_{BE} drop below V_{BB}, or -2.1 V. Since the base of each input is at a low level of -1.8 V, each base–emitter junction has only 0.3 V and all input transistors are cut off. R_{C2} draws current through $Q5$ that results in a voltage drop of about 1 V, making the OR output one V_{BE} drop below this, at -1.8 V or the low level. The current in R_{C1} is negligible and the NOR output is one V_{BE} drop below ground, at -0.8 V or the high level. This verifies the OR and NOR operations of the circuit.

The propagation delay of the ECL gate is 2 ns, and the power dissipation is 25 mW. This gives a speed–power product of 50, which is about the same as for the Schottky TTL. The noise margin is about 0.3 V and not as good as in the TTL gate. High fan-out is possible in the ECL gate because of the high input impedance of the differential amplifier and the low output impedance of the emitter-follower. Because of the extreme high speed of the signals, external wires act like transmission lines. Except for very short wires of a few centimeters, ECL outputs must use coaxial cables with a resistor termination to reduce line reflections.

The graphic symbol for the ECL gate is shown in Fig. 10-18(a). Two outputs are available: one for the NOR function and the other for the OR function. The outputs of two or more ECL gates can be connected together to form wired logic. As shown in



(a) Single gate (b) Wired combination of two gates

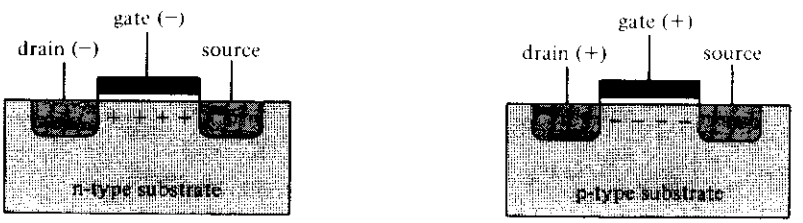
FIGURE 10-18
Graphic symbols of ECL gates

Fig. 10-18(b), an *external* wired connection of two NOR outputs produces a wired-OR function. An *internal* wired connection of two OR outputs is employed in some ECL ICs to produce a wired-AND (sometimes called dot-AND) logic. This property may be utilized when ECL gates are used to form the OR-AND-INVERT and the OR-AND functions.

10-7 METAL-OXIDE SEMICONDUCTOR (MOS)

The field-effect transistor (FET) is a unipolar transistor, since its operation depends on the flow of only one type of carrier. There are two types of field-effect transistors: the junction field-effect transistor (JFET) and the metal-oxide semi-conductor (MOS). The former is used in linear circuits and the latter in digital circuits. MOS transistors can be fabricated in less area than bipolar transistors.

The basic structure of the MOS transistor is shown in Fig. 10-19. The p-channel MOS consists of a lightly doped substrate of n-type silicon material. Two regions are heavily doped by diffusion with p-type impurities to form the *source* and *drain*. The region between the two p-type sections serves as the *channel*. The *gate* is a metal plate separated from the channel by an insulated dielectric of silicon dioxide. A negative



(a) p-channel (b) n-channel

FIGURE 10-19
Basic structure of MOS transistor

voltage (with respect to the substrate) at the gate terminal causes an induced electric field in the channel that attracts p-type carriers from the substrate. As the magnitude of the negative voltage on the gate increases, the region below the gate accumulates more positive carriers, the conductivity increases, and current can flow from source to drain provided a voltage difference is maintained between these two terminals.

There are four basic types of MOS structures. The channel can be a p- or n-type, depending on whether the majority carriers are holes or electrons. The mode of operation can be enhancement or depletion, depending on the state of the channel region at zero gate voltage. If the channel is initially doped lightly with p-type impurity (diffused channel), a conducting channel exists at zero gate voltage and the device is said to operate in the *depletion* mode. In this mode, current flows unless the channel is depleted by an applied gate field. If the region beneath the gate is left initially uncharged, a channel must be induced by the gate field before current can flow. Thus, the channel current is enhanced by the gate voltage and such a device is said to operate in the *enhancement* mode.

The source is the terminal through which the majority carriers enter the bar. The drain is the terminal through which the majority carriers leave the bar. In a p-channel MOS, the source terminal is connected to the substrate and a negative voltage is applied to the drain terminal. When the gate voltage is above a threshold voltage V_T (about -2 V), no current flows in the channel and the drain-to-source path is like an open circuit. When the gate voltage is sufficiently negative below V_T, a channel is formed and p-type carriers flow from source to drain. P-type carriers are positive and correspond to a positive current flow from source to drain.

In the n-channel MOS, the source terminal is connected to the substrate and a positive voltage is applied to the drain terminal. When the gate voltage is below the threshold voltage V_T (about 2 V), no current flows in the channel. When the gate voltage is sufficiently positive above V_T to form the channel, n-type carriers flow from source to drain. n-type carriers are negative, which corresponds to a positive current flow from drain to source. The threshold voltage may vary from 1 to 4 V, depending on the particular process used.

The graphic symbols for the MOS transistors are shown in Fig. 10-20. The accepted symbol for the enhancement type is the one with the broken-line connection between source and drain. In this symbol, the substrate can be identified and is shown connected

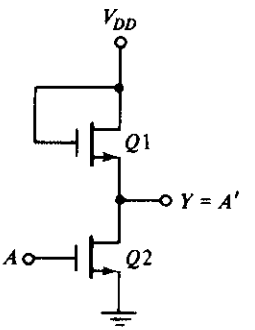
(a) p-channel (b) n-channel

FIGURE 10-20
Symbols for MOS transistors

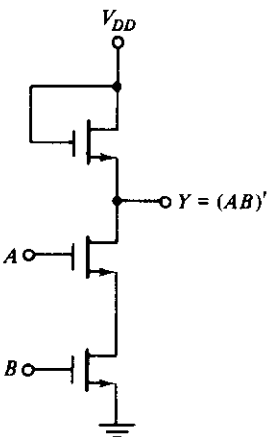
to the source. We will use an alternative symbol that omits the substrate; in this symbol, the arrow is placed in the source terminal to show the direction of *positive* current flow (from source to drain in the p-channel and from drain to source in the n-channel).

Because of the symmetrical construction of source and drain, the MOS transistor can be operated as a bilateral device. Although normally operated so that carriers flow from source to drain, there are circumstances when it is convenient to allow carrier flow from drain to source (see Problem 10-12).

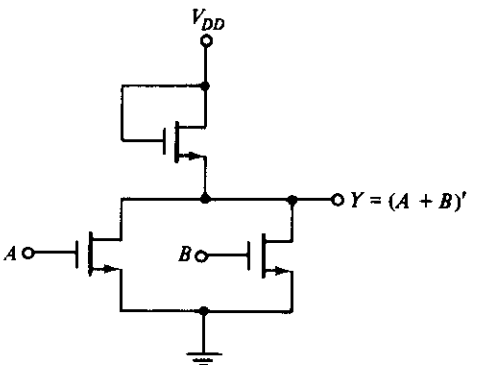
One advantage of the MOS device is that it can be used not only as a transistor, but as a resistor as well. A resistor is obtained from the MOS by permanently biasing the



(a) Inverter



(b) NAND gate



(c) NOR gate

FIGURE 10-21
n-channel MOS logic circuits

gate terminal for conduction. The ratio of the source–drain voltage to the channel current then determines the value of the resistance. Different resistor values may be constructed during manufacturing by fixing the channel length and width of the MOS device.

Three logic circuits using MOS devices are shown in Fig. 10-21. For an n-channel MOS, supply voltage V_{DD} is positive (about 5 V) to allow positive current flow from drain to source. The two voltage levels are a function of the threshold voltage V_T. The low level is anywhere from zero to V_T, and the high level ranges from V_T to V_{DD}. The n-channel gates usually employ positive logic. The p-channel MOS circuits use a negative voltage for V_{DD} to allow positive current flow from source to drain. The two voltage levels are both negative above and below the negative threshold voltage V_T. P-channel gates usually employ negative logic.

The inverter circuit shown in Fig. 10-21(a) uses two MOS devices. $Q1$ acts as the load resistor and $Q2$ as the active device. The load resistor MOS has its gate connected to V_{DD}, thus maintaining it always in the conduction state. When the input voltage is low (below V_T), $Q2$ turns off. Since $Q1$ is always on, the output voltage is at about V_{DD}. When the input voltage is high (above V_T), $Q2$ turns on. Current flows from V_{DD} through the load resistor $Q1$ and into $Q2$. The geometry of the two MOS devices must be such that the resistance of $Q2$, when conducting, is much less than the resistance of $Q1$ to maintain the output Y at a voltage below V_T.

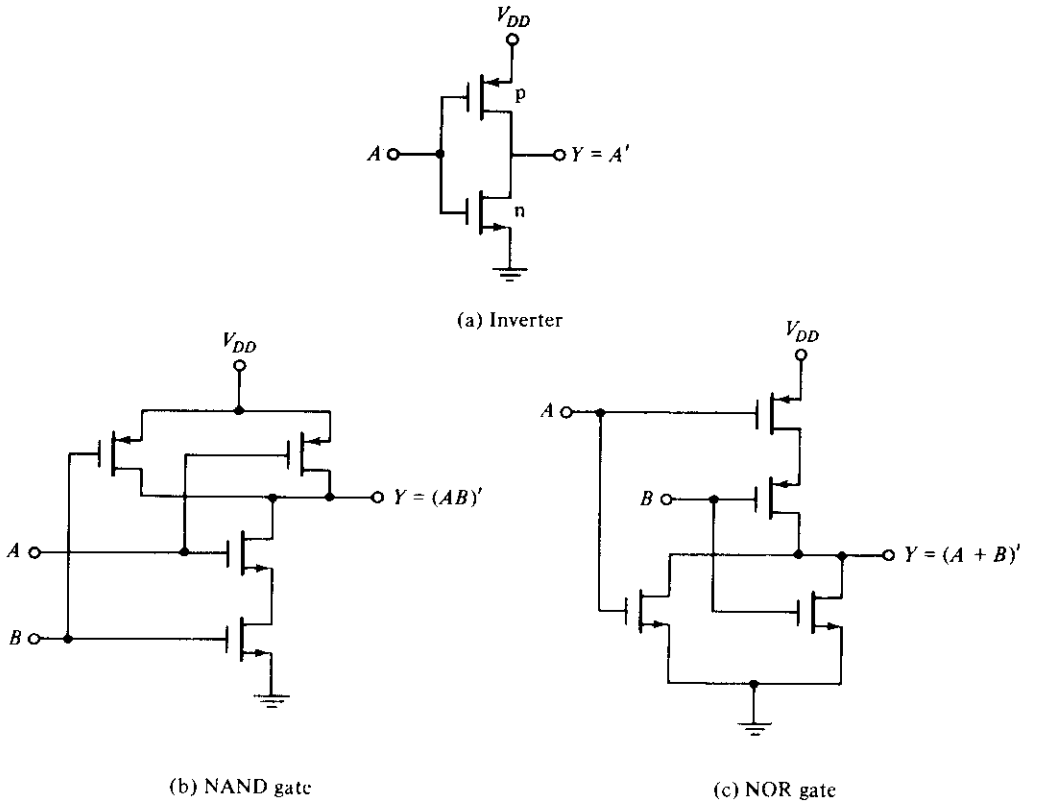
The NAND gate shown in Fig. 10-21(b) uses transistors in series. Inputs A and B must both be high for all transistors to conduct and cause the output to go low. If either input is low, the corresponding transistor is turned off and the output is high. Again, the series resistance formed by the two active MOS devices must be much less than the resistance of the load-resistor MOS. The NOR gate shown in Fig. 10-21(c) uses transistors in parallel. If either input is high, the corresponding transistor conducts and the output is low. If all inputs are low, all active transistors are off and the output is high.

10-8 COMPLEMENTARY MOS (CMOS)

Complementary MOS circuits take advantage of the fact that both n-channel and p-channel devices can be fabricated on the same substrate. CMOS circuits consist of both types of MOS devices interconnected to form logic functions. The basic circuit is the inverter, which consists of one p-channel transistor and one n-channel transistor, as shown in Fig. 10-22(a). The source terminal of the p-channel device is at V_{DD}, and the source terminal of the n-channel device is at ground. The value of V_{DD} may be anywhere from +3 to +18 V. The two voltage levels are 0 V for the low level and V_{DD} for the high level.

To understand the operation of the inverter, we must review the behavior of the MOS transistor from the previous section:

1. The n-channel MOS conducts when its gate-to-source voltage is positive.



(a) Inverter

(b) NAND gate

(c) NOR gate

FIGURE 10-22
CMOS logic circuits

2. The p-channel MOS conducts when its gate-to-source voltage is negative.
3. Either type of device is turned off if its gate-to-source voltage is zero.

Now consider the operation of the inverter. When the input is low, both gates are at zero potential. The input is at $-V_{DD}$ relative to the source of the p-channel device and at 0 V relative to the source of the n-channel device. The result is that the p-channel device is turned on and the n-channel device is turned off. Under these conditions, there is a low-impedance path from V_{DD} to the output and a very high-impedance path from output to ground. Therefore, the output voltage approaches the high level V_{DD} under normal loading conditions. When the input is high, both gates are at V_{DD} and the situation is reversed: The p-channel device is off and the n-channel device is on. The result is that the output approaches the low level of 0 V.

Two other CMOS basic gates are shown in Fig. 10-22. A two-input NAND gate consists of two p-type units in parallel and two n-type units in series, as shown in Fig. 10-22(b). If all inputs are high, both p-channel transistors turn off and both n-channel

transistors turn on. The output has a low impedance to ground and produces a low state. If any input is low, the associated n-channel transistor is turned off and the associated p-channel transistor is turned on. The output is coupled to V_{DD} and goes to the high state. Multiple-input NAND gates may be formed by placing equal numbers of p-type and n-type transistors in parallel and series, respectively, in an arrangement similar to that shown in Fig. 10-22(b).

A two-input NOR gate consists of two n-type units in parallel and two p-type units in series, as shown in Fig. 10-22(c). When all inputs are low, both p-channel units are on and both n-channel units are off. The output is coupled to V_{DD} and goes to the high state. If any input is high, the associated p-channel transistor is turned off and the associated n-channel transistor turns on. This connects the output to ground, causing a low-level output.

CMOS Characteristics

When a CMOS logic circuit is in a static state, its power dissipation is very low. This is because there is always an off transistor in the current path when the state of the circuit is not changing. As a result, a typical CMOS gate has a static power dissipation on the order of 0.01 mW. However, when the circuit is changing state at a rate of 1 MHz, the power dissipation increases to about 1 mW.

CMOS logic is usually specified for a single power-supply operation over the voltage range between 3 and 18 V with a typical V_{DD} value of 5 V. Operating CMOS at a larger value of supply voltage reduces the propagation delay time and improves the noise margin, but the power dissipation is increased. The propagation delay time with $V_{DD} = 5$ V ranges from 8 to 50 ns, depending on the type of CMOS used. The noise margin is usually about 40 percent of the V_{DD} supply voltage. The fan-out of CMOS gates is 50 when operated at a frequency of less than 1 MHz. The fan-out decreases with increase in frequency of operation.

There are several series of the CMOS digital logic family (see Table 2-10). The original design of CMOS ICs is recognized from the 4000 number designation. The 74C series are pin- and function-compatible with TTL devices having the same number. For example, CMOS IC type 74C04 has six inverters with the same pin configuration as TTL type 7404. The performance characteristics of the 74C series are about the same as the 4000 series. The high-speed CMOS 74HC series is an improvement of the 74C series with a tenfold increase in switching speed. The 74HCT series is electrically compatible with TTL ICs. This means that the circuits in this series can be connected to inputs and outputs of TTL ICs without the need of additional interfacing circuits.

The CMOS fabrication process is simpler than TTL and provides a greater packing density. This means that more circuits can be placed on a given area of silicon at a reduced cost per function. This property of CMOS, together with its low power dissipation, excellent noise immunity, and reasonable propagation delay, makes it a strong contender for a popular standard as a digital logic family.

10-9 CMOS TRANSMISSION GATE CIRCUITS

A special CMOS circuit that is not available in the other digital logic families is the *transmission gate*. The transmission gate is essentially an electronic switch that is controlled by an input logic level. It is used for simplifying the construction of various digital components when fabricated with CMOS technology.

Figure 10-23(a) shows the basic circuit of the transmission gate. It consists of one n-channel and one p-channel MOS transistor connected in parallel. The graphic symbol used here is the conventional symbol that shows the substrate, as indicated in Fig. 10-20. The n-channel substrate is connected to ground and the p-channel substrate is connected to V_{DD}. When the N gate is at V_{DD} and the P gate is at ground, both transistors conduct and there is a closed path between input X and output Y. When the N gate is at ground and the P gate at V_{DD}, both transistors are off and there is an open circuit between X and Y. Figure 10-23(b) shows the block diagram of the transmission gate. Note that the terminal of the p-channel gate is marked with the negation small-circle symbol. Figure 10-23(c) demonstrates the behavior of the switch in terms of positive-logic assignment with V_{DD} equivalent to logic-1 and ground equivalent to logic-0.

The transmission gate is usually connected to an inverter, as shown in Fig. 10-24.

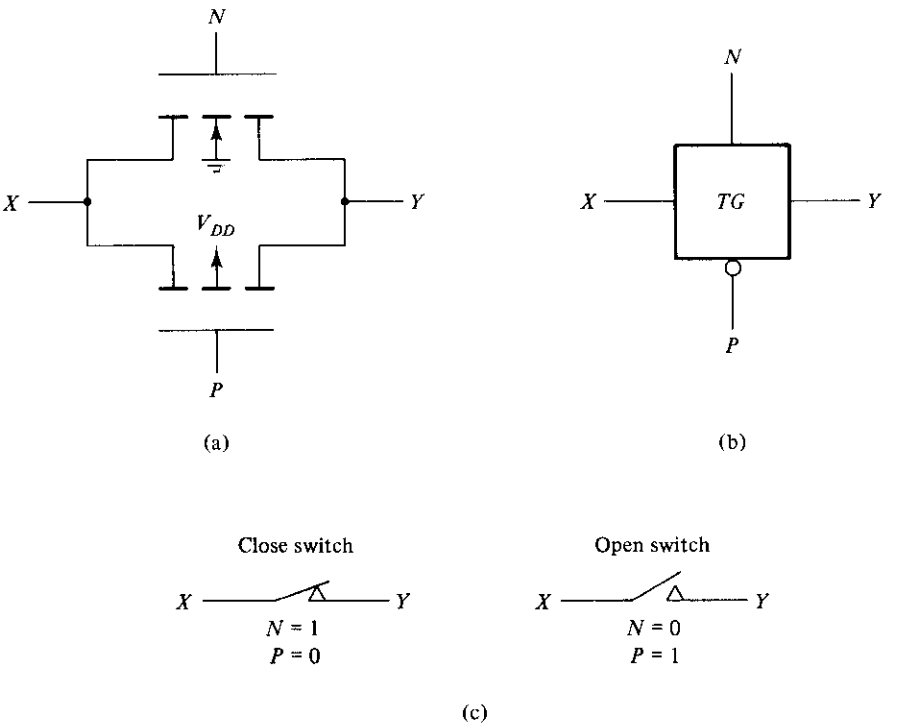


FIGURE 10-23
Transmission gate (TG)

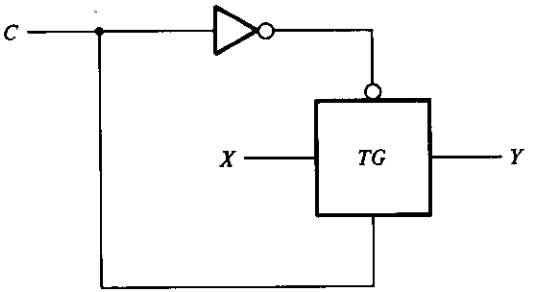
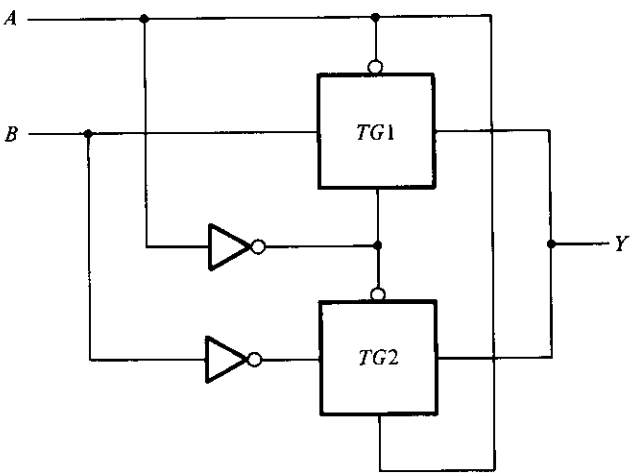


FIGURE 10-24
Bilateral switch

This type of arrangement is referred to as a *bilateral switch*. The control input C is connected directly to the n-channel gate and its inverse to the p-channel gate. When $C = 1$, the switch is closed, producing a path between X and Y. When $C = 0$, the switch is open, disconnecting the path between X and Y.

Various circuits can be constructed using the transmission gate. In order to demonstrate its usefulness as a component in the CMOS family, we will show three circuit examples.

The exclusive-OR gate can be constructed with two transmission gates and two inverters, as shown in Fig. 10-25. Input A controls the paths in the transmission gates and input B is connected to output Y through the gates. When input A is equal to 0, transmission gate $TG1$ is closed and output Y is equal to input B. When input A is equal to 1, $TG2$ is closed and output Y is equal to the complement of input B. This results in the exclusive-OR truth table, as indicated in the table of Fig. 10-25.



A	B	$TG1$	$TG2$	Y
0	0	close	open	0
0	1	close	open	1
1	0	open	close	1
1	1	open	close	0

FIGURE 10-25
Exclusive-OR constructed with transmission gates

Another circuit that can be constructed with transmission gates is the multiplexer. A 4-to-1-line multiplexer implemented with transmission gates is shown in Fig. 10-26. The *TG* circuit provides a transmission path between its horizontal input and output lines when the two vertical control inputs have the value of 1 in the uncircled terminal and 0 in the circled terminal. With an opposite polarity in the control inputs, the path disconnects and the circuit behaves like an open switch. The two selection inputs, S_1 and S_0, control the transmission path in the *TG* circuits. Inside each box is marked the

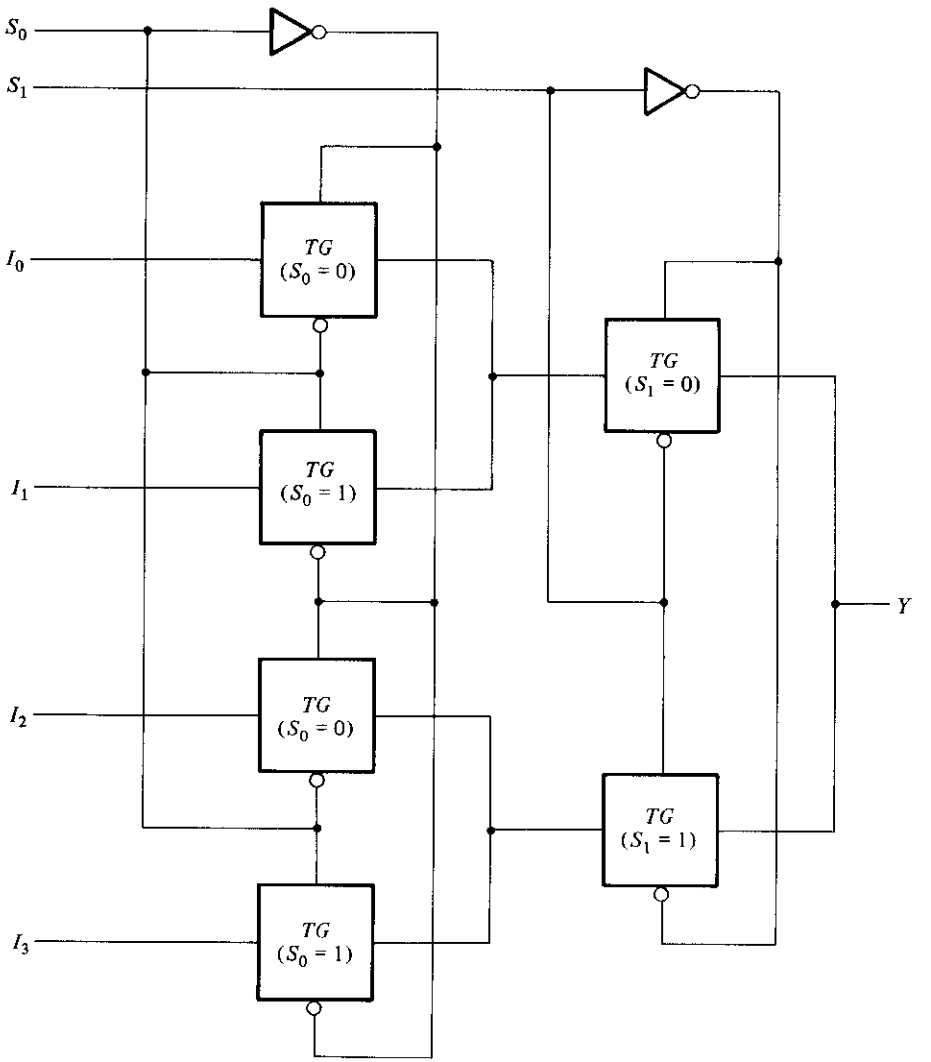


FIGURE 10-26
Multiplexer with transmission gates

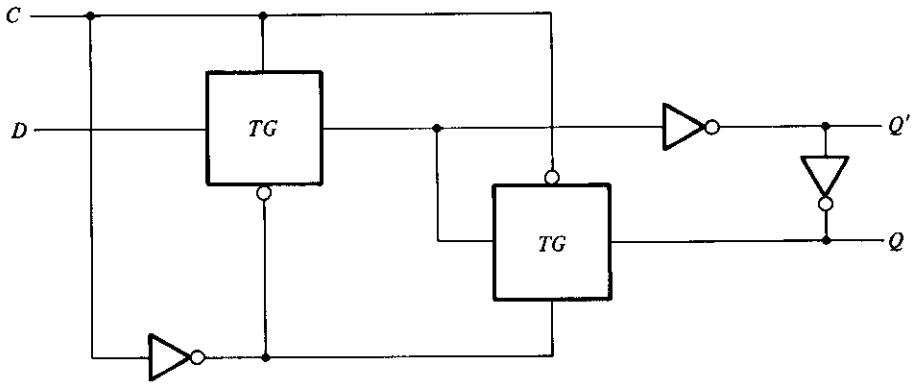


FIGURE 10-27
Gated *D* latch with transmission gates

condition for the transmission gate switch to be closed. Thus, if $S_0 = 0$ and $S_1 = 0$, there is a closed path from input I_0 to output Y through the two *TG*s marked with $S_0 = 0$ and $S_1 = 0$. The other three inputs are disconnected from the output by one of the other *TG* circuits.

The level-sensitive *D* flip-flop commonly referred to as gated *D* latch can be constructed with transmission gates, as shown in Fig. 10-27. The *C* input controls two transmission gates *TG*. When $C = 1$, the *TG* connected to input *D* has a closed path and the one connected to output *Q* has an open path. This produces an equivalent circuit from input *D* through two inverters to output *Q*. Thus, the output follows the data input as long as *C* remains active. When *C* switches to 0, the first *TG* disconnects input *D* from the circuit and the second *TG* produces a closed path between the two inverters at the output. Thus, the value that was present at input *D* at the time that *C* went from 1 to 0 is retained at the *Q* output.

A master–slave *D* flip-flop can be constructed with two circuits of the type shown in Fig. 10-27. The first circuit is the master and the second is the slave. Thus, a master–slave *D* flip-flop can be constructed with four transmission gates and six inverters.

REFERENCES

1. HODGES, D. A., and H. G. JACKSON, *Analysis and Design of Digital Integrated Circuits*, 2nd Ed. New York: McGraw-Hill, 1988.
2. TAUB, H., and D. SCHILLING, *Digital Integrated Electronics*. New York: McGraw-Hill, 1977.
3. GRINICH, V. H., and H. G. JACKSON, *Introduction to Integrated Circuits*. New York: McGraw-Hill, 1975.
4. TOCCI, R. J., *Digital Systems Principles and Applications*, 4th Ed., Englewood Cliffs, NJ: Prentice-Hall, 1988.
5. *The TTL Data Book*. Dallas: Texas Instruments, 1988.
6. *CMOS Logic Data Book*. Dallas: Texas Intruments, 1984.

7. MORRIS, R. L., and J. R. MILLER, *Designing with TTL Integrated Circuits*. New York: McGraw-Hill, 1971.
8. GLASER, A. B., and G. E. SUBAK-SHARPE, *Integrated Circuit Engineering*. Reading, MA: Addison-Wesley, 1977.
9. HAMILTON, D. J., and W. G. HOWARD, *Basic Integrated Circuit Engineering*. New York: McGraw-Hill, 1975.

PROBLEMS

10-1 The following are the specifications for the Schottky TTL 74S00 quadruple 2-input NAND gates. Calculate the fan-out, power dissipation, propagation delay, and noise margin of the Schottky NAND gate.

Parameter	Name	Value
V_{CC}	Supply voltage	5 V
I_{CCH}	High-level supply current (four gates)	10 mA
I_{CCL}	Low-level supply current (four gates)	20 mA
V_{OH}	High-level output voltage (min)	2.7 V
V_{OL}	Low-level output voltage (max)	0.5 V
V_{IH}	High-level input voltage (min)	2 V
V_{IL}	Low-level input voltage (max)	0.8 V
I_{OH}	High-level output current (max)	1 mA
I_{OL}	Low-level output current (max)	20 mA
I_{IH}	High-level input current (max)	0.05 mA
I_{IL}	Low-level input current (max)	2 mA
t_{PLH}	Low-to-high delay	3 ns
t_{PHL}	High-to-low delay	3 ns

10-2 (a) Determine the high-level output voltage of the RTL gate for a fan-out of 5. (b) Determine the minimum input voltage required to drive an RTL transistor to saturation when $h_{FE} = 20$. (c) From the results in (a) and (b), determine the noise margin of the RTL gate when the input is high and the fan-out is 5.

10-3 Show that the output transistor of the DTL gate of Fig. 10-9 goes into saturation when all inputs are high. Assume that $h_{FE} = 20$.

10-4 Connect the output Y of the DTL gate shown in Fig. 10-9 to N inputs of other similar gates. Assume that the output transistor is saturated and its base current is 0.44 mA. Let $h_{FE} = 20$.

(a) Calculate the current in the 2 kΩ resistor.
(b) Calculate the current coming from each input connected to the gate.
(c) Calculate the total collector current in the output transistor as a function of N.
(d) Find the value of N that will keep the transistor in saturation.
(e) What is the fan-out of the gate?

10-5 Let all inputs in the open-collector TTL gate of Fig. 10-11 be in the high state of 3 V.
(a) Determine the voltages in the base, collector, and emitter of all transistors.
(b) Determine the minimum h_{FE} of $Q2$ that ensures that this transistor saturates.
(c) Calculate the base current of $Q3$.
(d) Assume that the minimum h_{FE} of $Q3$ is 6.18. What is the maximum current that can be tolerated in the collector to ensure saturation of $Q3$?
(e) What is the minimum value of R_L that can be tolerated to ensure saturation of $Q3$?

10-6 (a) Using the actual output transistors of two open-collector TTL gates, show (by means of a truth table) that when connected together to an external resistor and V_{CC}, the wired connection produces an AND function.
(b) Prove that two open-collector TTL inverters when connected together produce the NOR function.

10-7 It was stated in Section 10-5 that totem-pole outputs should not be tied together to form wired logic. To see why this is prohibitive, connect two such circuits together and let the output of one gate be in the high state and the output of the other gate be in the low state. Show that the load current (which is the sum of the base and collector currents of the saturated transistor $Q4$ in Fig. 10-14) is about 32 mA. Compare this value with the recommended load current in the high state of 0.4 mA.

10-8 For the following conditions, list the transistors that are off and those that are conducting in the three-state TTL gate of Fig. 10-16(c). (For $Q1$ and $Q6$, it would be necessary to list the states in the base–emitter and base–collector junctions separately.)
(a) When C is low and A is low.
(b) When C is low and A is high.
(c) When C is high.

What is the state of the output in each case?

10-9 Calculate the emitter current I_E across R_E in the ECL gate of Fig. 10-17 when:
(a) At least one input is high at -0.8 V.
(b) All inputs are low at -1.8 V.
Now assume that $I_C = I_E$. Calculate the voltage drop across the collector resistor in each case and show that it is about 1 V as required.

10-10 Calculate the noise margin of the ECL gate.

10-11 Using the NOR outputs of two ECL gates, show that when connected together to an external resistor and negative supply voltage, the wired connection produces an OR function.

10-12 The MOS transistor is bilateral, i.e., current may flow from source to drain or from drain to source. Using this property, derive a circuit that implements the Boolean function

$$Y = (AB + CD + AED + CEB)'$$

using six MOS transistors.

10-13 (a) Show the circuit of a four-input NAND gate using CMOS transistors. (b) Repeat for a four-input NOR gate.

10-14 Construct an exclusive-NOR circuit with two inverters and two transmission gates.

10-15 Construct an 8-to-1-line multiplexer using transmission gates and inverters.

10-16 Draw the logic diagram of a master–slave D flip-flop using transmission gates and inverters.