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PAGE 4:	TK1: CH0 MEMORY I/F
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PAGE 9:	TK1: CSI/DSI/HDMI/USB
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PAGE 13:	HDMI TYPE A CONN
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PAGE 17:	USB PORTS
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PAGE 28:	+3.3V VR
PAGE 29:	+5V VR
PAGE 30:	LOAD SWITCHES
PAGE 31:	PMIC: LOGIC AND GPIOS
PAGE 32:	PMIC: CNTL, INT SW, LDOS
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PAGE 41:	BASENET REPORT
PAGE 42:	BASENET REPORT
PAGE 43:	CREF PART REPORT
PAGE 44:	CREF PART REPORT
PAGE 45:	CREF PART REPORT
PAGE 46:	CREF PART REPORT
PAGE 47:	CREF PART REPORT
PAGE 48:	CREF PART REPORT
PAGE 49:	CREF PART REPORT

TK1 Compact Development Module
602-7R375-0000-D00
SCH REV 4.02
5/7/2014
FAB REV D
BOM REV E

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050

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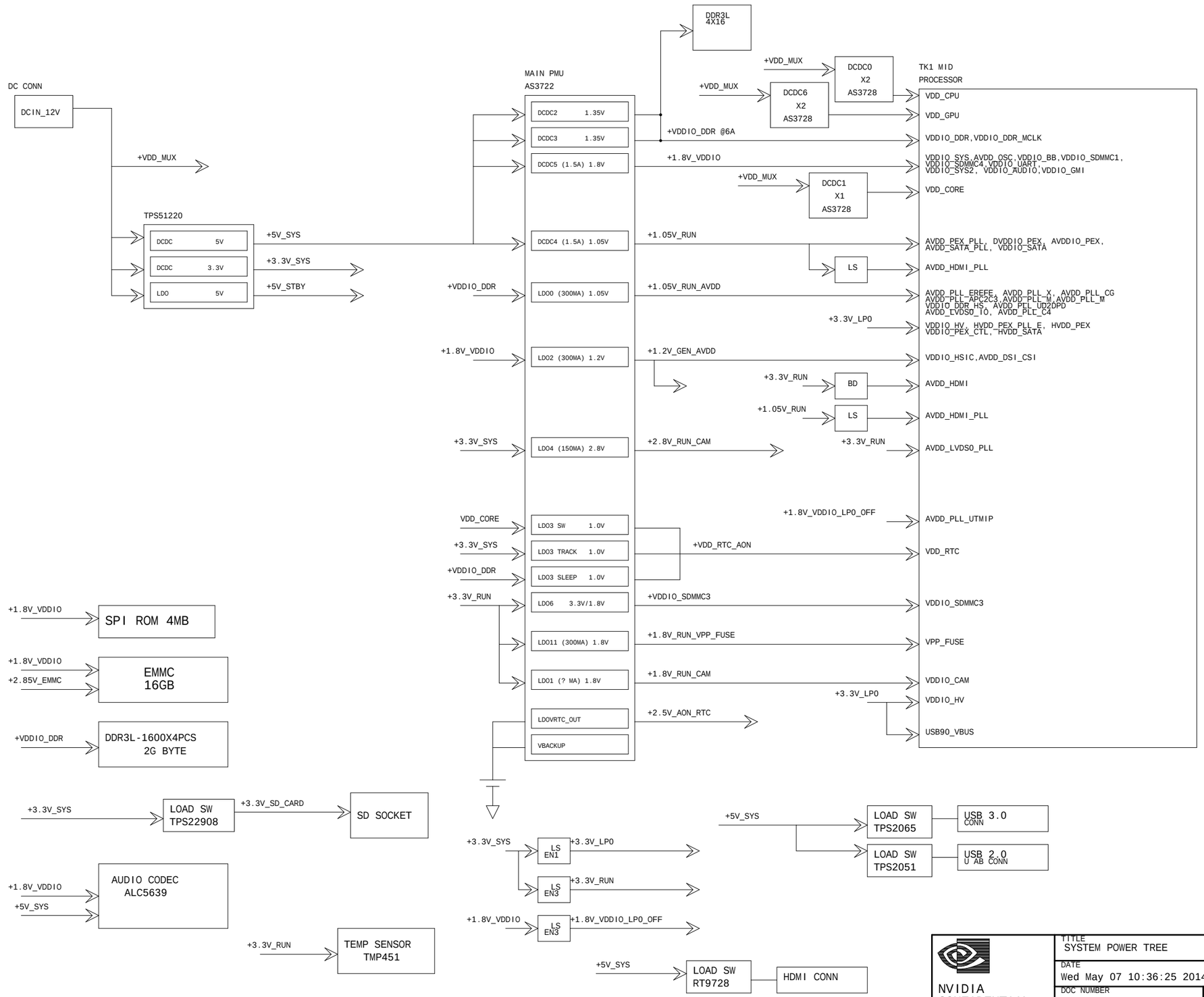
TITLE	COVER PAGE
TK1 Compact Development Module	
DATE	
Mon Apr 07 09:02:33 2014	
DOC NUMBER	
602-7R375-0000-D00	PAGE 1 OF 49



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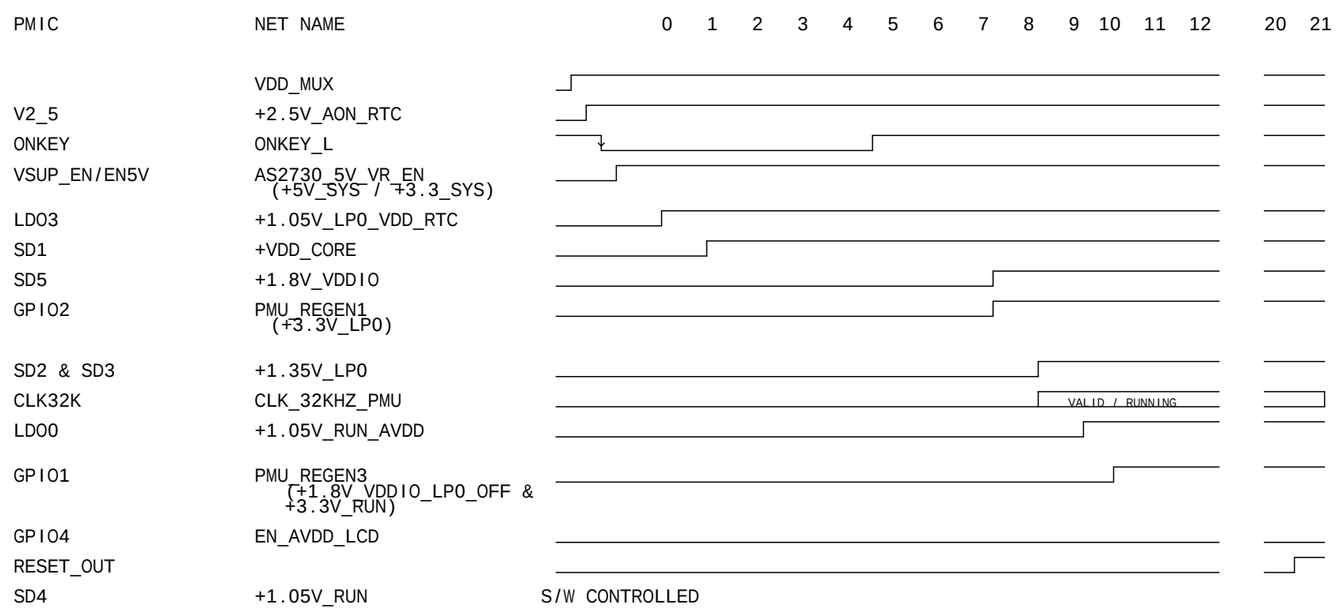
TITLE	SYSTEM POWER TREE
DATE	Wed May 07 10:36:25 2014
DOC NUMBER	602-7R375-0000-D00
REV	4.02
PAGE	2

POWER SEQUENCING



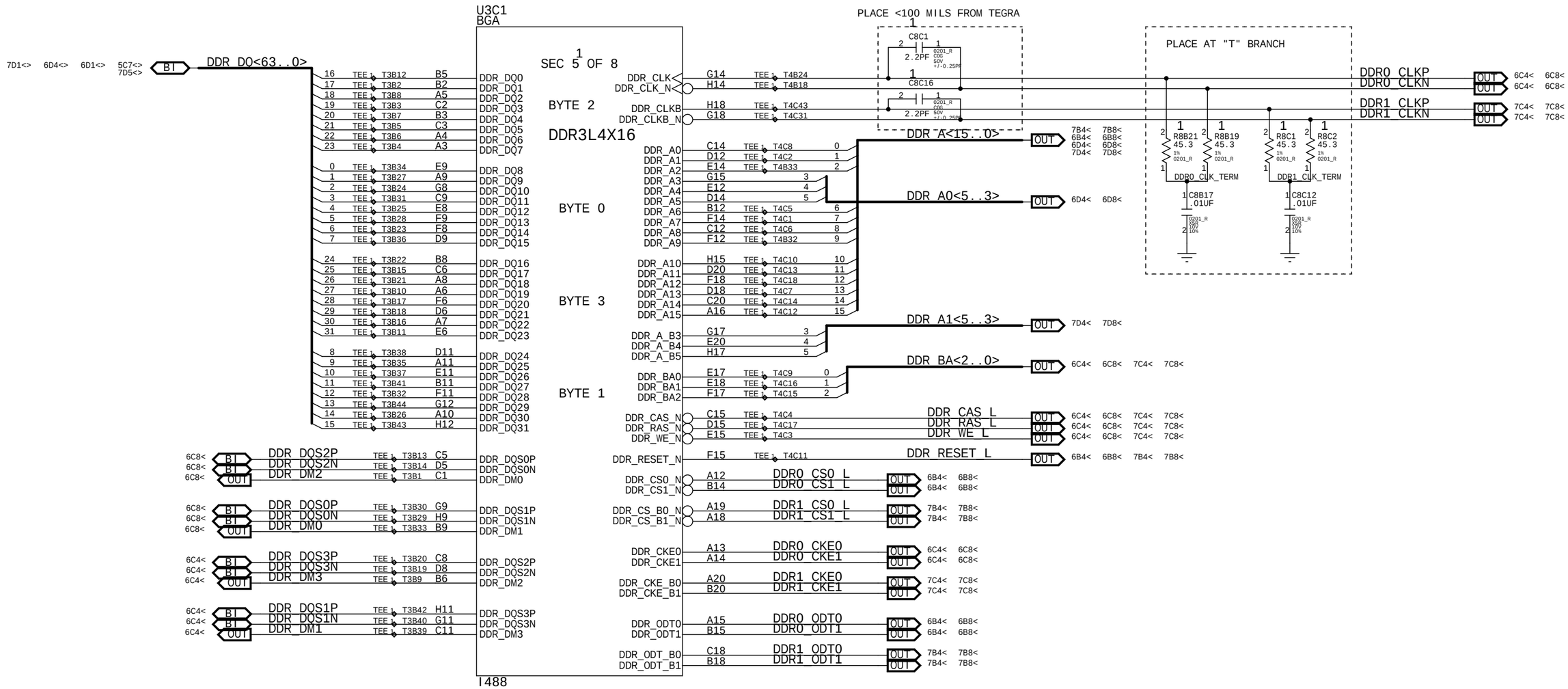
I2C ADDRESS MAP

BUS	DEVICE	ADDRESS
GEN1_I2C - 1.8V	AUDIO CODEC	7'H1C, 8'H38
	TEMPERATURE SENSOR	7'H4C, 8'H98
	BOARD ID	7'H56, 8'HAC
	EXPANSION	UNKNOWN
GEN1_I2C - 3.3V	HALF MINI PCIE	UNKNOWN
GEN2_I2C - 3.3V	EXPANSION	UNKNOWN
PWR_I2C - 1.8V	PMIC AS3722	7'H40, 8'H80
	EXPANSION	UNKNOWN
CAM_I2C - 3.3V	EXPANSION	UNKNOWN

Fri Apr 11 09:12:47 2014

NVIDIA CONFIDENTIAL

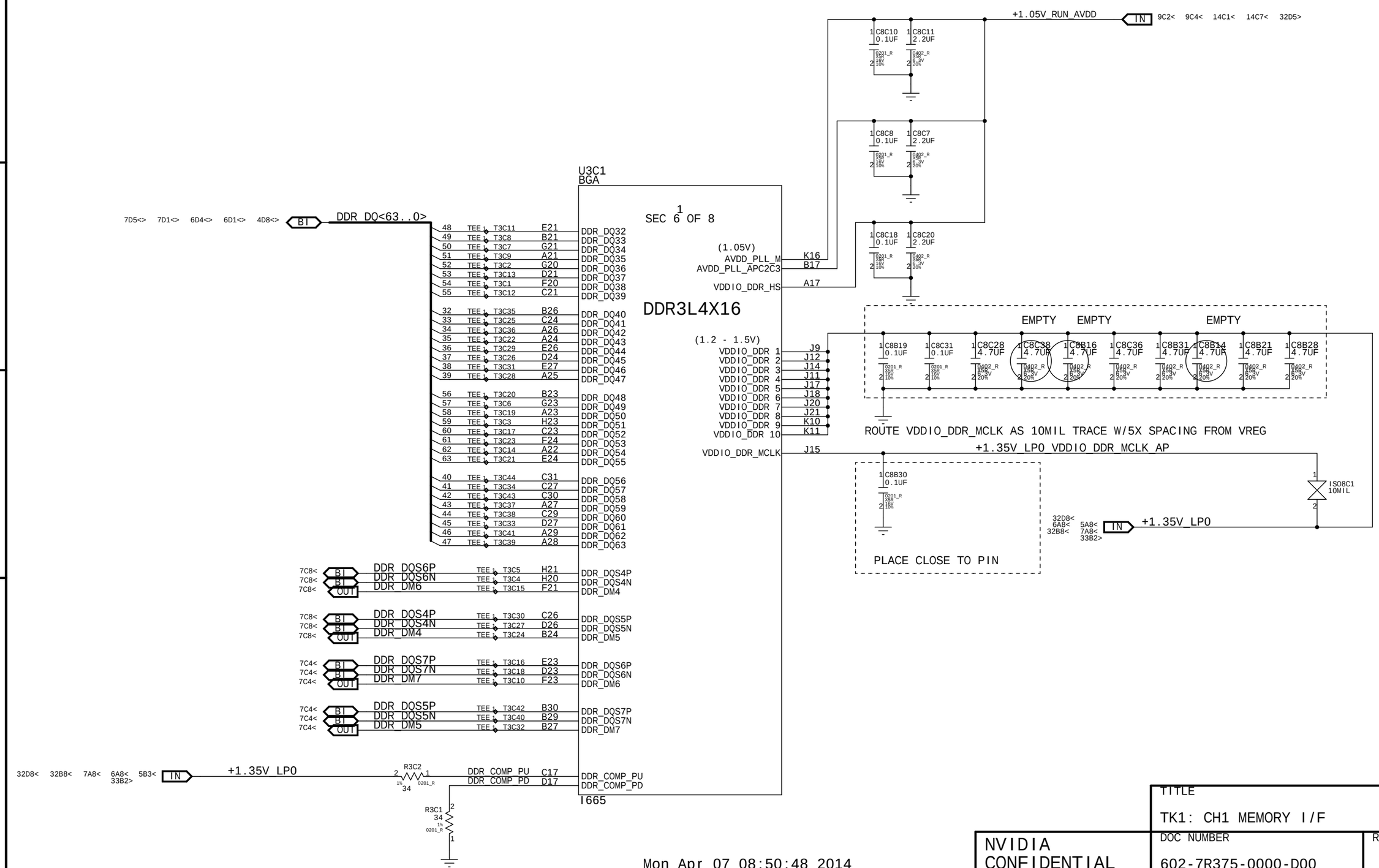
TITLE	DOC NUMBER	REV	PAGE
I2C ADDRESS MAP	602-7R375-0000-D00	4.02	3



Mon Apr 07 08:50:46 2014

NVIDIA CONFIDENTIAL

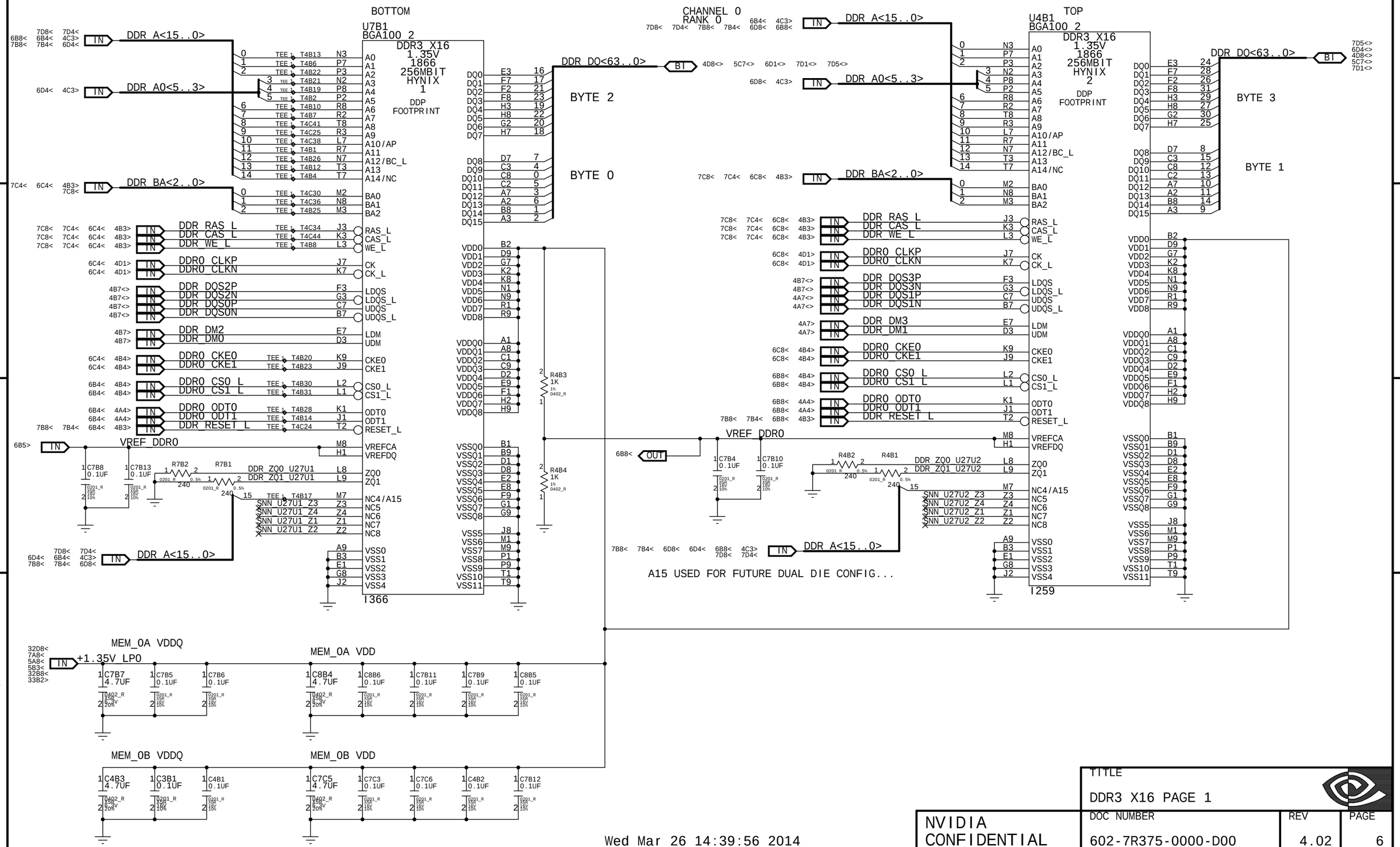
TITLE		
TK1: CH0 MEMORY I/F		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	4



Mon Apr 07 08:50:48 2014

NVIDIA CONFIDENTIAL

TITLE		
TK1: CH1 MEMORY I/F		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	5



TITLE		
DDR3 X16 PAGE 1		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	6

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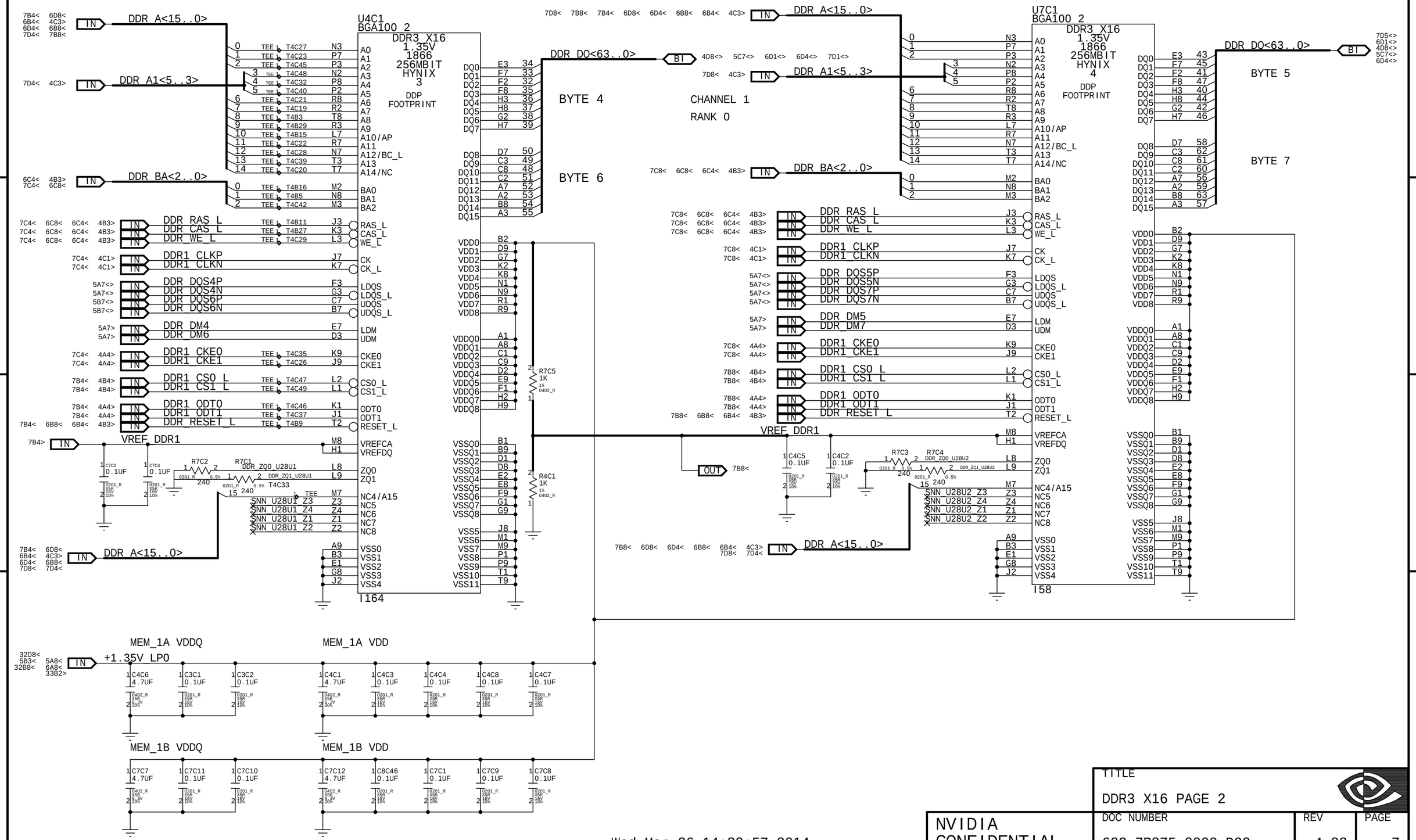
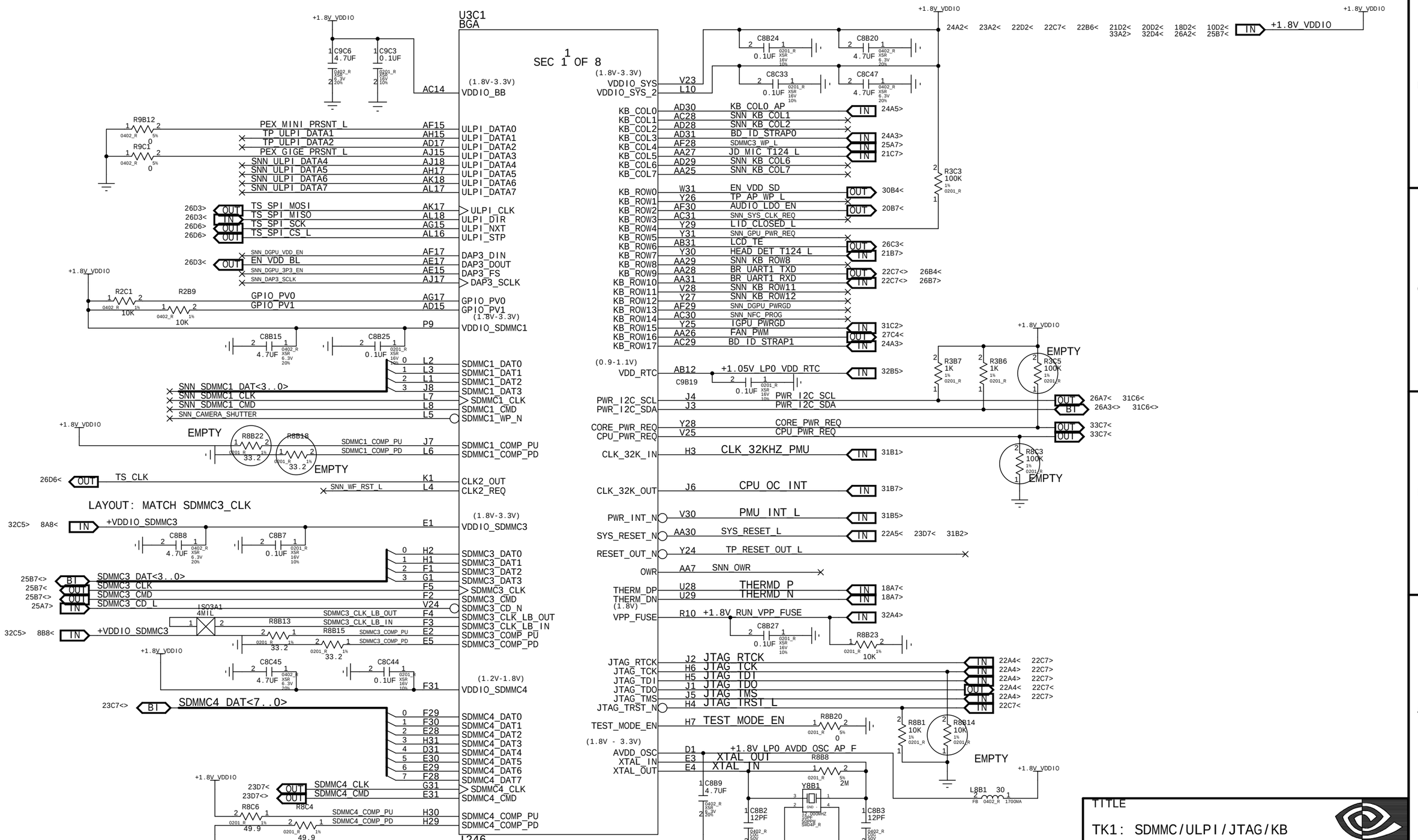


Wed Mar 26 14:39:57 2014

NVIDIA CONFIDENTIAL

TITLE		
DDR3 X16 PAGE 2		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	7

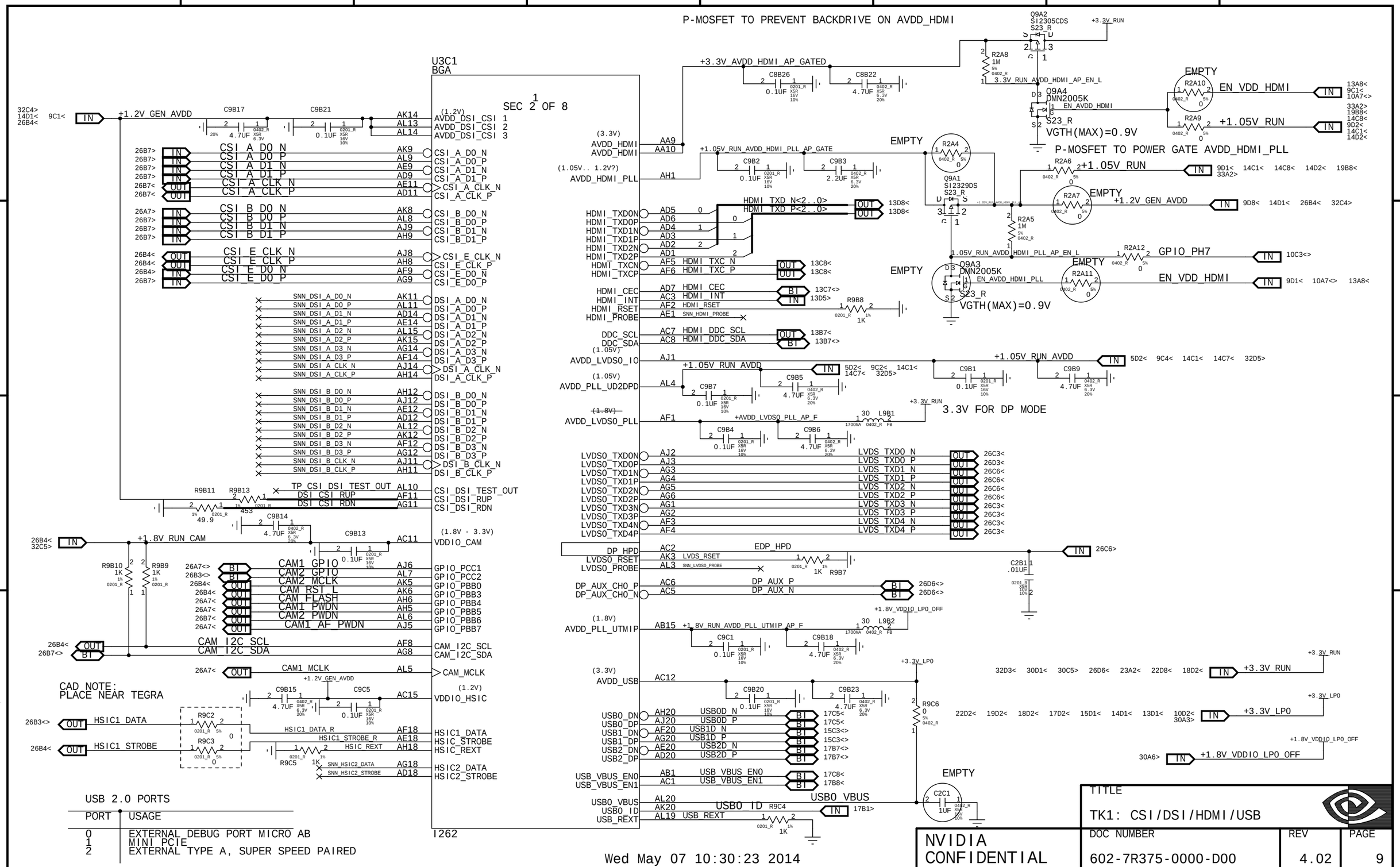


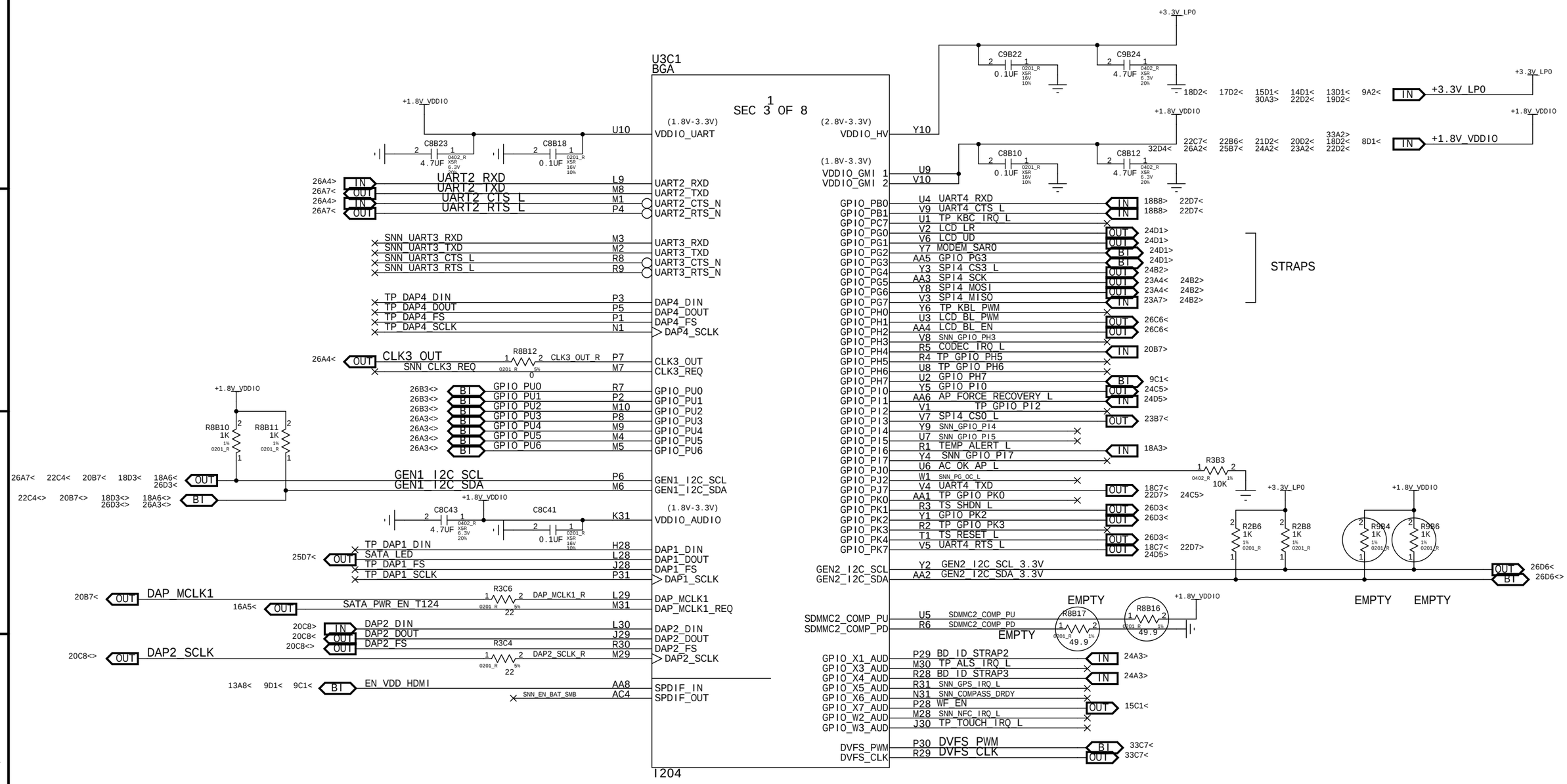
TITLE

TK1: SDMMC/ULPI/JTAG/KB

NVIDIA CONFIDENTIAL

DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	8


P-MOSFET TO PREVENT BACKDRIVE ON AVDD_HDMI
P-MOSFET TO POWER GATE AVDD_HDMI_PLL
U3C1
BGA
SEC 2 OF 8
+1.2V_GEN_AVDD
+3.3V_AVDD_HDMI_AP_GATED
+1.05V_RUN_AVDD_HDMI_PLL_AP_GATE
+1.05V_RUN_AVDD_HDMI_PLL_AP_EN_L
+3.3V_RUN_AVDD_HDMI_AP_EN_L
EN_AVDD_HDMI
EN_AVDD_HDMI_PLL
VGTH(MAX)=0.9V
EN_VDD_HDMI
+1.05V_RUN
+1.2V_GEN_AVDD
GPIO PH7
+1.05V_RUN_AVDD
3.3V FOR DP MODE
+1.8V_RUN_CAM
CAD NOTE:
PLACE NEAR TEGRA
USB 2.0 PORTS
PORT USAGE
0 EXTERNAL DEBUG PORT MICRO AB
1 MINI PCIE
2 EXTERNAL TYPE A, SUPER SPEED PAIRED
Wed May 07 10:30:23 2014
TITLE
TK1: CSI/DSI/HDMI/USB
NVIDIA
CONFIDENTIAL
DOC NUMBER
602-7R375-0000-D00
REV
4.02
PAGE
9



TITLE		
TK1: UART/GMI/DAP/SPI		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	10

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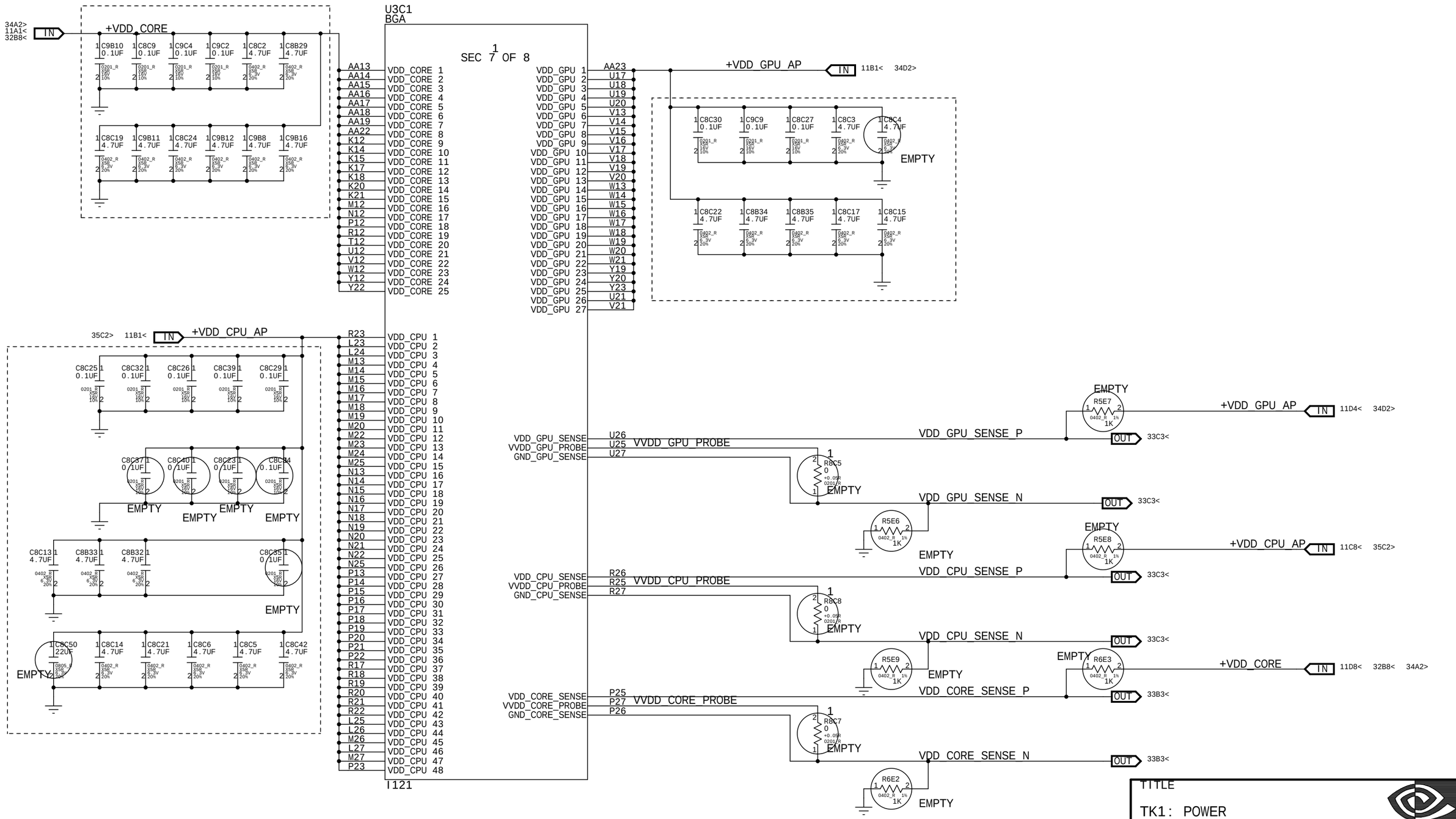
Mon Apr 07 08:50:54 2014



TITLE

TK1: POWER

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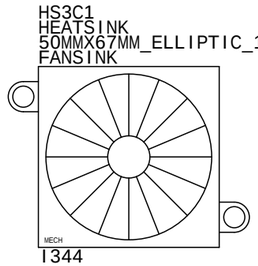
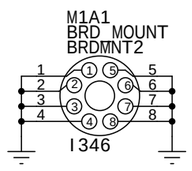
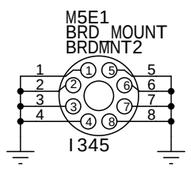
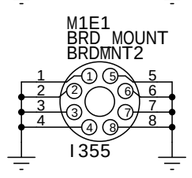
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	11

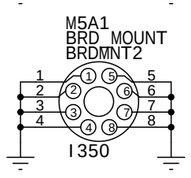
Mon Apr 07 08:50:56 2014

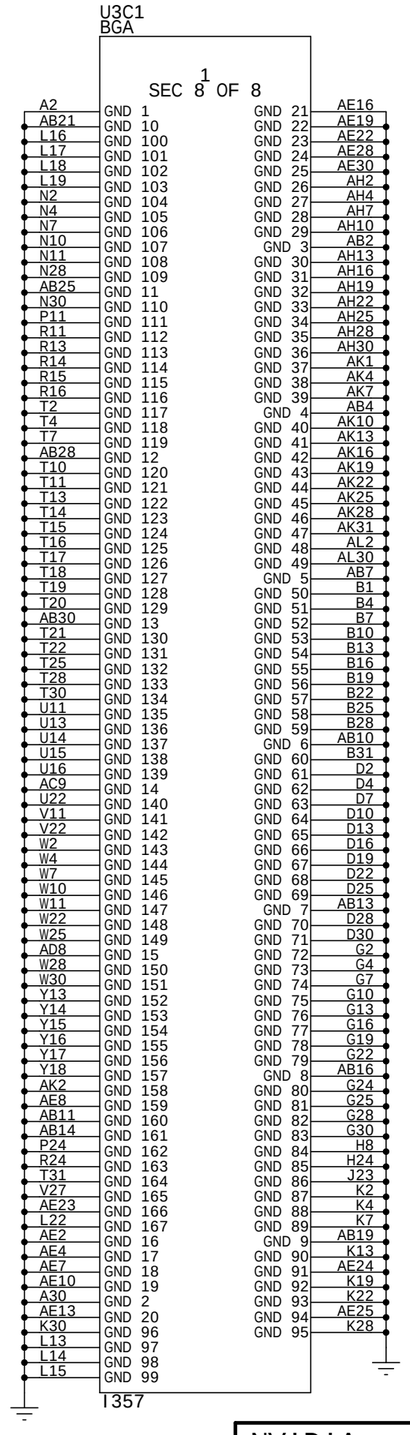












Mon Apr 07 08:50:57 2014

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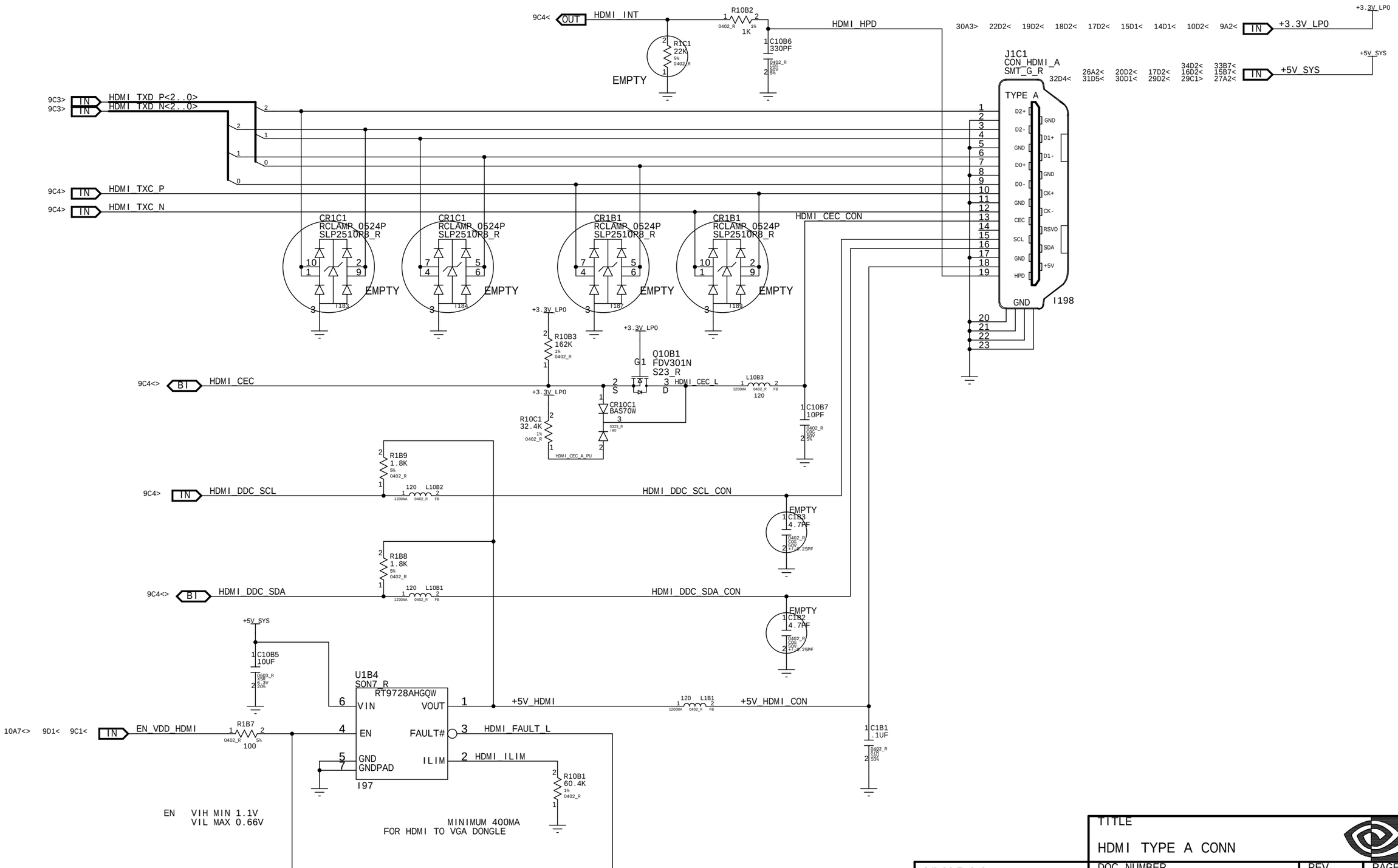
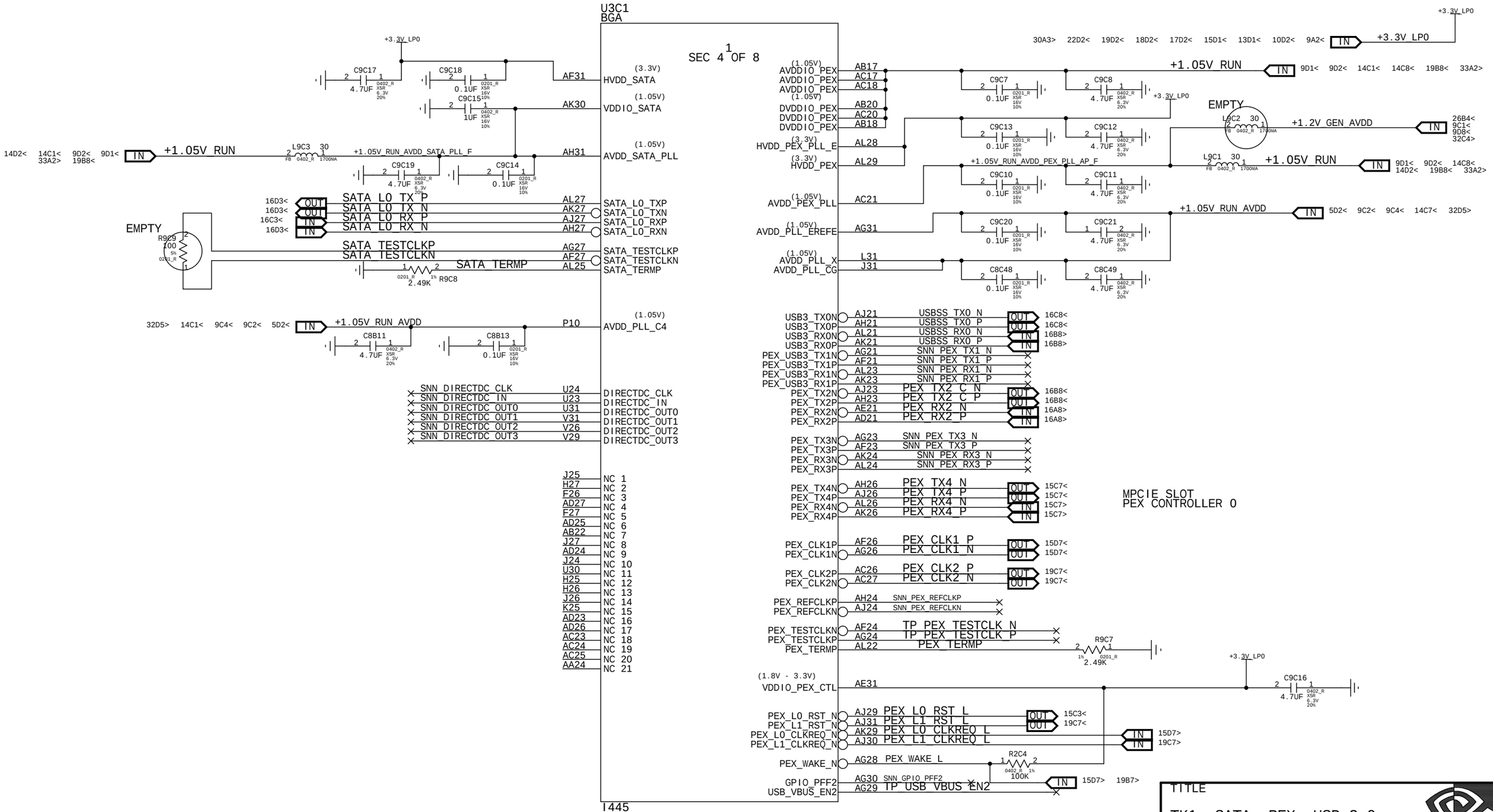
TITLE		
TK1: GND		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	12



Wed Mar 26 14:40:02 2014

NVIDIA CONFIDENTIAL

TITLE		
HDMI TYPE A CONN		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	13

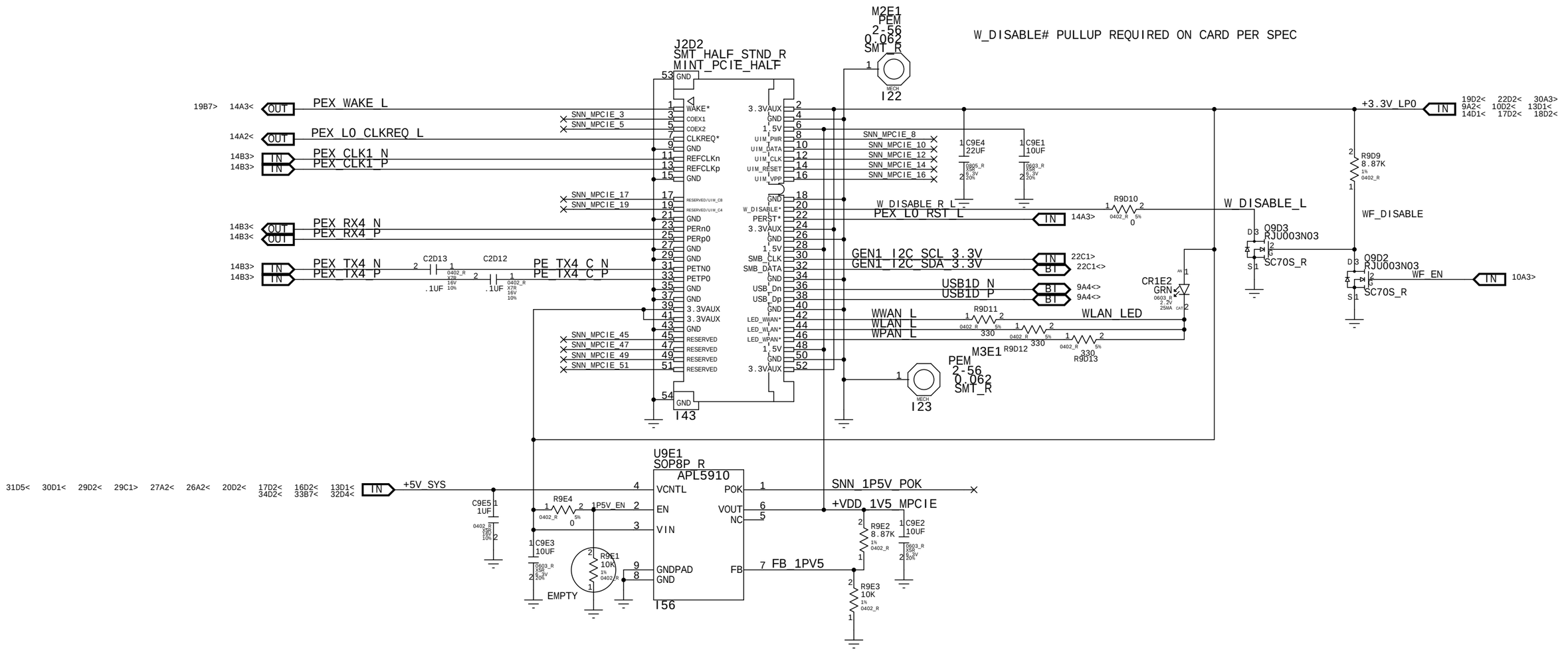


TITLE

TK1: SATA, PEX, USB 3.0

NVIDIA CONFIDENTIAL	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.02	14

Mon Apr 07 08:50:59 2014

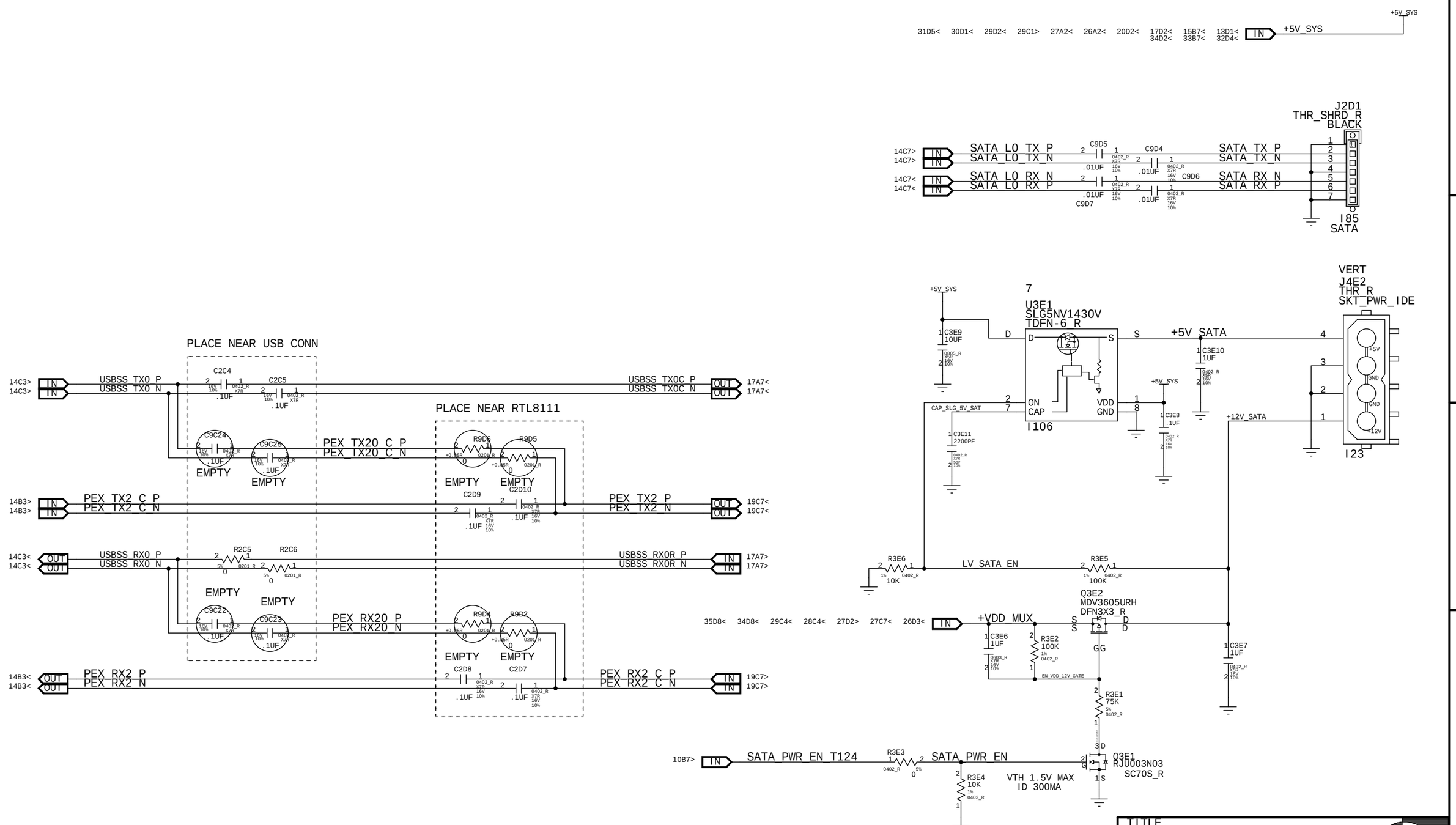


WIRELESS CARDS CAN WAKE FROM LP0 BUT NOT OFF

Wed Mar 26 14:40:03 2014

NVIDIA CONFIDENTIAL

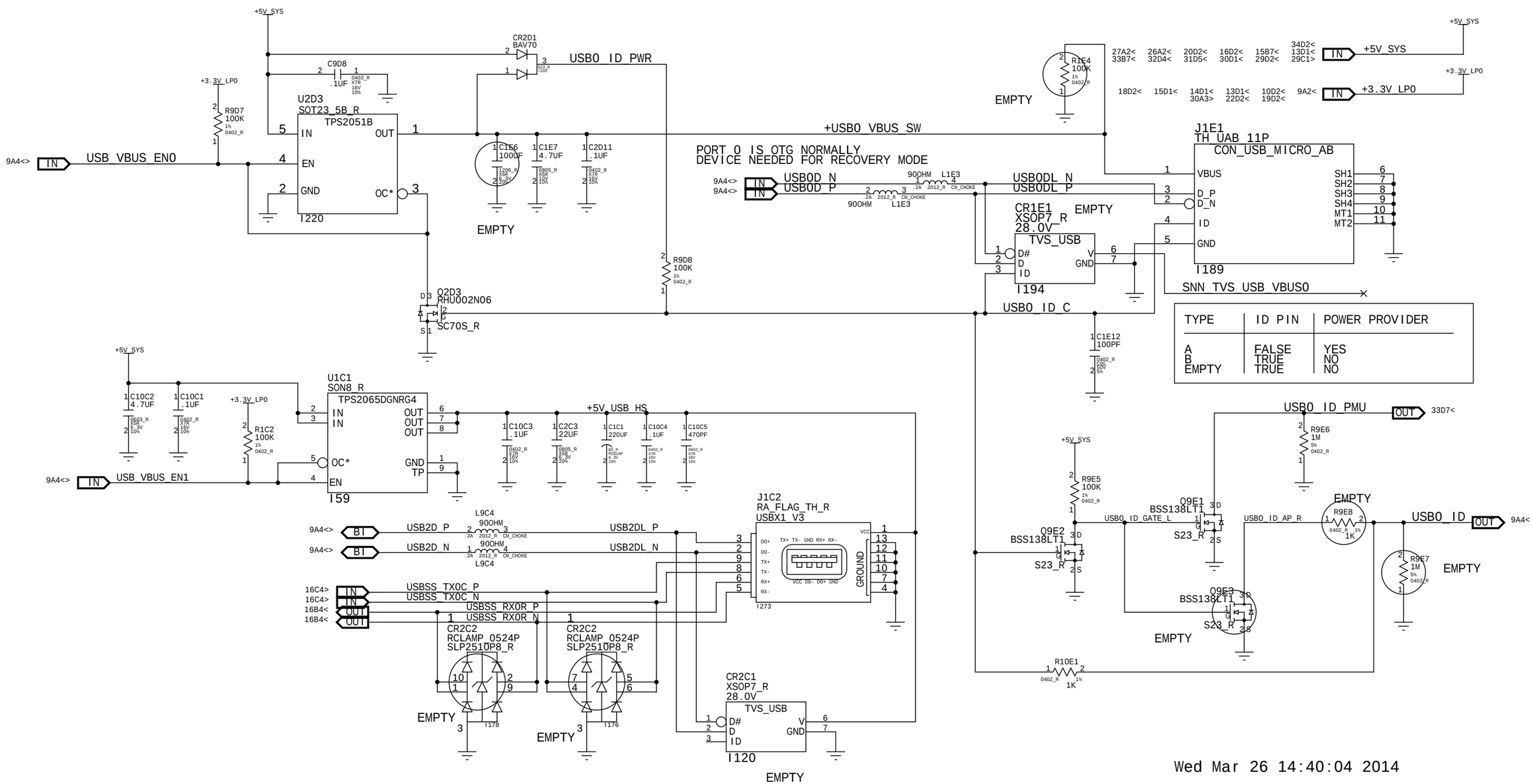
TITLE		
MINI HALF PCIE		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	15



Wed Mar 26 14:40:04 2014

NVIDIA CONFIDENTIAL

TITLE		
PEX OPTIONS AND SATA		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	16



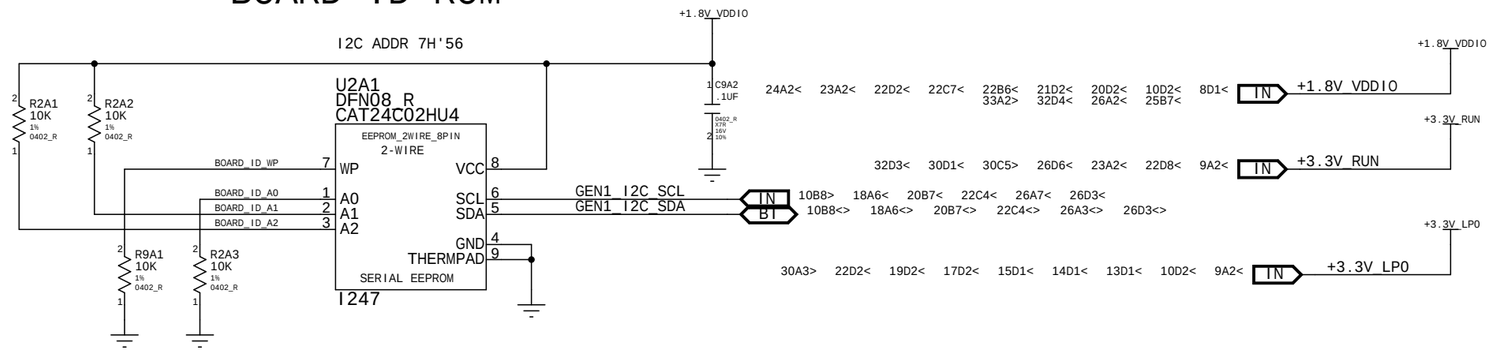
TITLE

USB PORTS

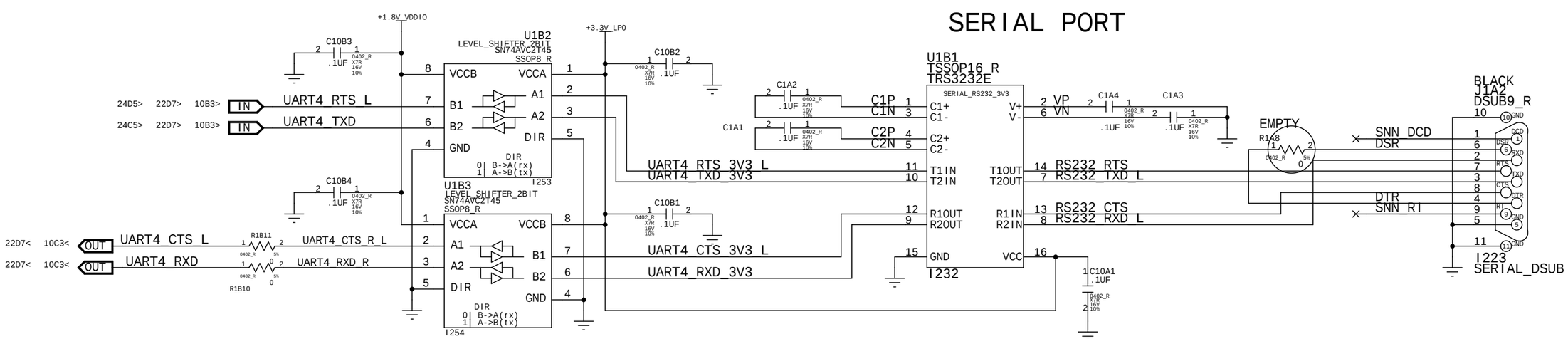
NVIDIA CONFIDENTIAL

DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	17

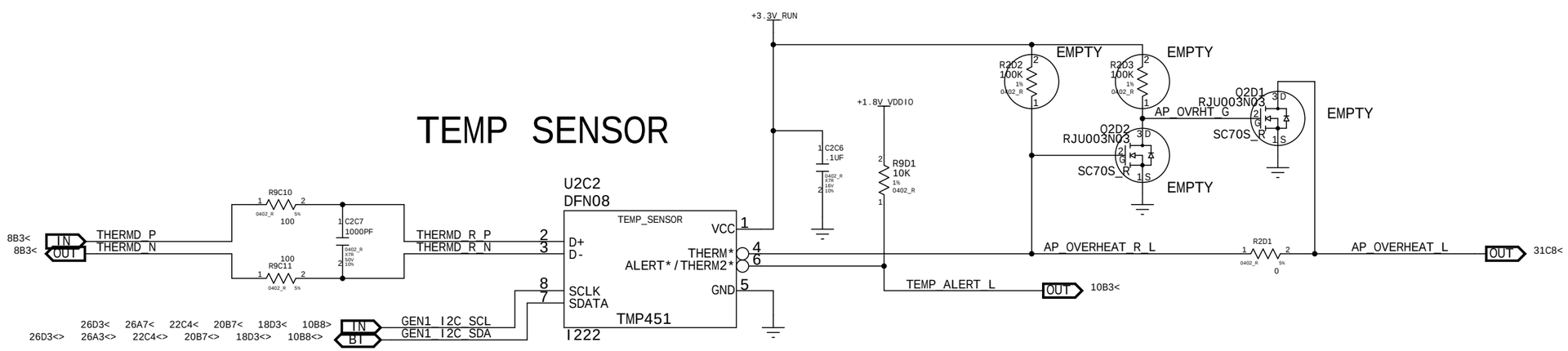
BOARD ID ROM



SERIAL PORT



TEMP SENSOR



I2C ADDR 7'H4C

Wed Mar 26 14:40:05 2014

TITLE		
TEMP SENSOR, SERIAL, ID		
NVIDIA CONFIDENTIAL	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.02	18

RISE TIME ON 3.3V RAIL MUST BE > 0.5MS

30A3> 22D2< 18D2< 17D2< 15D1< 14D1< 13D1< 10D2< 9A2< IN +3.3V_LP0

+3.3V_LP0

EMPTY

R9D3 10K 1% 0402_R

U2D2
QFN-33_R
RTL8111GS

14B3> IN PEX_CLK2_P
14A3> IN PEX_CLK2_N
14A2< OUT PEX_L1_CLKREQ_L
16B4> IN PEX_TX2_P
16B4> IN PEX_TX2_N
16A4< OUT PEX_RX2_C_P
16A4< OUT PEX_RX2_C_N
14A3> IN PEX_L1_RST_L

15 REFCLK_P
16 REFCLK_N
12 CLKREQB
13 HSIP
14 HSIN
17 HSOP
18 HSON
19 PERSTB

BIOS PULL HIGH/LOW ON PIN
TO ISOLATE LEAVE/ENTER DSM

EMPTY R2D9 100K 1% 0402_R

R2D10 100K 1% 0402_R

LAN_ISOLATE_L 20 ISOLATEB

30C8< 30A8< 27C4< 31C2< IN PMU_REGEN3

EMPTY R9D14 10K 0402_R 1%

LAN_ISOLATE

Q9D1 MMBT3904

EMPTY S363_R

14C1< 33A2> 14D2< 9D2< 14C8< 9D1< IN +1.05V_RUN

R2D11 10K 0402_R 1%

LAN_ISO_BASE

Q9D1 MMBT3904

S303_R

EMPTY

EMPTY

21 LANWAKEB

15D7> 14A3< OUT PEX_WAKE_L

R2D8 0 0402_R 5%

PEX0_WAKE_R_L

XTAL_LAN_P 28 CKXTAL1

XTAL_LAN_N 29 CKXTAL2

C2D3 20PF 0402_R COG 50V 5%

HC49_S I359 30_30PPM Y2C1 25.000MHZ

C1D1 20PF 0402_R COG 50V 5%

33 GND

I404

AVDD33 11
AVDD33 32

C1D4 .1UF 0402_R X7R 16V 10%

C1D2 .1UF 0402_R X7R 16V 10%

EMPTY C1D5 4.7UF 0603_R X5R 6.3V 10%

EMPTY C1D3 4.7UF 0603_R X5R 6.3V 10%

VDDREG 23

C9D3 .1UF 0402_R X7R 16V 10%

C9D2 4.7UF 0603_R X5R 6.3V 10%

TWO INDUCTOR FOOTPRINTS
FOR AVAILABILITY REASONS

EMPTY

4.7UH L2D1 55MA 2016_R SMD
4.7UH L2D2 0.7A SMD_R SMD

REGOUT 24 +1.05V_LAN_REGOUT_L

C2D2 .1UF 0402_R X7R 16V 10%

C2D1 4.7UF 0603_R X5R 6.3V 10%

AVDD10 3
AVDD10 8
AVDD10 30

C10D2 .1UF 0402_R X7R 16V 10%

C10D3 .1UF 0402_R X7R 16V 10%

C10D1 .1UF 0402_R X7R 16V 10%

+1.05V_LAN_REGOUT

DVDD10 22

C2D4 .1UF 0402_R X7R 16V 10%

C2D6 1UF 0402_R X5R 16V 10%

C2D5 .1UF 0402_R X7R 16V 10%

LINK 10 = OFF
LINK 100 = SOLID ORANGE
LINK 1000 = SOLID GREEN
LINK ACT = BLINK YELLOW

J1D1
RJ45_2_R
RJ45_1X1GBIT_MAG_LED

MDIP0 1 LAN_MDI0_P
MDIN0 2 LAN_MDI0_N
MDIP1 4 LAN_MDI1_P
MDIN1 5 LAN_MDI1_N
MDIP2 6 LAN_MDI2_P
MDIN2 7 LAN_MDI2_N
MDIP3 9 LAN_MDI3_P
MDIN3 10 LAN_MDI3_N

9 MX0+
10 MX0-
7 MX1+
8 MX1-
5 MX2+
6 MX2-
3 MX3+
4 MX3-

VCC 2
CH_GND 1

LAN_TRCT1 C1C2 .01UF 0402_R X7R 16V 10%

LAN_CH_GND R1D2 0 0402_R 5%

GND 11
GND 12

+3.3V_LP0

RSET 31 LAN_RSET R1D1 2.49K 0402_R 1%

I382 16 14 15 13

ORNG GRN YLW

LED0 27 LAN_LED0
LED1/GPO 26 LAN_LED1
LED2 25 LAN_LED2

R2D4 240 0402_R 1% LAN_LED_100

R2D5 240 0402_R 1% LAN_LED_1000

R2D6 510 0402_R 5% LAN_LED0_ACT_L

C1D7 .1UF 0402_R X7R 16V 10%

EMPTY

Wed Mar 26 14:40:05 2014

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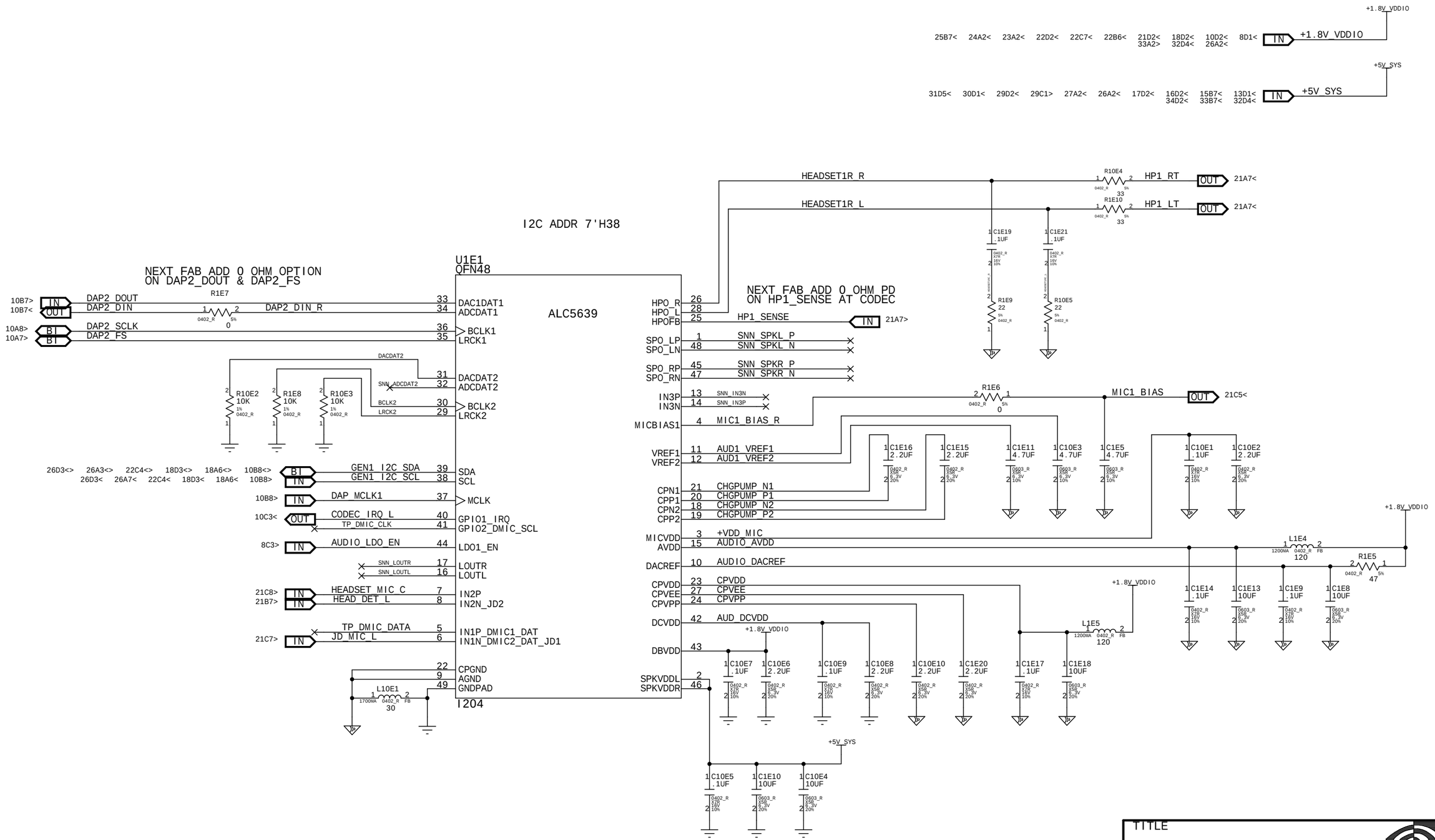
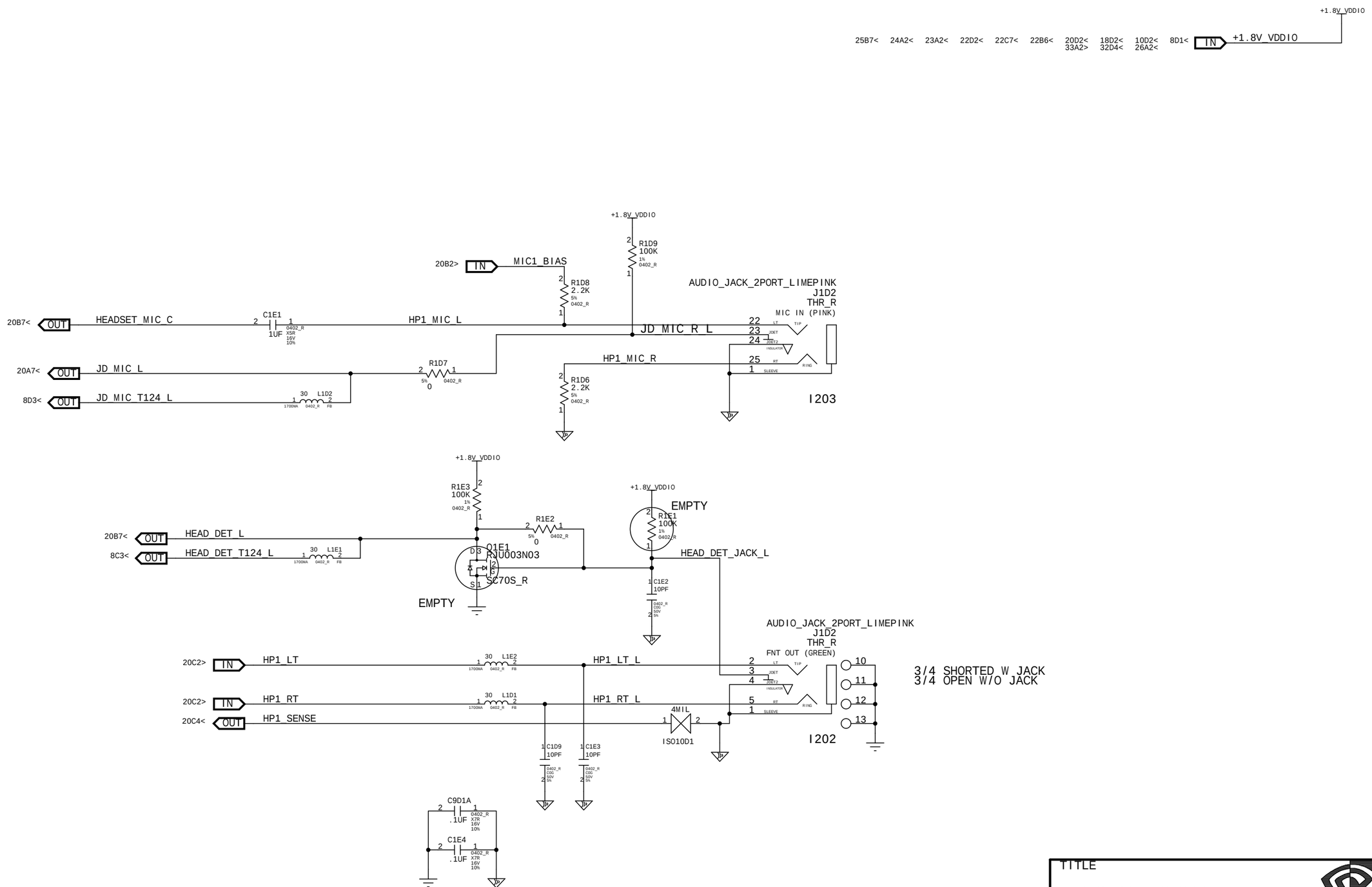
TITLE		
PEX GIGE LAN/PHY		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	19



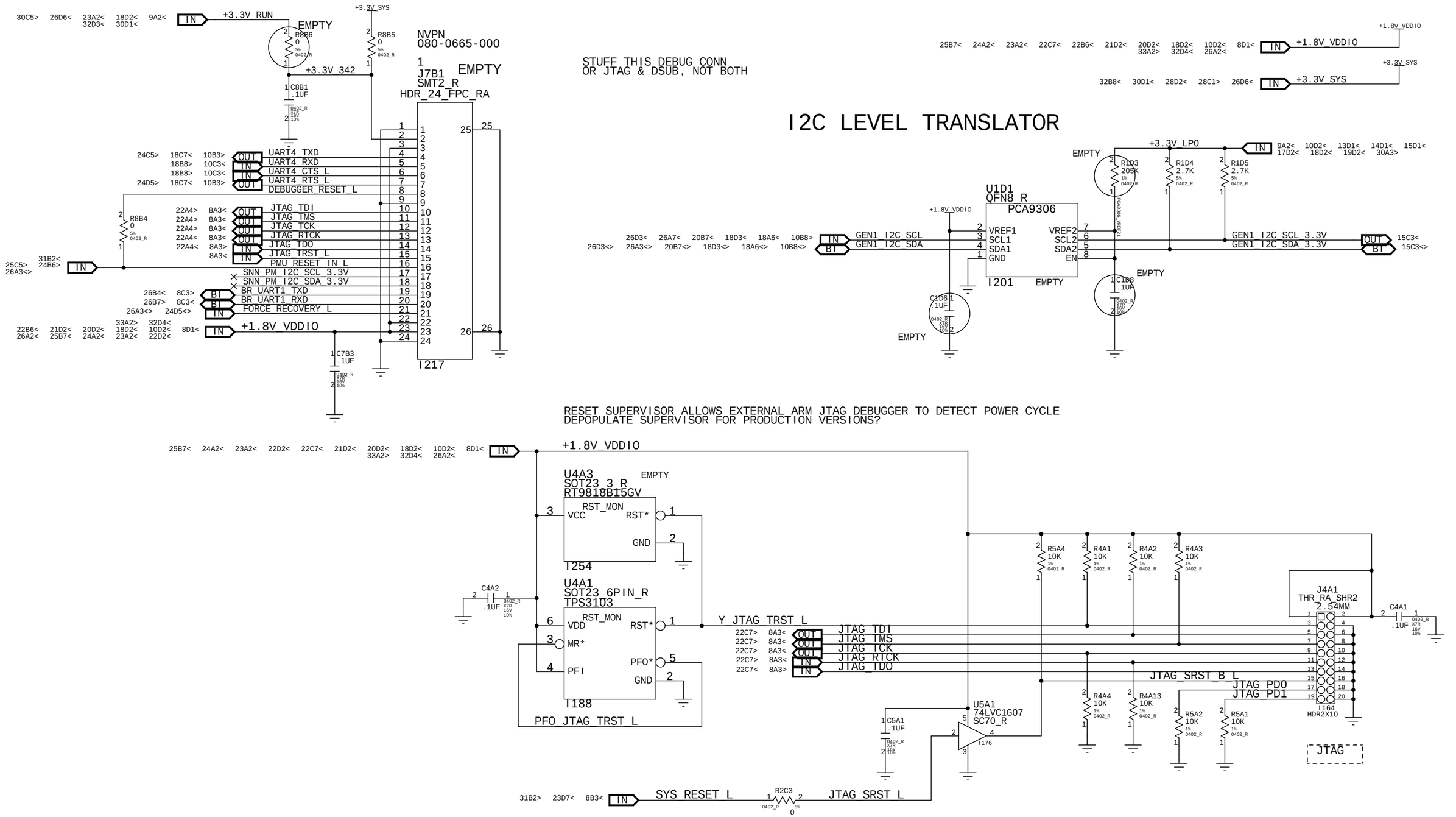
Mon Mar 31 17:28:55 2014

NVIDIA CONFIDENTIAL	TITLE: AUDIO CODEC		
	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.02	20



Wed Mar 26 14:40:07 2014

NVIDIA CONFIDENTIAL	TITLE: AUDIO CONNECTORS		
	DOC NUMBER: 602-7R375-0000-D00	REV: 4.02	PAGE: 21



TITLE

JTAG CONN; I2C TRANSLATER

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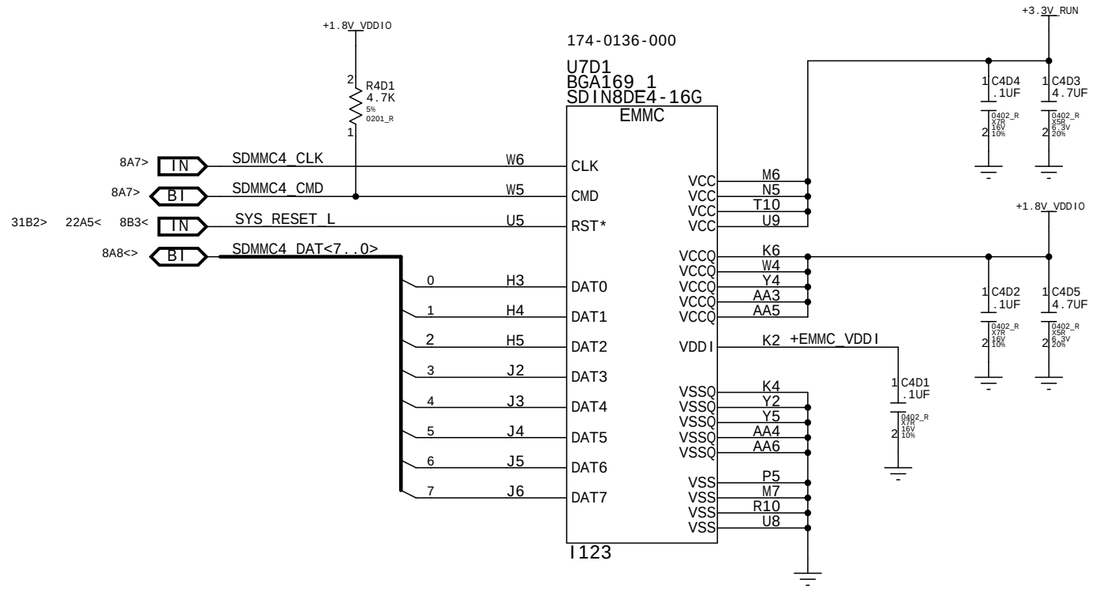
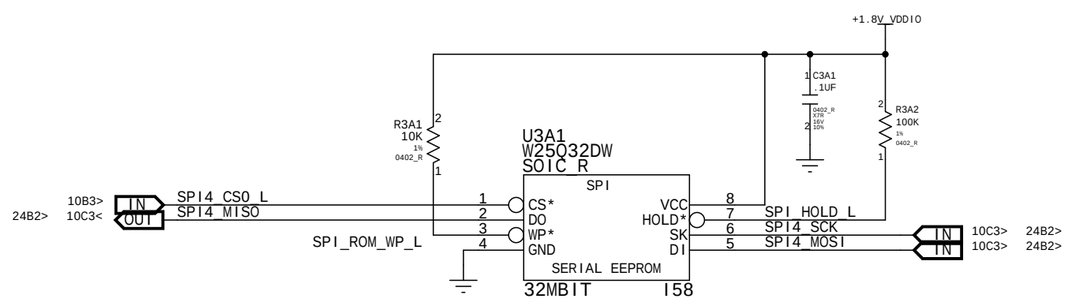
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	22

Wed May 07 10:39:43 2014

EMMC 4.51



SPI BOOT ROM

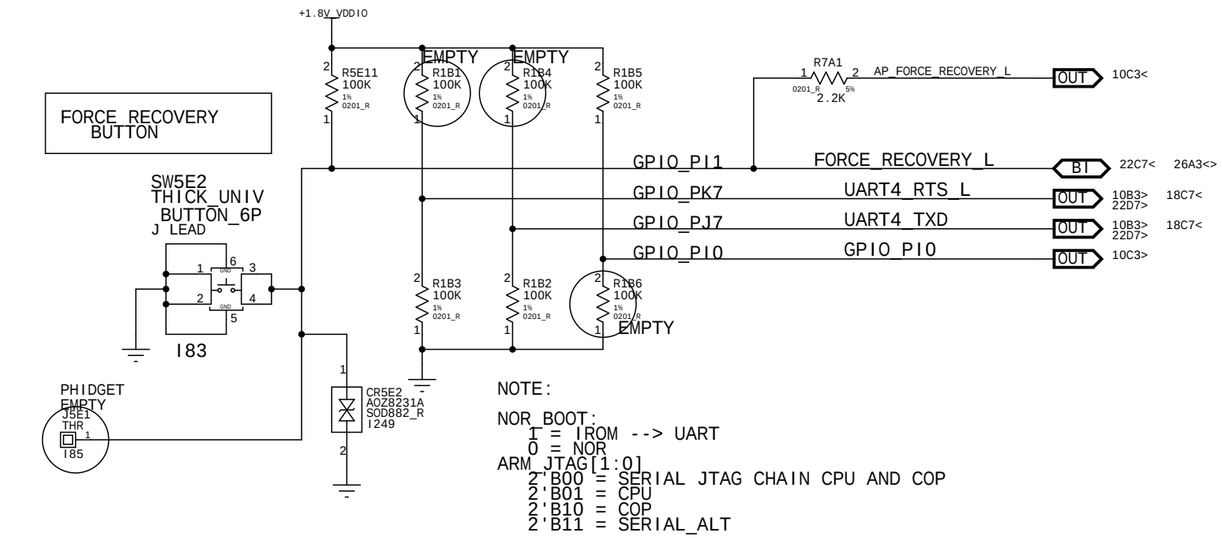


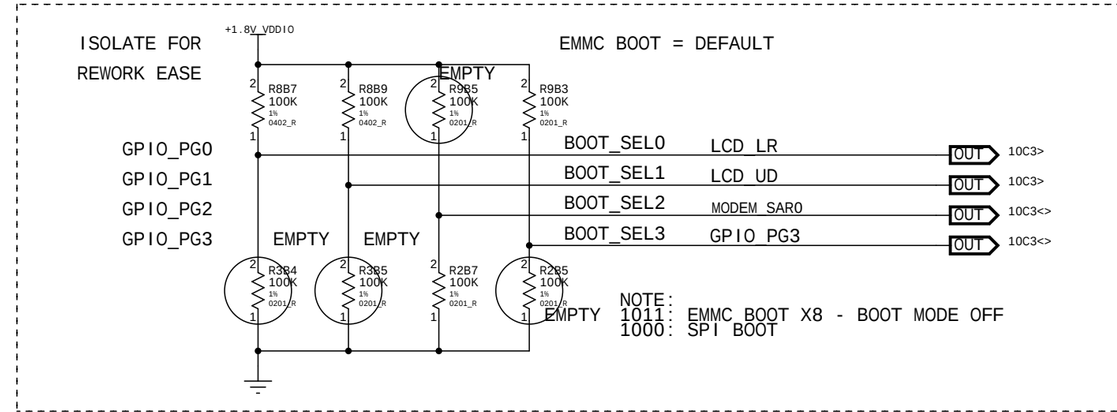
32D3< 30D1< 30C5> 26D6< 22D8< 18D2< 9A2< IN +3.3V_RUN (+3.3V_RUN)

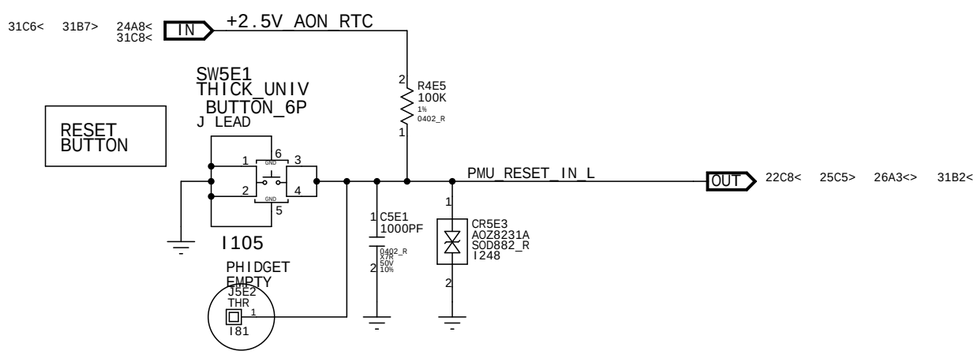
25B7< 24A2< 22D2< 22C7< 22B6< 21D2< 20D2< 33A2> 18D2< 32D4> 10D2< 26A2< 8D1< IN +1.8V_VDDIO (+1.8V_VDDIO)

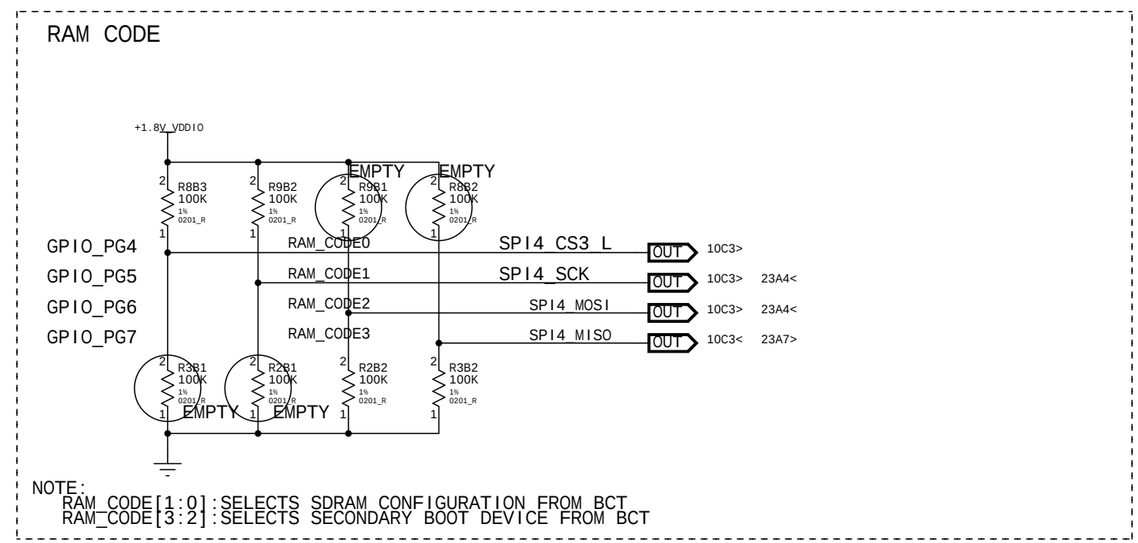
Wed Mar 26 14:40:08 2014

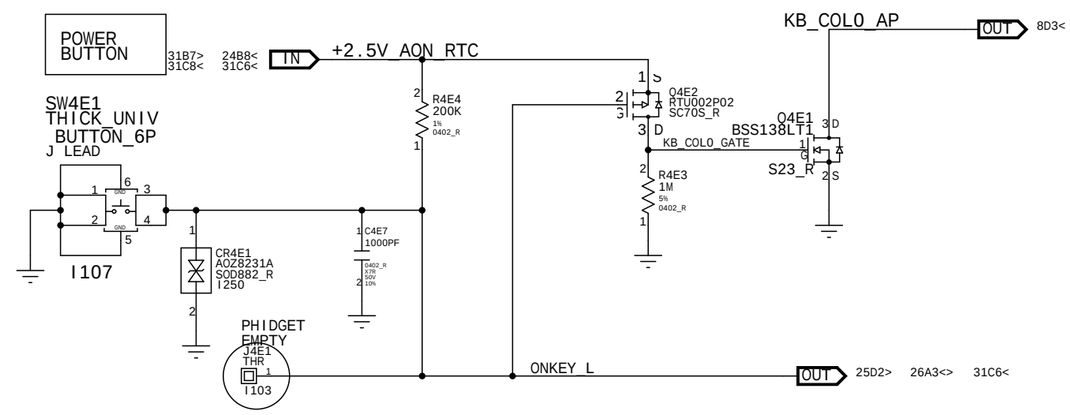
NVIDIA CONFIDENTIAL	TITLE: EMMC,SPI ROM		
	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.02	23

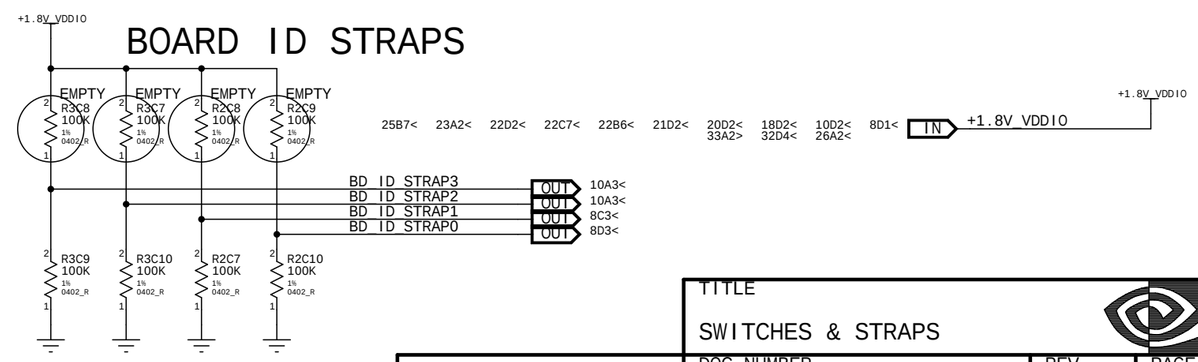






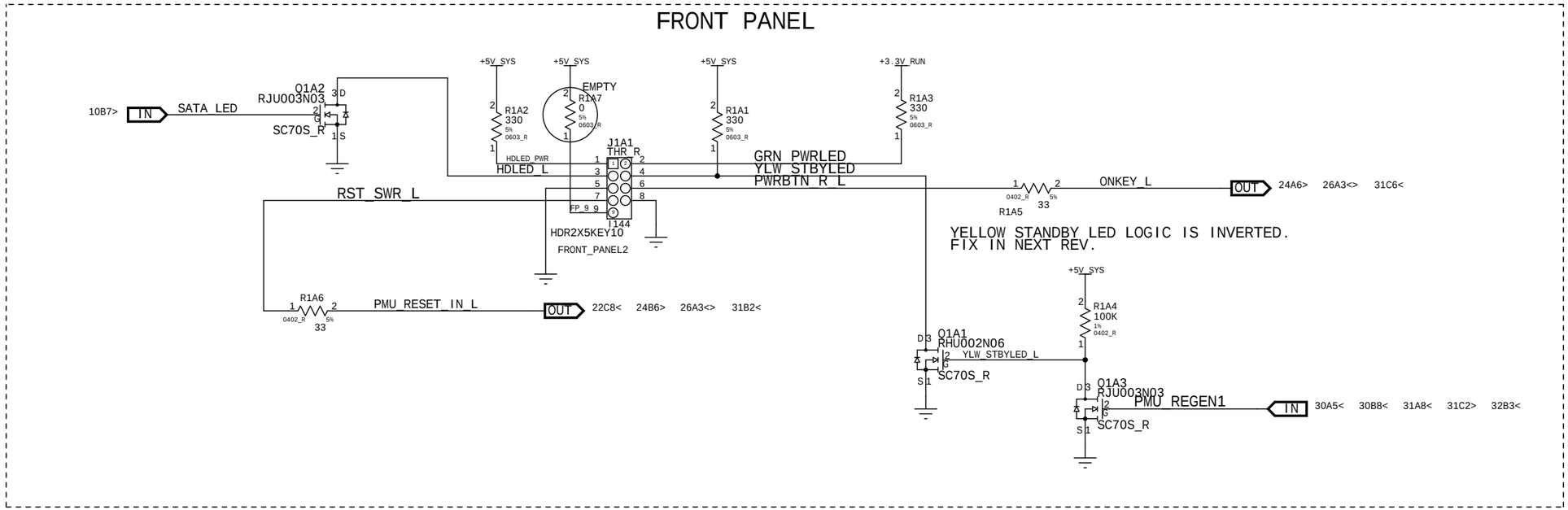


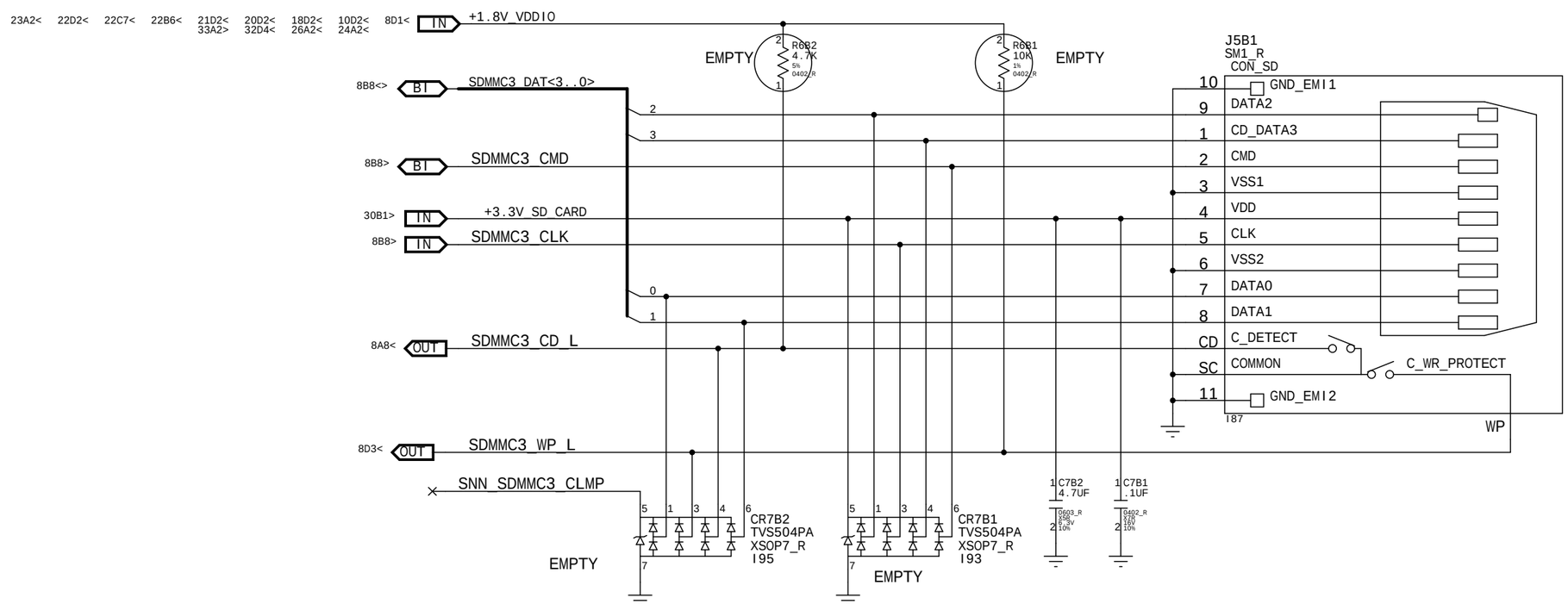




Tue Apr 08 14:39:29 2014

NVIDIA CONFIDENTIAL	TITLE: SWITCHES & STRAPS		
	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.02	24

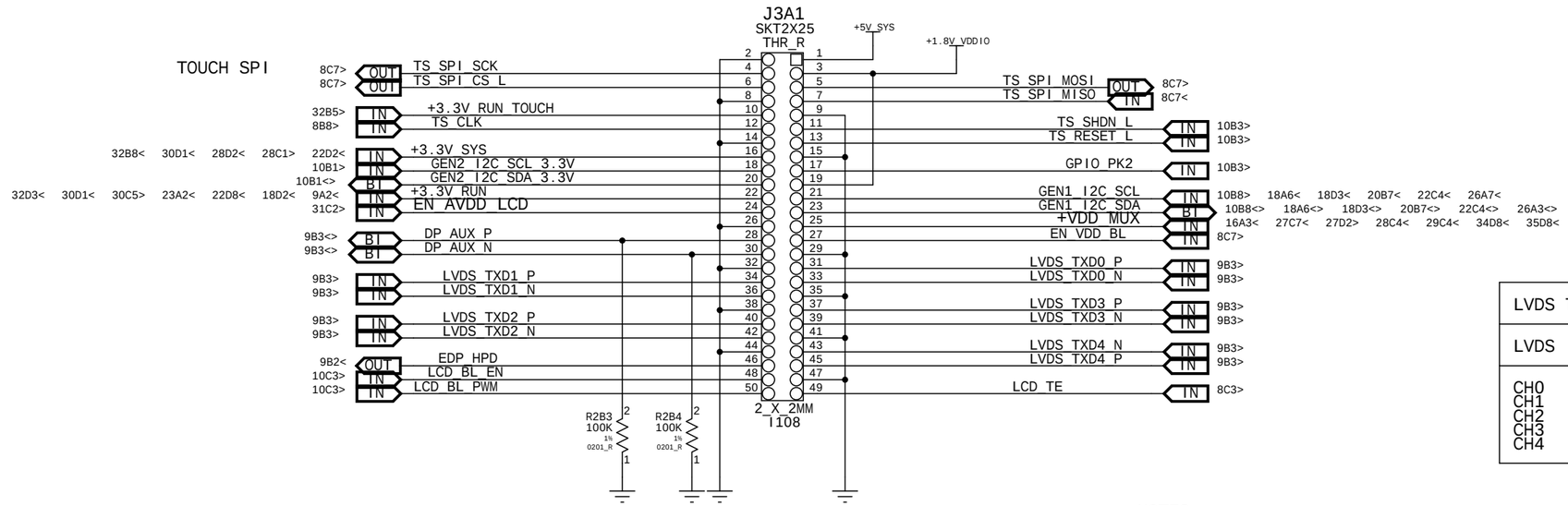




Wed May 07 10:30:26 2014

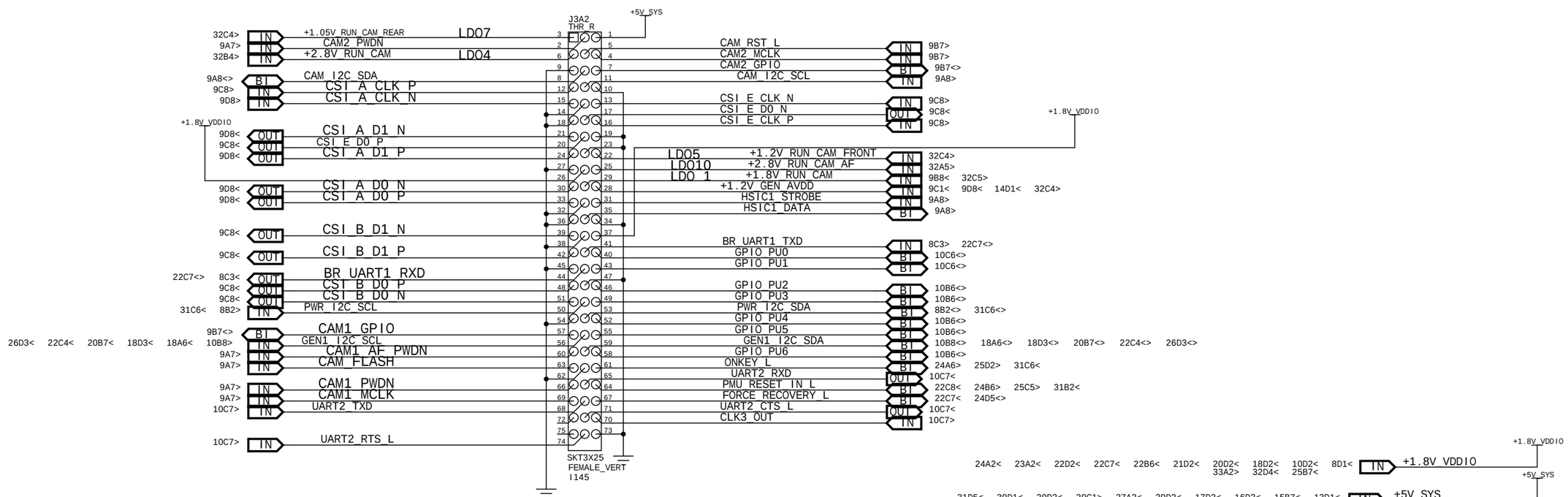
NVIDIA CONFIDENTIAL

TITLE		
SD CONN & FRONT PANEL HDR		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	25



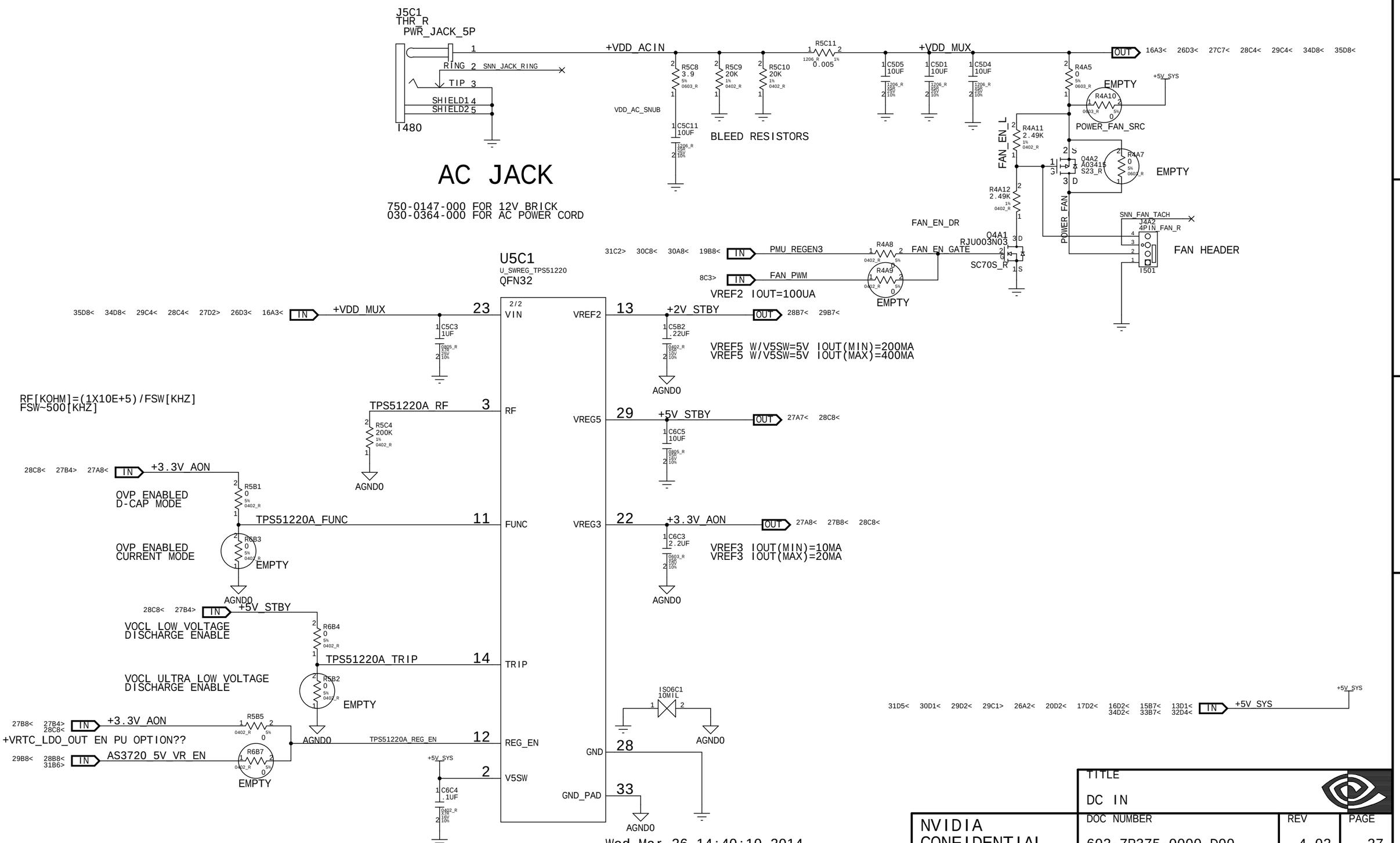
LVDS TO EDP MUX	
LVDS	EDP
CH0	CH2
CH1	CH1
CH2	CH0
CH3	---
CH4	CH3

NOTES:
LVDS / EDP MODULES MAY USE +3.3V RUN
OR +3.3V_RUN GATED BY EN_AVDD_LCD (PMIC GPIO4)



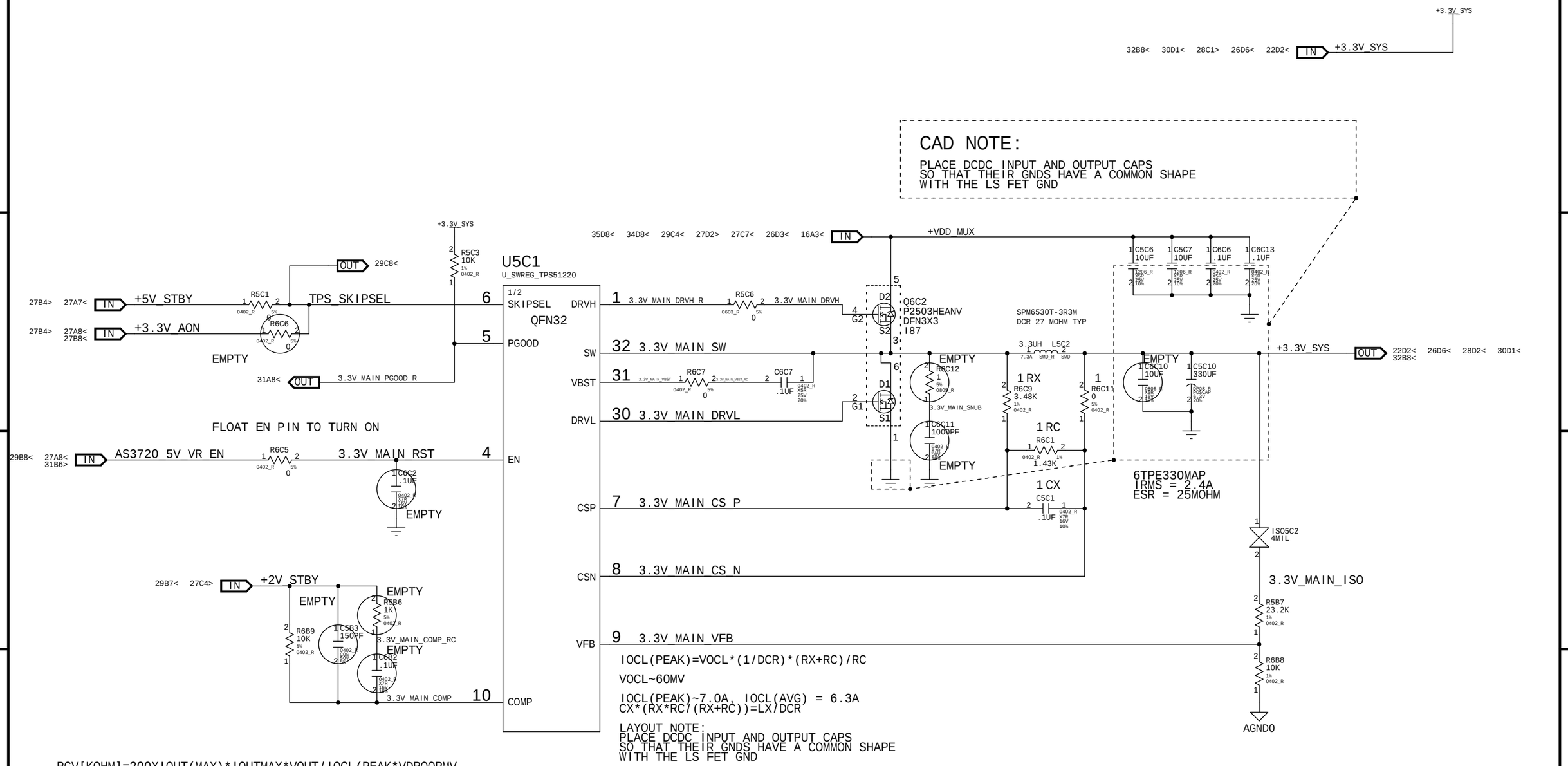
Wed Mar 26 14:40:09 2014

NVIDIA CONFIDENTIAL	TITLE: EXP:TOUCH/DISP & GENERAL		
	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.02	26



TITLE		
DC IN		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	27

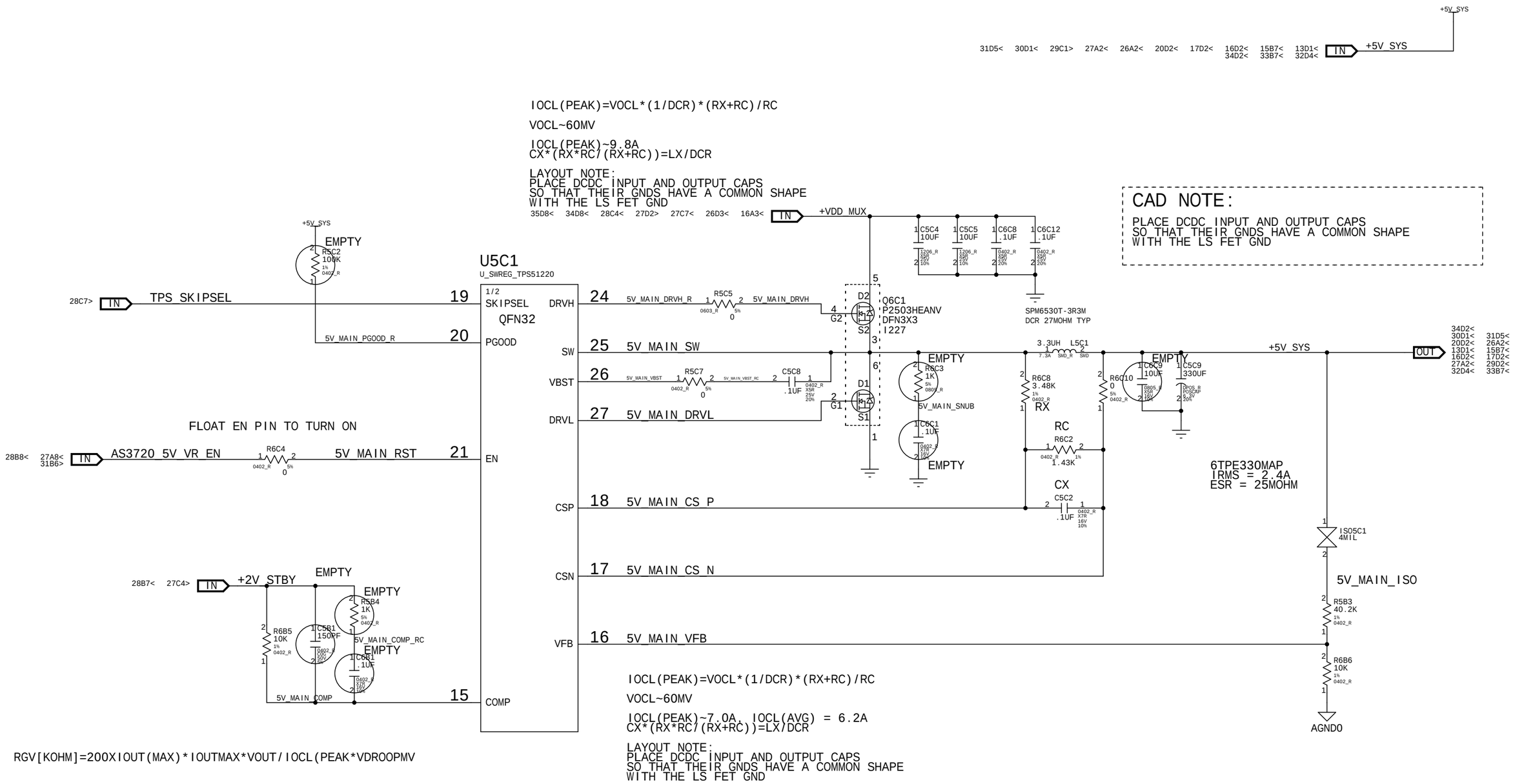
NVIDIA CONFIDENTIAL



Wed Mar 26 14:40:11 2014

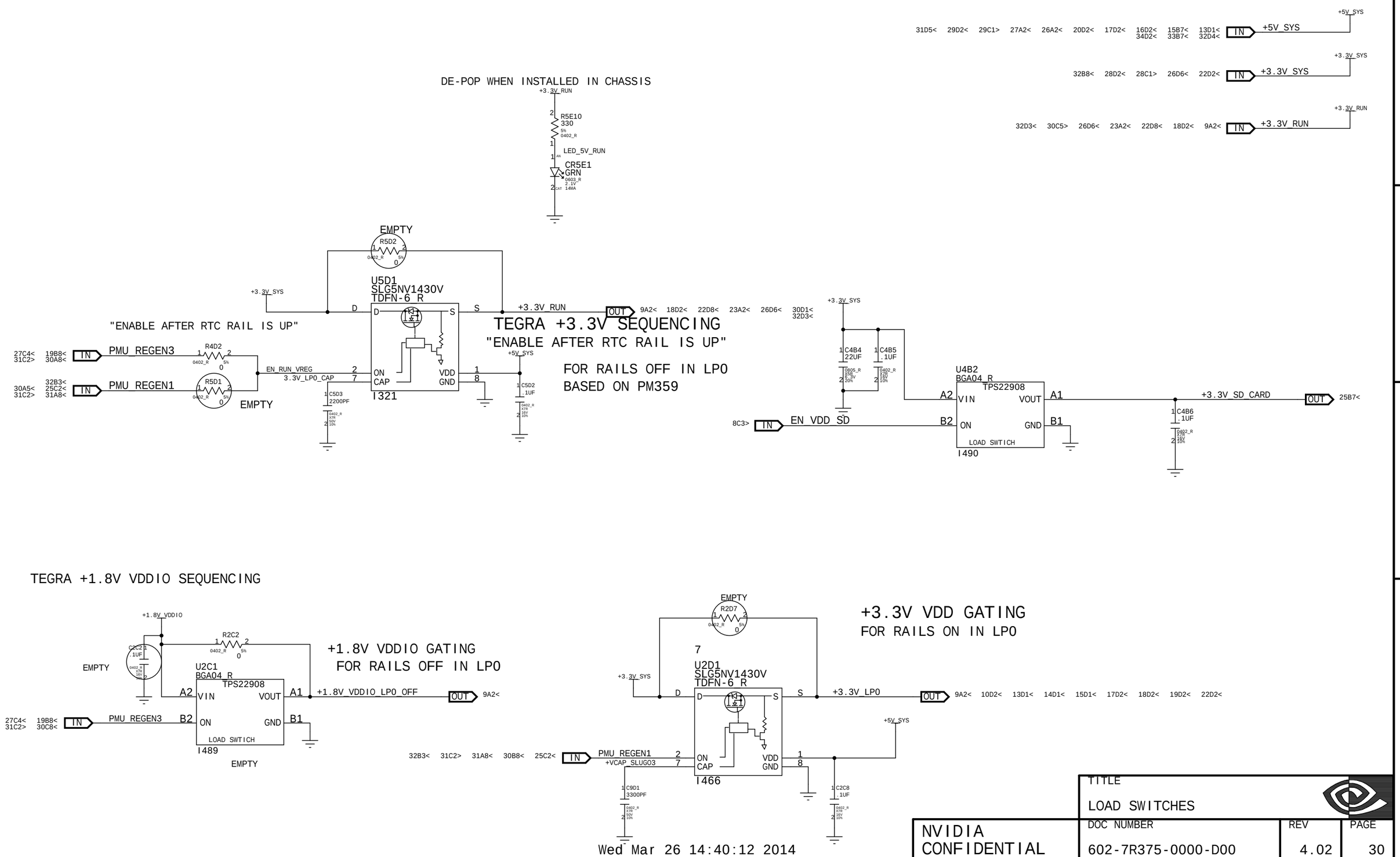
NVIDIA CONFIDENTIAL

TITLE		
+3.3V VR		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	28



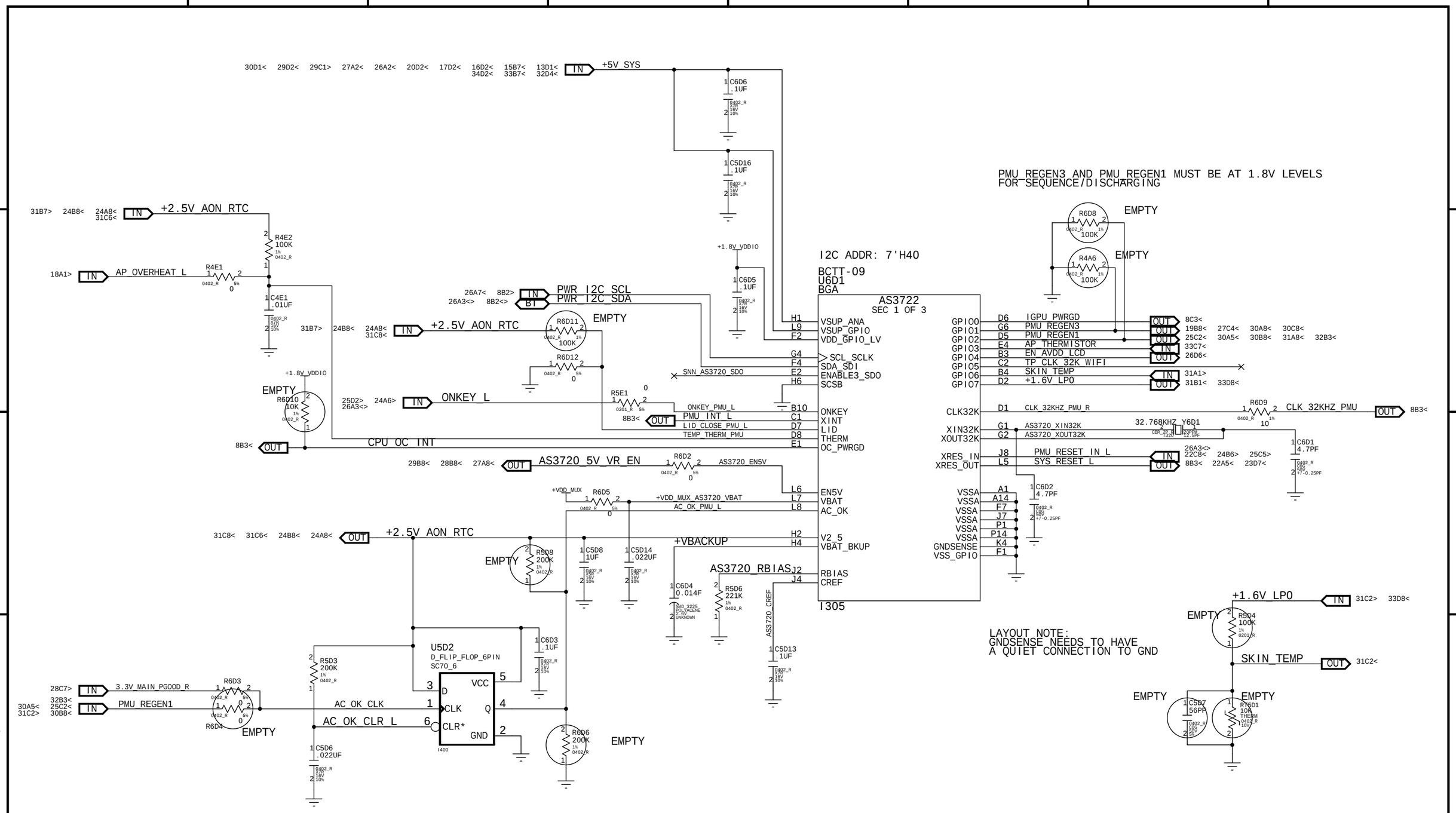
TITLE: +5V VR			
NVIDIA CONFIDENTIAL	DOC NUMBER: 602-7R375-0000-D00	REV: 4.02	PAGE: 29

Wed Mar 26 14:40:11 2014



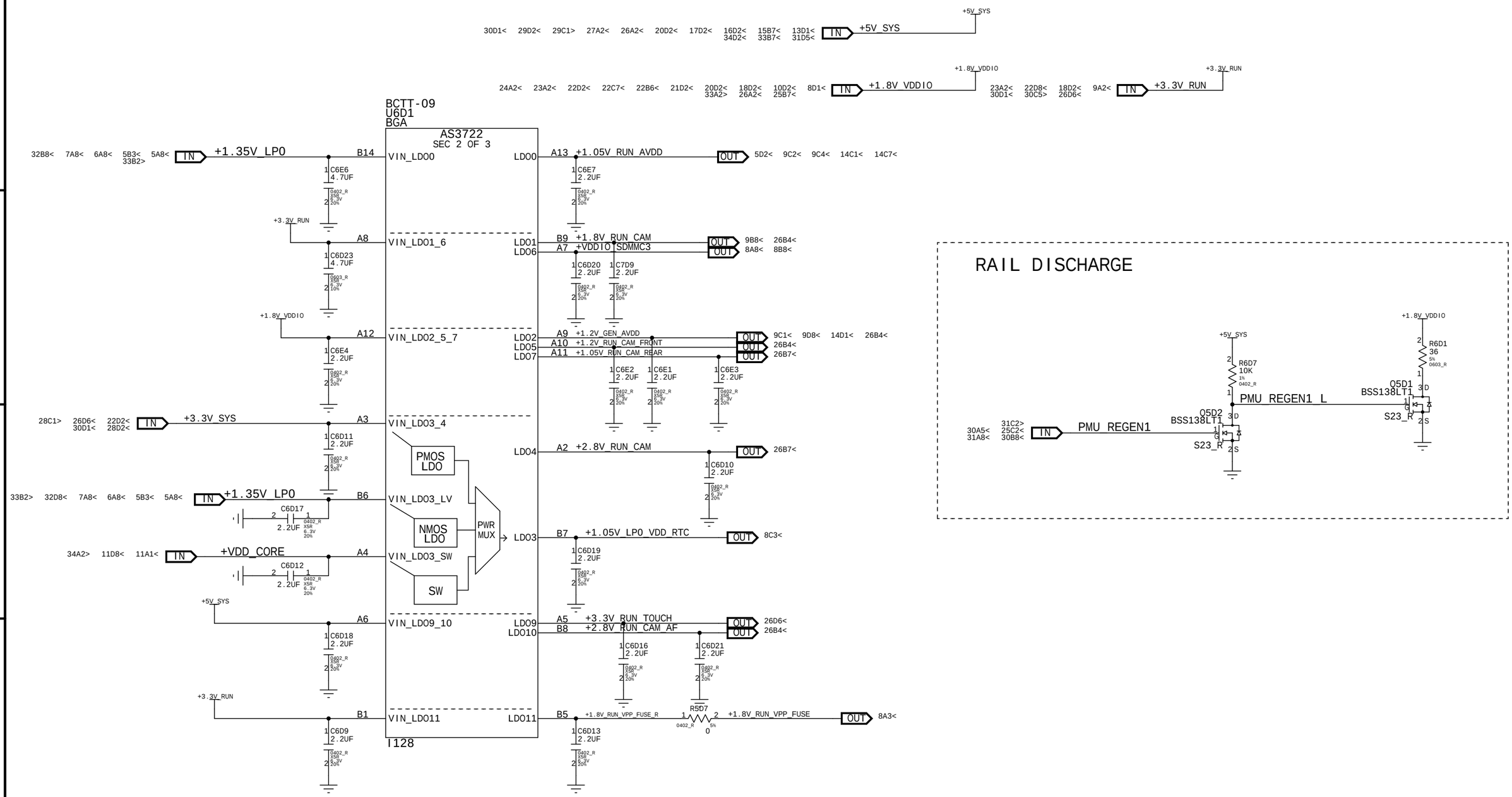
Wed Mar 26 14:40:12 2014

NVIDIA CONFIDENTIAL	TITLE: LOAD SWITCHES		
	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.02	30



Wed Mar 26 14:40:12 2014

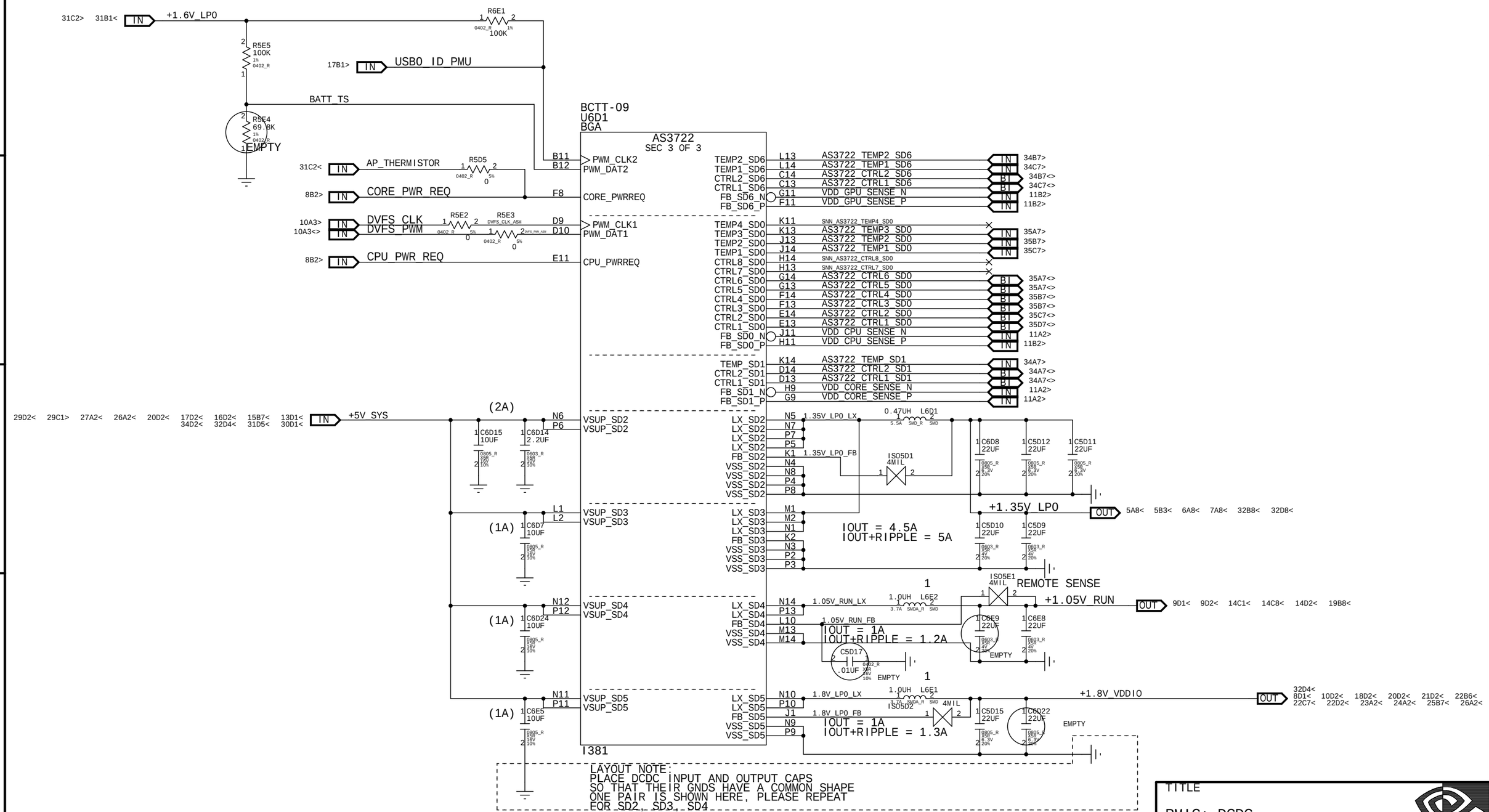
NVIDIA CONFIDENTIAL	TITLE: PMIC: LOGIC AND GPIOS		
	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.02	31



Wed Mar 26 14:40:13 2014

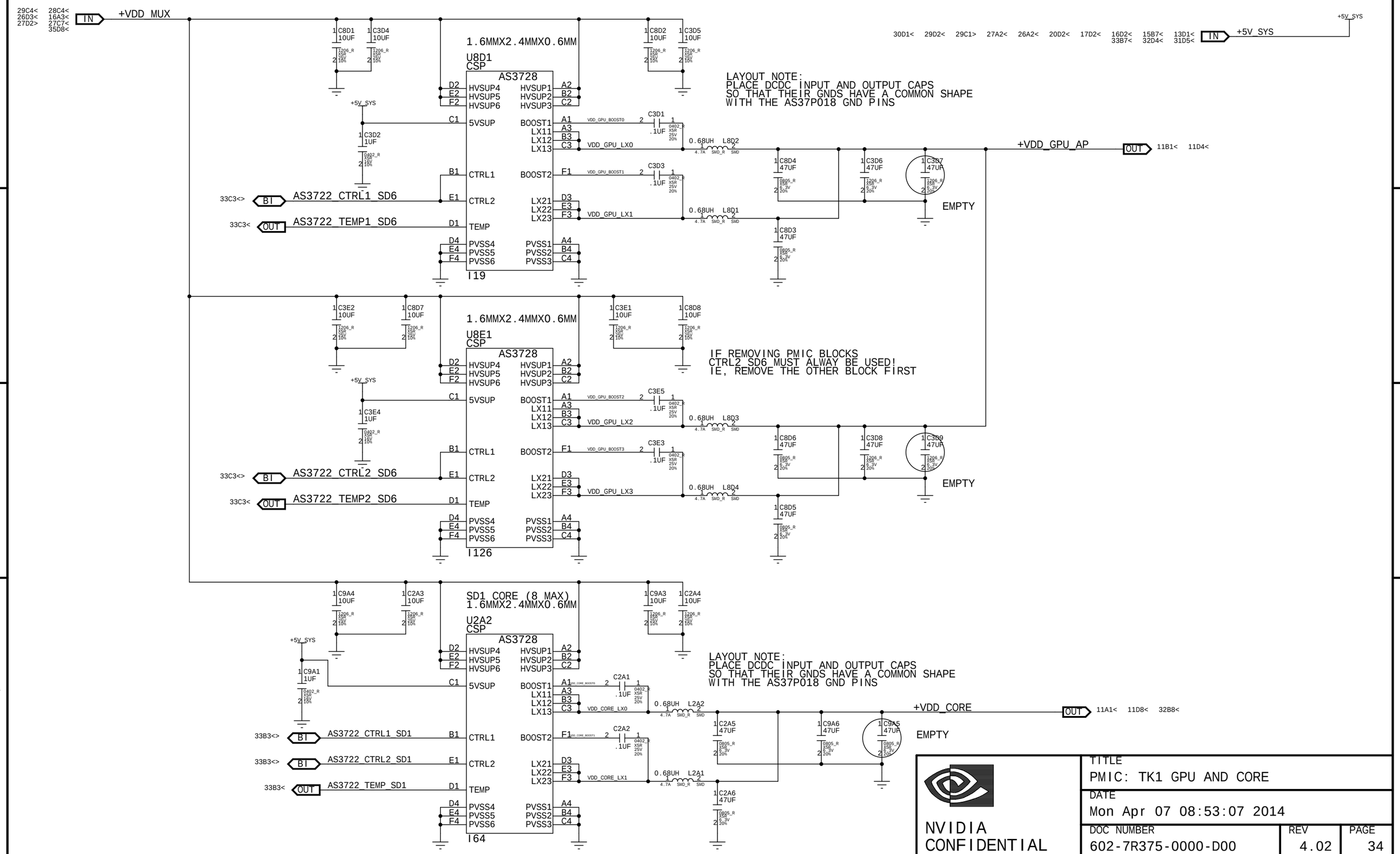
NVIDIA CONFIDENTIAL

TITLE		
PMIC: CNTL, INT SW, LDOS		
DOC NUMBER	REV	PAGE
602-7R375-0000-D00	4.02	32



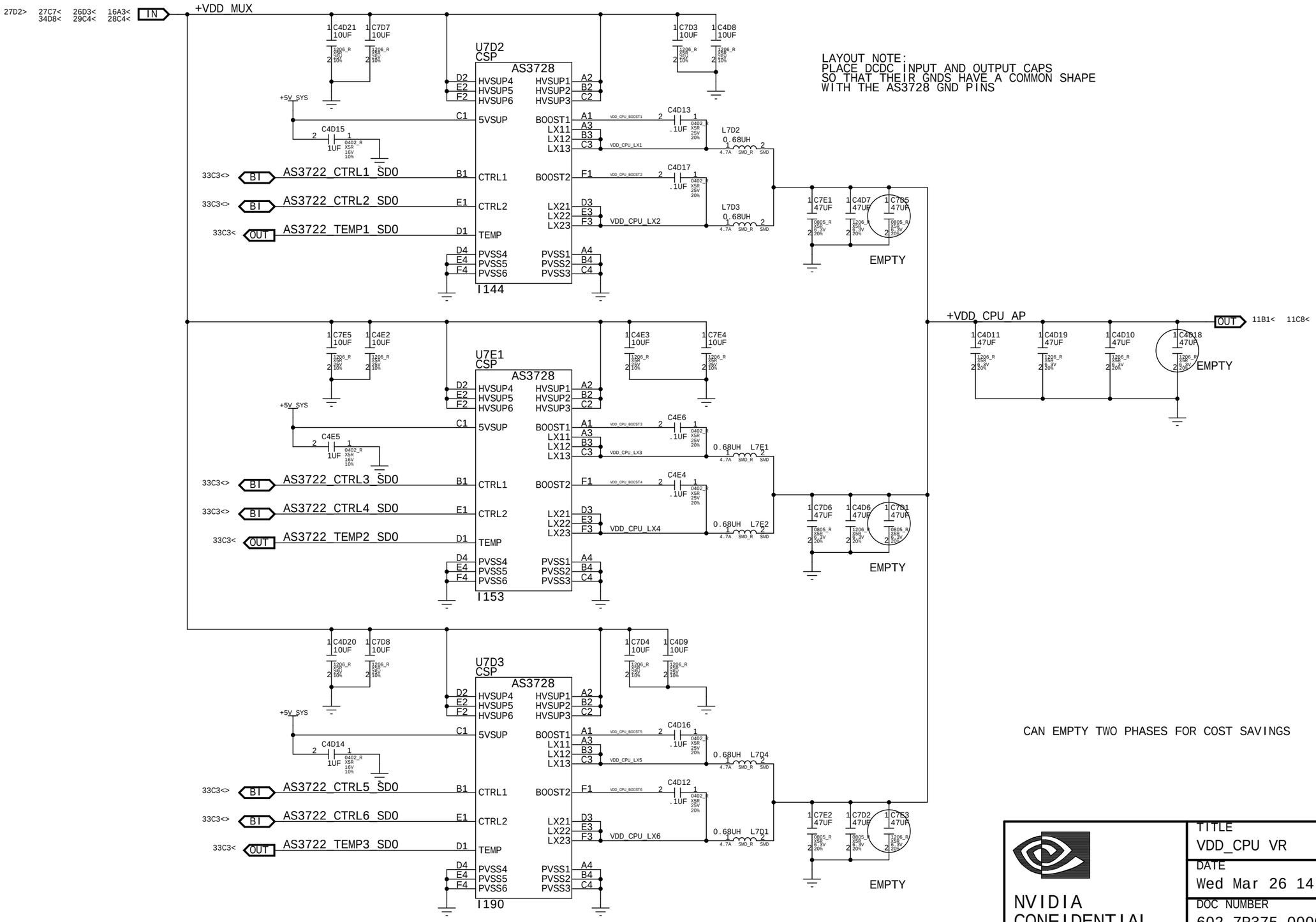
Wed Mar 26 14:40:13 2014

NVIDIA CONFIDENTIAL	TITLE: PMIC: DCDC		
	DOC NUMBER	REV	PAGE
	602-7R375-0000-D00	4.02	33



NVIDIA CONFIDENTIAL

TITLE: PMIC: TK1 GPU AND CORE		
DATE: Mon Apr 07 08:53:07 2014		
DOC NUMBER: 602-7R375-0000-D00	REV: 4.02	PAGE: 34



NVIDIA CONFIDENTIAL

TITLE	VDD_CPU VR
DATE	Wed Mar 26 14:40:14 2014
DOC NUMBER	602-7R375-0000-D00
REV	4.02
PAGE	35

REVISION HISTORY

REVISION 1.00

BOM REVISION D

- RELEASED FAB A

REVISION 1.01

BOM REVISION E

- RELEASED FAB A
- UPDATE I2C MAP (P3)
- STUFF USB_VBUS_EN(0:1) PULLUPS (P17)
- STUFF USB0_VBUS RESISTOR TO 3.3V (P9)
- UPDATE EOL_HDMI CONN (P13)
- CHANGE R5C10 TO 5 MOHM FOR COST SAVINGS (P27)
- CHANGE R3E5 -> 100K OHM; SATA POWER DIVIDER (P16)
- CHANGE DFF CLEAR (P31)
- CHANGE PMIC TO OTP TYPE 9 (P31-33)
- EMPTY C4B2, EXCESS BYPASS FOR 3.3V SD CARD (P30)
- CHANGE SLEW RATE CAP C9D1 TO 3.3NF (P30)
- EMPTY 3.3V RESISTORS ON GEN2 I2C, STUFF 1.8V (P10)
- EMPTY R2D6 & R2D8, ADD R2D7 FOR LAN ISOLATEB (P19)
- BYPASS & EMPTY LOAD SWITCH U2C1 (P30)

REVISION 2.00

BOM REVISION B

- CHANGE RC ON DFF W/ CLOCK OPTIONS (P28,31)
- WIRE GPIO_PK2 TO EXPANSION HDR (P10, P26)
- WIRE +5V_SYS TO R2A5 (P25)
- RESIZE 0 OHM BYPASS RESISTORS TO 0402 (P30)
- CHANGE GEN2_I2C PULLUPS TO +3.3V_LP0 (P10)
- RESIZE FAN RESISTORS (P27)
- REWIRE ISOLATEB ON LAN (P19)
- DIRECT WIRE VDD_GPIO_LV TO +1.8V_VDDIO (P31)
- REPLACE POWER FETS ON 3.3V SWITCHER (P28)
- REPLACE SD CARD SWITCH (P30)
- EMPTY USB ESD PROTECTION (P17)
- EMPTY SD ESD PROTECTION (P25)
- ADD BLEED RESISTORS ON DC INPUT (P27)
- SIMPLIFY FEEDBACK, DROP BLEED RESISTORS (P11)
- TUNE +5V_SYS & +3V3_SYS FOR 3.3UH INDUCTORS (P27-29)
- ADD DEBUG CONNECTOR (P22)
- ADD TEMP SENSOR BUFFERING OPTIONS (P18)
- RELEASED FAB B

REVISION 3.00

BOM REVISION A

- MODIFY EXPANSION HEADER (P11,P26)
- STUFF FRONT PANEL HEADER (P25)
- CHANGE AUDIO HEADER TO LIME/PINK (P21)
- RELEASED FAB C

REVISION 4.00

- REWIRE ONKEY TO KB_COL0 FET (P24)
- REMOVE LED DIODE (P25)
- UART4 INPUTS STUFFING OPTIONS (P24)
- ADD EMI CAP (P21)
- ADD EMI CAP ON VDD_MUX (P29)
- REPLACE EOL SNUBBERS (P24)
- ADD PMU_REGEN3 OPTION FOR LAN (P21)
- RELEASED FAB D

REVISION 4.01

- COSMETIC COMMENT CLEANUP (MULTIPLE PAGES)
- REPLACE Q4E2 (P24)
- RELEASE BOM B FAB D

REVISION 4.02

- ADJUST SEQUENCE ON SD5 (P2)
- ADD FRONT PANEL NOTE - YELLOW STDBY LED (P25)
- REPLACE Q9A1, Q9A2 - AVAILABILITY (P9)
- REPLACE J1A1 - AVAILABILITY (P25)
- RELEASE BOM E FAB D

Wed May 07 10:30:25 2014

Title: Basenet Report
Design: beaver_t124_fabd
Date: May 7 10:45:19 2014

Base nets and synonyms for
beaver_t124_lib.BEAVER_T124_FABD(@beaver_t124_lib.beaver
_t124_fabd(sch_1))

Base Signal	Location([Zone][dir])
+1.2V_GEN_AVDD	9C1< 9D8< 14D1< 26B4< 32C4>
+1.2V_RUN_CAM_FRONT	26B4< 32C4>
+1.05V_LAN_REGOUT	19B3
+1.05V_LAN_REGOUT_L	19C4
+1.05V_LPO_VDD_RTC	8C3< 32B5>
+1.05V_RUN	9D1< 9D2< 14C1< 14C8< 14D2< 19B8< 33A2>
+1.05V_RUN_AVDD	5D2< 9C2< 9C4< 14C1< 14C7< 32D5>
+1.05V_RUN_AVDD_HDMI_PLL_AP	9C3
+1.05V_RUN_AVDD_HDMI_PLL_AP_GATE	9D5
+1.05V_RUN_AVDD_PEX_PLL_AP_F	14C3
+1.05V_RUN_AVDD_SATA_PLL_F	14C7
+1.05V_RUN_CAM_REAR	26B7< 32C4>
+1.6V_LPO	31B1< 31C2> 33D8<
+1.8V_LPO_AVDD_OSC_AP_F	8A4
+1.8V_RUN_AVDD_PLL_UTMIP_AP_F	9A5
+1.8V_RUN_CAM	9B8< 26B4< 32C5>
+1.8V_RUN_VPP_FUSE	8A3< 32A4>
+1.8V_RUN_VPP_FUSE_R	32A5
+1.8V_VDDIO	8D1< 10D2< 18D2< 20D2< 21D2< 22B6< 22C7< 22D2< 23A2< 24A2< 25B7< 26A2< 32D4< 33A2>
+1.8V_VDDIO_LPO_OFF	9A2< 30A6>
+1.35V_LPO	5A8< 5B3< 6A8< 7A8< 32B8< 32D8< 33B2>
+1.35V_LPO_VDDIO_DDR_MCLK_AP	5B3
+2.5V_AON_RTC	24A8< 24B8< 31B7> 31C6< 31C8<
+2.8V_RUN_CAM	26B7< 32B4>
+2.8V_RUN_CAM_AF	26B4< 32A5>
+2V_STBY	27C4> 28B7< 29B7<
+3.3V_342	22D7
+3.3V_AON	27A8< 27B4> 27B8< 28C8<
+3.3V_AVDD_HDMI_AP_GATED	9D5
+3.3V_LPO	9A2< 10D2< 13D1< 14D1< 15D1< 17D2< 18D2< 19D2< 22D2< 30A3>
+3.3V_RUN	9B3 9D2 18B4 23D4 25D4 30D5 32A7 32C7 9A2< 18D2< 22D8< 23A2< 26D6< 30C5> 30D1< 32D3< 9B3 9D2 18B4 23D4 25D4 30D5 32A7 32C7 9A2< 18D2< 22D8< 23A2< 26D6< 30C5> 30D1< 32D3<
+3.3V_RUN	9B3 9D2 18B4 23D4 25D4 30D5 32A7 32C7 9A2< 18D2< 22D8< 23A2< 26D6< 30C5> 30D1< 32D3< 9B3 9D2 18B4 23D4 25D4 30D5 32A7 32C7 9A2< 18D2< 22D8< 23A2< 26D6< 30C5> 30D1< 32D3<
+3.3V_RUN_TOUCH	26D6< 32B5>
+3.3V_SD_CARD	25B7< 30B1>
+3.3V_SYS	22D2< 26D6< 28C1> 28D2< 30D1< 32B8<
+5V_HDMI	13A5
+5V_HDMI_CON	13A4
+5V_SATA	16C2
+5V_STBY	27A7< 27B4> 28C8<
+5V_SYS	13D1< 15B7< 16D2< 17D2< 20D2< 26A2< 27A2< 29C1> 29D2< 30D1< 31D5< 32D4< 33B7< 34D2<
+5V_USB_HS	17B5
+12V_SATA	16B2
+AVDD_LVDS0_PLL_AP_F	9B4
+EMMC_VDDI	23C4
+USB0_VBUS_SW	17C4
+VBACKUP	31B5
+VCAP_SLUGO3	30A5
+VDDIO_SDMMC3	8A8< 8B8< 32C5>
+VDD_1V5_MPCIE	15B4
+VDD_ACIN	27D5
+VDD_CORE	11A1< 11D8< 32B8< 34A2>
+VDD_CPU_AP	11B1< 11C8< 35C2>
+VDD_GPU_AP	11B1< 11D4< 34D2>
+VDD_MIC	20B4
+VDD_MUX	16A3< 26D3< 27C7< 27D2> 28C4< 29C4< 34D8< 35D8<
+VDD_MUX_AS3720_VBAT	31B5
1.05V_RUN_AVDD_HDMI_PLL_AP_EN_L	9C3
1.05V_RUN_FB	33A4
1.05V_RUN_LX	33A4
1.8V_LPO_FB	33A4
1.8V_LPO_LX	33A4
1.35V_LPO_FB	33B4
1.35V_LPO_LX	33B4
1P5V_EN	15B5
3.3V_LPO_CAP	30B7
3.3V_MAIN_COMP	28A7
3.3V_MAIN_COMP_RC	28B7
3.3V_MAIN_CS_N	28B5
3.3V_MAIN_CS_P	28B5
3.3V_MAIN_DRVH	28C5
3.3V_MAIN_DRVH_R	28C5
3.3V_MAIN_DRVL	28C5
3.3V_MAIN_ISO	28B2
3.3V_MAIN_PGOOD_R	28C7> 31A8<
3.3V_MAIN_RST	28B7
3.3V_MAIN_SNUB	28C4
3.3V_MAIN_SW	28C5
3.3V_MAIN_VBST	28C5
3.3V_MAIN_VBST_RC	28C5
3.3V_MAIN_VFB	28B5
3.3V_RUN_AVDD_HDMI_AP_EN_L	9D3
5V_MAIN_COMP	29A7
5V_MAIN_COMP_RC	29A7
5V_MAIN_CS_N	29B5
5V_MAIN_CS_P	29B5
5V_MAIN_DRVH	29C5
5V_MAIN_DRVH_R	29C5
5V_MAIN_DRVL	29B5
5V_MAIN_ISO	29B2
5V_MAIN_PGOOD_R	29C7
5V_MAIN_RST	29B7
5V_MAIN_SNUB	29B4
5V_MAIN_SW	29C5
5V_MAIN_VBST	29B5
5V_MAIN_VBST_RC	29B5
5V_MAIN_VFB	29A5
AC_OK_AP_L	10B4
AC_OK_CLK	31A7
AC_OK_CLR_L	31A7
AC_OK_PMU_L	31B5
AP_FORCE_RECOVERY_L	10C3< 24D5>
AP_OVERHEAT_L	18A1> 31C8<
AP_OVERHEAT_R_L	18A3
AP_OVRHT_G	18A3
AP_THERMISTOR	31C2< 33C7<
AS3720_5V_VR_EN	27A8< 28B8< 29B8< 31B6>
AS3720_CREF	31A4
AS3720_EN5V	31B5
AS3720_RBIAS	31B5
AS3720_XIN32K	31B3
AS3720_XOUT32K	31B3
AS3722_CTRL1_SD0	33C3<> 35D7<>
AS3722_CTRL1_SD1	33B3<> 34A7<>
AS3722_CTRL1_SD6	33C3<> 34C7<>
AS3722_CTRL2_SD0	33C3<> 35C7<>
AS3722_CTRL2_SD1	33B3<> 34A7<>
AS3722_CTRL2_SD6	33C3<> 34B7<>
AS3722_CTRL3_SD0	33C3<> 35B7<>
AS3722_CTRL4_SD0	33C3<> 35B7<>
AS3722_CTRL5_SD0	33C3<> 35A7<>
AS3722_CTRL6_SD0	33C3<> 35A7<>
AS3722_TEMP1_SD0	33C3< 35C7>
AS3722_TEMP1_SD6	33C3< 34C7>
AS3722_TEMP2_SD0	33C3< 35B7>
AS3722_TEMP2_SD6	33C3< 34B7>
AS3722_TEMP3_SD0	33C3< 35A7>
AS3722_TEMP_SD1	33B3< 34A7>
AUD1_VREF1	20B4
AUD1_VREF2	20B4
AUDIO_AVDD	20B4
AUDIO_DACREF	20B4
AUDIO_GND	20A1 20A1 20A2 20A2 20A3 20A3 20A3 20A3 20A6 20B2 20B2 20B2 20B3 20B3 20C3 20C3 21B5 21A5 21A5 21B4

	21B5 21C4
AUDIO_LDO_EN	8C3> 20B7<
AUD_DCVDD	20A4
BATT_TS	33D7
BCLK2	20B6
BD_ID_STRAP0	8D3< 24A3>
BD_ID_STRAP1	8C3< 24A3>
BD_ID_STRAP2	10A3< 24A3>
BD_ID_STRAP3	10A3< 24A3>
BOARD_ID_A0	18D5
BOARD_ID_A1	18D5
BOARD_ID_A2	18D5
BOARD_ID_WP	18D5
BR_UART1_RXD	8C3< 22C7<> 26B7>
BR_UART1_TXD	8C3> 22C7<> 26B4<
C1N	18C4
C1P	18C4
C2N	18C4
C2P	18C4
CAM1_AF_PWDN	9A7> 26A7<
CAM1_GPIO	9B7<> 26A7<>
CAM1_MCLK	9A7> 26A7<
CAM1_PWDN	9A7> 26A7<
CAM2_GPIO	9B7<> 26B3<>
CAM2_MCLK	9B7> 26B4<
CAM2_PWDN	9A7> 26B7<
CAM_FLASH	9A7> 26A7<
CAM_I2C_SCL	9A8> 26B4<
CAM_I2C_SDA	9A8<> 26B7<>
CAM_RST_L	9B7> 26B4<
CAP_SLG_5V_SAT	16B3
CHGPUMP_N1	20B4
CHGPUMP_N2	20B4
CHGPUMP_P1	20B4
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CLK3_OUT	10C7> 26A4<
CLK3_OUT_R	10C6
CLK_32KHZ_PMU	8B3< 31B1>
CLK_32KHZ_PMU_R	31B3
CODEC_IRQ_L	10C3< 20B7>
CORE_PWR_REQ	8B2> 33C7<
CPU_OC_INT	8B3< 31B7>
CPU_PWR_REQ	8B2> 33C7<
CPVDD	20B4
CPVEE	20B4
CPVPP	20B4
CSI_A_CLK_N	9D8> 26B7<
CSI_A_CLK_P	9C8> 26B7<
CSI_A_D0_N	9D8< 26B7>
CSI_A_D0_P	9D8< 26B7>
CSI_A_D1_N	9D8< 26B7>
CSI_A_D1_P	9D8< 26B7>
CSI_B_D0_N	9C8< 26A7>
CSI_B_D0_P	9C8< 26B7>
CSI_B_D1_N	9C8< 26B7>
CSI_B_D1_P	9C8< 26B7>
CSI_E_CLK_N	9C8> 26B4<

CSI_E_CLK_P	9C8> 26B4<
CSI_E_D0_N	9C8< 26B4>
CSI_E_D0_P	9C8< 26B7>
DACDAT2	20C6
DAP2_DIN	10B7< 20C8>
DAP2_DIN_R	20C7
DAP2_DOUT	10B7> 20C8<
DAP2_FS	10A7> 20C8<>
DAP2_SCLK	10A8> 20C8<>
DAP2_SCLK_R	10A6
DAP_MCLK1	10B8> 20B7<
DAP_MCLK1_R	10B6
DDR0_CKE0	4B4> 6C4< 6C8<
DDR0_CKE1	4B4> 6C4< 6C8<
DDR0_CLKN	4D1> 6C4< 6C8<
DDR0_CLKP	4D1> 6C4< 6C8<
DDR0_CLK_TERM	4C3
DDR0_CS0_L	4B4> 6B4< 6B8<
DDR0_CS1_L	4B4> 6B4< 6B8<
DDR0_ODT0	4A4> 6B4< 6B8<
DDR0_ODT1	4A4> 6B4< 6B8<
DDR1_CKE0	4A4> 7C4< 7C8<
DDR1_CKE1	4A4> 7C4< 7C8<
DDR1_CLKN	4C1> 7C4< 7C8<
DDR1_CLKP	4C1> 7C4< 7C8<
DDR1_CLK_TERM	4C2
DDR1_CS0_L	4B4> 7B4< 7B8<
DDR1_CS1_L	4B4> 7B4< 7B8<
DDR1_ODT0	4A4> 7B4< 7B8<
DDR1_ODT1	4A4> 7B4< 7B8<
DDR_A0<5..3>	4C3> 6D4< 6D8<
DDR_A1<5..3>	4C3> 7D4< 7D8<
DDR_A<15..0>	4C3> 6B4< 6B8< 6D4< 6D8< 7B4< 7B8<
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DDR_BA<2..0>	4B3> 6C4< 6C8< 7C4< 7C8<
DDR_CAS_L	4B3> 6C4< 6C8< 7C4< 7C8<
DDR_COMP_PD	5A6
DDR_COMP_PU	5A6
DDR_DM0	4B7> 6C8<
DDR_DM1	4A7> 6C4<
DDR_DM2	4B7> 6C8<
DDR_DM3	4A7> 6C4<
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DDR_DM5	5A7> 7C4<
DDR_DM6	5A7> 7C8<
DDR_DM7	5A7> 7C4<
DDR_DQ<63..0>	4D8<> 5C7<> 6D1<> 6D4<> 7D1<> 7D5<>
DDR_DQS0N	4B7<> 6C8<
DDR_DQS0P	4B7<> 6C8<
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DDR_DQS1P	4A7<> 6C4<
DDR_DQS2N	4B7<> 6C8<
DDR_DQS2P	4B7<> 6C8<
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DDR_DQS5N	5A7<> 7C4<
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DDR_DQS6N	5B7<> 7C8<
DDR_DQS6P	5B7<> 7C8<
DDR_DQS7N	5A7<> 7C4<
DDR_DQS7P	5A7<> 7C4<
DDR_RAS_L	4B3> 6C4< 6C8< 7C4< 7C8<
DDR_RESET_L	4B3> 6B4< 6B8< 7B4< 7B8<
DDR_WE_L	4B3> 6C4< 6C8< 7C4< 7C8<
DDR_ZQ0_U27U1	6B7
DDR_ZQ0_U27U2	6B3
DDR_ZQ0_U28U1	7B7
DDR_ZQ0_U28U2	7B3
DDR_ZQ1_U27U1	6B7
DDR_ZQ1_U27U2	6B3
DDR_ZQ1_U28U1	7B7
DDR_ZQ1_U28U2	7B3
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DP_AUX_P	9B3<> 26D6<>
DSI_CSI_RDN	9B7
DSI_CSI_RUP	9B7
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DVFS_CLK	10A3> 33C7<
DVFS_CLK_ASM	33C6
DVFS_PWM	10A3<> 33C7<
DVFS_PWM_ASM	33C6
EDP_HPD	9B2< 26C6>
EN_AVDD_HDMI	9D2
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EN_AVDD_LCD	26D6< 31C2>
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EN_VDD_BL	8C7> 26D3<
EN_VDD_HDMI	9C1< 9D1< 10A7<> 13A8<
EN_VDD_SD	8C3> 30B4<
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FAN_EN_GATE	27C3
FAN_EN_L	27D3
FAN_PWM	8C3> 27C4<
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FORCE_RECOVERY_L	22C7< 24D5<> 26A3<>
FP_9	25D5
GEN1_I2C_SCL	10B8> 18A6< 18D3< 20B7< 22C4< 26A7<
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GEN1_I2C_SCL_3.3V	15C3< 22C1>
GEN1_I2C_SDA	10B8<> 18A6<> 18D3<> 20B7<> 22C4<>
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GEN1_I2C_SDA_3.3V	15C3<> 22C1<>
GEN2_I2C_SCL_3.3V	10B1> 26D6<
GEN2_I2C_SDA_3.3V	10B1<> 26D6<>
GND	4C2 4C3 5A6 5B4 5B4 5C4 5C4 5D4 6A2
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	6B5 6B8 6B8 7A2 7A3 7A6 7A7 7A7 7A7
	7A8 7A8 7B4 7B4 7B6 7B8 7B8 8A3 8A3

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GPIO_PU5	10B6<> 26A3<>
GPIO_PU6	10B6<> 26A3<>
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HDMI_CEC	9C4<> 13C7<>
HDMI_CEC_A_PU	13B5
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HDMI_DDC_SCL	9C4> 13B7<
HDMI_DDC_SCL_CON	13B5
HDMI_DDC_SDA	9C4<> 13B7<>
HDMI_DDC_SDA_CON	13B5
HDMI_FAULT_L	13A6
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HDMI_INT	9C4< 13D5>
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HDMI_TXC_N	9C4> 13C8<
HDMI_TXC_P	9C4> 13C8<
HDMI_TXD_N<2..0>	9C3> 13D8<
HDMI_TXD_P<2..0>	9C3> 13D8<
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HSIC1_DATA	9A8> 26B3<>
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HSIC1_STROBE	9A8> 26B4<
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JD_MIC_R_L	21C4
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JTAG_RTCK	8A3< 22A4< 22C7>
JTAG_SRST_B_L	22A2
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JTAG_TCK	8A3< 22A4> 22C7>
JTAG_TDI	8A3< 22A4> 22C7>
JTAG_TDO	8A3> 22A4< 22C7<
JTAG_TMS	8A3< 22A4> 22C7>
JTAG_TRST_L	8A3< 22C7<
KB_COL0_AP	8D3< 24A5>
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LAN_RSET	19A4
LAN_TRCT1	19B1
LCD_BL_EN	10C3> 26C6<
LCD_BL_PWM	10C3> 26C6<
LCD_LR	10C3> 24D1>
LCD_TE	8C3> 26C3<
LCD_UD	10C3> 24D1>
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LVDS_RSET	9B5
LVDS_TXD0_N	9B3> 26C3<
LVDS_TXD0_P	9B3> 26D3<
LVDS_TXD1_N	9B3> 26C6<
LVDS_TXD1_P	9B3> 26C6<
LVDS_TXD2_N	9B3> 26C6<
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LVDS_TXD3_P	9B3> 26C3<
LVDS_TXD4_N	9B3> 26C3<
LVDS_TXD4_P	9B3> 26C3<
LV_SATA_EN	16B3
MIC1_BIAS	20B2> 21C5<
MIC1_BIAS_R	20B4
MODEM_SAR0	10C3<> 24D1>
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ONKEY_PMU_L	31B5
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PEX_CLK1_P	14B3> 15D7<
PEX_CLK2_N	14A3> 19C7<
PEX_CLK2_P	14B3> 19C7<
PEX_GIGE_PRSNT_L	8D7
PEX_L0_CLKREQ_L	14A2< 15D7>
PEX_L0_RST_L	14A3> 15C3<
PEX_L1_CLKREQ_L	14A2< 19C7>
PEX_L1_RST_L	14A3> 19C7<
PEX_MINI_PRSNT_L	8D7
PEX_RX2_C_N	16A4< 19C7>
PEX_RX2_C_P	16A4< 19C7>
PEX_RX2_N	14B3< 16A8>
PEX_RX2_P	14B3< 16A8>
PEX_RX4_N	14B3< 15C7>
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PEX_RX20_N	16A7
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PEX_TERMP	14A3
PEX_TX2_C_N	14B3> 16B8<
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PEX_TX20_C_N	16B7
PEX_TX20_C_P	16B7
PEX_WAKE_L	14A3< 15D7> 19B7>
PE_TX4_C_N	15C6
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PMU_REGEN1_L	32B2
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PMU_RESET_IN_L	22C8< 24B6> 25C5> 26A3<> 31B2<
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PWR_I2C_SCL	8B2> 26A7< 31C6<
PWR_I2C_SDA	8B2<> 26A3<> 31C6<>
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SATA_L0_RX_N	14C7< 16D3<
SATA_L0_RX_P	14C7< 16C3<
SATA_L0_TX_N	14C7> 16D3<
SATA_L0_TX_P	14C7> 16D3<
SATA_LED	10B7> 25D7<
SATA_PWR_EN	16A3
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SATA_RX_N	16D2

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SATA_TESTCLKP	14C7
SATA_TX_N	16D2
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SDMMC1_COMP_PU	8B6
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SDMMC3_CD_L	8A8< 25A7>
SDMMC3_CLK	8B8> 25B7<
SDMMC3_CLK_LB_IN	8A7
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SDMMC3_CMD	8B8> 25B7<>
SDMMC3_COMP_PD	8A6
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SDMMC3_DAT<3..0>	8B8<> 25B7<>
SDMMC3_WP_L	8D3< 25A7>
SDMMC4_CLK	8A7> 23D7<
SDMMC4_CMD	8A7> 23D7<>
SDMMC4_COMP_PD	8A6
SDMMC4_COMP_PU	8A6
SDMMC4_DAT<7..0>	8A8<> 23C7<>
SKIN_TEMP	31A1> 31C2<
SNN_1P5V_POK	15B4
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SNN_DIRECTDC_OUT0	14B6
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SNN_DSI_A_D3_P	9C7
SNN_DSI_B_CLK_N	9B7
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SNN_DSI_B_D1_N	9B7
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C7D5	CAP_0805_R	[35C4]
C7D6	CAP_0805_R	[35B4]
C7D7	CAP_1206_R	[35D7]
C7D8	CAP_1206_R	[35A7]
C7D9	CAP_0402_R	[32C5]
C7E1	CAP_0805_R	[35C4]
C7E2	CAP_0805_R	[35A4]
C7E3	CAP_1206_R	[35A4]
C7E4	CAP_1206_R	[35C5]
C7E5	CAP_1206_R	[35C7]
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C8B2	CAP_0402_R	[8A4]
C8B3	CAP_0402_R	[8A4]
C8B4	CAP_0402_R	[6A7]
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C8B6	CAP_0201_R	[6A6]
C8B7	CAP_0201_R	[8B7]
C8B8	CAP_0402_R	[8B7]
C8B9	CAP_0402_R	[8A4]
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C8B12	CAP_0402_R	[10D3]
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C8B15	CAP_0402_R	[8C7]
C8B16	CAP_0402_R	[5C3]
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C8B18	CAP_0201_R	[10D6]
C8B19	CAP_0201_R	[5C4]
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C8B23	CAP_0402_R	[10D6]
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C8B27	CAP_0201_R	[8A4]
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C8B29	CAP_0402_R	[11D7]
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R3A2	RES_0402_R	[23B4]
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U4A3	RST_MON_SOT23_3_R	[22B5]
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U5C1	U_SWREG_TPS51220_QFN32	[28B6]
U5C1	U_SWREG_TPS51220_QFN32	[29B6]
U5D1	SLG5NV1430V_TDFN-6_R	[30C6]
U5D2	D_FLIP_FLOP_6PIN_SC70_6	[31A6]
U6D1	AS3722_BGA	[31B4]
U6D1	AS3722_BGA	[32C6]
U6D1	AS3722_BGA	[33B5]
U7B1	DDR3_X16_BGA100_2	[6C6]
U7C1	DDR3_X16_BGA100_2	[7C2]
U7D1	EMMC_BGA169_1	[23C5]
U7D2	AS3728_CSP	[35D6]
U7D3	AS3728_CSP	[35A6]
U7E1	AS3728_CSP	[35B6]
U8D1	AS3728_CSP	[34D6]
U8E1	AS3728_CSP	[34B6]
U9E1	APL5910_SOP8P_R	[15B5]
Y2C1	XTAL_HC49_R	[19A6]
Y6D1	XTAL_CER_2P_R	[31B2]
Y8B1	XTAL_SMD4P_R	[8A4]

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