Lab title

your names

April 18, 2018

1 Introduction

Introduction with problem overview, your design procedure, and rationale. Be as brief as possible to let me know the big picture of the lab.

2 Interface

Since we have already shown our inputs and outputs for the non-pipelined datapath, there is no need to detail every input and output again. Therefore, you can leave this section blank.

3 Design

This section should show your pipeline analysis spreadsheet where we showed the contents of the pipeline buffers. If you can display it in a readable way in this document, then please do so. Otherwise, include the document or an image of the document in your Git repository and point to that document (it does not have to be a link, just a description of where it is in your repository).

4 Implementation

Show your Verilog code that is pertinent to pipelining. This should include (but is not limited to) datapath.v, iFetch.v, iDecode.v, iExecute.v, iMemory.v, and iWriteBack.v. You only need to show the code in this section. No commentary is necessary.

5 Test

This is where you should show the instructions you used to test your pipeline and the results. Please include:

1. List of assembly commands that you used to test your pipeline

2. Binary for the commands that you used to test your pipeline

3. Simulation Results from these commands. Please make sure that I can see all values in the table. This might be difficult, as there are a lot of signals. You can use multiple diagrams if necessary.

6 Conclusions

Describe the behavior you achieved in your pipeline. Did it work correctly? How long did it take to execute? How long would it take on a non-pipelined datapath? Can you make it run faster by reducing the cycle time? What can be done in future labs to make it run faster?