Baylor University

Department of

Electrical and Computer Engineering

ELC 5311 (graduates), 4396(undergrad)

Advanced Digital Logic Laboratories

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Contents

Lab 1

Basys 2 Programming

We are going to begin with a simple project to turn on LEDs when the switch under them is on. There are eight switches (called sw⟨7⟩ ...sw⟨0⟩), and eight LEDs (called Led⟨7⟩ ...Led⟨0⟩). Our first easy part will be to assign the LEDs to be identical to the switches, see Code 1.1.

Listing 1.1: Verilog code for pass-through

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    13:04:38 08/22/2015
// Design Name:
// Module Name:    pass_through
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module pass_through(
    input [7:0] sw,
        input mclk,
        input btn,
    output [7:0] Led,
    output [0:6] seg,
    output dp,
    output [3:0] an
    );
        wire [3:0] count2;
        wire [15:0] count1;
```

```
        wire [25:0] count0;

assign Led=sw;

sseg_driver my_sseg_conv(
    .num(count2),
    .sseg(seg),
    .dp(dp)
    );

counter #(26) my_timer(
        .clk(mclk),
        .reset(0),
        .count(count0)
        );

counter #(16) my_count(
        .clk(count0[25]),
        .reset(btn),
        .count(count1)
        );

assign count2= count0[19]?
                                                    count0[18]?count1[15:12]:count1[11:8] :
                                                    count0[18]?count1[7:4]:count1[3:0];

assign an    = count0[19]?
                                                    count0[18]?4'b0111:4'b1011 :
                                                    count0[18]?4'b1101:4'b1110;



endmodule
```