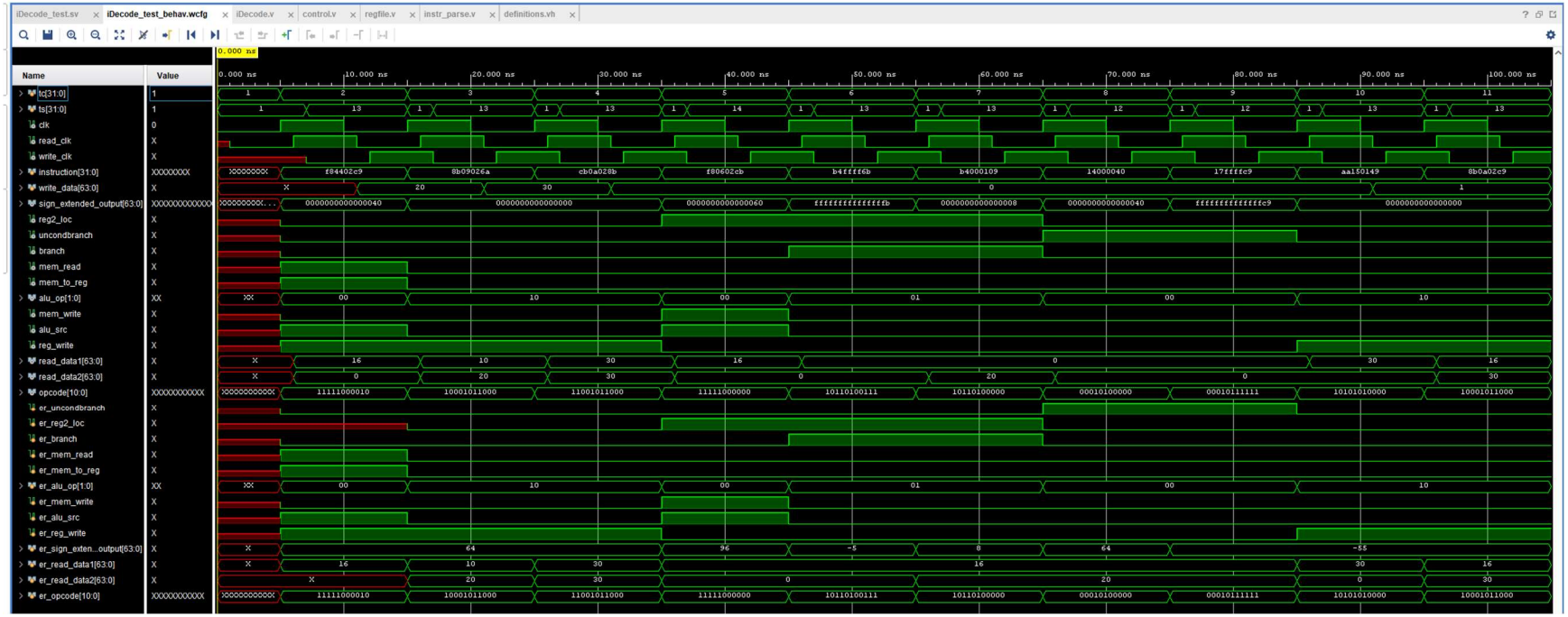
Lab 6 Report – Reese Ford

02/26/2024

	A	B	C	D	E	F	G	H	I	J	K	L
		Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6	Instruction 7	Instruction 8	Instruction 9	Instruction 10	
2	Instruction	LDUR X9, [X22, #64]	ADD X10, X19, X9	SUB X11, X20, X10	STUR X11, [X22, #96]	CBZ X11, -5	CBZ X9, 8	B 64	B -55	ORR X9, X10, X21	AND X9, X22, X10	
3	Machine Instruction (hex)	F844 02C9	8B09 026A	CB0A 028B	F806 02CB	B4FF FF6B	B400 0109	1400 0040	17FF FFC9	AA15 0149	8B0A 02C9	
4	opcode (binary)	11111000010	10001011000	11001011000	11111000000	10110100	10110100	000101	000101	10101010000	10001011000	
5	sign_extended_output (hex)	40	N/A	N/A	60	FFFFFFFFFFFFFFFB	8	40	FFFFFFFFFFFFFFC9	N/A	N/A	
6	reg2_loc	N/A	0	0	1	1	1	0	0	0	0	
7	uncondbranch	0	0	0	0	0	0	1	1	0	0	
8	branch	0	0	0	0	1	1	0	0	0	0	
9	mem_read	1	0	0	0	0	0	0	0	0	0	
10	mem_to_reg	1	0	0	N/A	N/A	N/A	0	0	0	0	
11	alu_op (binary)	00	10	10	00	01	01	0	0	10	10	
12	mem_write	0	0	0	1	0	0	0	0	0	0	
13	alu_src	1	0	0	1	0	0	0	0	0	0	
14	reg_write	1	1	1	0	0	0	0	0	1	1	
15	read_data1	16	10	30	16	0	20	N/A	N/A	30	16	
16	read_data2	N/A	20	30	0	N/A	N/A	N/A	N/A	0	30	
17	write_data	20	30	0	N/A	N/A	N/A	N/A	N/A	1	1	
18												
19	X9	**20**	20	20	20	20	20	20	20	**1**	**1**	
20	X10		**30**	30	30	30	30	30	30	30	30	
21	X11			**0**	0	0	0	0	0	0	0	
22	X19	10	10	10	10	10	10	10	10	10	10	
23	X20	30	30	30	30	30	30	30	30	30	30	
24	X21	0	0	0	0	0	0	0	0	0	0	
25	X22	16	16	16	16	16	16	16	16	16	16	
26												



******* BEGIN TEST RESULTS *******

Test Case 1: | LDUR X9, [X22, #64]

+++ Step 1: Pass: |opcode| time = 7 ns | er = 11111000010 | ar = 11111000010 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |sign_extended_output| time = 7 ns | er = 40 | ar = 40 | er_bits = 64 | ar_bits = 64 +++

+++ Step 3: Pass: |reg2_loc| time = 7 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 7 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |branch| time = 7 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_read| time = 7 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_to_reg| time = 7 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |alu_op| time = 7 ns | er = 0 | ar = 0 | er_bits = 2 | ar_bits = 2 +++

+++ Step 9: Pass: |mem_write| time = 7 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_src| time = 7 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |reg_write| time = 7 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |read_data1| time = 7 ns | er = 16 | ar = 16 | er_bits = 64 | ar_bits = 64 +++

Test Case 2: | ADD X10, X19, X9

+++ Step 1: Pass: |opcode| time = 17 ns | er = 10001011000 | ar = 10001011000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |reg2_loc| time = 17 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 3: Pass: |uncondbranch| time = 17 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |branch| time = 17 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |mem_read| time = 17 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_to_reg| time = 17 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |alu_op| time = 17 ns | er = 10 | ar = 10 | er_bits = 2 | ar_bits = 2 +++

+++ Step 8: Pass: |mem_write| time = 17 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |alu_src| time = 17 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |reg_write| time = 17 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |read_data1| time = 17 ns | er = 10 | ar = 10 | er_bits = 64 | ar_bits = 64 +++

+++ Step 12: Pass: |read_data2| time = 17 ns | er = 20 | ar = 20 | er_bits = 64 | ar_bits = 64 +++

Test Case 3: | SUB X11, X20, X10

+++ Step 1: Pass: |opcode| time = 27 ns | er = 11001011000 | ar = 11001011000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |reg2_loc| time = 27 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 3: Pass: |uncondbranch| time = 27 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |branch| time = 27 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |mem_read| time = 27 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_to_reg| time = 27 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |alu_op| time = 27 ns | er = 10 | ar = 10 | er_bits = 2 | ar_bits = 2 +++

+++ Step 8: Pass: |mem_write| time = 27 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |alu_src| time = 27 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |reg_write| time = 27 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |read_data1| time = 27 ns | er = 30 | ar = 30 | er_bits = 64 | ar_bits = 64 +++

+++ Step 12: Pass: |read_data2| time = 27 ns | er = 30 | ar = 30 | er_bits = 64 | ar_bits = 64 +++

Test Case 4: | STUR X11, [X22, #96]

+++ Step 1: Pass: |opcode| time = 37 ns | er = 11111000000 | ar = 11111000000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |sign_extended_output| time = 37 ns | er = 60 | ar = 60 | er_bits = 64 | ar_bits = 64 +++

+++ Step 3: Pass: |reg2_loc| time = 37 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 37 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |branch| time = 37 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_read| time = 37 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_to_reg| time = 37 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |alu_op| time = 37 ns | er = 0 | ar = 0 | er_bits = 2 | ar_bits = 2 +++

+++ Step 9: Pass: |mem_write| time = 37 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_src| time = 37 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |reg_write| time = 37 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |read_data1| time = 37 ns | er = 16 | ar = 16 | er_bits = 64 | ar_bits = 64 +++

+++ Step 13: Pass: |read_data2| time = 37 ns | er = 0 | ar = 0 | er_bits = 64 | ar_bits = 64 +++

Test Case 5: | CBZ X11, -5

+++ Step 1: Pass: |opcode| time = 47 ns | er = 10110100111 | ar = 10110100111 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |sign_extended_output| time = 47 ns | er = fffffffffffffffb | ar = fffffffffffffffb | er_bits = 64 | ar_bits = 64 +++

+++ Step 3: Pass: |reg2_loc| time = 47 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 47 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |branch| time = 47 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_read| time = 47 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_to_reg| time = 47 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |alu_op| time = 47 ns | er = 1 | ar = 1 | er_bits = 2 | ar_bits = 2 +++

+++ Step 9: Pass: |mem_write| time = 47 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_src| time = 47 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |reg_write| time = 47 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |read_data2| time = 47 ns | er = 0 | ar = 0 | er_bits = 64 | ar_bits = 64 +++

Test Case 6: | CBZ X9, 8

+++ Step 1: Pass: |opcode| time = 57 ns | er = 10110100000 | ar = 10110100000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |sign_extended_output| time = 57 ns | er = 8 | ar = 8 | er_bits = 64 | ar_bits = 64 +++

+++ Step 3: Pass: |reg2_loc| time = 57 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 57 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |branch| time = 57 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_read| time = 57 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_to_reg| time = 57 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |alu_op| time = 57 ns | er = 1 | ar = 1 | er_bits = 2 | ar_bits = 2 +++

+++ Step 9: Pass: |mem_write| time = 57 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_src| time = 57 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |reg_write| time = 57 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |read_data2| time = 57 ns | er = 20 | ar = 20 | er_bits = 64 | ar_bits = 64 +++

Test Case 7: | B 64

+++ Step 1: Pass: |opcode| time = 67 ns | er = 10100000 | ar = 10100000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |sign_extended_output| time = 67 ns | er = 40 | ar = 40 | er_bits = 64 | ar_bits = 64 +++

+++ Step 3: Pass: |reg2_loc| time = 67 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 67 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |branch| time = 67 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_read| time = 67 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_to_reg| time = 67 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |alu_op| time = 67 ns | er = 0 | ar = 0 | er_bits = 2 | ar_bits = 2 +++

+++ Step 9: Pass: |mem_write| time = 67 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_src| time = 67 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |reg_write| time = 67 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

Test Case 8: | B -55

+++ Step 1: Pass: |opcode| time = 77 ns | er = 10111111 | ar = 10111111 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |sign_extended_output| time = 77 ns | er = fffffffffffffc9 | ar = fffffffffffffc9 | er_bits = 64 | ar_bits = 64 +++

+++ Step 3: Pass: |reg2_loc| time = 77 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 77 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |branch| time = 77 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_read| time = 77 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_to_reg| time = 77 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |alu_op| time = 77 ns | er = 0 | ar = 0 | er_bits = 2 | ar_bits = 2 +++

+++ Step 9: Pass: |mem_write| time = 77 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_src| time = 77 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |reg_write| time = 77 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

Test Case 9: | ORR X9, X10, X21

+++ Step 1: Pass: |opcode| time = 87 ns | er = 10101010000 | ar = 10101010000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |reg2_loc| time = 87 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 3: Pass: |uncondbranch| time = 87 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |branch| time = 87 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |mem_read| time = 87 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_to_reg| time = 87 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |alu_op| time = 87 ns | er = 10 | ar = 10 | er_bits = 2 | ar_bits = 2 +++

+++ Step 8: Pass: |mem_write| time = 87 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |alu_src| time = 87 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |reg_write| time = 87 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |read_data1| time = 87 ns | er = 30 | ar = 30 | er_bits = 64 | ar_bits = 64 +++

+++ Step 12: Pass: |read_data2| time = 87 ns | er = 0 | ar = 0 | er_bits = 64 | ar_bits = 64 +++

Test Case 10: | AND X9, X22, X10

+++ Step 1: Pass: |opcode| time = 97 ns | er = 10001011000 | ar = 10001011000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 2: Pass: |reg2_loc| time = 97 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 3: Pass: |uncondbranch| time = 97 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 4: Pass: |branch| time = 97 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |mem_read| time = 97 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |mem_to_reg| time = 97 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |alu_op| time = 97 ns | er = 10 | ar = 10 | er_bits = 2 | ar_bits = 2 +++

+++ Step 8: Pass: |mem_write| time = 97 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |alu_src| time = 97 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |reg_write| time = 97 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |read_data1| time = 97 ns | er = 16 | ar = 16 | er_bits = 64 | ar_bits = 64 +++

+++ Step 12: Pass: |read_data2| time = 97 ns | er = 30 | ar = 30 | er_bits = 64 | ar_bits = 64 +++

Pass Count = 119

Fail Count = 0

******* END TEST RESULTS *******