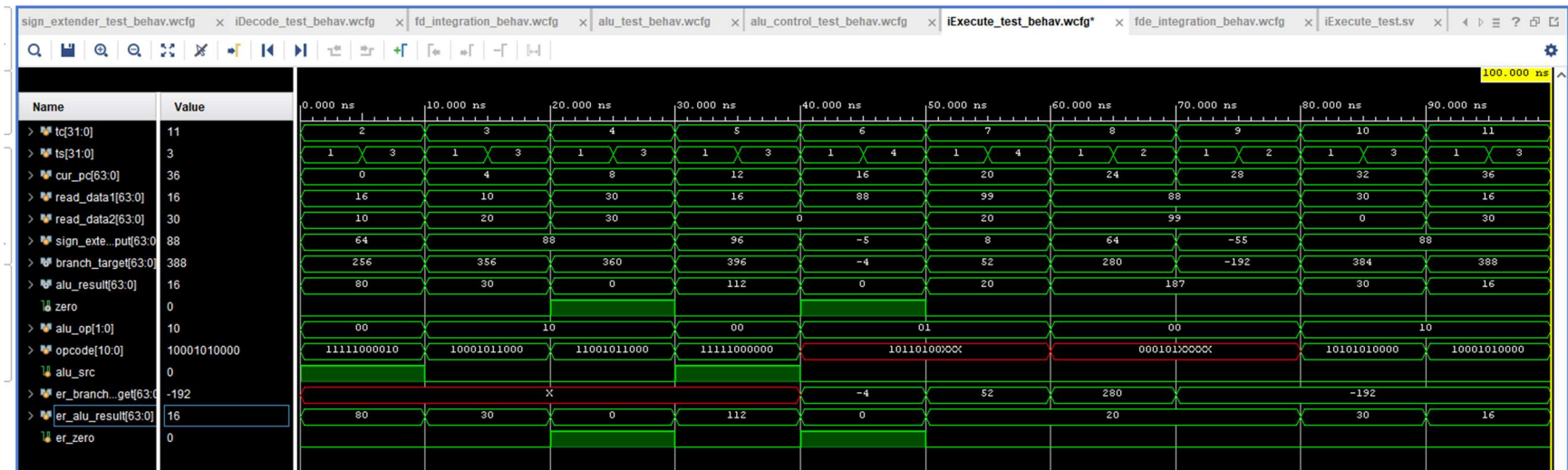


# Reese Ford – Lab 9 Report

04/09/2024



\*\*\*\*\* BEGIN TEST RESULTS \*\*\*\*\*

Test Case 1: | LDUR X9, [X22, #64]

+++ Step 1: Pass: |alu\_result| time = 5 ns | er = 80 | ar = 80 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |zero| time = 5 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 2: | ADD X10, X19, X9

+++ Step 1: Pass: |alu\_result| time = 15 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |zero| time = 15 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 3: | SUB X11, X20, X10

+++ Step 1: Pass: |alu\_result| time = 25 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |zero| time = 25 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 4: | STUR X11, [X22, #96]

+++ Step 1: Pass: |alu\_result| time = 35 ns | er = 112 | ar = 112 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |zero| time = 35 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 5: | CBZ X11, -5

+++ Step 1: Pass: |branch\_target| time = 45 ns | er = -4 | ar = -4 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |alu\_result| time = 45 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 3: Pass: |zero| time = 45 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 6: | CBZ X9, 8

+++ Step 1: Pass: |branch\_target| time = 55 ns | er = 52 | ar = 52 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |alu\_result| time = 55 ns | er = 20 | ar = 20 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 3: Pass: |zero| time = 55 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 7: | B 64

+++ Step 1: Pass: |branch\_target| time = 65 ns | er = 280 | ar = 280 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 8: | B -55

+++ Step 1: Pass: |branch\_target| time = 75 ns | er = -192 | ar = -192 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 9: | ORR X9, X10, X21

+++ Step 1: Pass: |alu\_result| time = 85 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |zero| time = 85 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 10: | AND X9, X22, X10

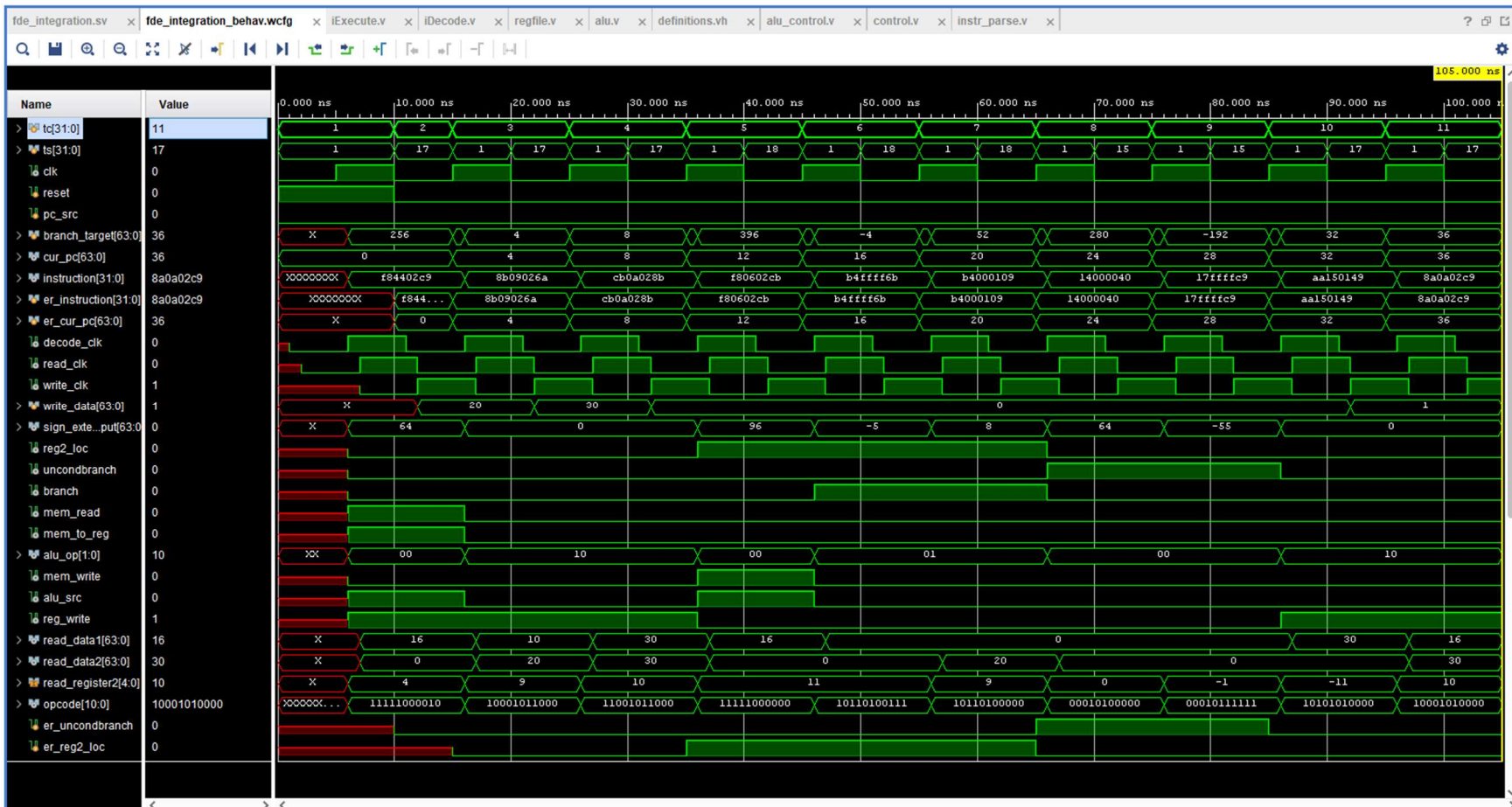
+++ Step 1: Pass: |alu\_result| time = 95 ns | er = 16 | ar = 16 | er\_bits = 64 | ar\_bits = 64 +++

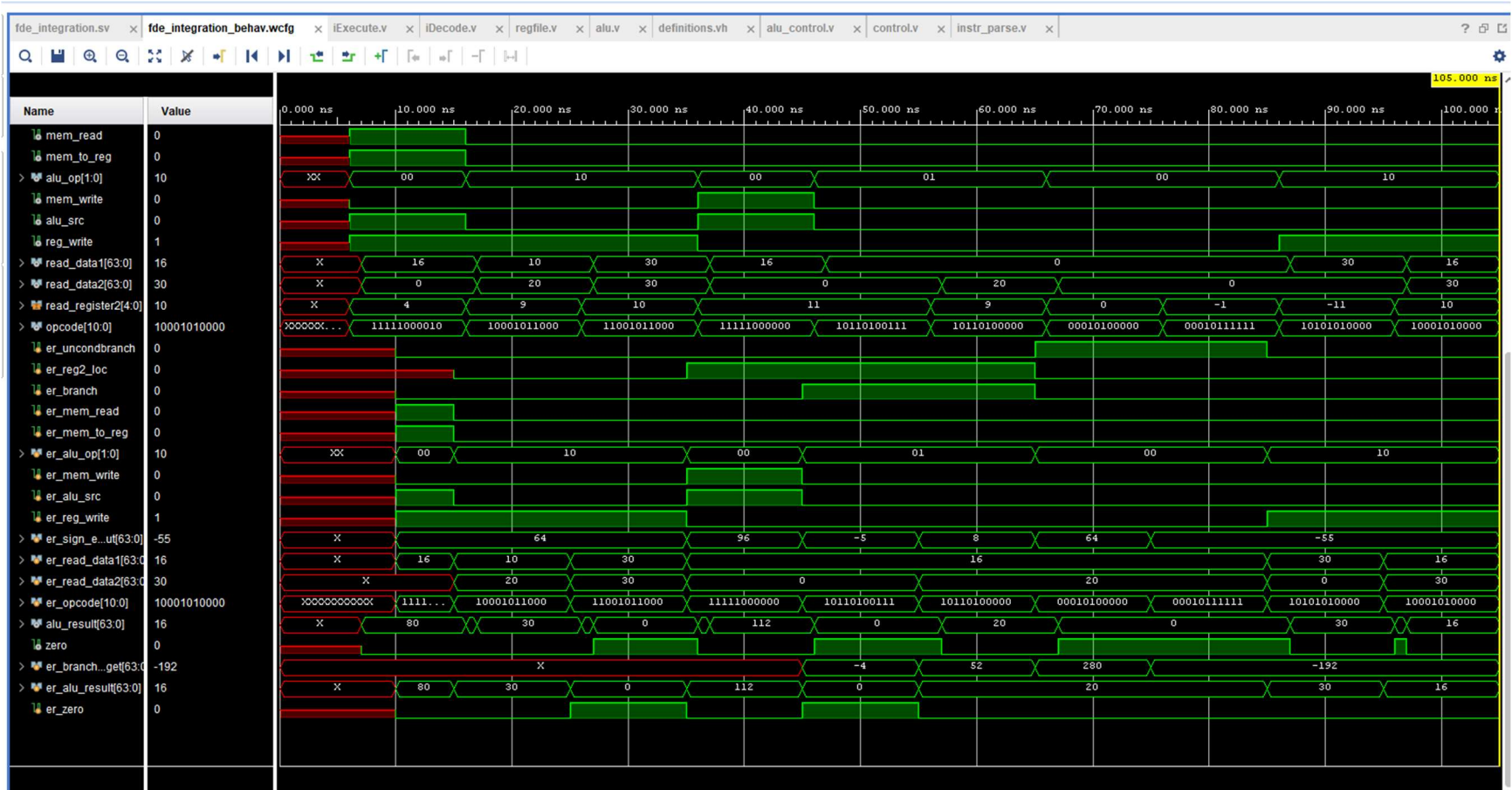
+++ Step 2: Pass: |zero| time = 95 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Pass Count = 20

Fail Count = 0

\*\*\*\*\* END TEST RESULTS \*\*\*\*\*





\*\*\*\*\* BEGIN TEST RESULTS \*\*\*\*\*

Test Case 1: | LDUR X9, [X22, #64]

+++ Step 1: Pass: |cur\_pc| time = 10 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 10 ns | er = f84402c9 | ar = f84402c9 | er\_bits = 32 | ar\_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 10 ns | er = 11111000010 | ar = 11111000010 | er\_bits = 11 | ar\_bits = 11 +++  
+++ Step 4: Pass: |sign\_extended\_output| time = 10 ns | er = 40 | ar = 40 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 5: Pass: |reg2\_loc| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 6: Pass: |uncondbranch| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 7: Pass: |branch| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 8: Pass: |mem\_read| time = 10 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 9: Pass: |mem\_to\_reg| time = 10 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 10: Pass: |alu\_op| time = 10 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++  
+++ Step 11: Pass: |mem\_write| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 12: Pass: |alu\_src| time = 10 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 13: Pass: |reg\_write| time = 10 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 14: Pass: |read\_data1| time = 10 ns | er = 16 | ar = 16 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 15: Pass: |alu\_result| time = 10 ns | er = 80 | ar = 80 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 16: Pass: |zero| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 2: | ADD X10, X19, X9

+++ Step 1: Pass: |cur\_pc| time = 20 ns | er = 4 | ar = 4 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 2: Pass: |instruction| time = 20 ns | er = 8b09026a | ar = 8b09026a | er\_bits = 32 | ar\_bits = 32 +++  
+++ Step 3: Pass: |opcode| time = 20 ns | er = 10001011000 | ar = 10001011000 | er\_bits = 11 | ar\_bits = 11 +++  
+++ Step 4: Pass: |reg2\_loc| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 5: Pass: |uncondbranch| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 6: Pass: |branch| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |mem\_read| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 8: Pass: |mem\_to\_reg| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 9: Pass: |alu\_op| time = 20 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++  
+++ Step 10: Pass: |mem\_write| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 11: Pass: |alu\_src| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 12: Pass: |reg\_write| time = 20 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 13: Pass: |read\_data1| time = 20 ns | er = 10 | ar = 10 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 14: Pass: |read\_data2| time = 20 ns | er = 20 | ar = 20 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 15: Pass: |alu\_result| time = 20 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 16: Pass: |zero| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

#### Test Case 3: | SUB X11, X20, X10

+++ Step 1: Pass: |cur\_pc| time = 30 ns | er = 8 | ar = 8 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 2: Pass: |instruction| time = 30 ns | er = cb0a028b | ar = cb0a028b | er\_bits = 32 | ar\_bits = 32 +++  
+++ Step 3: Pass: |opcode| time = 30 ns | er = 11001011000 | ar = 11001011000 | er\_bits = 11 | ar\_bits = 11 +++  
+++ Step 4: Pass: |reg2\_loc| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 5: Pass: |uncondbranch| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 6: Pass: |branch| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 7: Pass: |mem\_read| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 8: Pass: |mem\_to\_reg| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 9: Pass: |alu\_op| time = 30 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++  
+++ Step 10: Pass: |mem\_write| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |alu\_src| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 12: Pass: |reg\_write| time = 30 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 13: Pass: |read\_data1| time = 30 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 14: Pass: |read\_data2| time = 30 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 15: Pass: |alu\_result| time = 30 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 16: Pass: |zero| time = 30 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 4: | STUR X11, [X22, #96]

+++ Step 1: Pass: |cur\_pc| time = 40 ns | er = 12 | ar = 12 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 2: Pass: |instruction| time = 40 ns | er = f80602cb | ar = f80602cb | er\_bits = 32 | ar\_bits = 32 +++  
+++ Step 3: Pass: |opcode| time = 40 ns | er = 11111000000 | ar = 11111000000 | er\_bits = 11 | ar\_bits = 11 +++  
+++ Step 4: Pass: |sign\_extended\_output| time = 40 ns | er = 60 | ar = 60 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 5: Pass: |reg2\_loc| time = 40 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 6: Pass: |uncondbranch| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 7: Pass: |branch| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 8: Pass: |mem\_read| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 9: Pass: |mem\_to\_reg| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 10: Pass: |alu\_op| time = 40 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++  
+++ Step 11: Pass: |mem\_write| time = 40 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 12: Pass: |alu\_src| time = 40 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 13: Pass: |reg\_write| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 14: Pass: |read\_data1| time = 40 ns | er = 16 | ar = 16 | er\_bits = 64 | ar\_bits = 64 +++



+++ Step 15: Pass: |read\_data2| time = 40 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 16: Pass: |alu\_result| time = 40 ns | er = 112 | ar = 112 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 17: Pass: |zero| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 5: | CBZ X11, -5

+++ Step 1: Pass: |cur\_pc| time = 50 ns | er = 16 | ar = 16 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 50 ns | er = b4ffff6b | ar = b4ffff6b | er\_bits = 32 | ar\_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 50 ns | er = 10110100111 | ar = 10110100111 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 4: Pass: |sign\_extended\_output| time = 50 ns | er = ffffffffbb | ar = ffffffffbb | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 5: Pass: |reg2\_loc| time = 50 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |uncondbranch| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |branch| time = 50 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |mem\_read| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |mem\_to\_reg| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |alu\_op| time = 50 ns | er = 1 | ar = 1 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 11: Pass: |mem\_write| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 12: Pass: |alu\_src| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 13: Pass: |reg\_write| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 14: Pass: |read\_data2| time = 50 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 15: Pass: |branch\_target| time = 50 ns | er = -4 | ar = -4 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 16: Pass: |alu\_result| time = 50 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 17: Pass: |zero| time = 50 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

#### Test Case 6: | CBZ X11, 8

+++ Step 1: Pass: |cur\_pc| time = 60 ns | er = 20 | ar = 20 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 2: Pass: |instruction| time = 60 ns | er = b4000109 | ar = b4000109 | er\_bits = 32 | ar\_bits = 32 +++  
+++ Step 3: Pass: |opcode| time = 60 ns | er = 10110100000 | ar = 10110100000 | er\_bits = 11 | ar\_bits = 11 +++  
+++ Step 4: Pass: |sign\_extended\_output| time = 60 ns | er = 8 | ar = 8 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 5: Pass: |reg2\_loc| time = 60 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 6: Pass: |uncondbranch| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 7: Pass: |branch| time = 60 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 8: Pass: |mem\_read| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 9: Pass: |mem\_to\_reg| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 10: Pass: |alu\_op| time = 60 ns | er = 1 | ar = 1 | er\_bits = 2 | ar\_bits = 2 +++  
+++ Step 11: Pass: |mem\_write| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 12: Pass: |alu\_src| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 13: Pass: |reg\_write| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 14: Pass: |read\_data2| time = 60 ns | er = 20 | ar = 20 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 15: Pass: |branch\_target| time = 60 ns | er = 52 | ar = 52 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 16: Pass: |alu\_result| time = 60 ns | er = 20 | ar = 20 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 17: Pass: |zero| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

#### Test Case 7: | B 64

+++ Step 1: Pass: |cur\_pc| time = 70 ns | er = 24 | ar = 24 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 2: Pass: |instruction| time = 70 ns | er = 14000040 | ar = 14000040 | er\_bits = 32 | ar\_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 70 ns | er = 10100000 | ar = 10100000 | er\_bits = 11 | ar\_bits = 11 +++  
+++ Step 4: Pass: |sign\_extended\_output| time = 70 ns | er = 40 | ar = 40 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 5: Pass: |reg2\_loc| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 6: Pass: |uncondbranch| time = 70 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 7: Pass: |branch| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 8: Pass: |mem\_read| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 9: Pass: |mem\_to\_reg| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 10: Pass: |alu\_op| time = 70 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++  
+++ Step 11: Pass: |mem\_write| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 12: Pass: |alu\_src| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 13: Pass: |reg\_write| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 14: Pass: |branch\_target| time = 70 ns | er = 280 | ar = 280 | er\_bits = 64 | ar\_bits = 64 +++

#### Test Case 8: | B -55

+++ Step 1: Pass: |cur\_pc| time = 80 ns | er = 28 | ar = 28 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 2: Pass: |instruction| time = 80 ns | er = 17ffffc9 | ar = 17ffffc9 | er\_bits = 32 | ar\_bits = 32 +++  
+++ Step 3: Pass: |opcode| time = 80 ns | er = 10111111 | ar = 10111111 | er\_bits = 11 | ar\_bits = 11 +++  
+++ Step 4: Pass: |sign\_extended\_output| time = 80 ns | er = ffffffffcc9 | ar = ffffffffcc9 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 5: Pass: |reg2\_loc| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 6: Pass: |uncondbranch| time = 80 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 7: Pass: |branch| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 8: Pass: |mem\_read| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |mem\_to\_reg| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 10: Pass: |alu\_op| time = 80 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++  
+++ Step 11: Pass: |mem\_write| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 12: Pass: |alu\_src| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 13: Pass: |reg\_write| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 14: Pass: |branch\_target| time = 80 ns | er = -192 | ar = -192 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 9: | ORR X9, X10, X21

+++ Step 1: Pass: |cur\_pc| time = 90 ns | er = 32 | ar = 32 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 2: Pass: |instruction| time = 90 ns | er = aa150149 | ar = aa150149 | er\_bits = 32 | ar\_bits = 32 +++  
+++ Step 3: Pass: |opcode| time = 90 ns | er = 10101010000 | ar = 10101010000 | er\_bits = 11 | ar\_bits = 11 +++  
+++ Step 4: Pass: |reg2\_loc| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 5: Pass: |uncondbranch| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 6: Pass: |branch| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 7: Pass: |mem\_read| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 8: Pass: |mem\_to\_reg| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 9: Pass: |alu\_op| time = 90 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++  
+++ Step 10: Pass: |mem\_write| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 11: Pass: |alu\_src| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 12: Pass: |reg\_write| time = 90 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++  
+++ Step 13: Pass: |read\_data1| time = 90 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++  
+++ Step 14: Pass: |read\_data2| time = 90 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 15: Pass: |alu\_result| time = 90 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 16: Pass: |zero| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 10: | AND X9, X22, X10

+++ Step 1: Pass: |cur\_pc| time = 100 ns | er = 36 | ar = 36 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 100 ns | er = 8a0a02c9 | ar = 8a0a02c9 | er\_bits = 32 | ar\_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 100 ns | er = 10001010000 | ar = 10001010000 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 4: Pass: |reg2\_loc| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |uncondbranch| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |branch| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |mem\_read| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |mem\_to\_reg| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |alu\_op| time = 100 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 10: Pass: |mem\_write| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |alu\_src| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 12: Pass: |reg\_write| time = 100 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 13: Pass: |read\_data1| time = 100 ns | er = 16 | ar = 16 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 14: Pass: |read\_data2| time = 100 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 15: Pass: |alu\_result| time = 100 ns | er = 16 | ar = 16 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 16: Pass: |zero| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Pass Count = 159

Fail Count = 0

\*\*\*\*\* END TEST RESULTS \*\*\*\*\*