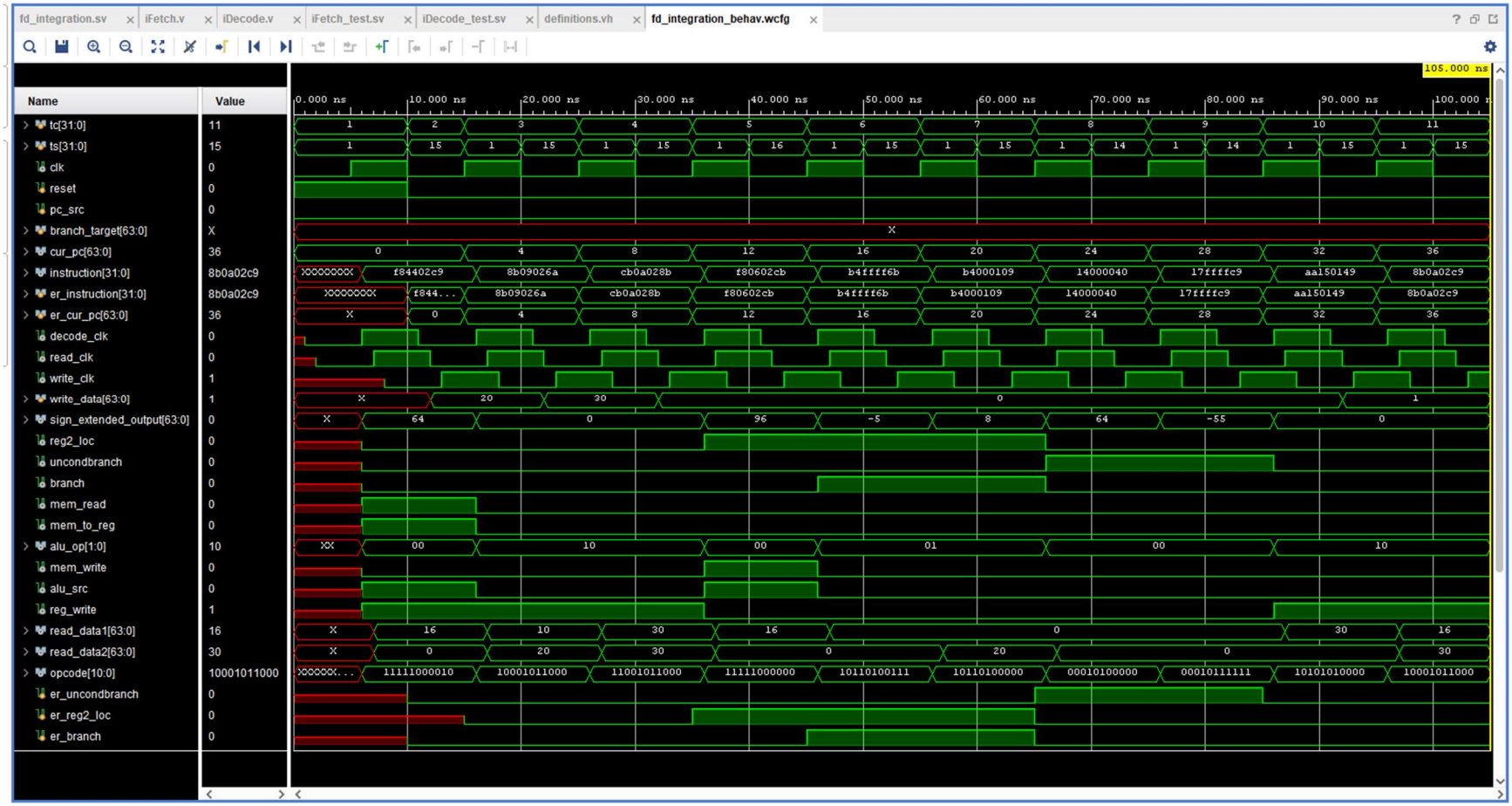
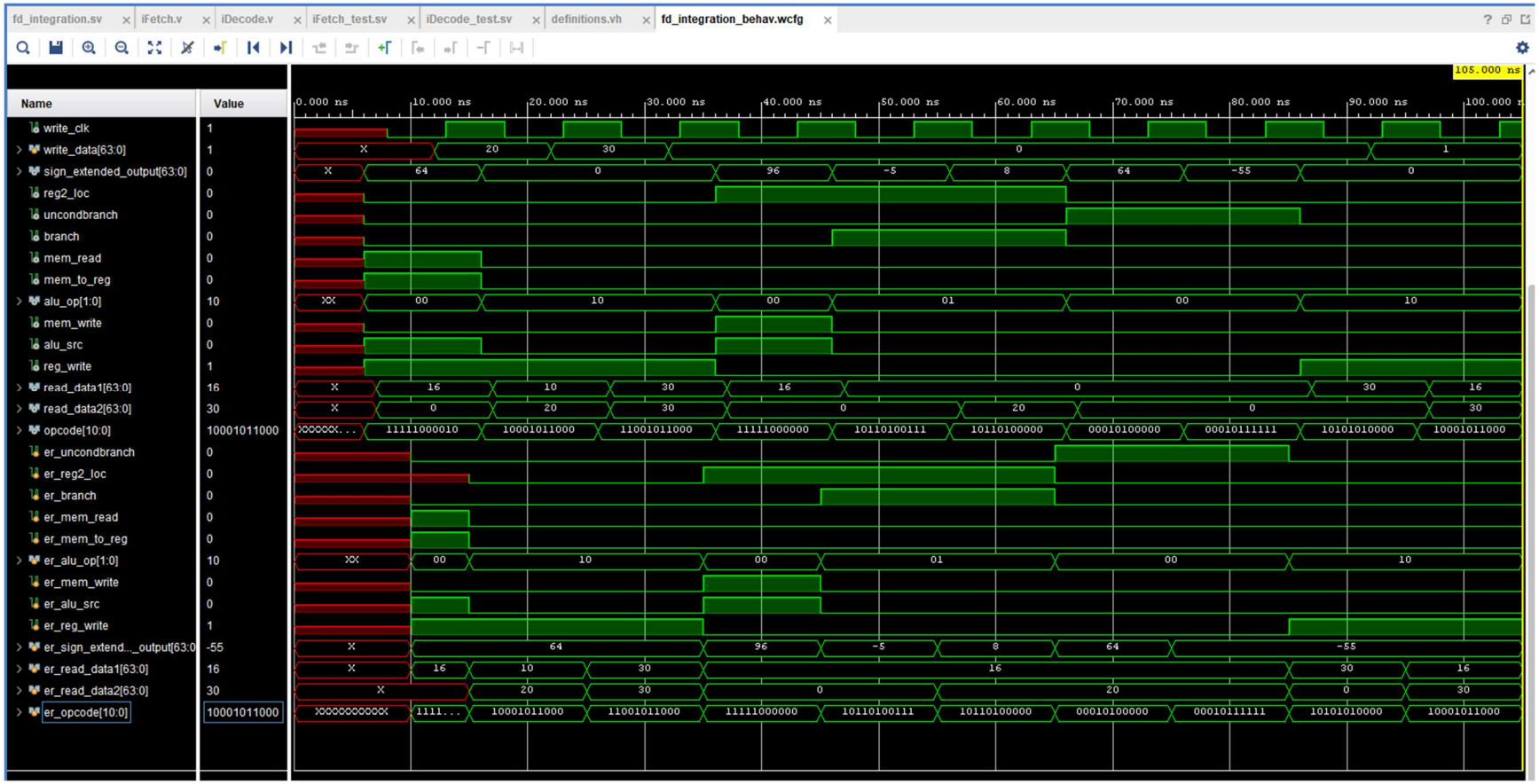
Reese Ford – Lab 7 Report

03/20/2024





******* BEGIN TEST RESULTS *******

Test Case 1: | LDUR X9, [X22, #64]

+++ Step 1: Pass: |cur_pc| time = 10 ns | er = 0 | ar = 0 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 10 ns | er = f84402c9 | ar = f84402c9 | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 10 ns | er = 11111000010 | ar = 11111000010 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |sign_extended_output| time = 10 ns | er = 40 | ar = 40 | er_bits = 64 | ar_bits = 64 +++

+++ Step 5: Pass: |reg2_loc| time = 10 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |uncondbranch| time = 10 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |branch| time = 10 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_read| time = 10 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |mem_to_reg| time = 10 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_op| time = 10 ns | er = 0 | ar = 0 | er_bits = 2 | ar_bits = 2 +++

+++ Step 11: Pass: |mem_write| time = 10 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |alu_src| time = 10 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |reg_write| time = 10 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 14: Pass: |read_data1| time = 10 ns | er = 16 | ar = 16 | er_bits = 64 | ar_bits = 64 +++

Test Case 2: | ADD X10, X19, X9

+++ Step 1: Pass: |cur_pc| time = 20 ns | er = 4 | ar = 4 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 20 ns | er = 8b09026a | ar = 8b09026a | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 20 ns | er = 10001011000 | ar = 10001011000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |reg2_loc| time = 20 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |uncondbranch| time = 20 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |branch| time = 20 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_read| time = 20 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_to_reg| time = 20 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |alu_op| time = 20 ns | er = 10 | ar = 10 | er_bits = 2 | ar_bits = 2 +++

+++ Step 10: Pass: |mem_write| time = 20 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |alu_src| time = 20 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |reg_write| time = 20 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |read_data1| time = 20 ns | er = 10 | ar = 10 | er_bits = 64 | ar_bits = 64 +++

+++ Step 14: Pass: |read_data2| time = 20 ns | er = 20 | ar = 20 | er_bits = 64 | ar_bits = 64 +++

Test Case 3: | SUB X11, X20, X10

+++ Step 1: Pass: |cur_pc| time = 30 ns | er = 8 | ar = 8 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 30 ns | er = cb0a028b | ar = cb0a028b | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 30 ns | er = 11001011000 | ar = 11001011000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |reg2_loc| time = 30 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |uncondbranch| time = 30 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |branch| time = 30 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_read| time = 30 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_to_reg| time = 30 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |alu_op| time = 30 ns | er = 10 | ar = 10 | er_bits = 2 | ar_bits = 2 +++

+++ Step 10: Pass: |mem_write| time = 30 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |alu_src| time = 30 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |reg_write| time = 30 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |read_data1| time = 30 ns | er = 30 | ar = 30 | er_bits = 64 | ar_bits = 64 +++

+++ Step 14: Pass: |read_data2| time = 30 ns | er = 30 | ar = 30 | er_bits = 64 | ar_bits = 64 +++

Test Case 4: | STUR X11, [X22, #96]

+++ Step 1: Pass: |cur_pc| time = 40 ns | er = 12 | ar = 12 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 40 ns | er = f80602cb | ar = f80602cb | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 40 ns | er = 11111000000 | ar = 11111000000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |sign_extended_output| time = 40 ns | er = 60 | ar = 60 | er_bits = 64 | ar_bits = 64 +++

+++ Step 5: Pass: |reg2_loc| time = 40 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |uncondbranch| time = 40 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |branch| time = 40 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_read| time = 40 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |mem_to_reg| time = 40 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_op| time = 40 ns | er = 0 | ar = 0 | er_bits = 2 | ar_bits = 2 +++

+++ Step 11: Pass: |mem_write| time = 40 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |alu_src| time = 40 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |reg_write| time = 40 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 14: Pass: |read_data1| time = 40 ns | er = 16 | ar = 16 | er_bits = 64 | ar_bits = 64 +++

+++ Step 15: Pass: |read_data2| time = 40 ns | er = 0 | ar = 0 | er_bits = 64 | ar_bits = 64 +++

Test Case 5: | CBZ X11, -5

+++ Step 1: Pass: |cur_pc| time = 50 ns | er = 16 | ar = 16 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 50 ns | er = b4ffff6b | ar = b4ffff6b | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 50 ns | er = 10110100111 | ar = 10110100111 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |sign_extended_output| time = 50 ns | er = fffffffffffffffb | ar = fffffffffffffffb | er_bits = 64 | ar_bits = 64 +++

+++ Step 5: Pass: |reg2_loc| time = 50 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |uncondbranch| time = 50 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |branch| time = 50 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_read| time = 50 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |mem_to_reg| time = 50 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_op| time = 50 ns | er = 1 | ar = 1 | er_bits = 2 | ar_bits = 2 +++

+++ Step 11: Pass: |mem_write| time = 50 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |alu_src| time = 50 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |reg_write| time = 50 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 14: Pass: |read_data2| time = 50 ns | er = 0 | ar = 0 | er_bits = 64 | ar_bits = 64 +++

Test Case 6: | CBZ X11, 8

+++ Step 1: Pass: |cur_pc| time = 60 ns | er = 20 | ar = 20 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 60 ns | er = b4000109 | ar = b4000109 | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 60 ns | er = 10110100000 | ar = 10110100000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |sign_extended_output| time = 60 ns | er = 8 | ar = 8 | er_bits = 64 | ar_bits = 64 +++

+++ Step 5: Pass: |reg2_loc| time = 60 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |uncondbranch| time = 60 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |branch| time = 60 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_read| time = 60 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |mem_to_reg| time = 60 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_op| time = 60 ns | er = 1 | ar = 1 | er_bits = 2 | ar_bits = 2 +++

+++ Step 11: Pass: |mem_write| time = 60 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |alu_src| time = 60 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |reg_write| time = 60 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 14: Pass: |read_data2| time = 60 ns | er = 20 | ar = 20 | er_bits = 64 | ar_bits = 64 +++

Test Case 7: | B 64

+++ Step 1: Pass: |cur_pc| time = 70 ns | er = 24 | ar = 24 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 70 ns | er = 14000040 | ar = 14000040 | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 70 ns | er = 10100000 | ar = 10100000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |sign_extended_output| time = 70 ns | er = 40 | ar = 40 | er_bits = 64 | ar_bits = 64 +++

+++ Step 5: Pass: |reg2_loc| time = 70 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |uncondbranch| time = 70 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |branch| time = 70 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_read| time = 70 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |mem_to_reg| time = 70 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_op| time = 70 ns | er = 0 | ar = 0 | er_bits = 2 | ar_bits = 2 +++

+++ Step 11: Pass: |mem_write| time = 70 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |alu_src| time = 70 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |reg_write| time = 70 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

Test Case 8: | B -55

+++ Step 1: Pass: |cur_pc| time = 80 ns | er = 28 | ar = 28 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 80 ns | er = 17ffffc9 | ar = 17ffffc9 | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 80 ns | er = 10111111 | ar = 10111111 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |sign_extended_output| time = 80 ns | er = fffffffffffffc9 | ar = fffffffffffffc9 | er_bits = 64 | ar_bits = 64 +++

+++ Step 5: Pass: |reg2_loc| time = 80 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |uncondbranch| time = 80 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |branch| time = 80 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_read| time = 80 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |mem_to_reg| time = 80 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 10: Pass: |alu_op| time = 80 ns | er = 0 | ar = 0 | er_bits = 2 | ar_bits = 2 +++

+++ Step 11: Pass: |mem_write| time = 80 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |alu_src| time = 80 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |reg_write| time = 80 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

Test Case 9: | ORR X9, X10, X21

+++ Step 1: Pass: |cur_pc| time = 90 ns | er = 32 | ar = 32 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 90 ns | er = aa150149 | ar = aa150149 | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 90 ns | er = 10101010000 | ar = 10101010000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |reg2_loc| time = 90 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |uncondbranch| time = 90 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |branch| time = 90 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_read| time = 90 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_to_reg| time = 90 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |alu_op| time = 90 ns | er = 10 | ar = 10 | er_bits = 2 | ar_bits = 2 +++

+++ Step 10: Pass: |mem_write| time = 90 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |alu_src| time = 90 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |reg_write| time = 90 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |read_data1| time = 90 ns | er = 30 | ar = 30 | er_bits = 64 | ar_bits = 64 +++

+++ Step 14: Pass: |read_data2| time = 90 ns | er = 0 | ar = 0 | er_bits = 64 | ar_bits = 64 +++

Test Case 10: | AND X9, X22, X10

+++ Step 1: Pass: |cur_pc| time = 100 ns | er = 36 | ar = 36 | er_bits = 64 | ar_bits = 64 +++

+++ Step 2: Pass: |instruction| time = 100 ns | er = 8b0a02c9 | ar = 8b0a02c9 | er_bits = 32 | ar_bits = 32 +++

+++ Step 3: Pass: |opcode| time = 100 ns | er = 10001011000 | ar = 10001011000 | er_bits = 11 | ar_bits = 11 +++

+++ Step 4: Pass: |reg2_loc| time = 100 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 5: Pass: |uncondbranch| time = 100 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 6: Pass: |branch| time = 100 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 7: Pass: |mem_read| time = 100 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 8: Pass: |mem_to_reg| time = 100 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 9: Pass: |alu_op| time = 100 ns | er = 10 | ar = 10 | er_bits = 2 | ar_bits = 2 +++

+++ Step 10: Pass: |mem_write| time = 100 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 11: Pass: |alu_src| time = 100 ns | er = 0 | ar = 0 | er_bits = 1 | ar_bits = 1 +++

+++ Step 12: Pass: |reg_write| time = 100 ns | er = 1 | ar = 1 | er_bits = 1 | ar_bits = 1 +++

+++ Step 13: Pass: |read_data1| time = 100 ns | er = 16 | ar = 16 | er_bits = 64 | ar_bits = 64 +++

+++ Step 14: Pass: |read_data2| time = 100 ns | er = 30 | ar = 30 | er_bits = 64 | ar_bits = 64 +++

Pass Count = 139

Fail Count = 0

******* END TEST RESULTS *******