Reese Ford – Lab5 Report

02/19/2024

A screenshot of a computer

Description automatically generated

\*\*\*\*\*\*\* BEGIN TEST RESULTS \*\*\*\*\*\*\*

Test Case 1: | ADD | opcode = 458

+++ Step 1: Pass: |reg2\_loc| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 10 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 10 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 10 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 2: | SUB | opcode = 658

+++ Step 1: Pass: |reg2\_loc| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 20 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 20 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 20 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 3: | AND | opcode = 450

+++ Step 1: Pass: |reg2\_loc| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 30 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 30 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 30 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 4: | ORR | opcode = 550

+++ Step 1: Pass: |reg2\_loc| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 40 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 40 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 40 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 5: | LDUR | opcode = 7c2

+++ Step 1: Pass: |reg2\_loc| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 50 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 50 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 50 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 50 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 50 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 50 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 6: | STUR | opcode = 7c0

+++ Step 1: Pass: |reg2\_loc| time = 60 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 60 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 60 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 60 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 60 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 7: | CBZ | opcode = 5a0

+++ Step 1: Pass: |reg2\_loc| time = 70 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 70 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 70 ns | er = 1 | ar = 1 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 70 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 8: | CBZ | opcode = 5a7

+++ Step 1: Pass: |reg2\_loc| time = 80 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 80 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 80 ns | er = 1 | ar = 1 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 80 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 9: | B | opcode = a0

+++ Step 1: Pass: |reg2\_loc| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 90 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 90 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 90 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 10: | B | opcode = af

+++ Step 1: Pass: |reg2\_loc| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 100 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 100 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 100 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 11: | Invalid | opcode = 765

+++ Step 1: Pass: |reg2\_loc| time = 120 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 2: Pass: |uncondbranch| time = 120 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |branch| time = 120 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |mem\_read| time = 120 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_to\_reg| time = 120 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |alu\_op| time = 120 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 7: Pass: |mem\_write| time = 120 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_src| time = 120 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |reg\_write| time = 120 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Pass Count = 99

Fail Count = 0

\*\*\*\*\*\*\* END TEST RESULTS \*\*\*\*\*\*\*