Lab 6 Report – Reese Ford

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A screenshot of a computer

Description automatically generated

A screenshot of a computer screen

Description automatically generated

\*\*\*\*\*\*\* BEGIN TEST RESULTS \*\*\*\*\*\*\*

Test Case 1: | LDUR X9, [X22, #64]

+++ Step 1: Pass: |opcode| time = 7 ns | er = 11111000010 | ar = 11111000010 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |sign\_extended\_output| time = 7 ns | er = 40 | ar = 40 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 3: Pass: |reg2\_loc| time = 7 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 7 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |branch| time = 7 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_read| time = 7 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |mem\_to\_reg| time = 7 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_op| time = 7 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 9: Pass: |mem\_write| time = 7 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |alu\_src| time = 7 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |reg\_write| time = 7 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 12: Pass: |read\_data1| time = 7 ns | er = 16 | ar = 16 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 2: | ADD X10, X19, X9

+++ Step 1: Pass: |opcode| time = 17 ns | er = 10001011000 | ar = 10001011000 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |reg2\_loc| time = 17 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |uncondbranch| time = 17 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |branch| time = 17 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_read| time = 17 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_to\_reg| time = 17 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |alu\_op| time = 17 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 8: Pass: |mem\_write| time = 17 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |alu\_src| time = 17 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |reg\_write| time = 17 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |read\_data1| time = 17 ns | er = 10 | ar = 10 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 12: Pass: |read\_data2| time = 17 ns | er = 20 | ar = 20 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 3: | SUB X11, X20, X10

+++ Step 1: Pass: |opcode| time = 27 ns | er = 11001011000 | ar = 11001011000 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |reg2\_loc| time = 27 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |uncondbranch| time = 27 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |branch| time = 27 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_read| time = 27 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_to\_reg| time = 27 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |alu\_op| time = 27 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 8: Pass: |mem\_write| time = 27 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |alu\_src| time = 27 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |reg\_write| time = 27 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |read\_data1| time = 27 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 12: Pass: |read\_data2| time = 27 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 4: | STUR X11, [X22, #96]

+++ Step 1: Pass: |opcode| time = 37 ns | er = 11111000000 | ar = 11111000000 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |sign\_extended\_output| time = 37 ns | er = 60 | ar = 60 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 3: Pass: |reg2\_loc| time = 37 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 37 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |branch| time = 37 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_read| time = 37 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |mem\_to\_reg| time = 37 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_op| time = 37 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 9: Pass: |mem\_write| time = 37 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |alu\_src| time = 37 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |reg\_write| time = 37 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 12: Pass: |read\_data1| time = 37 ns | er = 16 | ar = 16 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 13: Pass: |read\_data2| time = 37 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 5: | CBZ X11, -5

+++ Step 1: Pass: |opcode| time = 47 ns | er = 10110100111 | ar = 10110100111 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |sign\_extended\_output| time = 47 ns | er = fffffffffffffffb | ar = fffffffffffffffb | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 3: Pass: |reg2\_loc| time = 47 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 47 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |branch| time = 47 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_read| time = 47 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |mem\_to\_reg| time = 47 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_op| time = 47 ns | er = 1 | ar = 1 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 9: Pass: |mem\_write| time = 47 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |alu\_src| time = 47 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |reg\_write| time = 47 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 12: Pass: |read\_data2| time = 47 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 6: | CBZ X9, 8

+++ Step 1: Pass: |opcode| time = 57 ns | er = 10110100000 | ar = 10110100000 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |sign\_extended\_output| time = 57 ns | er = 8 | ar = 8 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 3: Pass: |reg2\_loc| time = 57 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 57 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |branch| time = 57 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_read| time = 57 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |mem\_to\_reg| time = 57 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_op| time = 57 ns | er = 1 | ar = 1 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 9: Pass: |mem\_write| time = 57 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |alu\_src| time = 57 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |reg\_write| time = 57 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 12: Pass: |read\_data2| time = 57 ns | er = 20 | ar = 20 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 7: | B 64

+++ Step 1: Pass: |opcode| time = 67 ns | er = 10100000 | ar = 10100000 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |sign\_extended\_output| time = 67 ns | er = 40 | ar = 40 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 3: Pass: |reg2\_loc| time = 67 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 67 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |branch| time = 67 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_read| time = 67 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |mem\_to\_reg| time = 67 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_op| time = 67 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 9: Pass: |mem\_write| time = 67 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |alu\_src| time = 67 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |reg\_write| time = 67 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 8: | B -55

+++ Step 1: Pass: |opcode| time = 77 ns | er = 10111111 | ar = 10111111 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |sign\_extended\_output| time = 77 ns | er = ffffffffffffffc9 | ar = ffffffffffffffc9 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 3: Pass: |reg2\_loc| time = 77 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |uncondbranch| time = 77 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |branch| time = 77 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_read| time = 77 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |mem\_to\_reg| time = 77 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 8: Pass: |alu\_op| time = 77 ns | er = 0 | ar = 0 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 9: Pass: |mem\_write| time = 77 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |alu\_src| time = 77 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |reg\_write| time = 77 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

Test Case 9: | ORR X9, X10, X21

+++ Step 1: Pass: |opcode| time = 87 ns | er = 10101010000 | ar = 10101010000 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |reg2\_loc| time = 87 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |uncondbranch| time = 87 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |branch| time = 87 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_read| time = 87 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_to\_reg| time = 87 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |alu\_op| time = 87 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 8: Pass: |mem\_write| time = 87 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |alu\_src| time = 87 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |reg\_write| time = 87 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |read\_data1| time = 87 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 12: Pass: |read\_data2| time = 87 ns | er = 0 | ar = 0 | er\_bits = 64 | ar\_bits = 64 +++

Test Case 10: | AND X9, X22, X10

+++ Step 1: Pass: |opcode| time = 97 ns | er = 10001011000 | ar = 10001011000 | er\_bits = 11 | ar\_bits = 11 +++

+++ Step 2: Pass: |reg2\_loc| time = 97 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 3: Pass: |uncondbranch| time = 97 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 4: Pass: |branch| time = 97 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 5: Pass: |mem\_read| time = 97 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 6: Pass: |mem\_to\_reg| time = 97 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 7: Pass: |alu\_op| time = 97 ns | er = 10 | ar = 10 | er\_bits = 2 | ar\_bits = 2 +++

+++ Step 8: Pass: |mem\_write| time = 97 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 9: Pass: |alu\_src| time = 97 ns | er = 0 | ar = 0 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 10: Pass: |reg\_write| time = 97 ns | er = 1 | ar = 1 | er\_bits = 1 | ar\_bits = 1 +++

+++ Step 11: Pass: |read\_data1| time = 97 ns | er = 16 | ar = 16 | er\_bits = 64 | ar\_bits = 64 +++

+++ Step 12: Pass: |read\_data2| time = 97 ns | er = 30 | ar = 30 | er\_bits = 64 | ar\_bits = 64 +++

Pass Count = 119

Fail Count = 0

\*\*\*\*\*\*\* END TEST RESULTS \*\*\*\*\*\*\*