

AFE4404 用于可穿戴光学心率监测和生物传感的超小型集成 AFE

1 特性

- 发送器：
 - 支持共阳极 LED 配置
 - 动态范围：100dB
 - 6 位可编程 LED 电流最高达 50mA（可扩展至 100mA）
 - 可编程 LED 接通时间
 - 同时支持 3 个 LED，适用于优化型血氧饱和度 (SpO2) 测量、心率监测 (HRM) 或多波长 HRM
- 接收器：
 - 以 24 位二进制补码格式表示光电二极管的电流输入
 - TIA 输入端的独立直流偏移减法 DAC，用于每个 LED 和环境相位
 - ADC 输出端的数字环境减法
 - 可编程互阻抗增益：10kΩ 至 2MΩ
 - 动态范围：100dB
 - 动态节能模式，可使电流降至 200μA 以下
- 脉冲频率：10SPS 至 1000SPS
- 灵活的脉冲排序和定时控制
- 灵活的时钟选项：
 - 外部时钟：4MHz 至 60MHz 输入时钟
 - 内部时钟：4MHz 振荡器
- I²C 接口
- 工作温度范围：-20°C 至 70°C
- 2.6mm × 1.6mm DSBGA 封装，0.5mm 间距
- 电源：Rx: 2V 至 3.6V；Tx: 3V 至 5.25V；IO: 1.8V 至 3.6V

2 应用

- 光学心率监测 (HRM)
- 心率变异分析 (HRV)
- 血氧饱和度 (SpO2 测量)
- 最大摄氧量
- 卡路里消耗

3 说明

AFE4404 是一款面向光学生物传感应用的模拟前端 (AFE)，例如心率监测 (HRM) 和血氧饱和度 (SpO2) 测量。该器件支持三个开关发光二极管 (LED) 和一个光电二极管。光电二极管的电流通过互阻抗放大器 (TIA) 转换为电压，并使用模数转换器 (ADC) 进行数字化。ADC 代码可使用 I²C 接口读出。AFE 还配有带 6 位电流控制的全集成 LED 驱动器。该器件具有宽动态范围的发送和接收电路，有助于感测超小信号电平。

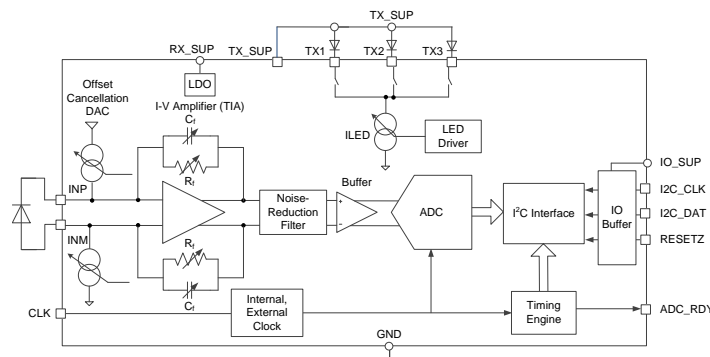
器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
AFE4404	DSBGA (15)	2.60mm × 1.60mm ⁽²⁾

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

(2) 请参见图 92 中的尺寸 D × E。

4 简化框图



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5 修订历史记录

日期	修订版本	注释
2015 年 6 月	*	首次发布。

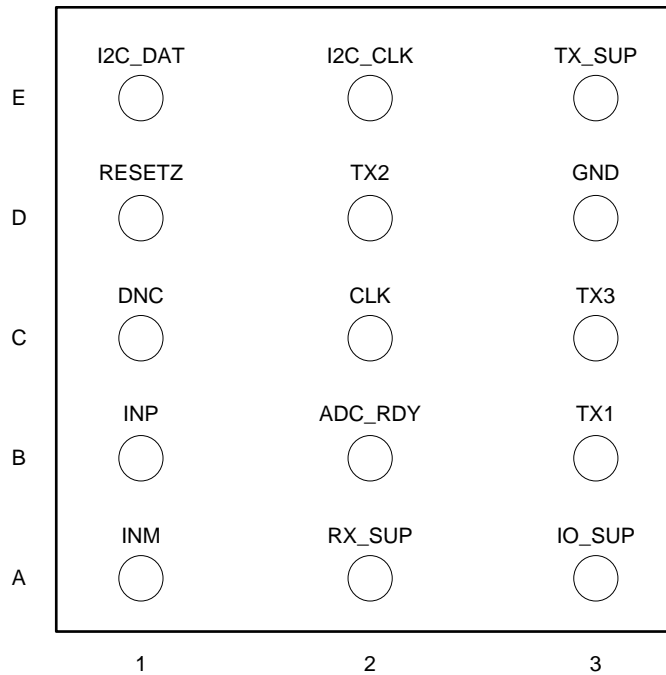
6 Device Comparison Table

PRODUCT	PACKAGE-LEAD	LED DRIVE CONFIGURATION	LED DRIVE CURRENT (mA, Max)	OPERATING TEMPERATURE RANGE	OPTIMIZED APPLICATION
AFE4400	VQFN-40	H-bridge, common anode	50	0°C to 70°C	Finger-clip pulse oximeters
AFE4490	VQFN-40	H-bridge, common anode	200	–40°C to 85°C	Clinical-grade pulse oximeters
AFE4403	DSBGA-36	H-bridge, common anode	100	–20°C to 70°C	Clinical pulse oximeter patches, wearables
AFE4404	DSBGA-15	Common anode	50 ⁽¹⁾	–20°C to 70°C	Wearable optical bio-sensing

(1) Mode that doubles the range to 100 mA with additional restrictions.

7 Pin Configuration and Functions

**YZP Package
15-Ball DSBGA
Bottom View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADC_RDY	B2	Digital	ADC ready interrupt signal (output)
CLK	C2	Digital	Clock input or output, selectable based on register. Default is input (external clock mode). Can be set via a register to output the clock when the oscillator is enabled. ⁽¹⁾⁽²⁾
DNC	C1		Do not connect (leave floating)
GND	D3	Ground	Common ground for transmitter and receiver
I2C_CLK	E2	Digital	I ² C clock input, external pullup resistor to IO_SUP (for example, 10 kΩ)
I2C_DAT	E1	Digital	I ² C data, external pullup resistor to IO_SUP (for example, 10 kΩ)
INM	A1	Analog	Connect only to anode of photodiode ⁽³⁾
INP	B1	Analog	Connect only to cathode of photodiode ⁽³⁾
IO_SUP	A3	Supply	Separate supply for digital I/O. Must be less than or equal to RX_SUP. Can be tied to RX_SUP.
RESETZ	D1	Digital	RESETZ or PWDN: function based on (active low) duration of RESETZ pulse ⁽⁴⁾ . A 25-μs to 50-μs duration = RESETZ active. A > 200-μs duration = PWDN active.
RX_SUP	A2	Supply	Receiver supply; 1-μF decapacitor to GND
TX1	B3	Analog	Transmit output, LED1
TX2	D2	Analog	Transmit output, LED2
TX3	C3	Analog	Transmit output, LED3
TX_SUP	E2	Supply	Transmitter supply; 1-μF decapacitor to GND

- (1) Depending on whether external clock mode or internal oscillator mode is used, extra series or shunt resistors are recommended on the CLK pin. For more details, refer to the [Typical Application](#) section.
- (2) In both hardware power-down (PVDN) and software power-down (PDNAFE) modes, the CLK pin is driven by the AFE to 0 V. Therefore, if operating in external clock mode, take care to shut off the external clock to the AFE when in these power-down modes.
- (3) Maintain the indicated polarity of photodiode connections to the AFE input pins.
- (4) A RESET pulse must be applied after power-up to ensure that the registers are all reset to their default values.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range	RX_SUP to GND	–0.3	4	V
	IO_SUP to GND	–0.3	4	V
	RX_SUP-IO_SUP	–0.3		V
	TX_SUP to GND	–0.3	6	V
Voltage applied to analog inputs		Max [–0.3, (GND – 0.3)]	Min [4, (RX_SUP + 0.3)]	V
Voltage applied to digital inputs		Max [–0.3, (GND – 0.3)]	Min [4, (IO_SUP + 0.3)]	V
Maximum duty cycle (cumulative): sum of all LED phase durations as a function of the total period	50-mA LED current mode (ILED_2X = 0)		10%	
	100-mA LED current mode (ILED_2X = 1)		3%	
Storage temperature, T _{stg}		–60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN		MAX	UNIT
RX_SUP	Receiver supply		2		3.6	V
IO_SUP	Input/output supply		1.7		Min (3.6, RX_SUP)	V
TX_SUP	Transmitter supply	50-mA LED current mode (ILED_2X = 0)	3.0 or (0.5 + V _{LED}) ⁽¹⁾ , whichever is greater		5.25	V
		100-mA LED current mode (ILED_2X = 1)	3.0 or (1.0 + V _{LED}) ⁽¹⁾ , whichever is greater		5.25	V
Digital inputs			0		IO_SUP	V
Analog inputs			0		RX_SUP	V
Operating temperature range			−20		70	°C

- (1) V_{LED} refers to the maximum voltage drop across the external LED (at maximum LED current). This value is usually governed by the forward drop voltage (V_{FB}) of the LED.

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AFE4404	UNIT
		YZP (DSBGA)	
		15 BALLS	
R _{θJA}	Junction-to-ambient thermal resistance	67.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	12.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	12.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

8.5 Electrical Characteristics

Minimum and maximum specifications are at $T_A = -20^{\circ}\text{C}$ to 70°C , typical specifications are at 25°C . $\text{TX_SUP} = 4\text{ V}$, $\text{RX_SUP} = \text{IO_SUP} = 3\text{ V}$, 100-Hz PRF, 8-MHz external clock (with CLKDIV_EXTMODE set to divide-by-2), detector $C_{\text{IN}} = 50\text{ pF}$, and CLKDIV_PRF set to 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE REPETITION FREQUENCY						
PRF ⁽¹⁾	Pulse repetition frequency		10 ⁽²⁾		1000	SPS
RECEIVER						
	Offset cancellation DAC current range			–7 to 7		μA
	Offset cancellation DAC current step			0.47		μA
	TIA gain setting			10k to 2M		Ω
	C_f setting			2.5 to 25		pF
	Switched RC filter bandwidth			2.5 ⁽³⁾		kHz
	ADC averages		1		16	
	Detector capacitance	Differential capacitance between INP, INN	10		200	pF
TRANSMITTER						
	LED current range	I _{LED_2X} = 0		0 to 50		mA
		I _{LED_2X} = 1		0 to 100		mA
	LED current resolution			6		Bits
CLOCKING (Internal Oscillator)						
	Frequency			4		MHz
	Accuracy	Room temperature		±1		%
	Frequency drift with temperature	Full temperature range		±0.5		%
	Jitter (RMS)			100		ps
	Output clock high level			IO_SUP		V
	Output clock low level			0		V
	Output clock rise and fall times	10% to 90%, 15-pF load capacitance on CLK pin		< 30		ns
CLOCKING (External Clock)						
	Frequency range ⁽⁴⁾		4		60	MHz
	Input clock high level			IO_SUP		V
	Input clock low level			0		V
	Input capacitance of CLK pin	Capacitance to ground		< 4		pF
I²C INTERFACE						
	Maximum clock speed			400		kHz
	I ² C slave address			58		Hex
PERFORMANCE						
	Receiver SNR	SNR over a 20-Hz bandwidth for a 500-kΩ gain setting, 50% FS output, 2% LED and sampling pulse duration, ADC averages set to 16		100		dBFS ⁽⁵⁾
	Transmitter SNR	SNR over a 20-Hz bandwidth for a 50-mA LED current setting		100		dBFS ⁽⁵⁾

(1) PRF refers to the rate at which samples from each of the four phases are output from the AFE.

(2) To extend the lower range of PRF down to 10 Hz, program the CLKDIV_PRF setting.

(3) The effective bandwidth of the switched RC filter scales as a function of the sampling duty cycle. For example, at 2% sampling width duty cycle, the effective bandwidth of the switched RC filter is approximately 50 Hz.

(4) With appropriate setting of the clock divider ratio (CLKDIV_EXTMODE).

(5) dBFS refers to a full scale voltage of 2 V.

Electrical Characteristics (continued)

Minimum and maximum specifications are at $T_A = -20^{\circ}\text{C}$ to 70°C , typical specifications are at 25°C . $\text{TX_SUP} = 4\text{ V}$, $\text{RX_SUP} = \text{IO_SUP} = 3\text{ V}$, 100-Hz PRF, 8-MHz external clock (with CLKDIV_EXTMODE set to divide-by-2), detector $\text{C}_{\text{IN}} = 50\text{ pF}$, and CLKDIV_PRF set to 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
RX_SUP current	Normal operation, external clock mode		620		μA	
	Normal operation, internal oscillator mode		670		μA	
	In dynamic power-down mode ⁽⁶⁾		300		μA	
	Hardware power-down (PWDN) mode ⁽⁷⁾		3		μA	
	Software power-down (PDNAFE) mode ⁽⁷⁾		35		μA	
IO_SUP current	Normal operation, external clock mode		20		μA	
	Normal operation, internal oscillator mode		5		μA	
	In dynamic power-down mode ⁽⁶⁾		20		μA	
	Hardware power-down (PWDN) mode ⁽⁷⁾		3		μA	
	Software power-down (PDNAFE) mode ⁽⁷⁾		5		μA	
TX_SUP current	Normal operation, external clock mode ⁽⁸⁾		25		μA	
	Normal operation, internal oscillator mode ⁽⁸⁾		25		μA	
	In dynamic power-down mode ⁽⁶⁾⁽⁸⁾		5		μA	
	Hardware power-down (PWDN) mode ⁽⁷⁾⁽⁸⁾		2		μA	
	Software power-down (PDNAFE) mode ⁽⁷⁾⁽⁸⁾		2		μA	
TRANSIENT RECOVERY						
t _{ACTIVE}	Recovery from PWDN mode	Time for signal chain to be functional ⁽⁹⁾	10		ms	
t _{CHANNEL}	Recovery from any event causing a change in signal characteristics	PRF = 100 Hz, sampling duty cycle (each phase) of 2% ⁽¹⁰⁾	200		ms	
DIGITAL INPUTS						
V _{IH}	High-level input voltage		0.9 × IO_SUP	IO_SUP	V	
V _{IL}	Low-level input voltage		0	0.1 × IO_SUP	V	
DIGITAL OUTPUTS						
V _{OH}	High-level output voltage		IO_SUP		V	
V _{OL}	Low-level output voltage		0		V	

(6) In dynamic power-down mode for 90% and active mode for 10% of the period.

(7) External clock mode with the external clock switched off.

(8) LED currents set to 0 mA.

(9) For full performance to be restored, a longer time as governed by t_{CHANNEL} can be applicable.

(10) t_{CHANNEL} scales inversely with the sampling duty cycle.

8.6 Timing Requirements

		MIN	TYP	MAX	UNIT
$t_{\text{I2C_RISE}}$	I ² C data rise time with a 10-k Ω pullup resistor with a 20-pF load from I ² C data to GND		1200		ns
$t_{\text{I2C_FALL}}$	I ² C data fall time (when the data line is pulled down by the AFE) with a 20-pF load from I ² C data to GND		28		ns
$t_{\text{ADC_RDY_RISE}}$	ADC_RDY rise time (10% to 90%) with a 15-pF capacitive load to ground		21		ns
$t_{\text{ADC_RDY_FALL}}$	ADC_RDY fall time (90% to 10%) with a 15-pF capacitive load to ground		21		ns

8.7 Typical Characteristics

At 25°C, TX_SUP = 4 V, RX_SUP = IO_SUP = 3.3 V, 100-Hz PRF, 25% duty cycle, $R_f = 500 \text{ k}\Omega$, C_f is adjusted to keep the TIA time constant at 1/10th of the sampling duration, 8-MHz external clock (with CLKDIV_EXTMODE set to divide-by-2), CLKDIV_PRF = 1, detector $C_{IN} = 50 \text{ pF}$, ADC averaging = max allowed, SNR (dBFS) = noise referred to full-scale range of 2 V, noise integrated from 1 Hz to Nyquist ($= \text{PRF} / 2$), and values assigned to CLKDIV_EXTMODE and CLK_DIV_PRF parameters correspond to division ratios controlled by these modes, unless otherwise specified.

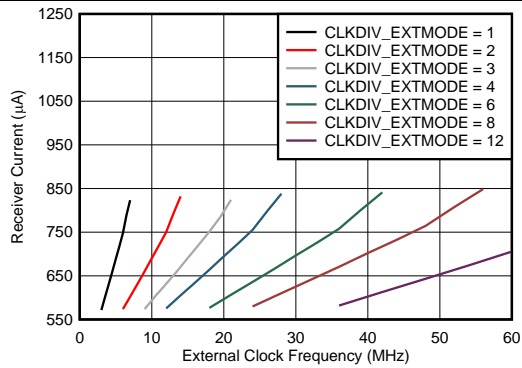
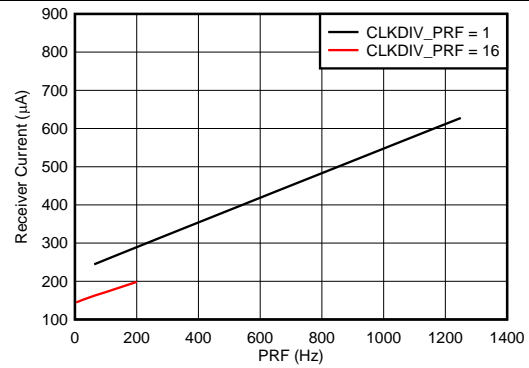
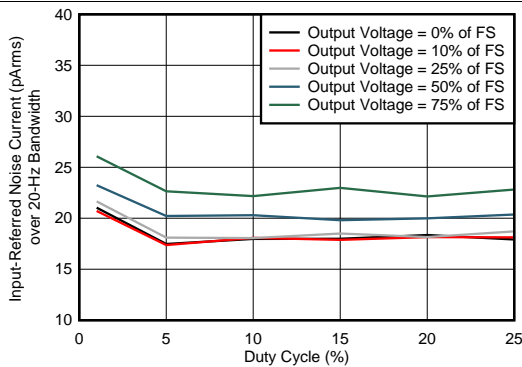


Figure 1. Receiver Current vs External Clock Frequency



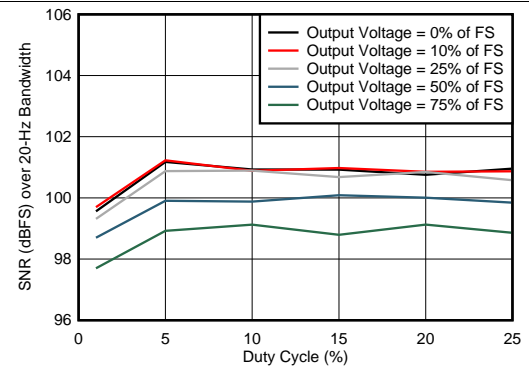
Active window = 500 μs , LED pulse = 100 μs ,
all four DYNAMIC bits set to 1

Figure 2. Receiver Current vs PRF in Dynamic Power-Down Mode



Duty cycle (x-axis) refers to the sampling duration expressed as a percentage of the pulse repetition period.

Figure 3. Input-Referred Noise Current in 20-Hz Bandwidth vs Duty Cycle for Different Output Levels (As a Percentage of Full-Scale)



Duty cycle (x-axis) refers to the sampling duration expressed as a percentage of the pulse repetition period.

Figure 4. Signal-to-Noise Ratio in 20-Hz Bandwidth vs Duty Cycle for Different Output Levels (As a Percentage of Full-Scale)

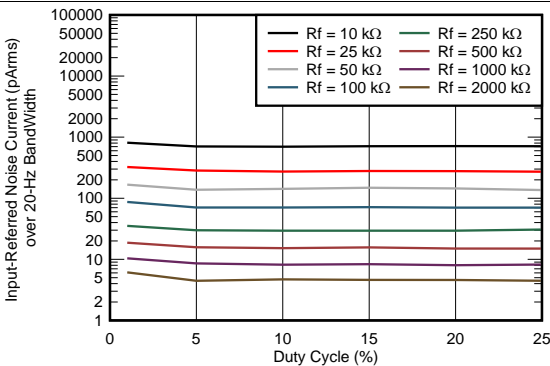


Figure 5. Receiver Input-Referred Noise Current in 20-Hz BW vs Duty Cycle (Different TIA Gain Settings)

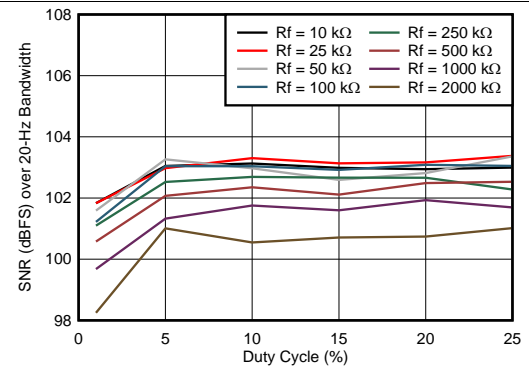


Figure 6. Receiver SNR in 20-Hz BW vs Duty Cycle (Different TIA Gain Settings)

Typical Characteristics (continued)

At 25°C, TX_SUP = 4 V, RX_SUP = IO_SUP = 3.3 V, 100-Hz PRF, 25% duty cycle, $R_f = 500 \text{ k}\Omega$, C_f is adjusted to keep the TIA time constant at 1/10th of the sampling duration, 8-MHz external clock (with CLKDIV_EXTMODE set to divide-by-2), CLKDIV_PRF = 1, detector $C_{IN} = 50 \text{ pF}$, ADC averaging = max allowed, SNR (dBFS) = noise referred to full-scale range of 2 V, noise integrated from 1 Hz to Nyquist ($= \text{PRF} / 2$), and values assigned to CLKDIV_EXTMODE and CLK_DIV_PRF parameters correspond to division ratios controlled by these modes, unless otherwise specified.

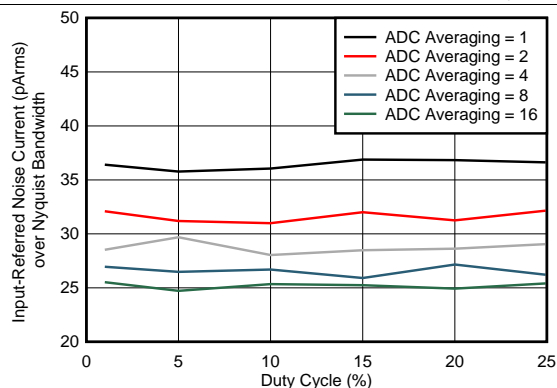


Figure 7. Receiver Input-Referred Noise Current over Nyquist Bandwidth vs Duty Cycle (Different ADC Averaging)

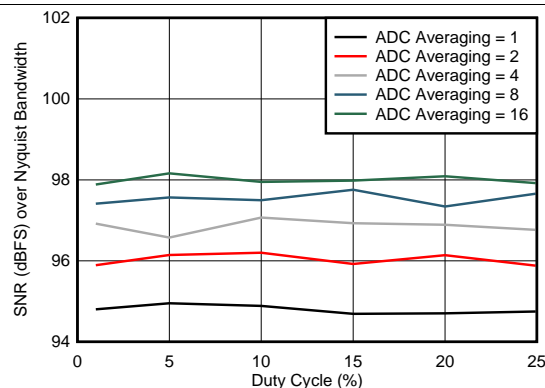


Figure 8. Receiver Signal-to-Noise Ratio over Nyquist Bandwidth vs Duty Cycle (Different ADC Averaging)

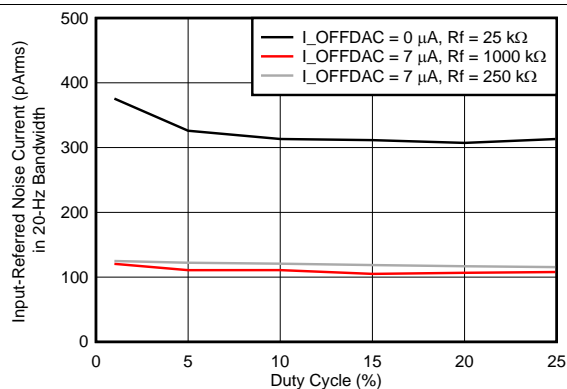


Figure 9. Receiver Input-Referred Noise in 20-Hz Bandwidth vs Duty Cycle (Different offset cancellation DAC Currents)

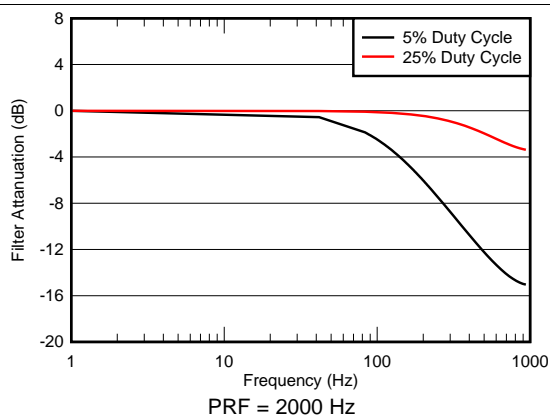


Figure 10. Response of the Switched-RC Filter at the AFE Output

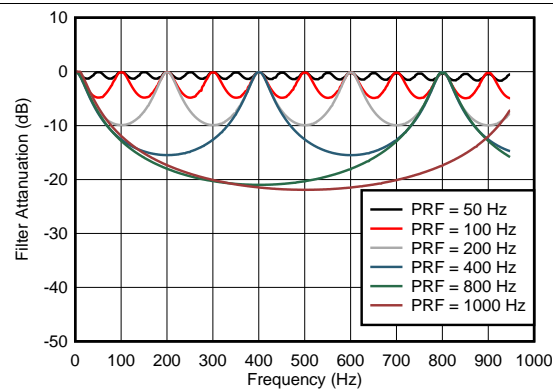


Figure 11. Filter Response for Multiple PRFs at 1% Duty Cycle

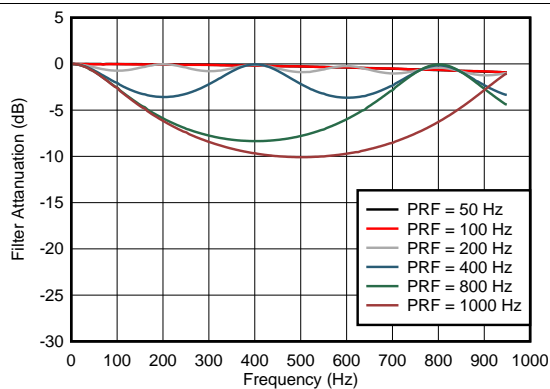


Figure 12. Filter Response for Multiple PRFs at 5% Duty Cycle

Typical Characteristics (continued)

At 25°C, TX_SUP = 4 V, RX_SUP = IO_SUP = 3.3 V, 100-Hz PRF, 25% duty cycle, $R_t = 500\text{ k}\Omega$, C_t is adjusted to keep the TIA time constant at 1/10th of the sampling duration, 8-MHz external clock (with CLKDIV_EXTMODE set to divide-by-2), CLKDIV_PRF = 1, detector $C_{IN} = 50\text{ pF}$, ADC averaging = max allowed, SNR (dBFS) = noise referred to full-scale range of 2 V, noise integrated from 1 Hz to Nyquist (= PRF / 2), and values assigned to CLKDIV_EXTMODE and CLK_DIV_PRF parameters correspond to division ratios controlled by these modes, unless otherwise specified.

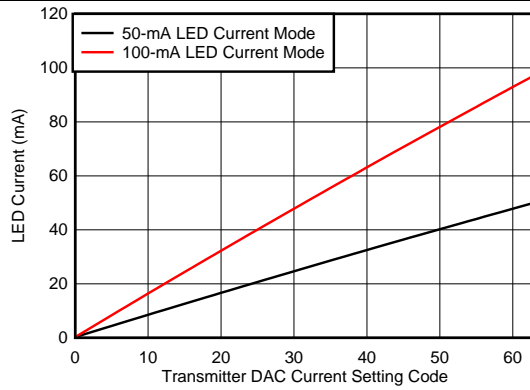


Figure 13. Transmitter Current Linearity

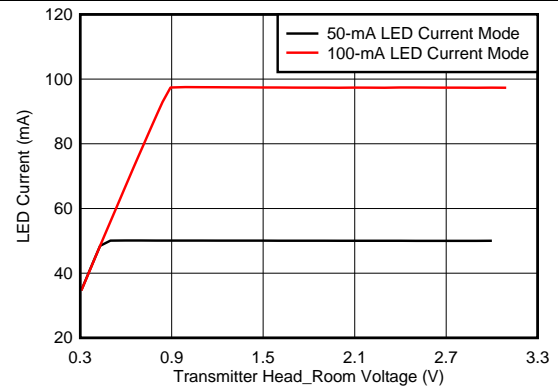


Figure 14. LED Current vs Transmitter Headroom Voltage

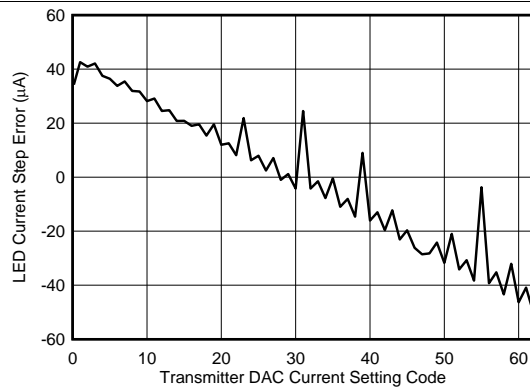


Figure 15. Transmitter DAC Current Step Error in 50-mA Mode

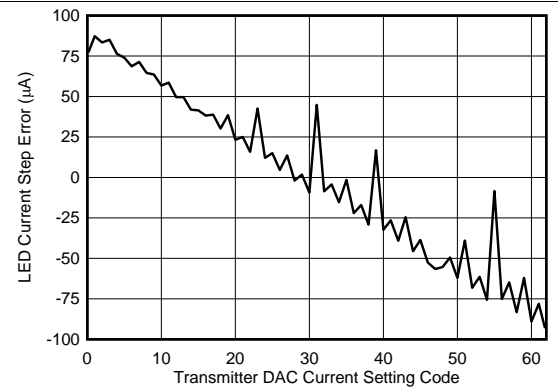


Figure 16. Transmitter DAC Current Step Error in 100-mA Mode

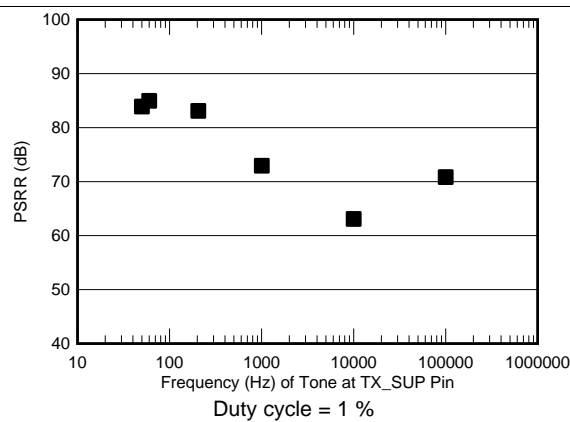


Figure 17. PSRR vs Tone Frequency at TX_SUP

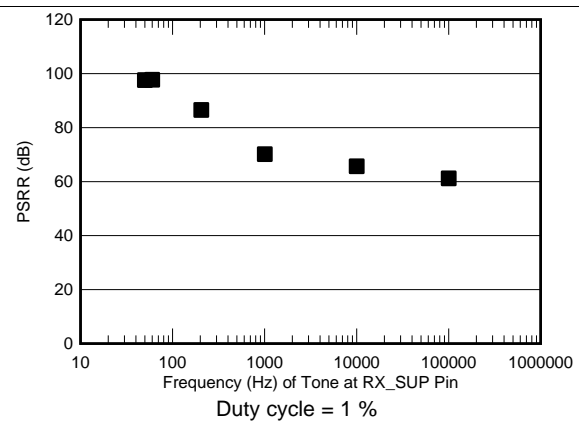


Figure 18. PSRR vs Tone Frequency at RX_SUP

Typical Characteristics (continued)

At 25°C, TX_SUP = 4 V, RX_SUP = IO_SUP = 3.3 V, 100-Hz PRF, 25% duty cycle, $R_f = 500\text{ k}\Omega$, C_f is adjusted to keep the TIA time constant at 1/10th of the sampling duration, 8-MHz external clock (with CLKDIV_EXTMODE set to divide-by-2), CLKDIV_PRF = 1, detector $C_{IN} = 50\text{ pF}$, ADC averaging = max allowed, SNR (dBFS) = noise referred to full-scale range of 2 V, noise integrated from 1 Hz to Nyquist (= PRF / 2), and values assigned to CLKDIV_EXTMODE and CLK_DIV_PRF parameters correspond to division ratios controlled by these modes, unless otherwise specified.

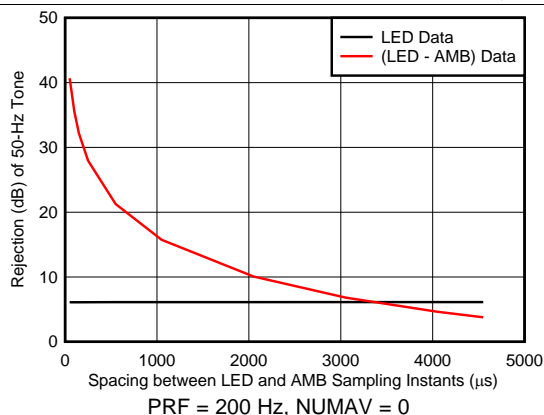


Figure 19. Rejection of a 50-Hz Differential Tone Across Spacing Between LED and Ambient Phases

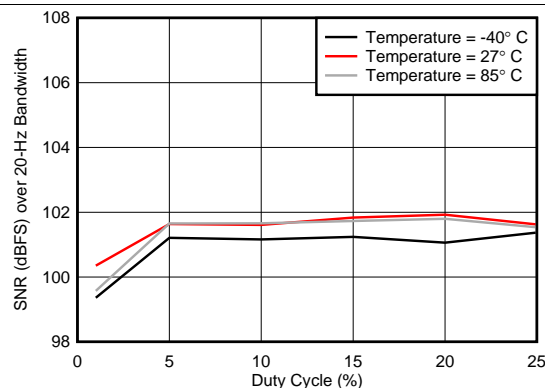


Figure 20. Receiver SNR in a 20-Hz Bandwidth vs Duty Cycle Across Different Temperatures

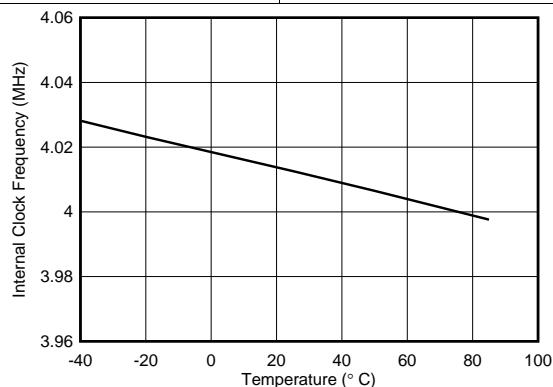


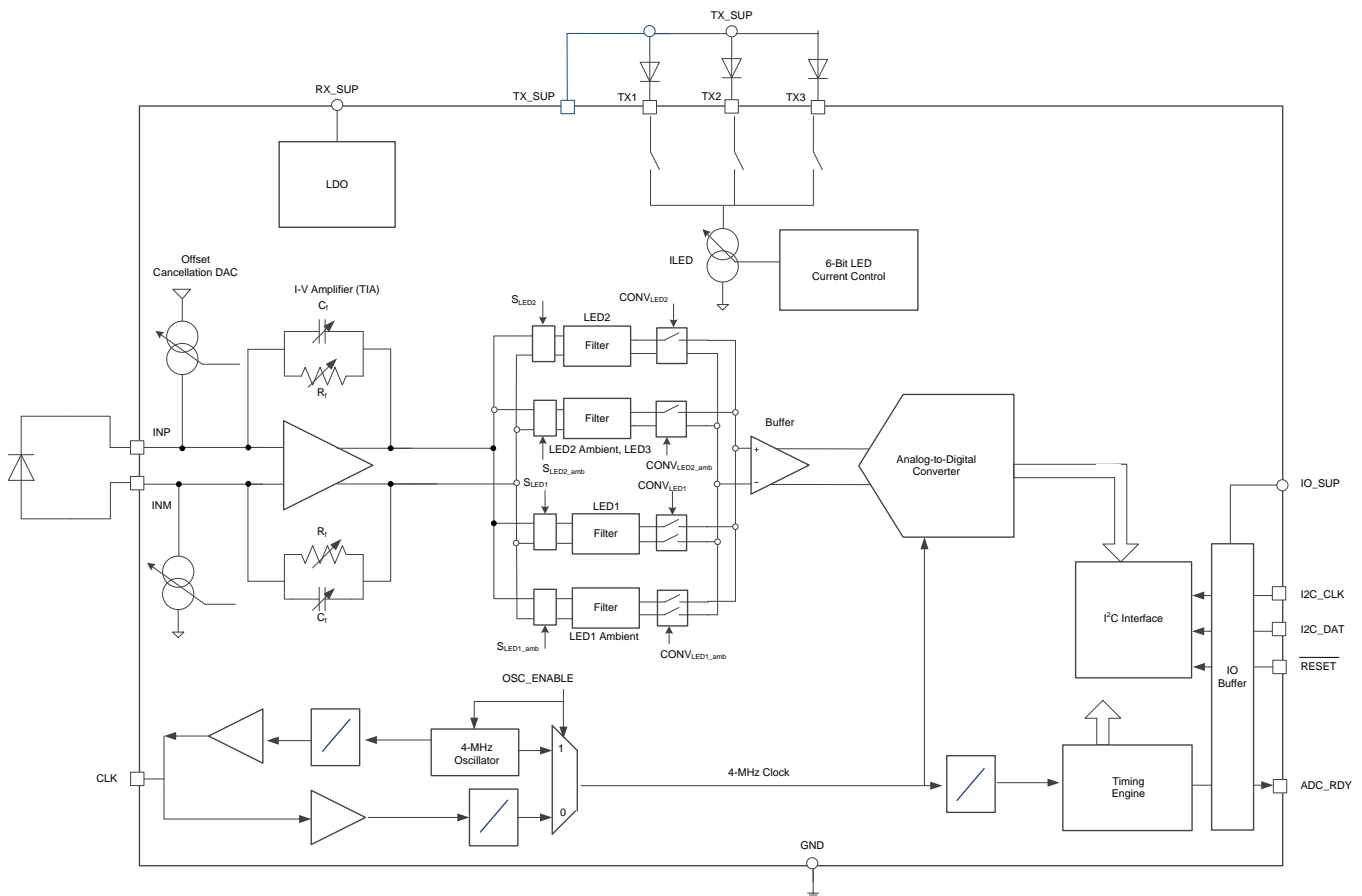
Figure 21. Internal Oscillator Frequency vs Temperature on a Typical Unit

9 Detailed Description

9.1 Overview

The AFE has an integrated transmitter and receiver for optical heart-rate monitoring and pulse oximetry applications. The system is characterized by a parameter termed the *pulse repetition frequency (PRF)* that determines the repetition periodicity of a sequence of operations. Every cycle of a PRF results in four 24-bit digital samples at the output of the AFE, each of which is stored in a separate register.

9.2 Functional Block Diagram

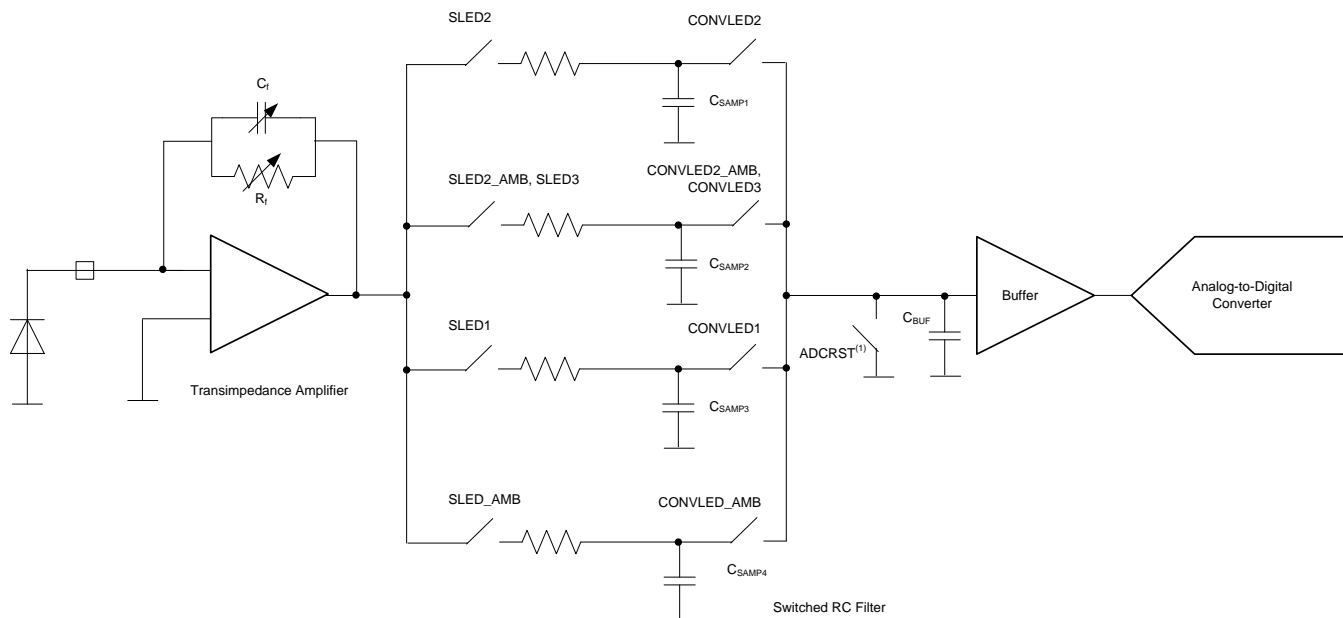


9.3 Feature Description

9.3.1 TIA and Switched RC Filter

The receiver input pins (INP, INM) are meant to be connected differentially to a photodiode. The signal current from the photodiode is converted to a differential voltage using a transimpedance amplifier (TIA). The TIA gain is set by its feedback resistor (R_f) and can be programmed from 10 k Ω to 2 M Ω . The transimpedance gain between the input current and output differential voltage of the TIA is equal to $2 \times R_f$. At the output of the TIA is a switched RC filter. There are four parallel instances of the filter, each of which are connected to the TIA output signal during one of four sampling phases.

The signal chain is kept fully differential throughout the receiver channel in order to enable excellent rejection of common-mode noise as well as noise on power supplies. For simplicity, the scheme with the four parallel filters is shown in Figure 22 for a single-ended representation of the signal chain. The ADCRST signal corresponds to the collection of active phases of four ADCRST pulses: ADCRST0, ADCRST1, ADCRST2, and ADCRST3.



NOTE: For simplicity, this circuit is shown in single-ended format.

(1) ADCRST corresponds to ADCRST0, ADCRST1, ADCRST2, or ADCRST3.

Figure 22. Four Sampling and Conversion Phases Diagram

Feature Description (continued)

9.3.1.1 Operation with Two and Three LEDs

The four sampling phases can correspond to either of the following signal state sequences received by the photodiode:

1. 2-LED mode: LED2 → ambient phase 2 → LED1 → ambient phase 1
2. 3-LED mode: LED2 → LED3 → LED1 → ambient

The sequence of the phases within a pulse repetition cycle is shown in [Figure 23](#).

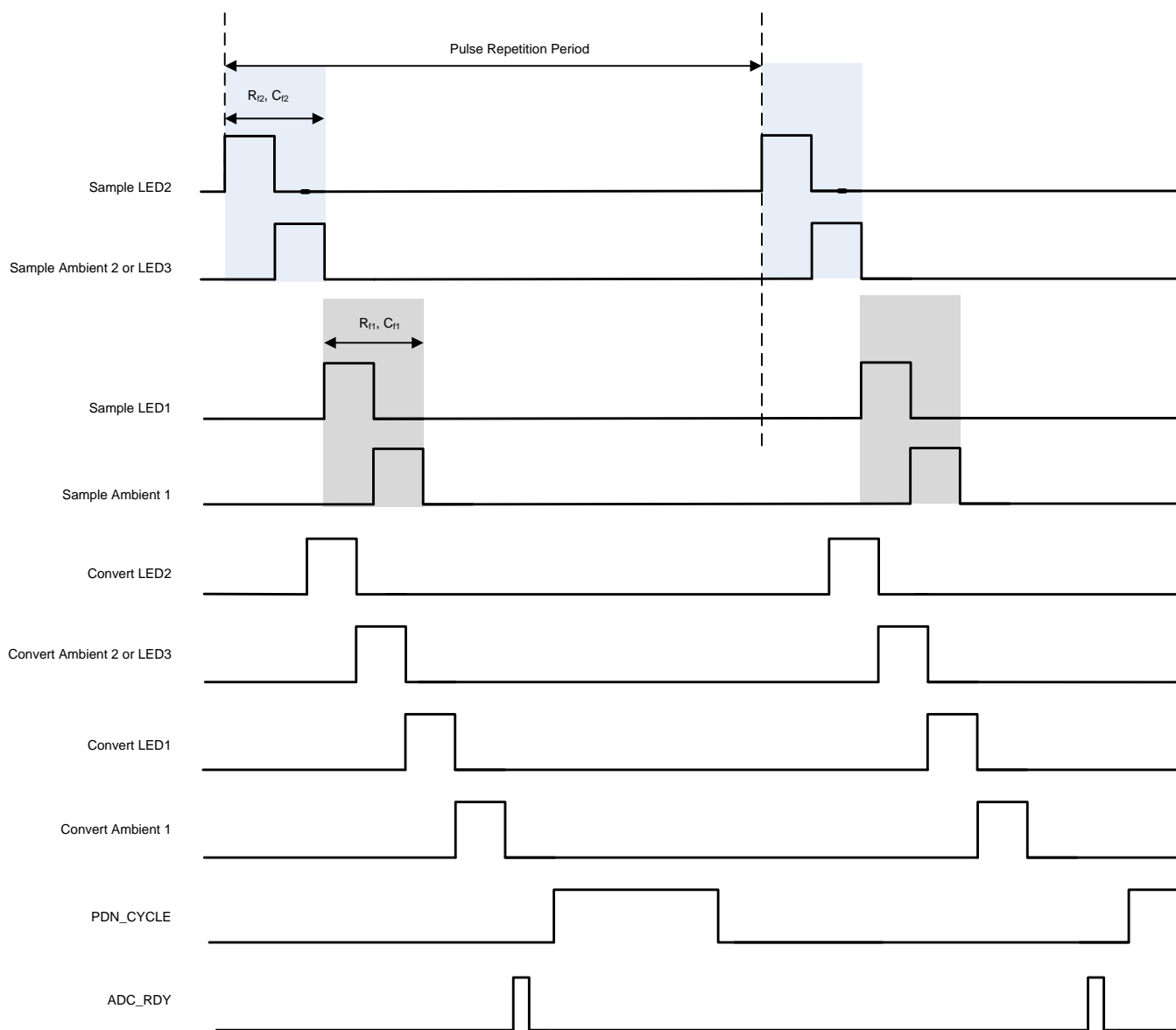


Figure 23. Sequence of Four Sampling and Conversion Phases

In the 2-LED mode, LED1 and LED2 are pulsed during the corresponding sampling instants. In the 3-LED mode, LED1, LED2, and LED3 are pulsed during the corresponding sampling instants. As mentioned in the [TIA Gain Settings](#) and [Operation with Two and Three LEDs](#) sections, the TIA gain (R_f) and feedback capacitor (C_f) can be programmed differently between two sets: R_{f1} / C_{f1} and R_{f2} / C_{f2} . The way these sets are applied to the four phases is shown in [Figure 23](#).

Feature Description (continued)

9.3.1.1.1 LED Current Setting

The default LED current range is from 0 mA to 50 mA. The individual currents of each of the three LEDs can be controlled independently, each with a separate 6-bit control.

Taken as a decimal number, the 6-bit setting provides 63 equal steps between 0 mA and 50 mA. Each increment of the ILED 6-bit code causes the LED current setting to increment by approximately 0.8 mA. For details, see [register 22h](#).

The LED current range can be doubled by setting the ILED_2X bit to 1. The accuracy of higher current settings close to 100 mA can be low because of current saturation of the driver. Each increment of the ILED 6-bit code causes the LED current to increment by approximately 1.6 mA when ILED_2X is set to 1.

9.3.1.2 TIA Gain Settings

The TIA gain is set by programming the value of R_f (the feedback resistor of the TIA). The R_f setting is controlled using the TIA_GAIN register bit. For details see [register 21h](#).

By default, the same TIA_GAIN setting is applied for all four phases of the receiver. Separate gains can be set for two of the four phases by setting the EN_SEP_GAIN bit. When the EN_SEP_GAIN bit is enabled, the TIA_GAIN register controls the R_{f1} setting and the TIA_GAIN_SEP register controls the R_{f2} settings.

Mapping of the R_{f1} / R_{f2} values to the two sets of 3-bit controls is described in [Table 49](#).

9.3.1.3 TIA Bandwidth Settings

TIA bandwidth settings are similar to TIA gain settings. The TIA bandwidth is set by programming the value of C_f (the feedback capacitance of the TIA). The product of R_f and C_f gives the time constant of the TIA and must be set approximately 1/5th (or less) of the LED or sampling pulse durations. This choice of time constant allows the TIA to pass the incoming pulses from the photodiode.

C_f is controlled using the TIA_CF register bit. For details, see [register 21](#).

By default, the same TIA_CF setting is applied for all four phases of the receiver. Similar to the TIA gain settings, a separate C_f can be set for two of the four phases by setting the EN_SEP_GAIN bit. When the EN_SEP_GAIN bit is enabled, the TIA_CF register controls the C_{f1} settings and TIA_CF_SEP controls the C_{f2} settings. Mapping the C_{f1} / C_{f2} values to the two sets of 3-bit controls is the same as illustrated in [Table 50](#).

9.3.2 Power Management

The AFE has three independent supplies for the transmitter, receiver, and I/O.

9.3.2.1 Transmitter Supply (TX_SUP)

The transmitter supply has a range of 3.0 V to 5.25 V. In the most common arrangement, this supply can be the same supply that the anodes of the LEDs are tied to, as shown in [Figure 24](#).

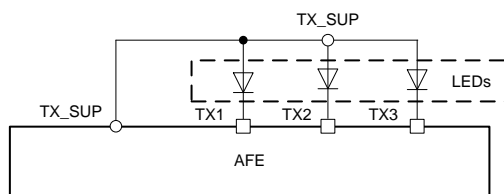


Figure 24. LED to Pin Connections

When the LEDs must be tied to a different supply, care must be taken to ensure that the LED supply is within 0.3 V of TX_SUP. This consideration of the LED supply voltage prevents the electrostatic distortion (ESD) diodes inside the AFE from turning on during the off state of the LEDs.

Feature Description (continued)

9.3.2.2 Receiver Supply (RX_SUP)

The receiver supply has a range of 2.0 V to 3.6 V. The AFE has internal low-dropout (LDO) regulators operating at 1.8 V that regulate both the analog and digital blocks inside the AFE. This rejection of supply noise from the internal LDOs, coupled with the differential nature of the architecture, enables excellent noise rejection on the supplies (for instance, 50-Hz noise).

9.3.2.3 I/O Supply (IO_SUP)

The I/O supply can either be tied to RX_SUP or can be separately driven. The motivation for a separate I/O supply is to interface with certain microcontrollers (MCUs) that require a 1.8-V I/O current. In this case, IO_SUP can be driven separately from RX_SUP and can be tied to 1.8 V.

9.3.2.4 Boost Converters Selection

If the supply voltage for TX_SUP (and the LEDs) is unavailable in the system, a boost converter may be required to generate the supply voltage. TI has a portfolio of boost converters from which an appropriate device can be selected. Some choices are listed in [Table 1](#).

Table 1. TI Boost Converter Details⁽¹⁾

TI PART NUMBER	SIZE (mm, L × W × H)	INPUT SUPPLY (V)	OUTPUT SUPPLY	TYPICAL QUIESCENT CURRENT (μA)	EXTERNAL COMPONENTS
TPS61254	1.2 × 1.3 × 0.625	2.3 to 5.5	Different parts with a fixed voltage up to 5 V	36	2 capacitors, 1 inductor
TPS61240	0.9 × 1.3 × 0.625	2.3 to 5.5	5 V (fixed)	30	2 capacitors, 1 inductor
TPS61252	2 × 2 × 0.75	2.3 to 6	Adjustable up to 6.5 V	30	3 capacitors, 1 inductor, 4 resistors
TPS61220	2 × 2.2 × 1	0.7 to 5.5	Adjustable from 1.8 V to 6 V	5.5	2 capacitors, 1 inductor, 2 resistors

(1) For the most current information, refer to the TI data sheets corresponding to each device (available for download from www.ti.com).

9.3.3 Offset Cancellation DAC

A typical optical heart-rate signal has a dc component and an ac component. Although a higher TIA gain maximizes the ac signal at the AFE output, the magnitude of the dc component limits the maximum gain possible in the TIA. In order to decouple the affect of the dc level on the allowed ac signal gain, a current digital-to-analog converter (DAC) is placed at the input of the device. By setting a programmable cancellation current (based on the dc current signal level), the effective signal that is gained up by the TIA can be reduced. This reduction in the effective signal current into the TIA results in the ability to set a higher TIA gain than what is otherwise possible without enabling the offset correction. In each of the four phases of operation, a separate programmable current value can be set by programming four different sets of register bits. These cancellation currents are automatically presented to the input of the TIA in the appropriate phase. The ability to set a different cancellation current in each of the four phases can be used to cancel out the ambient current in the ambient phase. In the LED on phase, this ability can be used to cancel out the sum of the ambient current and dc current of the heart-rate signal. The polarities of the signal current and offset cancellation current is illustrated in [Figure 25](#). The polarity of the offset cancellation current can be reversed by programming the POL_OFFDAC bits.

With zero input current and zero current in the offset cancellation DAC, the output of the AFE will be close to zero. Based on the channel offset, the output voltage for zero input current could be a small positive or negative value, usually in the range of several mV. With the photodiode connected as shown in Figure 25 and a signal current coming from the photodiode, the output code of the device is expected to be positive with the offset cancellation DAC set to zero ($I_{\text{offset}} = 0$). With I_{offset} set negative ($\text{POL_OFFFAC} = 1$), a dc offset can be subtracted from the signal and the ac signal can be amplified with a higher gain than what is otherwise possible.

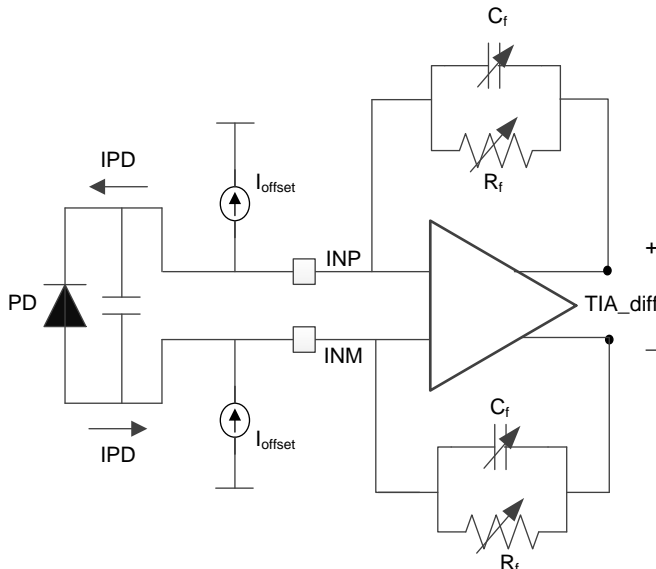


Figure 25. Offset Cancellation Current Polarity Diagram

A breakdown of the signal current and voltage levels is provided in Table 2 for a variety of signal levels. In Table 2, the current transfer ratio (CTR) is used to describe the relationship between the set LED current and the resulting photodiode current (IPD). CTR is the ratio of the photodiode current for a given LED current and is a function of the optical and mechanical parameters as well as human physiology.

Table 2. Signal Current and Voltage Levels for a Hypothetical Use Case⁽¹⁾

PHASE	I _{LED} (mA)	CTR (μA / mA)	I _{sig} (μA)	I _{amb} (μA)	IPD (μA)	I _{OFFDAC} (μA)	I _{eff} (μA)	R _f (MΩ)	TIA _{diff} (V)
LED2	25	0.025	0.625	1	1.625	–1.4	0.225	1	0.45
LED3	50	0.025	1.25	1	2.25	–1.87	0.38	0.5	0.38
LED1	12.5	0.025	0.3125	1	1.3125	–0.93	0.3825	0.5	0.3825
AMB1	0	0.025	0	1	1	–0.93	0.07	2	0.28

(1) I_{LED} is the set LED current; CTR is the current transfer ratio (in μA / mA); I_{sig} is the photodiode signal current resulting from LED pulsing ($I_{\text{sig}} = I_{\text{LED}} \times \text{CTR}$); I_{amb} is the current in the photodiode resulting from ambient light (that is present in all phases and adds to I_{sig}); IPD is the total input current ($I_{\text{sig}} + I_{\text{amb}}$); I_{OFFDAC} is the current setting of the offset cancellation DAC; I_{eff} is the effective current after offset cancellation ($I_{\text{sig}} + I_{\text{OFFDAC}}$); R_f is the TIA gain setting; and TIA_{diff} is the output differential signal of the TIA (note that this signal must be within the range of ±1 V).

9.3.3.1 Offset Cancellation DAC Controls

The I_{OFFDAC} bits control the magnitude of the current subtracted (or added) at the TIA input. The POL_{OFFDAC} bits control the polarity of the current and determine whether the current is subtracted from or added to the input. For details, see register 3Ah.

9.3.4 Analog-to-Digital Converter (ADC)

The AFE has an ADC that provides a 22-bit representation of the current from the photodiode. The ADC codes corresponding to the various sampling phases can be read out from 24-bit registers in twos complement format. The ADC full-scale input range is ± 1.2 V and spans bits 21 to 0. The mapping of the ADC input voltage to the ADC code is shown in [Table 3](#).

Table 3. Mapping the ADC Input Voltage to the ADC Code

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT	24-BIT ADC OUTPUT CODE
-1.2 V	111000000000000000000000
$(-1.2 / 2^{21})$ V	111111111111111111111111
0	000000000000000000000000
$(1.2 / 2^{21})$ V	000000000000000000000001
1.2 V	000111111111111111111111

The two MSBs of the 24-bit word serve as sign-extension bits to the 22-bit ADC code and are equal to the MSB of the 22-bit ADC code when the input to the ADC is within its full-scale range, as shown in [Table 4](#).

Table 4. Using Sign-Extension Bits to Determine the Input Operating Voltage

BITS 23-21	INPUT STATUS
000	Positive and lower than positive full-scale (within full-scale range)
111	Negative and higher than negative full-scale (within full-scale range)
001	Positive and higher than positive full-scale (outside full-scale range)
110	Negative and lower than negative full-scale (outside full-scale range)

Noted that the TIA has an operating range of ± 1 V even though the ADC input full-scale range is ± 1.2 V, as shown in [Figure 26](#). When setting the TIA gain, ensure that the signal at the TIA output does not exceed ± 1 V.

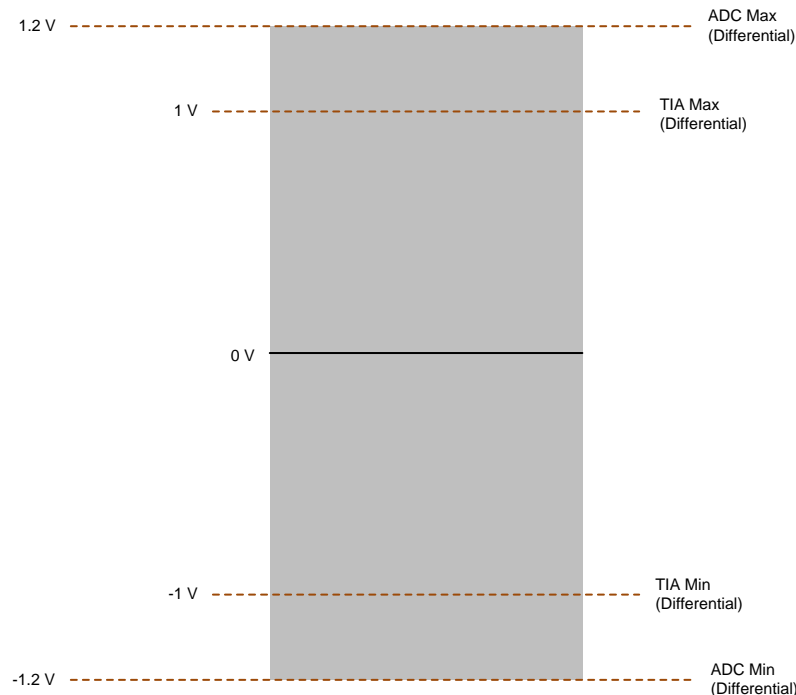


Figure 26. TIA and ADC Dynamic Ranges

9.3.5 I²C Interface

The AFE has an I²C interface for communication. The I2C_CLK and I2C_DAT lines require external pullup resistors to IO_SUP. Refer to the I²C protocol standards documents for details of the I²C interface. This section only describes certain key features of the interface. The data on I2C_DAT must be stable during the high level of I2C_CLK and may transition during the low level of I2C_CLK, as shown in [Figure 27](#).

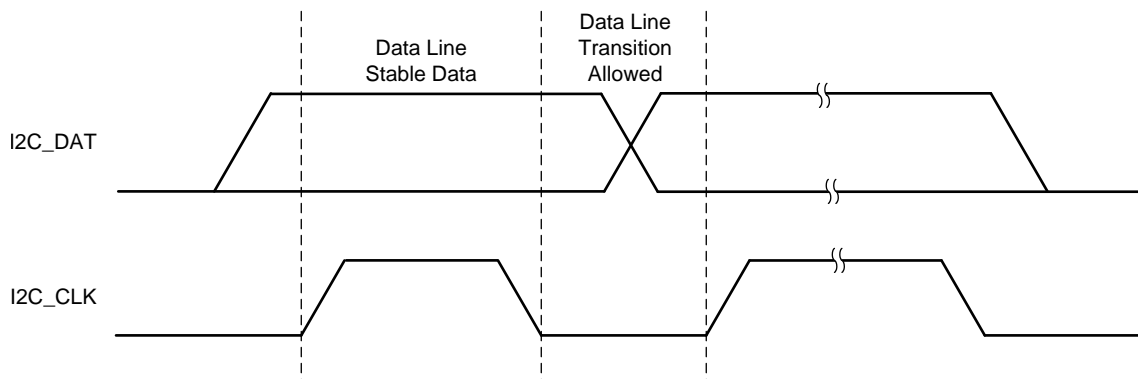


Figure 27. Allowed Transition of I2C_DAT while Transmission of Data Bits

The start condition is indicated by a high-to-low transition of the I2C_DAT line when the I2C_CLK is high. A stop condition is indicated by a low-to-high transition of the I2C_DAT line when the I2C_CLK is high. [Figure 28](#) shows the start and stop conditions.

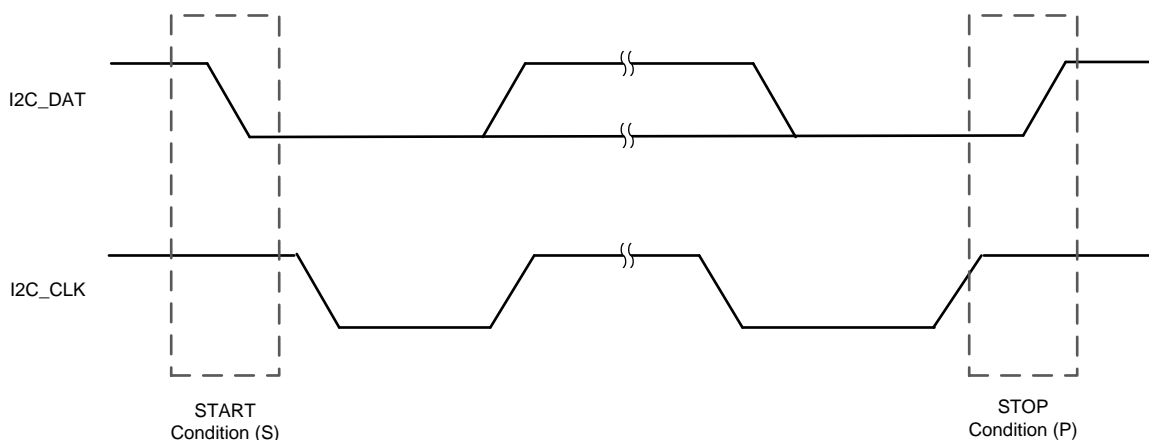
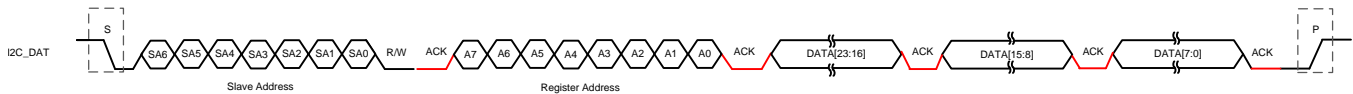


Figure 28. Transition of I2C_DAT during Start and Stop Conditions

With the previously mentioned protocols for data, start, and stop conditions in place, the write and read operations are as shown in Figure 29 and Figure 30, respectively. In Figure 29 and Figure 30, the slave address for the AFE (indicated as SA6 to SA0) is a 7-bit representation of address 58h. The R/W bit is the read/write bit and is set to '1' for Read and '0' for Write. Only the ADC output registers (addressed from 2Ah to 2Fh) can be read out without the need for setting the REG_READ bit. Prior to reading out any other register, the REG_READ bit needs to be additionally set to '1'. In Figure 29 and Figure 30, the activity performed by the host is shown in black whereas the activity from the AFE is shown in red. Thus, after the host sends the slave address during a write operation, the AFE pulls the I2C_DAT line low (shown as ACK) if the slave address matches 58h. Similarly, the host pulls the I2C_DAT line high (shown as NACK) as acknowledgment of a successfully completed read operation involving three bytes of data. Continuous read/write mode is not supported.



- (1) Activity performed by the host is shown in black whereas the activity from the AFE is shown in red. Continuous read/write mode is not supported.

Figure 29. I²C Write Option Timing



Figure 30. I²C Read Option Timing

9.3.6 Timing Engine

The AFE has a fully-integrated timing engine that can be programmed to generate all clock phases for synchronized transmit drive, receive sampling, and data conversion. To enable the timing engine (after powering up the device), enable the TIMEREN bit.

9.3.6.1 Timer and PRF Controls

The timing engine inside the AFE has a 16-bit counter. The duration of the count with respect to an internal clock (the timer clock) determines the pulse repetition period. The pulse repetition frequency (PRF) can be set using the PRPCT register bits that represent the high value of the counter (the low value of the counter is 0). The counter automatically counts until reaching PRPCT and then returns to 0 to start the next count. To suspend the count and keep the counter in reset state, enable the TM_COUNT_RST bit.

9.3.6.2 Timing Control Registers

The start and stop counts for the various dynamic signals generated by the timing engine are shown in [Table 5](#). The timing edge numbers are in reference to [Figure 31](#).

Table 5. Timing Register and Edge Details

TIMING SIGNAL	DESCRIPTION	REGISTER ADDRESS (Hex)	TIMING EDGE
LED2STC	Sample LED2 start	1h	TE3
LED2ENDC	Sample LED2 end	2h	TE4
LED1LEDSTC	LED1 start	3h	TE17
LED1LEDENDC	LED1 end	4h	TE18
ALED2STC\LED3STC	Sample ambient 2 (or sample LED3) start	5h	TE11
ALED2ENDC\LED3ENDC	Sample ambient 2 (or sample LED3) end	6h	TE12
LED1STC	Sample LED1 start	7h	TE19
LED1ENDC	Sample LED1 end	8h	TE20
LED2LEDSTC	LED2 start	9h	TE1
LED2LEDENDC	LED2 end	Ah	TE2
ALED1STC	Sample ambient 1 start	Bh	TE25
ALED1ENDC	Sample ambient 1 end	Ch	TE26
LED2CONVST	LED2 convert phase start	Dh	TE7
LED2CONVEND	LED2 convert phase end	Eh	TE8
ALED2CONVST\LED3CONVST	Ambient 2 (or LED3) convert phase start	Fh	TE15
ALED2CONVEND\LED3CONVEND	Ambient 2 (or LED3) convert phase end	10h	TE16
LED1CONVST	LED1 convert phase start	11h	TE23
LED1CONVEND	LED1 convert phase end	12h	TE24
ALED1CONVST	Ambient 1 convert phase start	13h	TE29
ALED1CONVEND	Ambient 1 convert phase end	14h	TE30
ADCRSTSTCT0	ADC reset phase 0 start	15h	TE5
ADCRSTENDCT0	ADC reset phase 0 end	16h	TE6
ADCRSTSTCT1	ADC reset phase 1 start	17h	TE13
ADCRSTENDCT1	ADC reset phase 1 end	18h	TE14
ADCRSTSTCT2	ADC reset phase 2 start	19h	TE21
ADCRSTENDCT2	ADC reset phase 2 end	1Ah	TE22
ADCRSTSTCT3	ADC reset phase 3 start	1Bh	TE27
ADCRSTENDCT3	ADC reset phase 3 end	1Ch	TE28

When three LEDs are used within a single period, the Ambient2 phase is replaced by the LED3 phase. The timing controls for driving the third LED are as shown in [Table 6](#).

Table 6. Timing Controls for Driving the Third LED

TIMING SIGNAL	DESCRIPTION	REGISTER ADDRESS (Hex)	TIMING EDGE
LED3LEDSTC	LED3 start	36h	TE9
LED3LEDENDC	LED3 end	37h	TE10

The timing diagram for when all three LEDs are active is shown in [Figure 31](#).

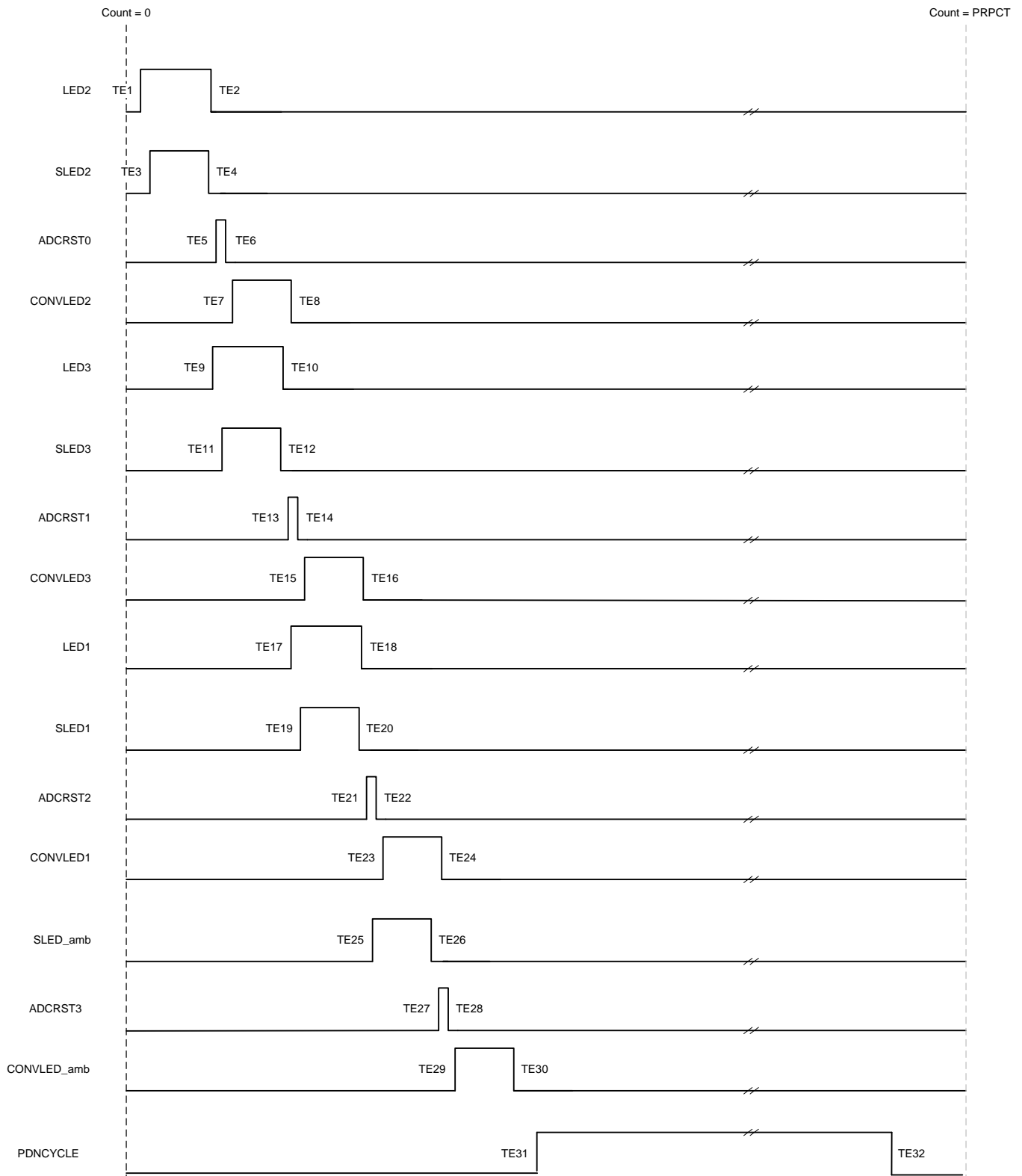


Figure 31. Timing Diagram

9.3.6.3 Receiver Timing

The timing engine can be programmed to set the different phases of the receiver. The relative timings of the LED phase, sampling phase, ADC reset phase, and ADC conversion phases are shown in Figure 32 and Table 7.

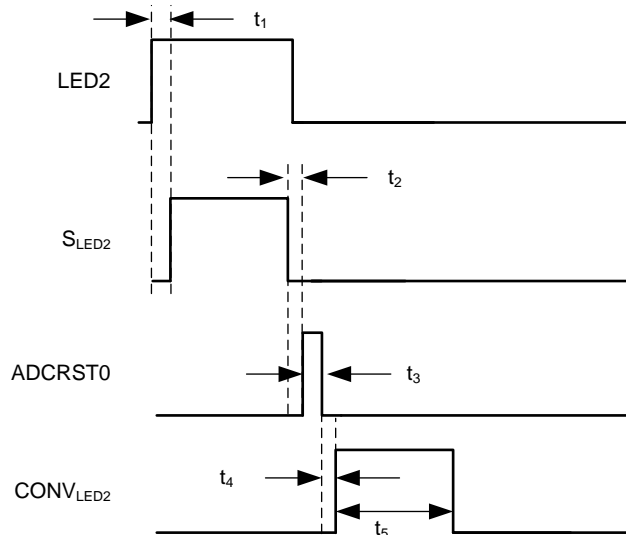


Figure 32. Receiver Timing Guidelines

Table 7. Receiver Timing Details

		MIN	MAX	UNIT
t ₁	Start of LED to start of sampling	Min [20, (0.2 × LED pulse duration)]		μs
t ₂	End of LED to start of ADC reset phase	2		Counts ⁽¹⁾
t ₃	Duration of ADC reset phase	6		Counts
t ₄	End of ADC reset phase to start of ADC conversion phase	1	1	Count
t ₅	Duration of ADC conversion phase ⁽²⁾	(NUMAV + 2) × 200 × t _{ADC} + 15 ⁽³⁾		μs

(1) Refers to one clock period of CLK_TE.

(2) See Figure 35 for notations of the clocking domain.

(3) t_{ADC} = 1 / f_{ADC}

The fourth ADCRST signal (ADCRST3) in a period also defines the start of the ADC_RDY pulse. The rising edge of the ADC_RDY signal can be used as an interrupt by the MCU to readout the registers corresponding to the preceding four conversions in that period. If any of the four conversion phases are not needed, then their duration can be set to 0. However, the corresponding ADCRSTx pulse must still be defined. All four ADCRSTx pulses must be defined in order to generate the ADC_RDY pulse. A scheme of the ADC_RDY pulse generation is shown in Figure 33. The ADC_RDY pulse timing is shown in Table 8.

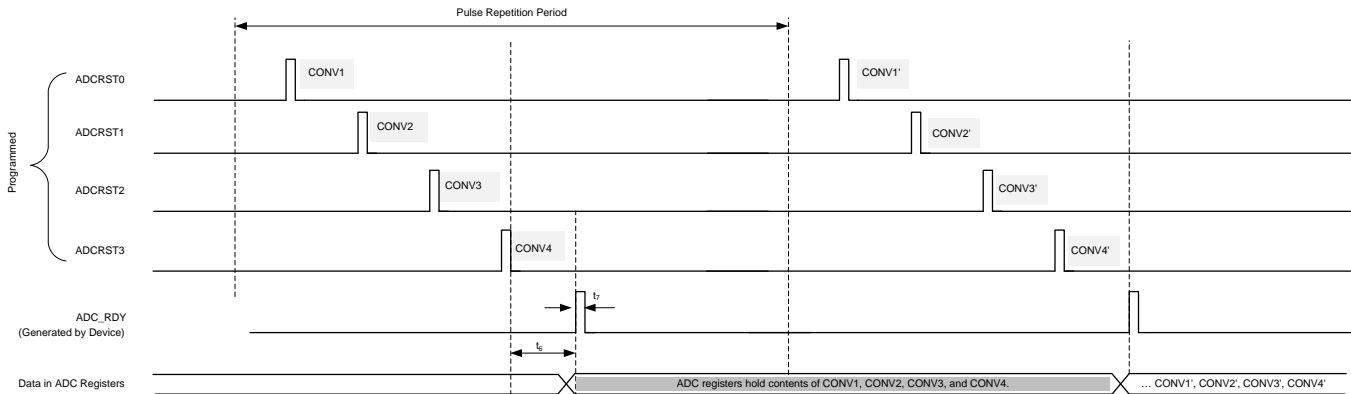


Figure 33. ADC_RDY Generation Scheme

Table 8. ADC_RDY Timing Details

	TYP	MAX	UNIT
t_6 End of fourth ADC reset phase to start of ADC_RDY pulse	$(NUMAV + 1) \times 200 \times t_{ADC}$	$(NUMAV + 2) \times 200 \times t_{ADC} + 15$	μs
t_7 ADC_RDY pulse duration	$t_{ADC}^{(1)}$		μs

- (1) If a larger pulse duration is needed for the ADC_RDY interrupt, use PROG_TG_EN to enable a programmable timing signal to come out of the ADC_RDY pin. The location of the signal can be set using the PROG_TG_STC and PROG_TG_ENDC counts.

9.3.6.4 Dynamic Power-Down Timing

The dynamic power-down feature can be used to shut down the receiver inside every cycle to save power, as shown in Figure 34 and Table 9.

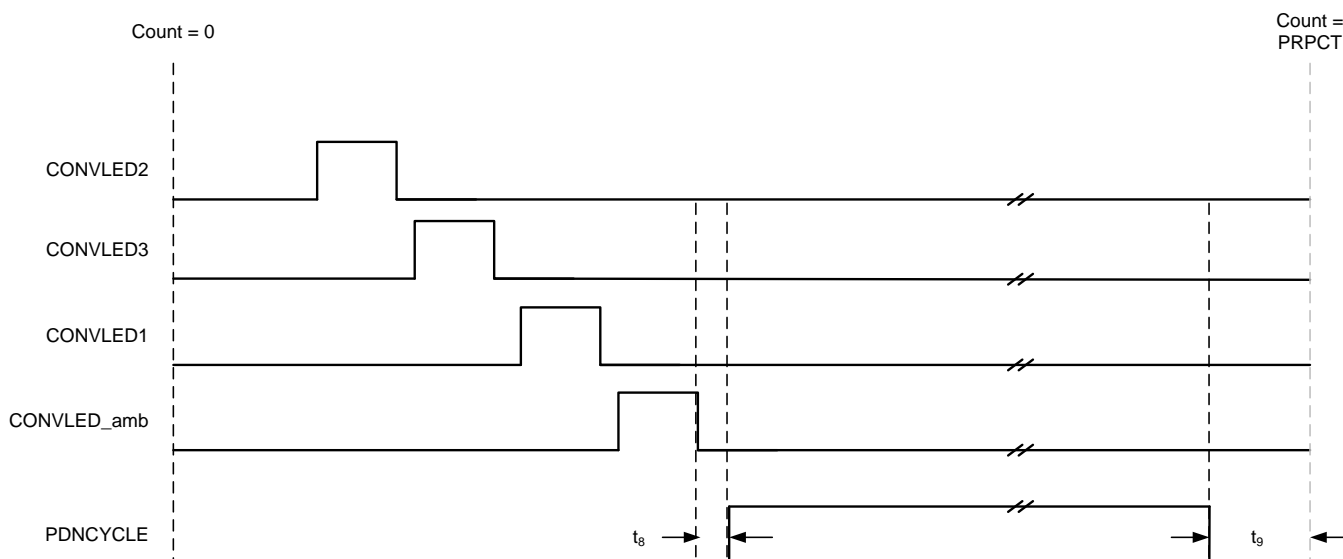


Figure 34. Dynamic Power-Down Timing Diagram

Table 9. Dynamic Power-Down Timing Details

		MIN	UNIT
t_8	End of 4th conversion phase to the start of PDNCYCLE	200	μ s
t_9	End of PDNCYCLE to start of next period	200	μ s

The timing controls for the PDNCYCLE pulse are shown in Table 10.

Table 10. Timing Controls for Dynamic Power-Down

TIMING SIGNAL	DESCRIPTION	REGISTER ADDRESS (Hex)	TIMING EDGE ⁽¹⁾
PDNCYCLESTC	PDNCYCL start	32h	TE31
PDNCYCLENDC	PDNCYCL end	33h	TE32

(1) Refer to Figure 31.

9.3.6.5 Sample Register Values

Table 11 lists a sample of the register settings for generating the different timing signals. These sample settings correspond to CLK_INT = 4 MHz and a PRF of 100 Hz. Three LEDs are used in a cycle, each with a duty cycle of 1%, corresponding to a pulse duration of 100 μ s. The conversion durations are set in order to accommodate four averages (NUMAV = 3). Two cases are described in Table 11: one for CLKDIV_PRF = 1 (CLK_TE = 4 MHz) and the other for CLKDIV_PRF = 16 (CLK_TE = 250 kHz).

Table 11. Sample Register Settings

SIGNAL ⁽¹⁾	REGISTER FIELD	NO DIVISION OF CLOCK TO TIMING ENGINE CLOCK (CLKDIV_PRF = 1)		ADC CLOCK TO TIMING ENGINE CLOCK DIVIDED BY 16 (CLK_DIV_PRF = 16)	
		TIME DURATION (μs)	REGISTER SETTING ⁽²⁾	TIME DURATION (μs)	REGISTER SETTING ⁽²⁾
PRF COUNTER	PRPCT	10000	39999 ⁽³⁾	10000	2499 ⁽³⁾
LED2	LED2LEDSTC	100	0	100	0
	LED2LEDENDC		399		24
S _{LED2}	LED2STC	80	80	80	5
	LED2ENDC		399		24
ADCRST0	ADCRSTSTCT0	1.75	401	8	26
	ADCRSTENDCT0		407		27
CONV _{LED2}	LED2CONVST	265	408	268	28
	LED2CONVEND		1467		94
LED3	LED3LEDSTC	100	400	100	25
	LED3LEDENDC		799		49
S _{LED3}	ALED2STC\LED3STC	80	480	80	30
	ALED2ENDC\LED3ENDC		799		49
ADCRST1	ADCRSTSTCT1	1.75	1469	8	96
	ADCRSTENDCT1		1475		97
CONV _{LED3}	ALED2CONVST\LED3CONVST	265	1476	268	98
	ALED2CONVEND\LED3CONVEND		2535		164
LED1	LED1LEDSTC	100	800	100	50
	LED1LEDENDC		1199		74
S _{LED1}	LED1STC	80	880	80	55
	LED1ENDC		1199		74
ADCRST2	ADCRSTSTCT2	1.75	2537	8	166
	ADCRSTENDCT2		2543		167
CONV _{LED1}	LED1CONVST	265	2544	268	168
	LED1CONVEND		3603		234
S _{LED_AMB}	ALED1STC	80	1279	80	79
	ALED1ENDC		1598		98
ADCRST3	ADCRSTSTCT3	1.75	3605	8	236
	ADCRSTENDCT3		3611		237
CONV _{LED_AMB}	ALED1CONVST	265	3612	268	238
	ALED1CONVEND		4671		304
PDNCYCLE	PDNCYCLESTC	8432.25	5471	8384	354
	PDNCYCLEENDC		39199		2449

(1) For signal names, refer to [Figure 22](#).

(2) Time duration = (end count – start count + 1) / f_{TE}.

(3) For PRPCT, start count = 0.

The timing described in [Table 11](#) minimizes the active time, thereby enabling the signal chain to be in the dynamic power-down state for the maximum fraction of time. In this timing, the LED active phase overlaps with the conversion phase corresponding to a previous LED. The ground bounce from the LED switching can couple into the receiver and cause a small interference between one phase and the next. In most intended applications, this bounce is not expected to cause any problems. However, if the lowest level of interference across phases must be attained, the timing registers can be programmed as shown in [Table 12](#).

Table 12. Sample Register Settings for Low Interference Across Phases

SIGNAL ⁽¹⁾	REGISTER FIELD	NO DIVISION OF CLOCK TO TIMING ENGINE CLOCK (CLKDIV_PRF = 1)	
		TIME DURATION (μs)	REGISTER SETTING
PRF COUNTER	PRPCT	10000	39999
LED2	LED2LEDSTC	99.75	0
	LED2LEDENDC		398
S _{LED2}	LED2STC	79.75	80
	LED2ENDC		398
ADCRST0	ADCRSTSTCT0	1.75	5600
	ADCRSTENDCT0		5606
CONV _{LED2}	LED2CONVST	115	5607
	LED2CONVEND		6066
LED3	LED3LEDSTC	99.75	400
	LED3LEDENDC		798
S _{LED3}	ALED2STC\ LED3STC	79.75	480
	ALED2ENDC\ LED3ENDC		798
ADCRST1	ADCRSTSTCT1	1.75	6068
	ADCRSTENDCT1		6074
CONV _{LED3}	ALED2CONVST\ LED3CONVST	115	6075
	ALED2CONVEND\ LED3CONVEND		6534
LED1	LED1LEDSTC	99.75	800
	LED1LEDENDC		1198
S _{LED1}	LED1STC	79.75	880
	LED1ENDC		1198
ADCRST2	ADCRSTSTCT2	1.75	6536
	ADCRSTENDCT2		6542
CONV _{LED1}	LED1CONVST	115.25	6543
	LED1CONVEND		7003
S _{LED_AMB}	ALED1STC	79.75	1280
	ALED1ENDC		1598
ADCRST3	ADCRSTSTCT3	1.75	7005
	ADCRSTENDCT3		7011
CONV _{LED_AMB}	ALED1CONVST	115	7012
	ALED1CONVEND		7471
PDNCYCLE	PDNCYCLESTC	7882.25	7671
	PDNCYCLEENDC		39199

(1) For signal names, refer to [Figure 22](#).

9.4 Device Functional Modes

9.4.1 Power Modes

The AFE has the following power modes:

1. Normal mode.
2. Hardware power-down mode (PWDN): this mode is set using the RESETZ pin. When the RESETZ pin is pulled low for more than 200 μ s, the device enters hardware power-down mode where the power consumption is very low (of a few μ A).
3. Software power-down mode (PDNAFE) using a register bit.
4. Dynamic power-down mode: this mode is enabled by setting the start and end points of the PDN_CYCLE signal that is controlled using the timing engine. During the PDN_CYCLE high phase, the functional blocks (as selected by the DYNAMICx bits) are powered down. When powering down the TIA in dynamic power-down mode, consideration must be given to the dynamics of the photodiode. When the TIA is powered down, the feedback mechanism is no longer available to maintain zero bias across the photodiode, resulting in a voltage drift across the photodiode. When the AFE comes out of dynamic power-down into active mode, a transient recovery time for the photodiode results. Additionally, the INP, INM pins can be shorted through a switch to an internal reference voltage (VCM) to keep the photodiode in zero bias whenever the TIA is in power-down mode. Maintaining zero bias across the photodiode is accomplished by setting the ENABLE_INPUT_SHORT bit to 1. By setting this bit in conjunction with the DYNAMIC3 bit, the dynamics of the photodiode can be better controlled during the dynamic power-down mode.

9.4.2 RESET Modes

The AFE has internal registers that must be reset before valid operation. There are two ways to reset the device:

1. Either through the RESETZ pin (a reset signal can be issued by pulsing the RESETZ pin low for a duration of time between 25 to 50 μ s) or
2. A software reset via the SW_RESET register bit.

9.4.3 Clocking Modes

The AFE has an internal oscillator that can generate a 4-MHz clock. This clock can be made to come out of the CLK pin for use by the rest of the system. The default mode is to use an external clock. The frequency range of this external clock is between 4 MHz to 60 MHz. A programmable internal division ratio between 1 to 12 must be set so that the divided clock is between 4 MHz to 6 MHz. For high-accuracy measurements, operating the AFE using an input (external) clock with high accuracy is preferable. If a high-accuracy measurement is required when using the internal oscillator, a correction scheme can be used in the MCU to digitally compensate for the inaccuracy in the oscillator. One method of this approach is to accurately estimate the PRF by measuring the ADC_RDY periodicity in terms of a high-accuracy MCU clock (for example, a 32-kHz clock) to establish the accurate PRF. This information can then be used to digitally correct the heart rate computation.

9.4.4 PRF Programmability

By default, the internal clock is 4 MHz. This clock also goes to the timing engine that has a 16-bit counter. The maximum setting of this counter (all 16 bits set to 1) determines the lowest value of PRF, resulting in a minimum PRF of 61 Hz. To extend the lower range of PRF, an independent programmable divider is introduced in the clock going to the timing engine. By programming this divider between 1 to 16 with the CLKDIV_PRF register control, the lower range of PRF can be extended from 61 Hz to approximately 4 Hz (limit the minimum PRF to 10 Hz). The various clocking domains and controls are described in [Figure 35](#) and [Table 13](#).

Device Functional Modes (continued)

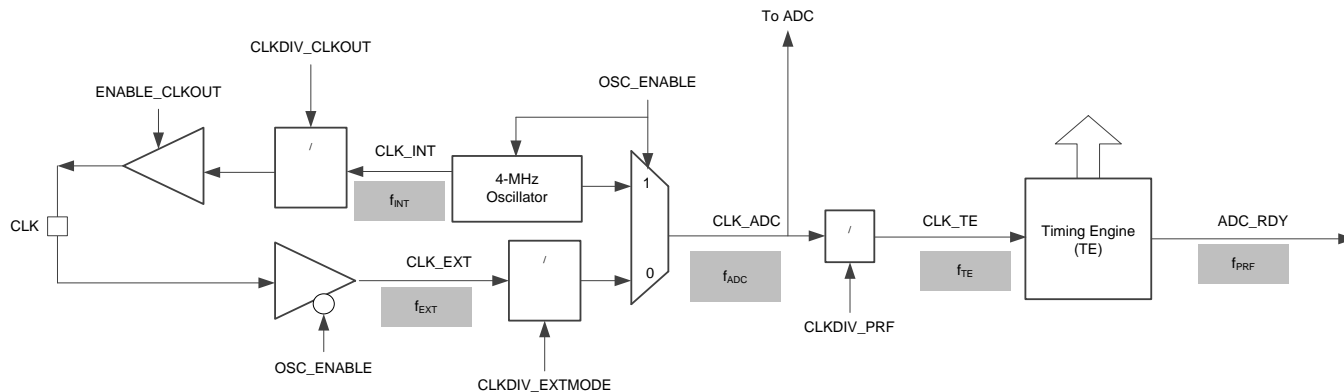


Figure 35. Clocking Domains Diagram

Table 13. Clock Domains and Operating Ranges

CLOCK	DESCRIPTION	FREQUENCY	FREQUENCY RANGE	COMMENTS
CLK_INT	Clock generated by the internal oscillator	f_{INT}	4 MHz ⁽¹⁾	Internal clock when the oscillator is enabled
CLK_EXT	External clock	f_{EXT}	4 MHz to 60 MHz	Set the division ratio with CLKDIV_EXTMODE so that CLK_ADC is 4 MHz to 6 MHz
CLK_ADC	Clock used by the ADC for conversion	f_{ADC}	4 MHz to 6 MHz	Selected as either an internal clock or a divided version of the external clock
CLK_TE	Clock used by the timing engine	f_{TE}	f_{ADC} divided by 1 to 16	Division ratio is set by CLKDIV_PRF
ADC_RDY	Interrupt to MCU at the same rate as the PRF	f_{PRF}	Limit to 10 Hz-1000 Hz, limited to 1000 / (division ratio as set by CLKDIV_PRF)	Set by PRPCT and f_{TE}

(1) Refer [Electrical Characteristics](#) for accuracy of Internal Oscillator.

9.4.5 Averaging Modes

To reduce the noise, the input to the ADC (sampled on the CSAMPx capacitors) can be converted by the ADC multiple times and averaged. The number of averages is set using the NUMAV register control based on [Equation 1](#):

$$\text{Number of Averages} = (\text{NUMAV} + 1) \quad (1)$$

By default, NUMAV = 0. Therefore, the default mode corresponds to when the ADC converts its input one time in each of the four phases and stores the content in the register corresponding to that phase.

When NUMAV is programmed (for example if NUMAV = 3), the ADC converts its input four times in each phase, averages the four conversions, and stores the averaged value in the register corresponding to that phase.

Averaging only helps in reducing ADC noise and not the front end noise because the input to the ADC is the same sampled voltage across all the ADC conversions used to generate the average (this voltage corresponds to the voltage sampled on the four CSAMPx capacitors in [Figure 22](#)). The number of samples that can be averaged ranges from 1 to 16 (when NUMAV is programmed from 0 to 15). A higher number of averages results in larger conversion times; see [Table 7](#).

Averaging is implemented in the following manner:

The number of ADC samples corresponding to the number of averages (NUMAV + 1) are accumulated, as shown in [Equation 2](#).

$$\text{SUMADC} = \sum_{i=1}^{(\text{NUMAV}+1)} (\text{ADC}_i)$$

where

- ADC_i = the i^{th} sample converted by the ADC. (2)

The accumulator output (SUMADC) is then divided by a factor D that is obtained by $D = 128 \div X$, with X being an integer.

The averaged output is shown in [Equation 3](#):

$$\text{ADCOUT} = \text{SUMADC} \div D$$

where

- $D = 128 \div X$, with X being an integer. (3)

This implementation gives an averaging function that is exact when the number of averages is a power of 2 but deviates from ideal values for other settings, as shown in [Table 14](#).

Table 14. Averaging Mode Settings

NUMAV	NUMBER OF AVERAGES	INTEGER (X)	DIVISION FACTOR (D)
0	1	128	1.0
1	2	64	2.0
2	3	43	2.97
3	4	32	4.0
4	5	26	4.92
5	6	21	6.10
6	7	18	7.11
7	8	16	8.0
8	9	14	9.14
9	10	13	9.85
10	11	12	10.67
11	12	11	11.64
12	13	10	12.8
13	14	9	14.22
14	15	9	14.22
15	16	8	16.0

9.4.6 Diagnostics Mode

The device includes a diagnostics mode to detect a short-circuit condition of the photodiode. To enable diagnostics mode, the `TIMEREN` and `DIAG_EN` register bits must be set to 1. An active clock must be used and the device must be in an active mode of operation. Diagnostic mode cannot be enabled when the device is in a power-down state.

The status of the diagnostics check is stored in the `PD_SHORT_FLAG` register bit and can be readout after approximately 8 ms from enabling the diagnostics mode. To readout this flag, the `REG_READ` register bit must be set. During the diagnostics mode, and immediately afterwards, the ADC output is not valid.

9.5 Register Map

Table 15. Register Map⁽¹⁾

ADDRESS (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW_RESET	DIAG_EN	TM_COUNT_RST	REG_READ
01h	0	0	0	0	0	0	0	0	LED2STC															
02h	0	0	0	0	0	0	0	0	LED2ENDC															
03h	0	0	0	0	0	0	0	0	LED1LEDSTC															
04h	0	0	0	0	0	0	0	0	LED1LEDENDC															
05h	0	0	0	0	0	0	0	0	ALED2STC\LED3STC															
06h	0	0	0	0	0	0	0	0	ALED2ENDC\LED3ENDC															
07h	0	0	0	0	0	0	0	0	LED1STC															
08h	0	0	0	0	0	0	0	0	LED1ENDC															
09h	0	0	0	0	0	0	0	0	LED2LEDSTC															
0Ah	0	0	0	0	0	0	0	0	LED2LEDENDC															
0Bh	0	0	0	0	0	0	0	0	ALED1STC															
0Ch	0	0	0	0	0	0	0	0	ALED1ENDC															
0Dh	0	0	0	0	0	0	0	0	LED2CONVST															
0Eh	0	0	0	0	0	0	0	0	LED2CONVEND															
0Fh	0	0	0	0	0	0	0	0	ALED2CONVST\LED3CONVST															
10h	0	0	0	0	0	0	0	0	ALED2CONVEND\LED3CONVEND															
11h	0	0	0	0	0	0	0	0	LED1CONVST															
12h	0	0	0	0	0	0	0	0	LED1CONVEND															
13h	0	0	0	0	0	0	0	0	ALED1CONVST															
14h	0	0	0	0	0	0	0	0	ALED1CONVEND															
15h	0	0	0	0	0	0	0	0	ADCRSTSTCT0															
16h	0	0	0	0	0	0	0	0	ADCRSTENDCT0															
17h	0	0	0	0	0	0	0	0	ADCRSTSTCT1															
18h	0	0	0	0	0	0	0	0	ADCRSTENDCT1															
19h	0	0	0	0	0	0	0	0	ADCRSTSTCT2															
1Ah	0	0	0	0	0	0	0	0	ADCRSTENDCT2															
1Bh	0	0	0	0	0	0	0	0	ADCRSTSTCT3															
1Ch	0	0	0	0	0	0	0	0	ADCRSTENDCT3															
1Dh	0	0	0	0	0	0	0	0	PRPCT															

(1) After reset, all register bits are reset to 0.

Register Map (continued)
Table 15. Register Map⁽¹⁾ (continued)

ADDRESS (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1Eh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TIMEREN	0	0	0	0	NUMAV			
20h	0	0	0	0	0	0	0	0	ENSEPGAIN	0	0	0	0	0	0	0	0	0	TIA_CF_SEP			TIA_GAIN_SEP		
21h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PROG_TG_EN	0	0	TIA_CF			TIA_GAIN		
22h	0	0	0	0	0	0	ILED3					ILED2					ILED1							
23h	0	0	0	DYNAMIC1	0	0	ILED_2X	0	0	DYNAMIC2	0	0	0	0	OSC_ENABLE	0	0	0	0	DYNAMIC3	DYNAMIC4	0	PDNRX	PDNAFE
28h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
29h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ENABLE_CLKOUT	0	0	0	0	CLKDIV_CLKOUT			0	
2Ah	LED2VAL																							
2Bh	ALED2VAL\LED3VAL																							
2Ch	LED1VAL																							
2Dh	ALED1VAL																							
2Eh	LED2-ALED2VAL ⁽²⁾																							
2Fh	LED1-ALED1VAL																							
30h	Read Only ⁽³⁾																							PD_SHORT_FLAG

⁽²⁾ Ignore the contents of this register when LED3 is used.

⁽³⁾ These bits are read-only and can be left blank.

Register Map (continued)

Table 15. Register Map⁽¹⁾ (continued)

ADDRESS (Hex)	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
31h	0	0	0	0	0	0	0	0	0	0	0	0	0	PD_DISCONNECT	0	0	0	0	ENABLE_INPUT_SHORT	0	0	CLKDIV_EXTMODE			
32h	0	0	0	0	0	0	0	0	PDNCYCLESTC																
33h	0	0	0	0	0	0	0	0	PDNCYCLEENDC																
34h	0	0	0	0	0	0	0	0	PROG_TG_STC																
35h	0	0	0	0	0	0	0	0	PROG_TG_ENDC																
36h	0	0	0	0	0	0	0	0	LED3LEDSTC																
37h	0	0	0	0	0	0	0	0	LED3LEDENDC																
39h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKDIV_PRF			
3Ah	0	0	0	0	POL_OFFDAC_LED2	I_OFFDAC_LED2				POL_OFFDAC_AMB1	I_OFFDAC_AMB1				POL_OFFDAC_LED1	I_OFFDAC_LED1				POL_OFFDAC_AMB2POL_OFFDAC_LED3	I_OFFDAC_AMB2\ I_OFFDAC_LED3				

9.5.1 Register 0h (address = 0h) [reset = 0h]

Figure 36. Register 0h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	SW_RESET	DIAG_EN	TM_COUNT_RST	REG_READ
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value after reset

Table 16. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
23-4	0	W	0h	Must write 0.
3	SW_RESET	W	0h	Self-clearing reset bit. For a software reset, write 1.
2	DIAG_EN	W	0h	0 = No action (default after reset) 1 = Diagnostic mode is enabled and the photodiode (PD) short diagnostics starts when this bit is set. At the end of the sequence (which takes approximately 8 ms to complete), the PD short fault status is stored in the PD_SHORT_FLAG register bit. Afterwards, the DIAG_EN register bit self-clears to 0.
1	TM_COUNT_RST	W	0h	Used to suspend the count and keep the counter in a reset state.
0	REG_READ	W	0h	Register readout enable for write registers (not needed for ADC output registers). 0 = Register write mode 1 = Enables the readout of write registers

9.5.2 Register 1h (address = 1h) [reset = 0h]

Figure 37. Register 1h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2STC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 17. Register 1h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED2STC	R/W	0h	Sample LED2 start

9.5.3 Register 2h (address = 2h) [reset = 0h]

Figure 38. Register 2h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 18. Register 2h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED2ENDC	R/W	0h	Sample LED2 end

9.5.4 Register 3h (address = 3h) [reset = 0h]

Figure 39. Register 3h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1LEDSTC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 19. Register 3h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED1LEDSTC	R/W	0h	LED1 start

9.5.5 Register 4h (address = 4h) [reset = 0h]

Figure 40. Register 4h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1LEDENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 20. Register 4h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED1LEDENDC	R/W	0h	LED1 end

9.5.6 Register 5h (address = 5h) [reset = 0h]

Figure 41. Register 5h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2STC\LED3STC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2STC\LED3STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 21. Register 5h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ALED2STC\LED3STC	R/W	0h	Sample ambient 2 (or sample LED3) start

9.5.7 Register 6h (address = 6h) [reset = 0h]

Figure 42. Register 6h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2ENDC\LED3ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2ENDC\LED3ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 22. Register 6h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ALED2ENDC\LED3ENDC	R/W	0h	Sample ambient 2 (or sample LED3) end

9.5.8 Register 7h (address = 7h) [reset = 0h]

Figure 43. Register 7h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1STC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 23. Register 7h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED1STC	R/W	0h	Sample LED1 start

9.5.9 Register 8h (address = 8h) [reset = 0h]

Figure 44. Register 8h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 24. Register 8h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED1ENDC	R/W	0h	Sample LED1 end

9.5.10 Register 9h (address = 9h) [reset = 0h]

Figure 45. Register 9h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2LEDSTC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 25. Register 9h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED2LEDSTC	R/W	0h	LED2 start

9.5.11 Register Ah (address = Ah) [reset = 0h]

Figure 46. Register Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2LEDENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 26. Register Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED2LEDENDC	R/W	0h	LED2 end

9.5.12 Register Bh (address = Bh) [reset = 0h]

Figure 47. Register Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1STC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1STC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 27. Register Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ALED1STC	R/W	0h	Sample ambient 1 start

9.5.13 Register Ch (address = Ch) [reset = 0h]
Figure 48. Register Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1ENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 28. Register Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ALED1ENDC	R/W	0h	Sample ambient 1 end

9.5.14 Register Dh (address = Dh) [reset = 0h]
Figure 49. Register Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
LED2CONVST							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 29. Register Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED2CONVST	R/W	0h	LED2 convert phase start

9.5.15 Register Eh (address = Eh) [reset = 0h]

Figure 50. Register Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
LED2CONVEND							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 30. Register Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED2CONVEND	R/W	0h	LED2 convert phase end

9.5.16 Register Fh (address = Fh) [reset = 0h]

Figure 51. Register Fh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2CONVST\LED3CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2CONVST\LED3CONVST							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 31. Register Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ALED2CONVST\LED3CONVST	R/W	0h	Ambient 2 (or LED3) convert phase start

9.5.17 Register 10h (address = 10h) [reset = 0h]
Figure 52. Register 10h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2CONVEND\LED3CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2CONVEND\LED3CONVEND							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 32. Register 10h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ALED2CONVEND\LED3CONVEND	R/W	0h	Ambient 2 (or LED3) convert phase end

9.5.18 Register 11h (address = 11h) [reset = 0h]
Figure 53. Register 11h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
LED1CONVST							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 33. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED1CONVST	R/W	0h	LED1 convert phase start

9.5.19 Register 12h (address = 12h) [reset = 0h]

Figure 54. Register 12h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
LED1CONVEND							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 34. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED1CONVEND	R/W	0h	LED1 convert phase end

9.5.20 Register 13h (address = 13h) [reset = 0h]

Figure 55. Register 13h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1CONVST							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 35. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED1CONVST	R/W	0h	Ambient 1 convert phase start

9.5.21 Register 14h (address = 14h) [reset = 0h]
Figure 56. Register 14h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1CONVEND							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 36. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ALED1CONVEND	R/W	0h	Ambient 1 convert phase end

9.5.22 Register 15h (address = 15h) [reset = 0h]
Figure 57. Register 15h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ADCRSTSTCT0							
R/W-0h							
7	6	5	4	3	2	1	0
ADCRSTSTCT0							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 37. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ADCRSTSTCT0	R/W	0h	ADC reset phase 0 start

9.5.23 Register 16h (address = 16h) [reset = 0h]

Figure 58. Register 16h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ADCRSTENDCT0							
R/W-0h							
7	6	5	4	3	2	1	0
ADCRSTENDCT0							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 38. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ADCRSTENDCT0	R/W	0h	ADC reset phase 0 end

9.5.24 Register 17h (address = 17h) [reset = 0h]

Figure 59. Register 17h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ADCRSTSTCT1							
R/W-0h							
7	6	5	4	3	2	1	0
ADCRSTSTCT1							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 39. Register 17h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ADCRSTSTCT1	R/W	0h	ADC reset phase 1 start

9.5.25 Register 18h (address = 18h) [reset = 0h]
Figure 60. Register 18h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ADCRSTENDCT1							
R/W-0h							
7	6	5	4	3	2	1	0
ADCRSTENDCT1							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 40. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ADCRSTENDCT1	R/W	0h	ADC reset phase 1 end

9.5.26 Register 19h (address = 19h) [reset = 0h]
Figure 61. Register 19h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ADCRSTSTCT2							
R/W-0h							
7	6	5	4	3	2	1	0
ADCRSTSTCT2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 41. Register 19h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ADCRSTSTCT2	R/W	0h	ADC reset phase 2 start

9.5.27 Register 1Ah (address = 1Ah) [reset = 0h]

Figure 62. Register 1Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ADCRSTENDCT2							
R/W-0h							
7	6	5	4	3	2	1	0
ADCRSTENDCT2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 42. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ADCRSTENDCT2	R/W	0h	ADC reset phase 2 end

9.5.28 Register 1Bh (address = 1Bh) [reset = 0h]

Figure 63. Register 1Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ADCRSTSTCT3							
R/W-0h							
7	6	5	4	3	2	1	0
ADCRSTSTCT3							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 43. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ADCRSTSTCT3	R/W	0h	ADC reset phase 3 start

9.5.29 Register 1Ch (address = 1Ch) [reset = 0h]
Figure 64. Register 1Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ADCRSTENDCT3							
R/W-0h							
7	6	5	4	3	2	1	0
ADCRSTENDCT3							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 44. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	ADCRSTENDCT3	R/W	0h	ADC reset phase 3 end

9.5.30 Register 1Dh (address = 1Dh) [reset = 0h]
Figure 65. Register 1Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PRPCT							
R/W-0h							
7	6	5	4	3	2	1	0
PRPCT							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 45. Register 1Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	PRPCT	R/W	0h	These bits are the count value for the counter that sets the PRF. The counter automatically counts until PRPCT and then returns back to 0 to start the next count.

9.5.31 Register 1Eh (address = 1Eh) [reset = 0h]

Figure 66. Register 1Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	TIMEREN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	NUMAV			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 46. Register 1Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-9	0	W	0h	Must write 0.
8	TIMEREN	R/W	0h	0 = Timer module disabled 1 = Enables timer module. This bit enables the timing engine that can be programmed to generate all clock phases for the synchronized transmit drive, receive sampling, and data conversion.
7-4	0	W	0h	Must write 0.
3-0	NUMAV	R/W	0h	These bits determine the number of ADC averages. By programming a higher ADC conversion time, the ADC can be set to do multiple conversions and average these multiple conversions to achieve lower noise. This programmability is set with the NUMAV bit control. The number of samples that are averaged is represented by the decimal equivalent of NUMAV + 1. For example, NUMAV = 0 represents no averaging, NUMAV = 2 represents averaging of three samples, and NUMAV = 15 represents averaging of 16 samples.

9.5.32 Register 20h (address = 20h) [reset = 0h]

Figure 67. Register 20h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ENSEPGAIN	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	TIA_CF_SEP			TIA_GAIN_SEP		
W-0h	W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 47. Register 20h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15	ENSEPGAIN	R/W	0h	0 = Single TIA gain for all phases 1 = Enables two separate sets of TIA gains
14-6	0	W	0h	Must write 0.
5-3	TIA_CF_SEP	R/W	0h	When ENSEPGAIN = 1, TIA_CF_SEP is the control for the C _{f2} setting.
2-0	TIA_GAIN_SEP	R/W	0h	When ENSEPGAIN = 1, TIA_GAIN_SEP is the control for the R _{f2} setting.

9.5.33 Register 21h (address = 21h) [reset = 0h]
Figure 68. Register 21h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	PROG_TG_EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	TIA_CF			TIA_GAIN		
W-0h	W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 48. Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
23-9	0	W	0h	Must write 0.
8	PROG_TG_EN	W	0h	This bit replaces the ADC_RDY output with a fully-programmable signal from the timing engine. The start and end points of this signal are set using the PROG_TG_STC and PROG_TG_ENDC controls.
7-6	0	W	0h	Must write 0.
5-3	TIA_CF	R/W	0h	When ENSEPGAIN = 0, these bits control the C_f setting (both C_{f1} and C_{f2}); see Table 50 for details. When ENSEPGAIN = 1, these bits control the C_{f1} setting.
2-0	TIA_GAIN	R/W	0h	When ENSEPGAIN = 0, these bits control the R_f setting (both R_{f1} and R_{f2}); see Table 49 for details. When ENSEPGAIN = 1, these bits control the R_{f1} setting.

Table 49. TIA_GAIN Register Settings

TIA_GAIN, TIA_GAIN_SEP REGISTER VALUE	R_f
0	500 k Ω
1	250 k Ω
2	100 k Ω
3	50 k Ω
4	25 k Ω
5	10 k Ω
6	1 M Ω
7	2 M Ω

Table 50. TIA_CF Register Settings

TIA_CF, TIA_CF_SEP REGISTER VALUE	C_f
0	5 pF
1	2.5 pF
2	10 pF
3	7.5 pF
4	20 pF
5	17.5 pF
6	25 pF
7	22.5 pF

9.5.34 Register 22h (address = 22h) [reset = 0h]

Figure 69. Register 22h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	ILED3	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	
15	14	13	12	11	10	9	8
ILED3				ILED2			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ILED2		ILED1					
R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 51. Register 22h Field Descriptions

Bit	Field	Type	Reset	Description
23-18	0	W	0h	Must write 0.
17-12	ILED3	R/W	0h	LED3 current control
11-6	ILED2	R/W	0h	LED2 current control
5-0	ILED1	R/W	0h	LED1 current control. Increments of the LED1 current setting are listed in Table 52 .

Table 52. ILED1 Register Settings

ILED1, ILED2, ILED3 REGISTER VALUES	LED CURRENT SETTING (mA)
0	0
1	0.8
2	1.6
3	2.4
...	...
63	50

9.5.35 Register 23h (address = 23h) [reset = 0h]
Figure 70. Register 23h

23	22	21	20	19	18	17	16
0	0	0	DYNAMIC1	0	0	ILED_2X	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	R/W-0h	W-0h
15	14	13	12	11	10	9	8
0	DYNAMIC2	0	0	0	0	OSC_ENABLE	0
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	DYNAMIC3	DYNAMIC4	0	PDNRX	PDNAFE
W-0h	W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 53. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	W	0h	Must write 0.
20	DYNAMIC1	R/W	0h	0 = Transmitter is not powered down 1 = Transmitter is powered down in dynamic power-down mode
19-18	0	W	0h	Must write 0.
17	ILED_2X	R/W	0h	0 = LED current range is 0 mA to 50 mA 1 = LED current range is 0 mA to 100 mA
16-15	0	W	0h	Must write 0.
14	DYNAMIC2	R/W	0h	0 = ADC is not powered down 1 = ADC is powered down in dynamic power-down mode
13-10	0	W	0h	Must write 0.
9	OSC_ENABLE	R/W	0h	0 = External clock mode (default). In this mode, the CLK pin functions as an input pin where the external clock can be input. 1 = Enables oscillator mode. In this mode, the 4-MHz internal oscillator is enabled.
8-5	0	W	0h	Must write 0.
4	DYNAMIC3	R/W	0h	0 = TIA is not powered down 1 = TIA is powered down in dynamic power-down mode
3	DYNAMIC4	R/W	0h	0 = Rest of ADC is not powered down 1 = Rest of ADC is powered down in dynamic power-down mode
2	0	W	0h	Must write 0.
1	PDNRX	R/W	0h	0 = Normal mode 1 = RX portion of the AFE is powered down
0	PDNAFE	R/W	0h	0 = Normal mode 1 = Entire AFE is powered down

9.5.36 Register 29h (address = 29h) [reset = 0h]

Figure 71. Register 29h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	ENABLE_CLKOUT	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	CLKDIV_CLKOUT				0
W-0h	W-0h	W-0h	R/W-0h				W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 54. Register 29h Field Descriptions

Bit	Field	Type	Reset	Description
23-10	0	W	0h	Must write 0.
9	ENABLE_CLKOUT	R/W	0h	In internal clock mode, the internally-generated clock can be output on the CLK pin. 0 = Disables the clock output 1 = Enables CLKOUT generation and buffering on the CLK pin. The frequency of the clock output on the CLK pin (in internal clock mode) can be set using a programmable divider controlled by the CLKDIV_CLKOUT register bit.
8-5	0	W	0h	Must write 0.
4-1	CLKDIV_CLKOUT	R/W	0h	Set the frequency of the clock output on the CLK pin (in the internal clock mode), as shown in Table 55 .

Table 55. CLKDIV_CLKOUT Register Settings

CLKDIV_CLKOUT REGISTER SETTINGS	DIVISION RATIO	FREQUENCY OF OUTPUT CLOCK IN MHz
0	1	4
1	2	2
2	4	1
3	8	0.5
4	16	0.25
5	32	0.125
6	64	0.0625
7	128	0.03125
8..15	Do not use	Do not use

9.5.37 Register 2Ah (address = 2Ah) [reset = 0h]
Figure 72. Register 2Ah

23	22	21	20	19	18	17	16
LED2VAL							
R-0h							
15	14	13	12	11	10	9	8
LED2VAL							
R-0h							
7	6	5	4	3	2	1	0
LED2VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 56. Register 2Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED2VAL	R	0h	These bits are the LED2 output code in 24-bit, twos complement format.

9.5.38 Register 2Bh (address = 2Bh) [reset = 0h]
Figure 73. Register 2Bh

23	22	21	20	19	18	17	16
ALED2VAL\LED3VAL							
R-0h							
15	14	13	12	11	10	9	8
ALED2VAL\LED3VAL							
R-0h							
7	6	5	4	3	2	1	0
ALED2VAL\LED3VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 57. Register 2Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	ALED2VAL\LED3VAL	R	0h	These bits are the ambient 2 or LED3 output code in 24-bit, twos complement format.

9.5.39 Register 2Ch (address = 2Ch) [reset = 0h]

Figure 74. Register 2Ch

23	22	21	20	19	18	17	16
LED1VAL							
R-0h							
15	14	13	12	11	10	9	8
LED1VAL							
R-0h							
7	6	5	4	3	2	1	0
LED1VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 58. Register 2Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED1VAL	R	0h	These bits are the LED1 output code in 24-bit, twos complement format.

9.5.40 Register 2Dh (address = 2Dh) [reset = 0h]

Figure 75. Register 2Dh

23	22	21	20	19	18	17	16
ALED1VAL							
R-0h							
15	14	13	12	11	10	9	8
ALED1VAL							
R-0h							
7	6	5	4	3	2	1	0
ALED1VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 59. Register 2Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	ALED1VAL	R	0h	These bits are the ambient 1 output code in 24-bit, twos complement format.

9.5.41 Register 2Eh (address = 2Eh) [reset = 0h]

Figure 76. Register 2Eh

23	22	21	20	19	18	17	16
LED2-ALED2VAL							
R-0h							
15	14	13	12	11	10	9	8
LED2-ALED2VAL							
R-0h							
7	6	5	4	3	2	1	0
LED2-ALED2VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 60. Register 2Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED2-ALED2VAL ⁽¹⁾	R	0h	These bits are the LED2-ambient2 output code in 24-bit, twos complement format.

(1) Ignore the content of this register when LED3 is used.

9.5.42 Register 2Fh (address = 2Fh) [reset = 0h]

Figure 77. Register 2Fh

23	22	21	20	19	18	17	16
LED1-ALED1VAL							
R-0h							
15	14	13	12	11	10	9	8
LED1-ALED1VAL							
R-0h							
7	6	5	4	3	2	1	0
LED1-ALED1VAL							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 61. Register 2Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED1-ALED1VAL	R	0h	These bits are the LED1-ambient1 output code in 24-bit, twos complement format.

9.5.43 Register 30h (address = 30h) [reset = 0h]

Figure 78. Register 30h

23	22	21	20	19	18	17	16
Read Only ⁽¹⁾							
R							
15	14	13	12	11	10	9	8
Read Only ⁽¹⁾							
R							
7	6	5	4	3	2	1	0
Read Only ⁽¹⁾							PD_SHORT_FLAG
R							R-0h

LEGEND: R = Read only; -n = value after reset

(1) These bits are read-only and can be left blank.

Table 62. Register 30h Field Descriptions

Bit	Field	Type	Reset	Description
23-1	Read Only	R	—	Read-only bits, do not write to these bits.
0	PD_SHORT_FLAG	R	0h	0 = Diagnostics detected no short across the PD 1 = Diagnostics detected a short across the PD

9.5.44 Register 31h (address = 31h) [reset = 0h]

Figure 79. Register 31h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	PD_DISCONNECT	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	ENABLE_INPUT_SHORT	0	0	CLKDIV_EXTMODE		
W-0h	W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 63. Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	W	0h	Must write 0.
10	PD_DISCONNECT	W	0h	This bit disconnects the PD signals (INP, INM) from the TIA inputs. When enabled, the current input to the TIA is determined completely by the offset cancellation DAC current (I_OFFDAC). Note that in this mode, the AFE no longer sets the bias for the PD.
9-6	0	W	0h	Must write 0.
5	ENABLE_INPUT_SHORT	R/W	0h	INP, INN are shorted to VCM whenever the TIA is in power-down.
4-3	0	W	0h	Must write 0.
2-0	CLKDIV_EXTMODE	R/W	0h	These bits are used to set the division ratio to allow flexible clocking in external clock mode. For details, see Table 64 .

Table 64. CLKDIV_EXTMODE Register Settings

CLKDIV_EXTMODE REGISTER SETTINGS	DIVISION RATIO	ALLOWED FREQUENCY RANGE OF EXTERNAL CLOCK IN MHz
0	2	8-12
1	8	32-48
2	Do not use	Do not use
3	12	48-60
4	4	16-24
5	1	4-6
6	6	24-36
7	Do not use	Do not use

9.5.45 Register 32h (address = 32h) [reset = 0h]

Figure 80. Register 32h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PDNCYCLESTC							
R/W-0h							
7	6	5	4	3	2	1	0
PDNCYCLESTC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 65. Register 32h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	PDNCYCLESTC	R/W	0h	PDN_CYCLE start

9.5.46 Register 33h (address = 33h) [reset = 0h]

Figure 81. Register 33h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PDNCYCLEENDC							
R/W-0h							
7	6	5	4	3	2	1	0
PDNCYCLEENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 66. Register 33h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	PDNCYCLEENDC	R/W	0h	PDN_CYCLE end

9.5.47 Register 34h (address = 34h) [reset = 0h]

Figure 82. Register 34h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_TG_STC							
W-0h							
7	6	5	4	3	2	1	0
PROG_TG_STC							
W-0h							

LEGEND: W = Write only; -n = value after reset

Table 67. Register 34h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	PROG_TG_STC	W	0h	These bits define the start time for the programmable timing engine signal that can replace ADC_RDY.

9.5.48 Register 35h (address = 35h) [reset = 0h]

Figure 83. Register 35h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_TG_ENDC							
W-0h							
7	6	5	4	3	2	1	0
PROG_TG_ENDC							
W-0h							

LEGEND: W = Write only; -n = value after reset

Table 68. Register 35h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	PROG_TG_ENDC	W	0h	These bits define the end time for the programmable timing engine signal that can replace ADC_RDY.

9.5.49 Register 36h (address = 36h) [reset = 0h]
Figure 84. Register 36h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED3LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED3LEDSTC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 69. Register 36h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED3LEDSTC	R/W	0h	LED3 start. If LED3 is not used, set these register bits to '0'.

9.5.50 Register 37h (address = 37h) [reset = 0h]
Figure 85. Register 37h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED3LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED3LEDENDC							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 70. Register 37h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0.
15-0	LED3LEDENDC	R/W	0h	LED3 end. If LED3 is not used, set these register bits to '0'.

9.5.51 Register 39h (address = 39h) [reset = 0h]

Figure 86. Register 39h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	CLKDIV_PRF		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 71. Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
23-3	0	W	0h	Must write 0.
2-0	CLKDIV_PRF	R/W	0h	Clock division ratio for the clock to the timing engine. For details, see Table 72 .

Table 72. CLKDIV_PRF Register Settings

CLKDIV_PRF REGISTER SETTINGS	DIVISION RATIO	FREQUENCY OF THE TIMING CLOCK in MHz (When the ADC Clock is 4 MHz)	LOWEST PRF SETTING (In Hz ⁽¹⁾)
0	1	4	61
1	Do not use	Do not use	Do not use
2	Do not use	Do not use	Do not use
3	Do not use	Do not use	Do not use
4	2	2	31
5	4	1	15
6	8	0.5	8
7	16	0.25	4

(1) Limit to 10 Hz.

9.5.52 Register 3Ah (address = 3Ah) [reset = 0h]
Figure 87. Register 3Ah

23	22	21	20	19	18	17	16
0	0	0	0	POL_OFFDAC_LED2	I_OFFDAC_LED2		
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
I_OFFDAC_LED2	POL_OFFDAC_AMB1	I_OFFDAC_AMB1				POL_OFFDAC_LED1	I_OFFDAC_LED1
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
I_OFFDAC_LED1			POL_OFFDAC_AMB2\ POL_OFFDAC_LED3	I_OFFDAC_AMB2\ I_OFFDAC_LED3			
R/W-0h			R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 73. Register 3Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	W	0h	Must write 0.
19	POL_OFFDAC_LED2	R/W	0h	Offset cancellation DAC polarity for LED2
18-15	I_OFFDAC_LED2	R/W	0h	Offset cancellation DAC setting for LED2
14	POL_OFFDAC_AMB1	R/W	0h	Offset cancellation DAC polarity for ambient 1
13-10	I_OFFDAC_AMB1	R/W	0h	Offset cancellation DAC setting for ambient 1
9	POL_OFFDAC_LED1	R/W	0h	Offset cancellation DAC polarity for LED1
8-5	I_OFFDAC_LED1	R/W	0h	Offset cancellation DAC setting for LED1, as described in Table 74 .
4	POL_OFFDAC_AMB2\ POL_OFFDAC_LED3	R/W	0h	Offset cancellation DAC polarity for ambient 2 (or LED3)
3-0	I_OFFDAC_AMB2\ I_OFFDAC_LED3	R/W	0h	Offset cancellation DAC setting for ambient 2 (or LED3)

Table 74. I_OFFDAC Register Settings⁽¹⁾⁽²⁾

I_OFFDAC REGISTER SETTINGS	OFFSET CANCELLATION DAC CURRENT (μA) WITH POL_OFFDAC = 0	OFFSET CANCELLATION DAC CURRENT (μA) WITH POL_OFFDAC = 1
0	0	0
1	0.47	–0.47
2	0.93	–0.93
3	1.4	–1.4
4	1.87	–1.87
5	2.33	–2.33
6	2.8	–2.8
7	3.27	–3.27
8	3.73	–3.73
9	4.2	–4.2
10	4.67	–4.67
11	5.13	–5.13
12	5.6	–5.6
13	6.07	–6.07
14	6.53	–6.53
15	7	–7

(1) I_OFFDAC can correspond to one of the four phases. POL_OFFDAC corresponds to the polarity control for the same phase.

(2) The offset cancellation DAC is not trimmed at production and, therefore, the value of the full-scale current can vary across units by ±20%.

10 Application and Implementation

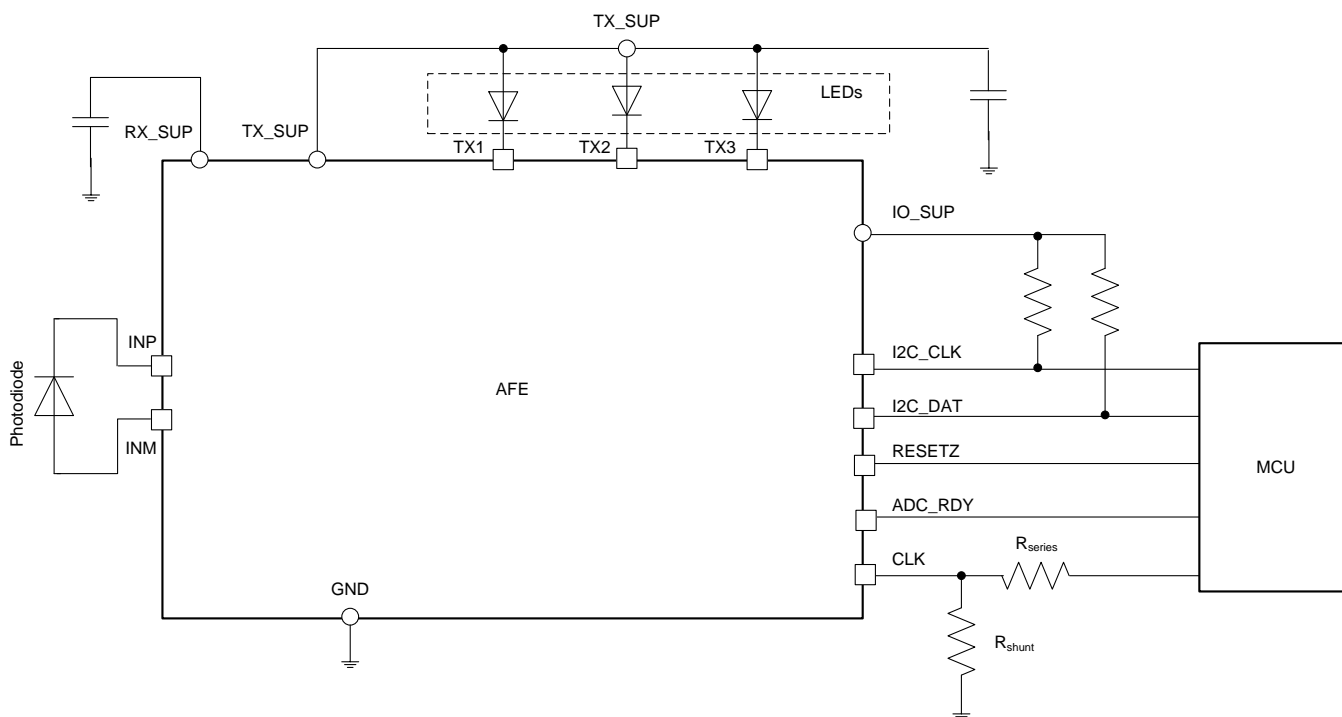
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The AFE is designed to operate with a minimal number of external components. Deriving the power supplies for the AFE from the available source of power in the system can require an additional external LDO or boost converter. A reset is essential after power-up to ensure that all registers are reset to their default values. TI also recommends that the entire system be operated using a single master clock. The AFE can either be set to accept an external clock derived from a master clock generated elsewhere in the system, or the AFE can provide its internal oscillator as an output clock to serve as the master clock for the rest of the system. If a single master clock is not possible, extra care must be taken to ensure that spurious energy from unrelated clocks does not get coupled into the AFE. If this energy does couple into the AFE the spurs get aliased based on the sampling operation. These aliased spurs can result in a faulty detection of parameters (such as heart rate). The photodiode outputs are specifically prone to picking up noise. Especially when operating in coexistence and close proximity with RF communication circuitry [such as Bluetooth® low energy (BLE)], a common-mode choke may become essential to add in the path of the AFE inputs to reject the interference.

10.2 Typical Application



NOTE: Use R_{series} in external clock mode and R_{shunt} in internal oscillator mode.

Figure 88. Typical AFE Connection

Typical Application (continued)

Figure 88 illustrates the typical connection of the AFE. The following points are to be noted:

1. Use decoupling capacitors (1 μ F or higher) placed close to the device to filter noise on RX_SUP and TX_SUP.
2. The voltage level used for IO_SUP must be the same as the I/O voltage level for the MCU.
3. In external clock mode, TI recommends connecting a series resistor (R_{series}) on the CLK pin. At power-up and before a RESET pulse is applied, the register bits can be in an uninitialized state. The CLK pin can possibly be configured as an output pin in this uninitialized state because the CLK pin is an I/O pin. In such a scenario, R_{series} limits the current (because the MCU also attempts to drive the CLK pin). For maximum frequency of the external clock (60 MHz), the R_{series} value is recommended to be 500 Ω .
4. In internal oscillator mode, a shunt resistor (R_{shunt}) equal to 500 k Ω is recommended to be connected to the CLK pin. At power-up and after reset, the device resets to the default mode of the external clock. The CLK pin is in a tri-state mode until the internal clock mode with the CLK output enabled is written through the I²C interface. The function of R_{shunt} is to pull down the CLK pin to a logic level of 0 so that the input clock to the MCU is at a logic level even when the CLK pin is tri-stated.
5. When in power-down mode (PWDN and PDNAFE) the CLK pin must be shut off (tri-stated or driven to zero), if externally driven.

10.2.1 Design Requirements

The AFE architecture is very flexible, and can be used for both high-performance saturation of peripheral capillary oxygen (SpO₂) applications as well as low-power, battery-operated heart-rate monitoring (HRM) applications as a result of this flexibility. The high dynamic range of the AFE enables excellent SNR for the signal of interest (usually small in amplitude) even in the presence of large-signal artifacts resulting from ambient and motion changes.

10.2.2 Detailed Design Procedure

The following important factors are key to extracting the full performance benefit from the AFE:

1. Good optics including bright LEDs and high-sensitivity photodiodes
2. Good mechanical design
3. A calibration loop that sets the optimal AFE settings based on the signal conditions

TI recommends that a system-level budgeting of dynamic range be initially done based on the following factors:

1. The range of the dc signal currents that are input to the AFE
2. The range of ac-to-dc ratio across different users
3. Signal current changes expected from artifacts (such as motion and ambient light changes)
4. The SNR required for heart-rate extraction algorithms to function successfully

Based on the above analysis, the available dynamic range from the AFE (approximately 100 dB) can be partitioned between the various components, and the target dc level for the calibration algorithm can also be arrived at.

10.2.3 Application Curves

This section outlines the trends described in the [Typical Characteristics](#) section from an application perspective.

Figure 1 illustrates the receiver current across different external clock frequencies. Each of the curves corresponds to a different CLKDIV_EXTMODE setting that determines the division ratio between the external clock and the internal clock (CLK_INT). The internal clock frequency must be in the range of 4 MHz to 6 MHz for proper operation, and each curve corresponds to a sweep of the external clock frequency that corresponds to an internal clock frequency sweep over the range of 4 MHz to 6 MHz.

Figure 2 illustrates the receiver current across the PRF with the dynamic power-down signal (PDN_CYCLE) enabled during the portion of the period when the receiver does not need to be active. The active period is maintained as 500 μ s for each PRF setting and the device is in power-down mode (set by PDN_CYCLE) for the rest of the period. Additionally, the timing margins indicated as t_8 and t_9 in [Figure 34](#) are included before and after the PDN_CYCLE pulse. The fraction of time that the device is in power-down mode over a period increases with reduction in the PRF because the period scales inversely with PRF. This timing is the reason why the curve

Typical Application (continued)

displays a reduction in the average receiver current with reduction in PRF. The curve corresponding to CLKDIV_PRF = 1 terminates at a lower PRF of approximately 61 Hz, which is determined by the maximum range of the 16-bit timing counter (4 MHz divided by 2^{16}). With the CLKDIV_PRF set to 16, the timer clock is divided by 16. Thus, the lower PRF range can be extended down to a few hertz (the recommended operation is to restrict the range to 10 Hz or higher). For the same PRF (for example 100 Hz), a higher CLKDIV_PRF setting results in a lower power consumption because the timer engine runs on a slower clock and takes less switching current.

The noise plots from [Figure 3](#) to [Figure 7](#) are taken at a PRF of 100 Hz. For this PRF setting, the noise at the output of the AFE is distributed from 0 Hz to 50 Hz. Plots that indicate the noise as over Nyquist bandwidth have integrated noise from 1 Hz to 50 Hz. The plots that indicate the noise as over 20-Hz bandwidth have integrated noise until 20 Hz. These plots are suitable for when additional low-pass filtering is implemented in the MCU to limit the noise bandwidth (in this case, to 20 Hz). This low-pass filtering can improve SNR because the PPG signal has information contained in the frequency band below 10 Hz.

[Figure 3](#) illustrates the input-referred noise current versus sampling duration duty cycle for different voltage levels at the receiver output. The PPG signal has a dc component that can cause the signal at the output of the receiver to be anywhere between $\pm FS$ (full-scale). The curves in [Figure 3](#) illustrate a slight increase in the noise around higher dc levels, which results from additional noise sources in the ADC. The input-referred noise current can be visualized as a noise current flowing into one of the input pins (for instance, INP) and flowing out of the other (for example, INM). The noise is computed on the samples that constitute the difference between the LED phase and the ambient phase.

[Figure 4](#) illustrates the SNR plots corresponding to the same data as [Figure 3](#). The input-referred noise and SNR can be related as follows: the input-referred noise current can be first referred to the receiver output using a factor of $2R_f$, where R_f is 500 k Ω for this case. This output-referred voltage gives the output noise that can then be referred to the full-scale value of 2 V (note that when the full-scale differential input to the ADC is 2.4 V_{PP}, the operating range is 2 V_{PP}, which is the valid operating range of the TIA).

[Figure 5](#) plots the input-referred noise current versus sampling duty cycle across different TIA gain settings.

[Figure 6](#) corresponds to the SNR plot of the data in [Figure 5](#). As illustrated in [Figure 5](#), a dynamic range of 100 dB or more can be achieved in the receiver for many of the TIA gain settings. A reduction in SNR for higher TIA gain settings is in line with what is expected from the receiver because a higher TIA gain setting implies a lower signal level at the input of the receiver.

[Figure 7](#) and [Figure 8](#) correspond to the input-referred noise current and corresponding SNR across the sampling duration duty cycle for different settings of the ADC averaging (as set by the NUMAV register setting). An ADC averaging of 1 implies no averaging. As illustrated in these curves, the SNR improves with averaging more samples. This improvement becomes more pronounced at lower TIA gain settings where the ADC noise has a higher affect on the overall receiver noise.

[Figure 9](#) refers to a hypothetical case that is used to illustrate the improvement in the receiver dynamic range when using the offset cancellation DAC. Assume that the dc level of the signal current corresponds to 7.25 μA . Without the offset cancellation DAC, assume operation is with a TIA gain of 25 k Ω , which causes the output of the receiver to be at 362.5 mV. If the offset cancellation DAC is enabled with a subtraction current of 7 μA (the maximum setting), then the signal level at the input of the TIA after the offset cancellation DAC subtraction is 0.25 μA . For this current, a TIA gain setting of 1 M Ω causes the TIA output to be at 500 mV. In effect, by enabling the offset cancellation DAC with the right setting, a higher TIA gain setting is allowed, which ends up reducing the contribution of the ADC noise and thereby reduces the input-referred noise current of the receiver. Note that the benefit from the offset cancellation DAC may not be so dramatic in an actual use case because perfect cancellation of the dc signal may not be achieved from the 0.5- μA resolution of the offset cancellation DAC. Even if achieved, the highest possible TIA gain setting on the residual current may cause receiver saturation with small changes in the dc signal level. For this reason, a safe value for the maximum gain setting when operating with the offset cancellation DAC is 250 k Ω or less. The third curve in [Figure 9](#) illustrates this case.

Typical Application (continued)

Figure 10 illustrates the effective response of the switched RC filter at the receiver output. The switched RC filter has a physical RC time constant that corresponds to a bandwidth of approximately 2.5 kHz. However, the effective bandwidth of the filter scales approximately with the sampling duration duty cycle. For a lower duty cycle, the effective filter bandwidth reduces as described from the comparison of a 5% duty cycle with a 25% duty cycle. At even lower duty cycles, the filter can double-up as a noise bandwidth reduction filter that can relax the digital-filtering requirements in the MCU.

Figure 11 illustrates the switched RC filter response for a sampling duty cycle of 1% across different PRF settings.

Figure 12 illustrates the switched RC filter response for a sampling duty cycle of 5% across different PRF settings.

Figure 13 illustrates the LED current value versus the LED current setting code. The mode marked as *50-mA LED Current Mode* corresponds to the default setting of `ILED_2X = 0`, whereas the mode marked as *100-mA LED Current Mode* corresponds to `ILED_2X = 1`. The ideal slope of these curves corresponds to 0.793 mA per code for the 50-mA current mode and 1.587 mA per code for the 100-mA current mode. However, a small deviation from these ideal values can exist from device to device, and can be viewed as a gain error in the LED current versus code. This deviation can be larger for the 100-mA current mode, with slight saturation of current especially at the high-current settings.

Figure 14 illustrates the LED current as a function of the voltage at the TX pin. The voltage at the TX pin is changed by connecting a load resistor from the TX pin to TX_SUP and changing the voltage of TX_SUP. In the 50-mA current mode, with a 50-mA current setting, the LED current starts to drop when the voltage at the TX pin goes below 0.5 V. In the 100-mA current mode, with a 100-mA current setting, the current starts to drop when the voltage at the TX pin goes below 1 V.

Figure 15 and **Figure 16** illustrate the LED current step error as a function of the LED current setting code for the 50-mA and 100-mA current modes. These plots are generated from the data in **Figure 13** after removing the gain error component (based on the best-fit curve).

Figure 17 illustrates the power-supply rejection ratio (PSRR) for a tone on the TX_SUP power rail. The frequency of the tone is swept and the magnitude of the same tone at the device output (LED-ambient) is monitored. Note that in cases where the tone frequency is greater than $PRF / 2$, power is monitored at the aliasing frequency. PSRR is computed as the RMS value of the output tone referred to the RMS value of the tone applied on the supply pin.

Figure 18 illustrates the PSRR for a tone applied on the RX_SUP power rail. PSRR is enhanced because of the presence of an internal LDO that drives the signal chain as well as the differential nature of the signal chain.

Figure 19 illustrates the rejection of a 50-Hz differential input tone. A differential current input with a frequency of 50 Hz is applied on the input pins. The magnitude of the tone at the output of the device (LED minus ambient phase) is converted to an input-referred current and compared with the magnitude of the injected current to estimate the rejection. The rejection is plotted as a function of the separation between the sampling instants of the LED and ambient phases. As illustrated in **Figure 19**, with reducing separation between the sampling instants, the rejection keeps improving because of an increased correlation of the injected tone between the two phases. A similar rejection is not obtained if only the LED phase data are considered.

Figure 20 illustrates the SNR in dBFS over a 20-Hz bandwidth across sampling duty cycle over multiple operating temperatures ranging from -40°C to 85°C .

Figure 21 illustrates the variation of the internal oscillator frequency over operating temperature on a typical unit.

10.2.3.1 Choosing the Right AFE Settings

The AFE signal chain offers several knobs that can be adjusted to achieve the SNR requirements needed for high-end, clinical, pulse-oximeter applications as well as for the low-power demands of battery-operated, optical, heart-rate monitoring applications. The knobs include TIA gain (R_f), TIA bandwidth, LED current (ILED), and offset cancellation DAC (`I_OFFDAC`). TI highly recommends running a calibration algorithm at startup and also periodically on the MCU to monitor the dc level at the output of the AFE and adjust the AFE signal chain settings to get close to the target dc level.

Typical Application (continued)

In addition to a target dc level, the high and low thresholds can also be determined (for example, 80% and 20% of full-scale), which can cause the algorithm to switch to a different TIA gain or LED current setting when the signal amplitude changes beyond the thresholds.

The optimum gain and LED current depends on the following conditions:

1. The current transfer ratio (CTR) from the LED to the photodiode
2. The perfusion index at the ADC output (the ac to dc ratio of the signal)

For clinical SPO2 applications demanding the highest SNR, where power may not be a primary concern, TI recommends setting the LED and sampling pulse durations to $> 200 \mu\text{s}$. To simplify system design, keeping the pulse duration fixed across use cases is easiest. Set the LED current to the highest value that can be afforded by the system power budget. Initialize the TIA gain to the lowest gain setting of $10 \text{ k}\Omega$ and use the initial calibration routine to determine the optimum gain. Set the ADC in averaging mode with the number of averages being the maximum afforded by the choice of pulse repetition period and pulse duration. Eight ADC averages is usually sufficient to obtain good SNR.

For power-critical, battery-operated applications, choose a sampling pulse duration between $50 \mu\text{s}$ to $100 \mu\text{s}$ and operate the device at a high TIA gain setting (for example, $1 \text{ M}\Omega$). Set the ADC in averaging mode with four to eight averages. Initialize the LED current to the desired lowest setting (of a few milliamps) and use the initial calibration routine to determine the optimum LED current setting up to the highest value allowed by the system power budget.

For pulse-oximeter applications using red and IR LEDs, the target dc level can be typically set to 50% of positive full-scale.

For HRM applications, the offset cancellation DAC can be additionally used such that the dc offset can be subtracted from the signal, thereby allowing for a larger TIA gain to be applied without saturating the signal.

The calibration routine must be designed in a manner that does not rely on the accuracy of the LED current, TIA gain, and offset cancellation DAC, thus allowing for device-to-device variations. Specifically, the offset cancellation DAC is not trimmed at production and can have a significant device-to-device variation ($\pm 20\%$). If the calibration routine requires an accurate estimate of the offset cancellation DAC, then the PD_DISCONNECT mode can be used to estimate the offset cancellation DAC range on a given unit. The PD_DISCONNECT mode disconnects the photodiode from the TIA inputs. In this mode $\text{IPD} = 0$ and, thus, the effective input current to the TIA comes solely from the offset cancellation DAC ($I_{\text{eff}} = I_{\text{OFFDAC}}$). As a result, the offset cancellation DAC value can be directly estimated from the AFE output code.

When the calibration loop is in the process of converging to the steady state, the device settings can continue to be refreshed to new values. Ideally, a time equal to t_{CHANNEL} is provided for the AFE to settle to any change in signal-chain settings. However, this time can lead to unacceptably large delays in the convergence of the calibration routine. Therefore, during the transient (when the calibration routine is in the transient phase), the wait times can be reduced to as low as $t_{\text{CHANNEL}} / 10$. After the calibration routine converges to the final settings, a wait time of t_{CHANNEL} can then be applied before high-accuracy data are read out from the AFE.

11 Power Supply Recommendations

The guidelines for power-supply sequencing and device initialization are shown in [Figure 89](#), [Figure 90](#), and [Table 75](#).

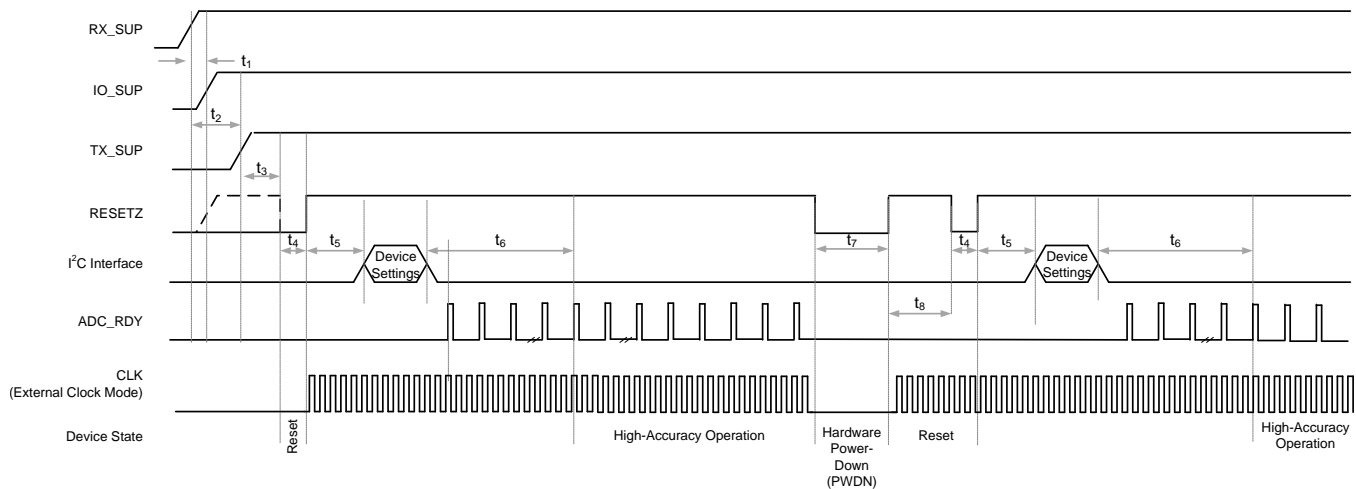


Figure 89. Power-Supply Sequencing, Device Initialization, and Hardware Power-Down Timing

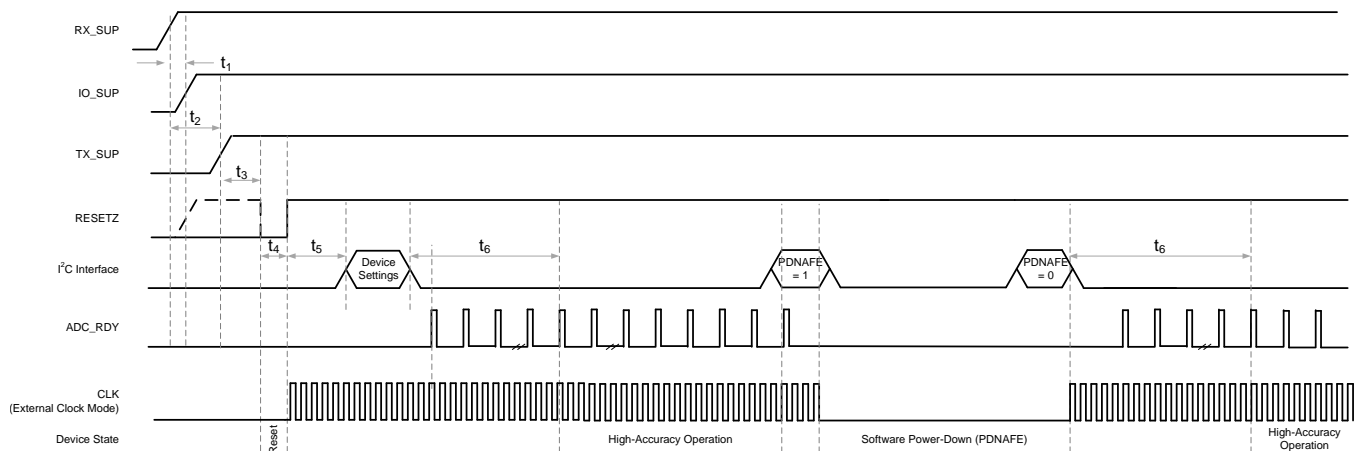


Figure 90. Power-Supply Sequencing, Device Initialization, and Software Power-Down Timing

Table 75. Timing Parameters for Power Supply Sequencing, Device Initialization, and Power-Down Timing

		VALUE
t_1	Time between RX_SUP and IO_SUP ramping up	Ramp up RX_SUP before or at the same time as IO_SUP. Keep t_1 as small as possible (for example, 10 ms).
t_2	Time between RX_SUP and TX_SUP ramping up	Keep t_2 as small as possible (for example, 10 ms).
t_3	Time between all supplies stabilizing and start of the RESETZ low-going pulse	> 10 ms
t_4	RESETZ pulse duration for the device to get reset	Between 25 μ s and 50 μ s
t_5	Time between resetting the device and issuing of I ² C commands	> 1 ms
t_6	Time between I ² C commands and the ADC_RDY pulse that corresponds to valid data	$t_{\text{CHANNEL}}^{(1)}$
t_7	RESETZ pulse duration for the device to enter PWDN (power-down) mode	> 200 μ s
t_8	Time from exiting power-down mode and subsequently resetting the device	> 10 ms

(1) The t_{CHANNEL} parameter is specified in the [Electrical Characteristics](#) table.

13 器件和文档支持

13.1 社区资源

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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13.3 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

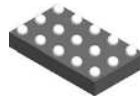
13.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

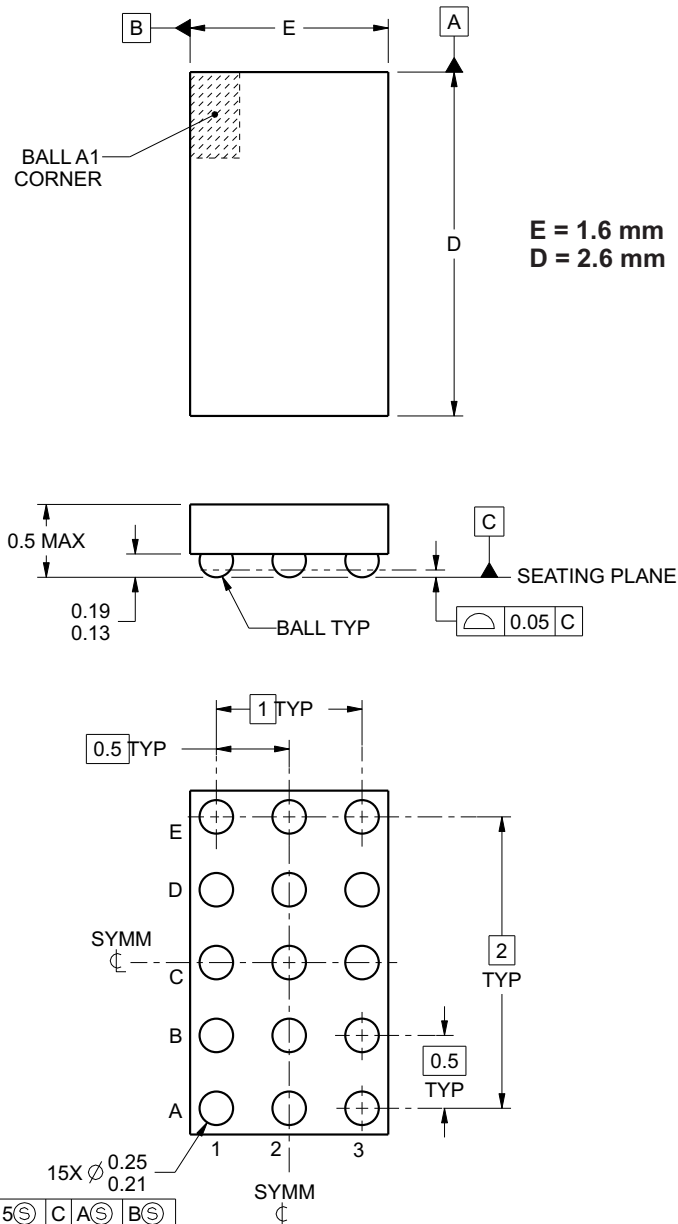


YZP0015

PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4221665/A 09/2014

NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

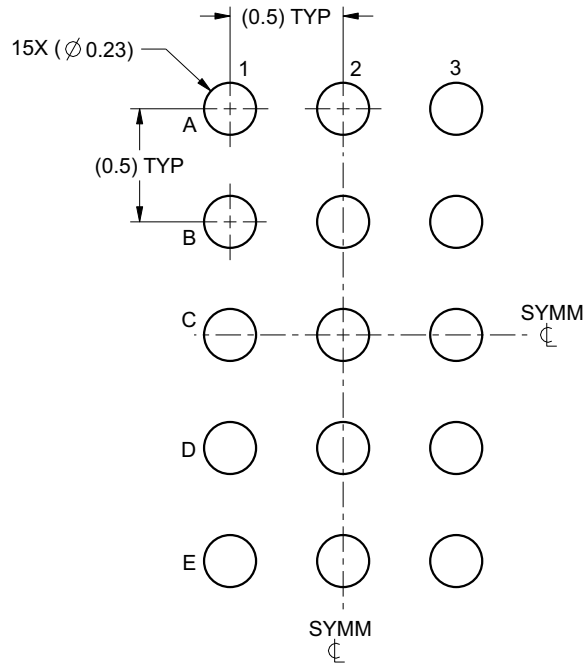
图 92. 封装外形

EXAMPLE BOARD LAYOUT

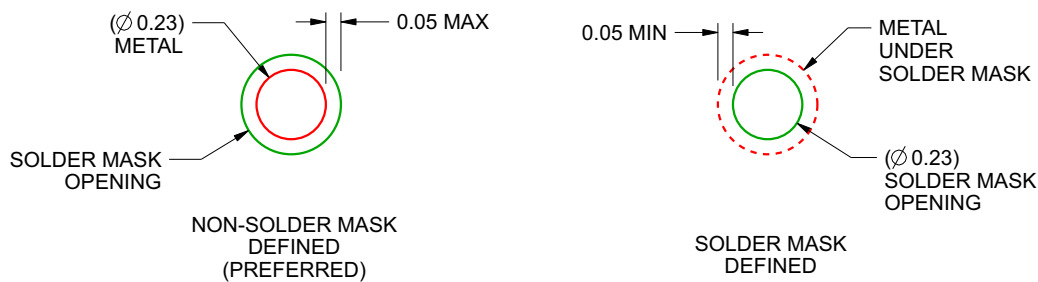
YZP0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

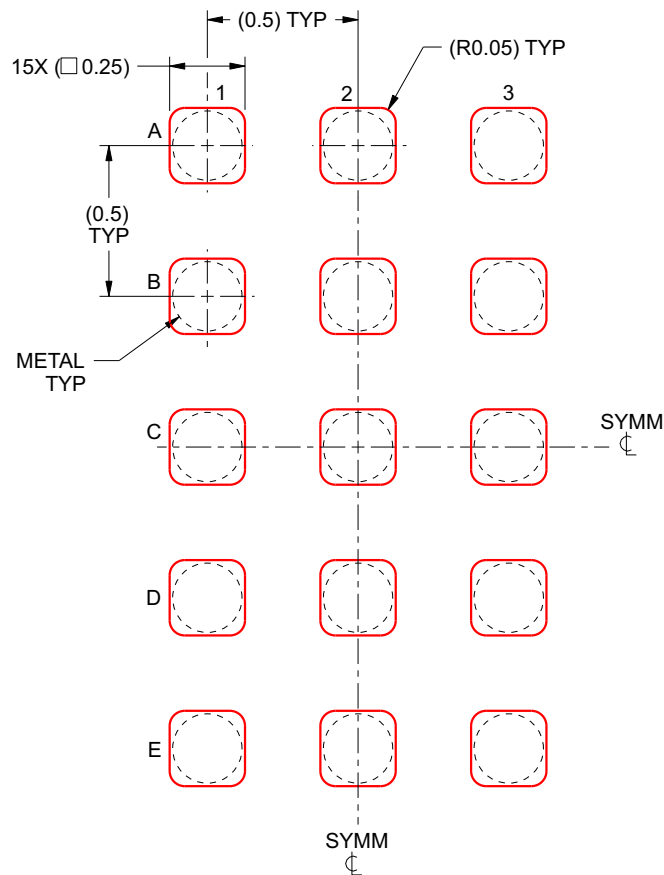
图 93. 电路板布局示例

EXAMPLE STENCIL DESIGN

YZP0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

图 94. 模板设计示例

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE4404YZPR	ACTIVE	DSBGA	YZP	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-20 to 70	AFE4404	Samples
AFE4404YZPT	ACTIVE	DSBGA	YZP	15	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-20 to 70	AFE4404	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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