**ME 365 EXPERIMENT 2**

**INTRODUCTION TO DIGITAL DATA ACQUISITION**

**Objectives**

After completing this experiment, you should be able to

• Understand and explain how an analog signal is converted to a digital signal

• Explain why clipping occurs and how to prevent it

• Explain why aliasing occurs and how to prevent it

• Determine the quantization interval for an analog to digital converter and how it is related to the quantization error

**Background**

For this experiment a simple "Digital Data Acquisition System" (DDAS) has been constructed. A simplified block diagram of the system is shown below. A more detailed diagram is shown in Figure 2 and a circuit diagram is shown in Figure 5. A single input is digitized with an analog to digital converter (ADC) and then converted back to an analog signal with a digital to analog converter (D/A), with the option of passing this output through a low pass filter.

0-3.3V

D/A

Zero order

Hold

Analog Input

ADC

integers

0 → 28 - 1

Timing Control

0-3.3V

Analog Output

Optional

Low pass

filter

**Figure 1: Block Diagram of analog to digital back to analog system.**

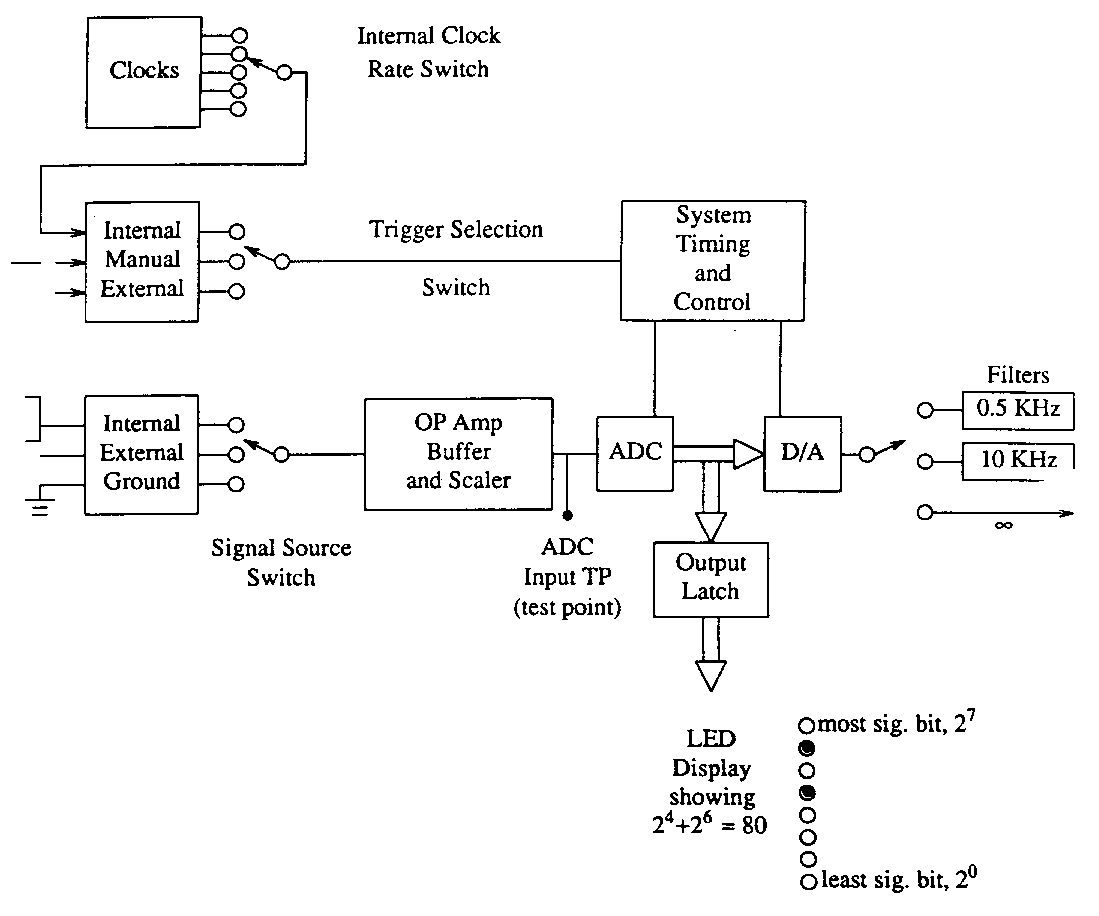
Note that there is no "front end" containing signal conditioning elements (filters and amplifiers). There are two golden rules for putting signals into analog to digital converters:

1. make sure that the signal amplitude is as big as possible but still within the input range of the analog to digital converter (amplify or attenuate the signal to achieve this).

2. make sure that the highest frequency in the signal is less than half the sample rate of the analog to digital converter (low pass filter the signal to be sure that this is true and make sure that the filter cut off frequency is much less than half the sample rate).

There is only a single input channel in this system. Multichannel systems like the one used in the PC in the ME365 Lab, have a *multiplexer* in front of the analog to digital converter. A multiplexer enables analog to digital conversion to take place on each channel in sequence. The *total* sample rate for a digital system is equal to the number of channels times the sample rate on each channel. So, if you are quoted a maximum sample rate of 44KHz. for a two channel system, that often means you can sample at 44,000 samples per second if you use 1 channel but you can only sample at 22,000 samples per second if you wish to use 2 channels.

Most systems would also have a *sample and hold* in front of the multiplexer. This piece of hardware holds the signal constant while the analog to digital conversion is taking place. If the analog to digital conversion is fast, relative to the speed at which the signals are changing, the system will work acceptably without a sample and hold. If you are doing multichannel data acquisition, then the sample and hold device becomes very important. This is because the sample and hold device holds all signals constant while it converts each signal in turn, and thus eliminates any time delays between samples taken on different channels.



**Figure 2: System Components**

**(Internal power supplies are not shown.)**

Consider now the function of each block in the above diagram.

System Timing and Control

This provides signals so that different parts of the system can be coordinated.

Trigger Selection Switch

由面板旋鈕選擇Clock 500, 1K, 10K, 20KHz

Signal Source Switch

由面板旋鈕選擇External Input, VR Input, Audio Input

c) Ground: The input can be grounded to check the zero offset of the system.

Analog to Digital Converter (ADC)

An analog to digital converter (ADC) converts an incoming voltage to an

integer code that it stores in binary. The formula for conversion is:



where n is the number of bits in the ADC. This ADC has 8 bits. There are 28 = 256 states: 128 for zero volts and above and 128 for negative voltages. The true input span of this ADC is – 5.00 volts to + 4.96 volts, and a single bit represents an input change of 40 milliVolts = 9.96 volts (input range) divided by (28 -1). This is sometimes called the quantization interval (Q), and it is also the resolution of the ADC,



Note: the input range of this device is often quoted to be +/-5 Volts,

and the quantization interval is calculated by using:



where the nominal input range in this case is 10 Volts. You will notice that both of these formulae give the same value for Q.

1000 0010

Binary Output

1000 0001

-20

-60

-100

60

20

100

Input Voltage (mV)

0111 1111

0111 1110

**Figure 3: Calibration curve for the ADC (resolution is 40 mV).**

The result of an analog to digital conversion is usually stored on a computer. To relate the integer codes back to the incoming voltages we use:

You will notice that the Stored Voltage and the Incoming Voltage are usually not equal. The maximum difference is +/- half the quantization interval which equals 20 mV in this system. This is called the maximum quantization error and = +/-Q/2 Volts.

In summary here is a table of the characteristics of this ADC plus buffer, and the PC ADC you will use in future Labs.

**Table 1: ADC Characteristics**

|  |  |
| --- | --- |
|  |  |
|  | This Lab. |
|  |  |
|  |  |
| true input span | 0 to 3.3 V |
|  |  |
| nominal input span | 0-3.3 V |
| minimum input voltage | 0 V |
| number of bits (n) | 8 |
| quantization interval (Q) | 12.9 mV |
| = resolution |  |
| max. quantization error (Q/2) | 6.45 mV |
| max. quantization error |  |
| as a % of full input range | .196% |
| = 50/(28 -1) |  |

Output Latches

Holding the output constant during the convert cycle requires a latch placed between the ADC and D/A. The latch also provides sufficient current to operate the light emitting diodes (LEDs) which indicate the binary state of the ADC output.

CU Digital to Analog Converter (D/A)

The D/A converts the digital output from the ADC back to an analog signal. The type of D/A used here is called a zero order hold because it converts its integer code back to a voltage:

The D/A holds this voltage constant until it is time to output the next sample. The output of the D/A when a sinusoidal signal is fed into the box is shown in Figure 4.

1.00

D/A Output (volts)

0.00

-1.00

0.05 0.10 0.15 0.20

Time (seconds)

**Figure 4: The output of the zero hold D/A when a sine wave is input into the system.**

During switching, spikes may appear on the analog output. The D/A requires a reference voltage. It is usual to low-pass filter the output of a D/A to eliminate the “stepped” effect of the zero order hold. The cut-off frequency of the filter is often set to frequencies between one-tenth of and one-third of the sample rate of the D/A. The choice is a function of the characteristics of the filter you are using.

Op-Amp Current to Voltage Converter-Filter

The output of the D/A converter is a current which must be converted to a voltage. Because of the high frequency switching spikes and the fact that the D/A output looks like a staircase, it may be desirable to filter the output signal. A three position switch allows the output to pass through single pole filters with cutoff frequencies of 5 kHz and 10 kHz or to pass through unfiltered ( • ).

AD_DA c_new

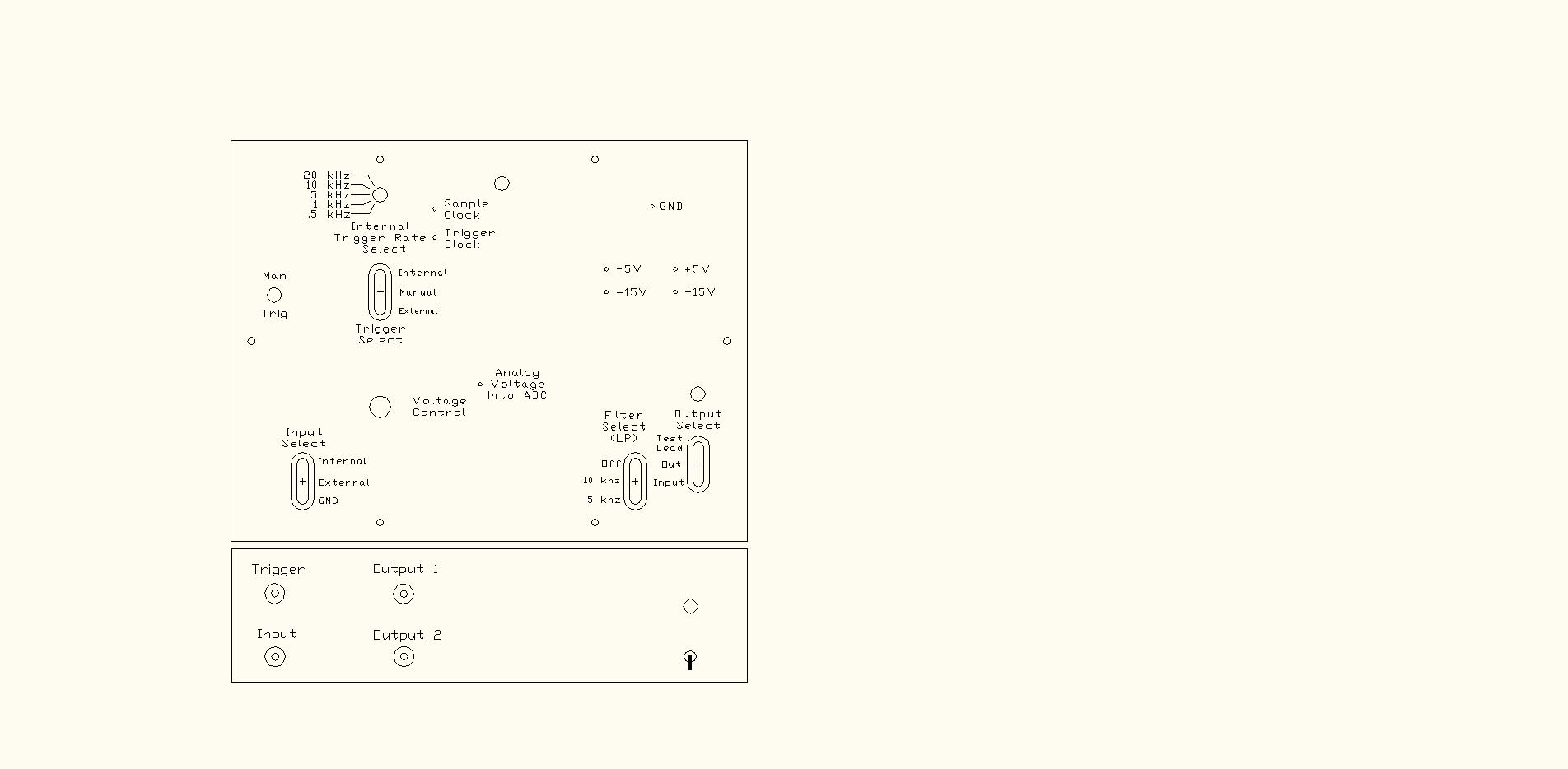
**Figure 5: Clock diagram for the ADC – D/A Box.**

AD_DA d2

**Figure 6: ADC – D/A Diagram for the ADC – D/A Box.**

AD_DA d3

**Figure 7: Power Diagram for the ADC – D/A Box.**



**Figure 8: Schematic of the ADC - D/A Box.**

**EXPERIMENT PROCEDURE**

Note the switch names will be capitalized and underlined while switch positions will just be underlined.

**1. Plug USB in**

盒子內部控制版 Red LED(POWER) solid on, blue LED blink

**3. Evaluate the ADC**

面板旋鈕選擇 Clock 20KHz, Resolution 8Bit, Filter 1KHz

Input選擇VR Input

觀察面板所顯示的ＬＥＤ數值，與三用電錶量到的ＡＤＣ ＩＮＰＵＴ

**Table 3: ADC Evaluation**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ADC | Theoretical | Theoretical | Measured | Measured Voltage |
| State | No Error Voltage  (Volts) | Range of Voltages | Range of Voltages | Span  (Volts) |
|  |  | with this Code  (Volts) | for this Code  (Volts) | (+/-20mV?) |
| 0000 0010 |  |  |  |  |
| 0000 0011 |  |  |  |  |
| 0000 0100 |  |  |  |  |
|  |  |  |  |  |
| 0111 1101 |  |  |  |  |
| 0111 1110 |  |  |  |  |
| 0111 1111 |  |  |  |  |
|  |  |  |  |  |
| 1000 0000 |  |  |  |  |
| 1000 0001 |  |  |  |  |
| 1000 0010 |  |  |  |  |
|  |  |  |  |  |
| 1111 1001 |  |  |  |  |
| 1111 1010 |  |  |  |  |
| 1111 1011 |  |  |  |  |

**4. Evaluate the Static Response of the D/A Converter**

面板旋鈕選擇 Clock 20KHz, Resolution 8Bit, Filter 1KHz

Input選擇VR Input

比較三用電錶量到的ＡＤＣ ＩＮＰＵＴ和ＤＡＣ ＩＮＰＵＴ

**Table 4: Static Response**

|  |  |  |
| --- | --- | --- |
| Input Voltage (V) | Output Voltage (V) | Error (mV) |
| **0.0V** |  |  |
| **0.5V** |  |  |
| **1.5V** |  |  |
| **2.0V** |  |  |
| **2.5V** |  |  |
| **3.0V** |  |  |
| **3.3V** |  |  |

Is the maximum error less than 1/2 LSB (least significant bit)?

**5. Dynamic Response of System**

Offset至1.5V訊號產生器調至100Hz, Offset調至1.5V, Amp調至輸出波型在範圍0~3V之內！重要！超過範圍電路會燒

最好請助教確認完再接上模組

Set the function generator to a sine wave with amplitude of 10 Volts peak to peak and a frequency above 100 Hz (**REMEMBER High Z Setting**). Connect the function generator to the INPUT jack on the front panel and to channel 1 on the oscilloscope. [NOTE: Never connect an external voltage source to OUTPUT 1 or 2 !!!]

面板旋鈕選擇 Clock 20KHz, Resolution 12Bit, Filter None

Input選擇External Input

Connect the OUTPUT to channel 2 on the oscilloscope.

Set RATE SELECT to 20kHz, 10 kHz, 5 kHz, 1 kHz, and .5 kHz. Observe the OUTPUT at each setting.

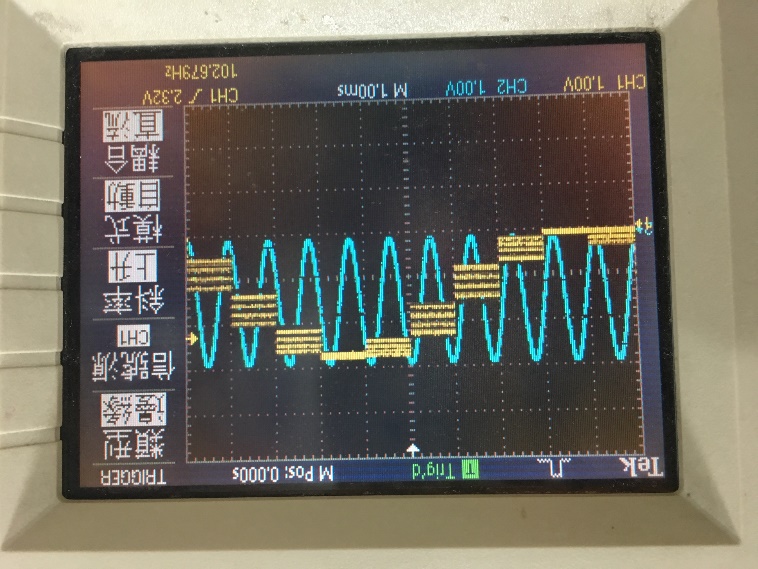
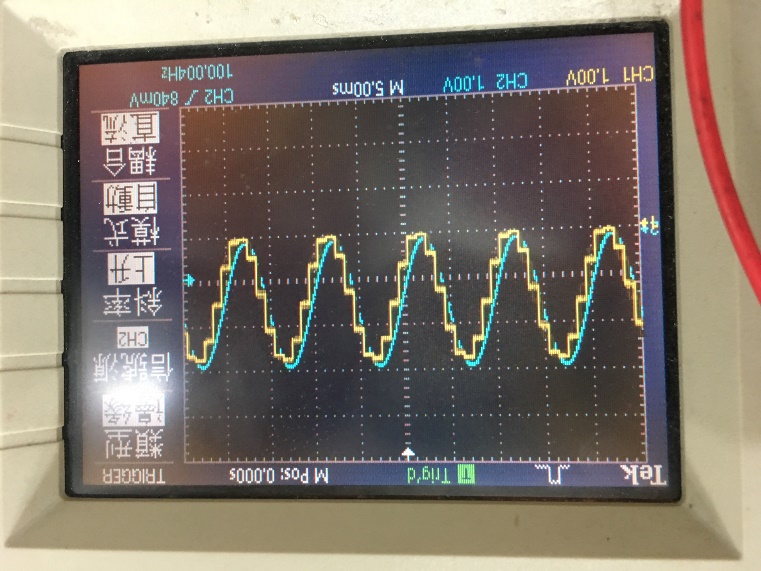
Now, with RATE SELECT at 1 kHz, set the function generator to about 1100 Hz and manually lower the frequency of the function generator by small (approximately 1 Hz) increments. Note that the signal you see on the scope has a very low frequency (can be made to approach D.C.). This is because the Nyquist criterion is not satisfied (less than 2 samples/cycle) and the output is "aliased".

Sketch the waveforms on Channels 1 and 2 of the oscilloscope below on the same graph.

1100 -> 500 -> 250 -> 200-> 100 -> 50 -> 10

1. 高低頻的鬼影- 取樣過慢aliasing 1100 -> 500
2. 500Hz 最低取樣2倍到10倍 500 -> 250 -> 200-> 100-
3. 貼近sine wave 100 -> 50 -> 10

順利地話示波器上會看到下面那樣的假影



**Channel 1 and Channel 2 waveform**

**6. Filter Effects**

面板旋鈕選擇 Clock 20KHz, Resolution 12Bit, Filter None

Input選擇External Input

方波比較明顯

正弦波只有一點點Phase Delay

或是調高頻率會比較明顯 100HZ->1KHZ

Set the function generator frequency to 100 Hz.

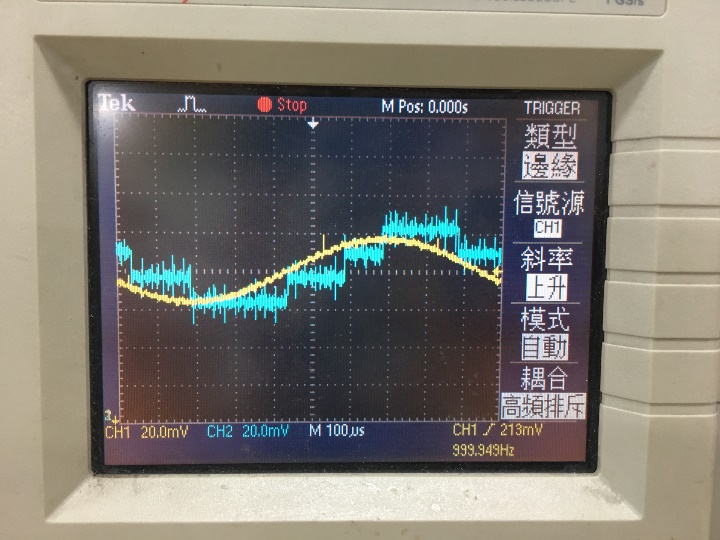
Set RATE SELECT to 20 kHz and observe the OUTPUT with the FILTER SELECT set at the 10 kHz cutoff.

Repeat with the FILTER SELECT set at the 5 kHz cutoff.

Observe the OUTPUT at various sample rate and filter cutoff frequency combinations. Note that at the lowest filter setting the OUTPUT will be attenuated and there will be a phase shift.

Now change the function generator OUTPUT to a square wave at 1 kHz and observe the OUTPUT for the various combinations.

**7. Small Amplitude Effects**

看起來只有雜訊

Set the function generator back to a 1 kHz sine wave and adjust its amplitude to 0.05 Volts peak to peak (0.04 Volts RMS).

How well does the OUTPUT represent the INPUT under the best selection of sample rate and filter setting?

Reduce the input voltage further to about 0.02 Volts RMS.

What is the main problem?

Illustrate your results with a sketch.

**8.** Demonstration of the effects of Analog to Digital and Digital to Analog

Conversion using CD player.

面板旋鈕選擇 Clock 20KHz, Resolution 12Bit, Filter None

Input選擇AUDIO Input

3.5MM 插音訊源，開到最大聲 ，手機好像比筆電輸出強

喇吧接上條條旋鈕看看效果如何

Audio input from phone, listen from headphone or speaker.

* Change ADC clock
* Change bit
* Change filter
* 1-2 song