24324

B.Tech 6th Semester (CSE) F-Scheme

Examination, May–2017

DIGITAL SYSTEM DESIGN

Paper-EE-310-F

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt **five** questions in all. **Question No.1 is compulsory** and then attempt **one** question from each of the four sections.*

1. (a) Write VHDL code for full adder using behavioural modelling. 5

(b) Explain operator overloading. 5

(c) What are generics? 5

(d) Differentiate between PLA and PAL. 5

Section-A

2. (a) Explain in detail about delay models used in VHDL. 10

(b) Discuss various operators used in VHDL. 10

3. Discuss all the data objects, data types and classes of VHDL. 20

Section-B

4. (a) Differentiate between :

(i) Array and Loop

(ii) Function and Procedure 10

(b) Write VHDL code for 8:1 multiplexer using data flow modelling. 10

5. (a) Write VHDL code for 1:16 demultiplexer using behavioural modelling. 10

(b) Explain process statement. 10

Section-C

6. (a) Write VHDL code for 4-bit SIPO register. 10

(b) Write VHDL code for decade counter. 10

7. (a) Write VHDL code for 3-bit Up-counter. 8

(b) Write VHDL code for Boolean expression $F= A+B\bar{C}$ using structural modelling and also implement the function using NOR-NOR logic. 12

Section-D

8. (a) How can ROM be used as PLA and PAL ? 10

(b) Write VHDL code for ALU. 10

9. Write down short notes on : 7,7,6

(i) FPGA

(ii) CPLD

(iii) GAL