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,	Collège Name:				
Colles	DELHI GLOBAL INSTITUTE	OF	TECH	NOL	.06
٥	Name: BAZGHA RAZI		. , ,	1111	5 7
	Course Code: PCC-CSE-205G	7			-111-
8831 5	Subject : Digital Electronics		A		
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	Tage No.
Au 1a)	In SR NAND gote circuit, the undefined input condition of set and reset is forbidden. It is the obrawback of SR flip flop. To overcome this drawback, an invester is needed. Connect invester between the set and reset inputs for producing another flip flop circuit called D flip flop.
	The input data appears at the output at the end of the clock pulse. Thus the transfer of data from the input to the output is delayed and hence it is known as D (delay) flip flop. This flip flop ensures that at the same time, both the inputs are never equal to 1 i.e., (S=R≠1). Block Diagram of D flip flop.
1	D-flip blop CLK O CLK O CLE CLE CLE CLE CLE CLE CLE

Circuit Diagram of D flip flop Cot (S) Cot (S)		Page No. Date
SR flip flop requires two inputs. By using an invertes, we can set and reset this outputs with only one input, So, the two input signal complement puch other. In D flip flop, if D is set to 1, the flip flop would be set and when it is set to I the flip flop become reset.		Circuit Diagram of D flip flop
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an invertes, we can set and reset the outputs with only one input. So, the two input signal complement part other. In D flip flop it to D is set to 1, the flip flop would be set and when it is set to I the flip flop become reset.	,	Resot (R)
The CLK (elock signal) is used to avoid this for Isolothing the data input from the flip floops latching circuitry. # ***		outputs with only one input. So, the two input signal complement such other.
		The CLK (elock signal) is used to avoid this for isolating the data input from the flip flops latching circuitry. # etk.

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			10 4-1	0 /	10.	
		31	ith Tay	ele for	D flip flog	2
		1		1 -1/2	Output (Qn+1)	
_			CLK	9rput(D)	0	
	-) X.	(No change)	
			0) <u> </u>	(140 0100)] = 1	
		0	-10	C 1 1/	is set to 1.	then the
		Oi	then the	ie., On+)) is some i	as input D.
		Wh	en the	CLK	is set to 0	, then these
		ů.	no c	hange i	is set to 0 m the output	
_						
					6-2-	· · · · · · · · · · · · · · · · · · ·
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	(a) latches	
1 ONS	The state of the s	Flip Flops
	1 0000	
4	Latches are building blocks of sequential circuits and these can be built from logic gates.	FORD Clara com 1 1 dla
	of sequential circuits and	also building
	these can be built land	blocks of sequential circuits
	logic partos	But these can be built from
	logue spales.	Flip-flope are also building blocks of sequential circuits. But these can be built from the latches.
	4 010	
_	Mork with only binary inputs.	Work will Long of
	inputs.	work with sing inputs as
		Work with binney Enputs as well as the clock signal.
	44 00 1	
	of san not be used as a	It can be used as
	It can not be used as a register.	It can be used as a register.
		The state of the s
F .	Latch continously checks	Dr. A. 12 1 0 1
	its inputs and chance of	of of Continously sheeks
	its input and changes its output correspondingly.	its inputs and changes its
	super realspondingly.	output correspondingly only
		rat times deformined by
		Clocking trans
		the flop continously checks its inputs and changes its output correspondingly only at times determined by clocking signal.
	It is level triggered, it means	10 0 10 0
	Il I Il I I I I I I I I	It is edge triggered, it means
	that the output of the present	that the output and the
	state and input of the next state	next state input changes
	depends on the level that is	when these is a change in
	binary input 1 or O.	clockpulse whother It may
		. 1
		a + ve or -ve clock pulse.
	-0 010 · · · · ·	the district of the state of
•	The latch is sensitive to the	Flip-lop is sensitive to a
	direction of the pulse and can	single change. They can transfer
	send or recieve the data when the	dato only cut the singul intant
		All I I I I I I I I I I I I I I I I I I
	switch is on.	and data carm't be changed until next signal change.
		ikki ayino o o
Complete III		

	Tage No. Date
che 26	Programmable Averay Logic
	DID (Desamonable logic device) we the components
	which don't have specific function with
	PLD (Programmable logic device) are the components which don't have specific function with them. User can perform certain function on
	So, PAL (Programmable Array Logic) is the
	type of PLD.
	PAL (Programmable Auray Logic) is a programmable logic device that has programmable AND array and fixed OR array. Block diagram of programmable Array Logic:
Ţ.	logic device that has programmable AND array
	and fixed OR wordy.
	Block diagram of programmable werray logic.
	Programmable Fixed
١٧	AND
	puts Array Array Inputs
	Here, the inputs of AND gates are programmable Each AND gate has both normal and complemented inputs of variables. So, according to our sequirement, we can program any of those inputs. So, only the required product terms by using these and AND gates are genetrated.
)t.	Each AND gote has both normal and complemented
	inputs of variables. So, according to our
	Signisement, we can program any of those
	by using these and AND gutes are genetrated.
	0
	Now, the inputs of OR gates are not of programmable type. So number of inputs to each OK gate will we be of fixed type.
	programmable type. So, number of inputs to
	were the of fixed upl

	Tage No.
	Hence, apply those required product terms to
	Octputs 10.60 RAL will be Boil like
	The advantage of PAI is floor
	of Boolean function instead of generating all the min terms by using programmable
X (V)	of the same of the
	Example: Comment of the control of t
9	Using PAL implement the following boolean functioner
	A = XY + XZ
	A = XY' + YZ'
	DO ECOXORDO .
	The given functions are in sum of products form. These are two product terms present in each Boolean function. So, we require 4 programmable AND gates and two fixed or gates feet the above two function.
	In each Boolean function So, we require
	gates for the above two function,
A.B.	
1	

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	Date
	y y z
	7 8 8
	T XY
	XZ'
	*
	A B
	The programmable AND gates have the access of both
	The programmable AND gotes have the access of both normal and complemented inputs of variables.
	Inputs X. X'X', Y, Y'Y' Z and Z'z' are available
	at the inputs of each AND gate. So program only
	the required literals In order to generate one product
	torms by our high AND gate. The symbol x is
	servis de programmable connections.
-	Inputs X, X'X', Y, Y'Y' Z and Z'Z' are available at the inputs of each AND gate. So program only the required literals In order to generate one product terms by each AND gate. The symbole X is used for programmable connections.
	of of or anter are at fixed type. So the
	The supers of the last and appropriated to insuls
	necessary product Alims are not the DP antes Donduce
	of each of yate. So may have on your
-	The inputs of OR gates are of fixed type. So the necessary product terms are connected to inputs of each OK gate. So that the OK gottes produce the respective book an furctions.
- 1	

	Tage Np.
oms 30)	Convert JK flip flop to T flip flop
Step1	JK flip flop is basically a gated SR flip flop means a SR flip flop with added layer of feedback. This feedback enables one of the two set/resol inputs so they cann't both carry an active signal to the multivibrator circuit.
,	Here the designed flip-flop is a T flip flop and the chosen one is a JK. Alip flop. The block sliagram is given below.
	T Next > J & - 0 State > K & B
Step 7:	T 9n 9n+1

	Page No.
Step3	next state table i.e., inputs of JK flip flop
	T On 9nx1 Excitation inputs D 0 0 0 0 d O 1 1 d 0 1 0 1 1 d 1 1 0 d 1
Stopl	for I am k. This k-map is called excitation map because it take value from excitation inputs.
	$(\overline{Q}_n) \circ (\overline{Q}_n) $
· · · · · · · · · · · · · · · · · · ·	Excitation Map for J imputs o J=T.

