Roll No. 3446065

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B. Tech 3rd Semester (CSE) Examination – December, 2019

DIGITAL ELECTRONICS

Paper : PCC-CSE-205-G

Time : Three Hours] *[Maximum Marks : 75*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt ***five*** questions in all, selecting ***one*** question from each Unit. Question Number 1 is ***compulsory***. All questions carry equal marks.

1. (a) State the DE Morgan's Theorem. 2.5

(b) What are the advantages and disadvantages of K-Method ? 2.5

(c) What is Full adder ? 2.5

(d) What is the difference between combinational circuits and sequential circuits ? 2.5

(c) Explain D-type flip-flop. 2.5

(f) Define Hold Time. 2.5

UNIT – I

2. (a) Realize AND, OR and NOT gate with the help of Universal gates NAND and NOR separately. 9

(b) Implement Boolean expressions for EX-OR gate using NAND gates. 6

3. Write short notes on :

(i) Error detecting and correcting code 8

(ii) Excess-3 and gray code 7

UNIT – II

4. Realize a function with the help of NAND gates : 15

$F(A, B, C. D) = \Sigma(0, 1, 4, 6, 9, 12, 15) + d(2, 3, 6)$

5. Write short notes on : 15

(i) BCD adder circuit

(ii) Priority Encoders

(iii) Multiplexer

UNIT – III

6. (a) Explain the working of Master-Slave JK Flip flop. 9

(b) What is the difference between Synchronous and Asynchronous counters ? 6

7. (a) Convert SR flip-flop to JK flip-flop. 9

(b) Explain the concept of Parallel to serial convertor. 6

UNIT – IV

8. (a) Implement a Full adder Using PLA. 9

(b) Explain the concept of Quantization and Encoding. 6

9. Write short note on : 15

(i) Field Programmable Gate array

(ii) Complex programmable logic devices

(iii) Content Addressable Memory
