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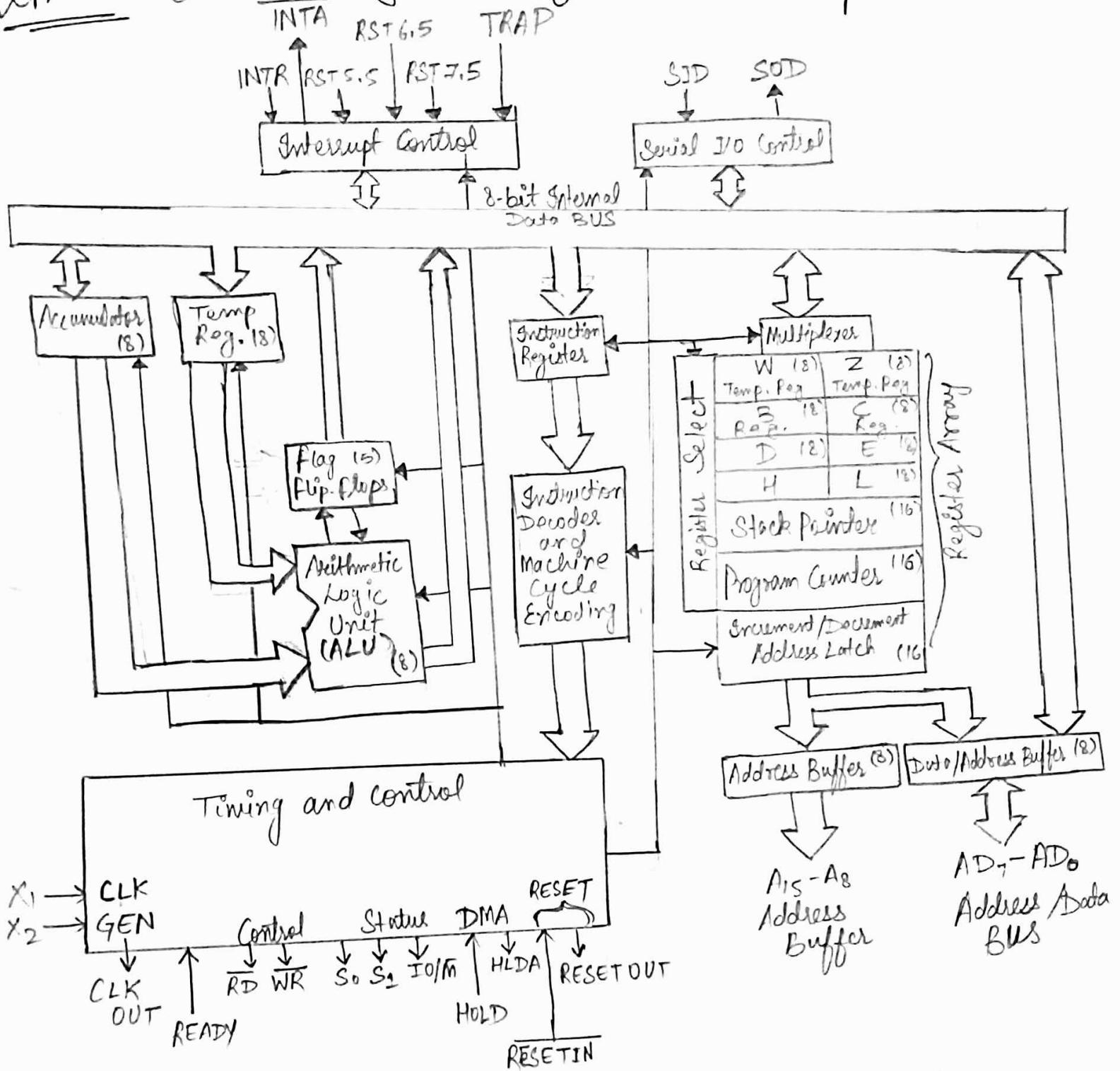
Class : B.Tech (CSE) , 3rd Year

College : Delhi Global Institute of Technology

Roll-No. : 04

Subject : Microprocessor Assignment

Ques 1 Block Diagram of 8085 microprocessor:



Each block of 8085 up is described below:

- i) **Registers:** There are six general purpose registers to store 8-bit data these are; B, C, D, E, H & L registers.

- ii) Accumulator : It is an 8 bit register that is part of ALU. It is used to store 8-bit data and to perform arithmetic and logical operations. The result of operation is stored in the accumulator, also known as register A.
- iii) Flags : It is combination of flip-flops. Based on result of arithmetic logical unit (ALU), flags indicate certain conditions. It is important in decision-making. Example of flags: zero (Z), carry (CY), sign (S), parity (P) and auxiliary carry (CȲ) flags.
- iv) Instruction decoder : After instruction fetch, instruction goes to instruction decoder.
- v) Program counter (PC) and stack pointer (SP) are two, 16-bit registers to hold memory addresses. The size of these registers is 16 bit because the memory addresses are 16 bits.
- vi) Address Bus used to carry address of memory. It is unidirectional and Data bus is bidirectional.

Ans 2 Addressing Modes : The different ways that a microprocessor can access data through an instruction is referred to as Addressing modes .

There are five addressing modes in 8085 up :-

i) Immediate addressing mode

8 or 16-bit data can be specified as a part of instruction . The instructions having 'i' letter fall under this category .

Example : a) MVI A, 24H

b) LXI H, 2040H

c) ADI , 24H

ii) Register addressing mode

Source operand, destination operand or both are contained in 8085 internal register . The name of register is specified in the instruction .

Example : a) MOV A, B

b) ADD B

iii) Direct Addressing mode

It specifies 16-bit address of the operand which is stored in memory directly in the instruction .

Example : a) LDA , 2000H

16-bit address of memory from where data has to be copied to accumulator.

b) LHLD .3000H

iv) Indirect addressing mode

The 16-bit memory address where the operand is stored is specified through contents of register pair.

Example a) MOV A, M

↳ means memory but the address of memory is indicated by HL register pair.

b) LDAX B

↳ BC register pair is indirectly specifying address of memory where operand is present.

v) Implied addressing mode

No operand is specified in the instruction. The operand on which operation has to be performed is hidden in the opcode itself.

Example : a) CMA (complement of contents of accumulator)

↳ opcode is telling about data hence no operand needs to be specified.

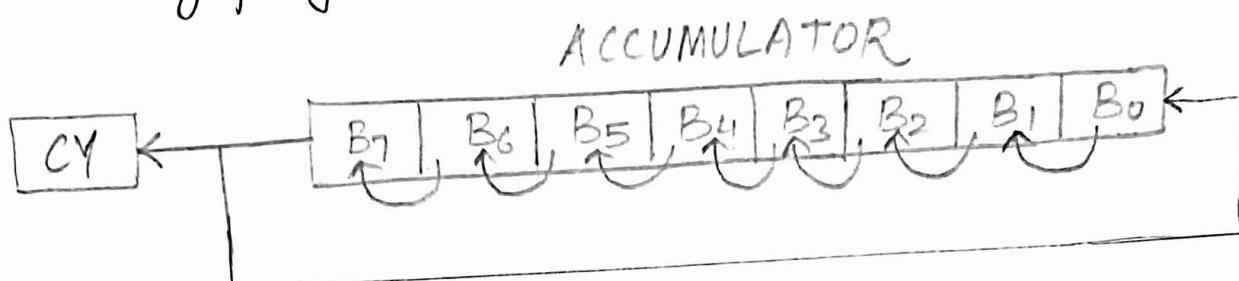
b) RAL

c) XCHG

d) RLC

Ans 3 Rotate instruction of 8085 up are:

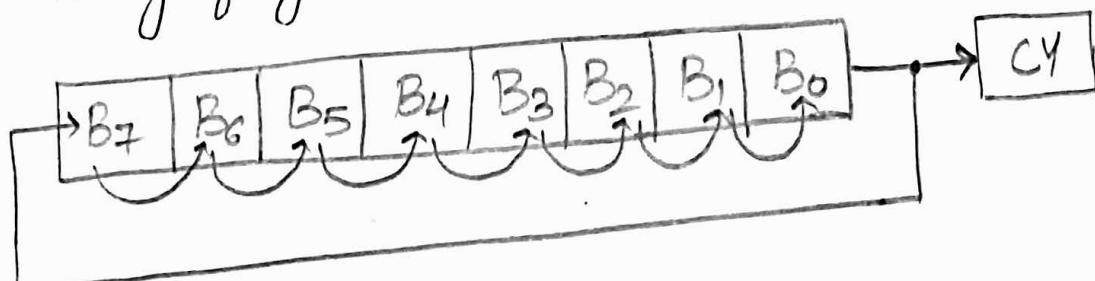
- i) RLC : This instruction rotates the content of accumulator left by one position . Bit B_7 (msb) is placed in bit B_0 (LSB) as well as carry flag .



Example : MVI A, 57H
RLC
HLT

$$\begin{array}{l} A = 01010111 \\ A = 10101110 \\ CY = 0 \end{array}$$

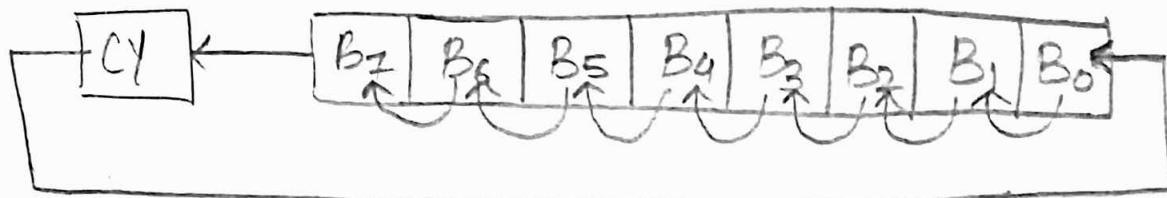
- ii) RRC : This instruction rotates the content of accumulator right by one position . Bit B_0 (LSB) is placed in B_7 (MSB) as well as in carry flag .



Example : MVI A, 9AH
RRC
HLT

$$\begin{array}{l} A = 10011010 \\ A = 01001101 \end{array}$$

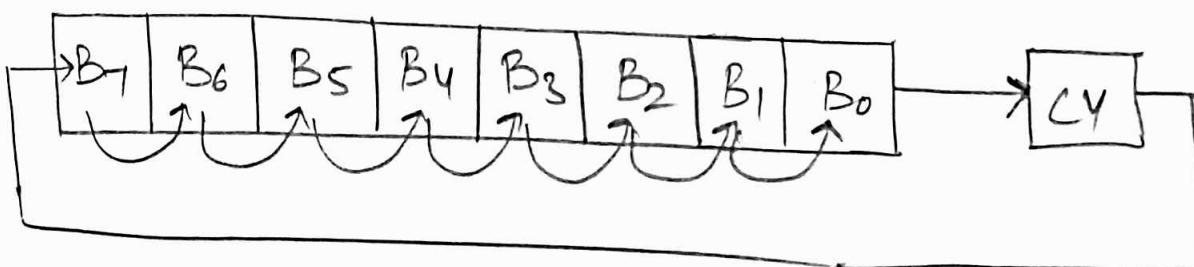
iii) RAL : This instruction rotates the content of accumulator left by one position. Bit B_7 (MSB) is placed in carry flag and CY flag is placed in bit B_0 (LSB).



Example : MVI A, ADH
RAL
HLT

$$\begin{array}{ll} A = 10101101 & CY = 0 \\ A = \underbrace{01011010}_{5AH} & CY = 5 \end{array}$$

iv) RAR : This instruction rotates the content of accumulator right by one position. Bit B_0 (LSB) is placed in CY flag and CY flag is placed in bit B_7 (MSB).



Example : MVI A, A3H
RAR
HLT

$$\begin{array}{ll} A = 1010\ 0011 & CY = 0 \\ B = \underbrace{0101\ 0001}_{51H} & CY = 1 \end{array}$$

Ans 4) Interrupts : Due to certain condition, the normal processing of up needs to be stopped to address the arised condition. This is known as interrupt. Interrupt is a process of data transfer whereby an external device can inform the up that it is ready for communication and hence it requests attention.

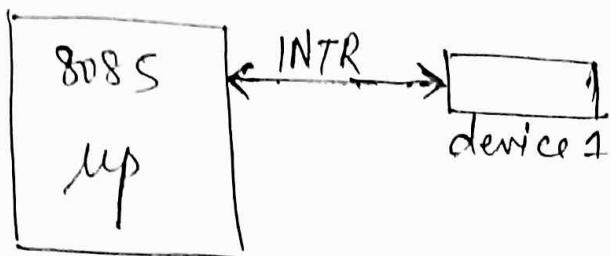
Interrupt request are classified in two categories:

- i) Maskable Interrupt : Microprocessor can ignore or delay a maskable interrupt request. If it is performing some critical task.
- ii) Non-maskable Interrupt : Microprocessor cannot ignore or delay non-maskable interrupt request. It has to be serviced immediately.

Vectored Interrupts : When an external device raises an interrupt request, up has to execute ISR associated with the interrupt, if the internal circuit of the up produces a CALL to a pre-determined memory location which is the starting address of ISR then that address is called vector address and such interrupts are called vector interrupts.

Enable interrupt instruction and disable interrupt instruction are machine control instruction which can enable / disable use of interrupts.

INTR is a non-vectorized interrupt



In general 8085 will perform some task. At some instant, inter signal becomes active. This means 8085 receives a interrupt request by device 1

Microprocessor will pause the main program and execution will begin from memory location of ISR written for INTR interrupt. After executing the ISR the CPU will return to the main program.

TRAP is non-maskable interrupt.

SIM is also known as set interrupt mask. It uses to mask individual interrupts.

Interrupt Type	Trigger Type	Priority	Maskable	Vector Address
TRAP	Edge/Level	1 st	No	0024H
RST 7.5	Edge	2 nd	Yes	003CH
RST 6.5	Level	3 rd	Yes	0034 H
RST 5.5	Level	4 th	Yes	002CH
INTR	Level	5 th	Yes	Generate externally

Ans 5 a) CMA : This instruction complements each bit of the accumulator.

Example : $A = 1000 \cdot 1000 = 88H$ | $A \leftarrow \bar{A}$
 $CMA = 77H$ | $\bar{A} = 01110111$

b) NOP : It stands for No operation. The instruction is fetched and decoded, however no operation is executed. It doesn't do any work for one instruction cycle.

c) HLT : It stands for halt. The HLT instruction used for terminating the program. It stops the execution of the program.

d) XCHG : This instruction exchanges the contents of the register H with that of D and L with that of E.

Operation - $H \leftrightarrow D$ and $L \leftrightarrow E$

Example : $DE = 2040H$, $HL = 7080H$

$XCHG \rightarrow H = 20H, L = 40H$
 $D = 70H, E = 80H$

e) DAD : This instruction adds the contents of the specified register pair to the contents of the HL register pair such as BC, DE, HL or stack pointer. Only higher order register is to be specified for register pair within the instruction.

Operation - : $HL \leftarrow HL + sp$

f) LDAX : This instruction copies the contents of memory location whose address is specified by the register pair into the accumulator. The rp is BC or DE register. The register pair is used as a memory pointer.
Operation : $A \leftarrow (\text{rp})$

g) SHLD : This instruction stores the contents of L register in the memory location given within the instruction is used to store the contents of H & L registers directly into the memory. The contents of the H and L registers remain unchanged.

h) CALL : This instruction is used in the main program to call a subroutine. The CALL instruction is stored on the stack by the CPU automatically and the program execution is transferred to the subroutine address.

i) RET : This instruction is used at the end of the subroutine to return to the main program. When the RET instruction is executed at the end of the subroutine, the memory address stored on the stack during CALL is retrieved back to the PC register so that the sequence of execution is resumed in the main program.

Ans 6 ALE signal in 8085 UP:

ALE signal is used to demultiplex the Address/data lines by enabling the D-latch. This signal is high during initial part of the instruction cycle. After that it remains in-active for the remaining part of instruction cycle. It automatically becomes high again during the initial part of next instruction cycle.

Ans 8 Instruction Set: It is a binary pattern designed inside a microprocessor to perform a specific function. The entire group of instructions, called the instruction set, determines what functions the microprocessor can perform. The 8085 instruction set is classified into the following three groups according to word size or byte size.

a) One-byte instruction: It includes the opcode and the operand in the same byte.

Example: MOV → copy the contents of the accumulator in register C.

ADD, CMA, etc

b) Two-byte instruction: In a 2-byte instruction, the first byte specifies the operation code and the second byte specifies the operand.

Example: MVI

These instructions would require 2 memory location each to store the binary codes.

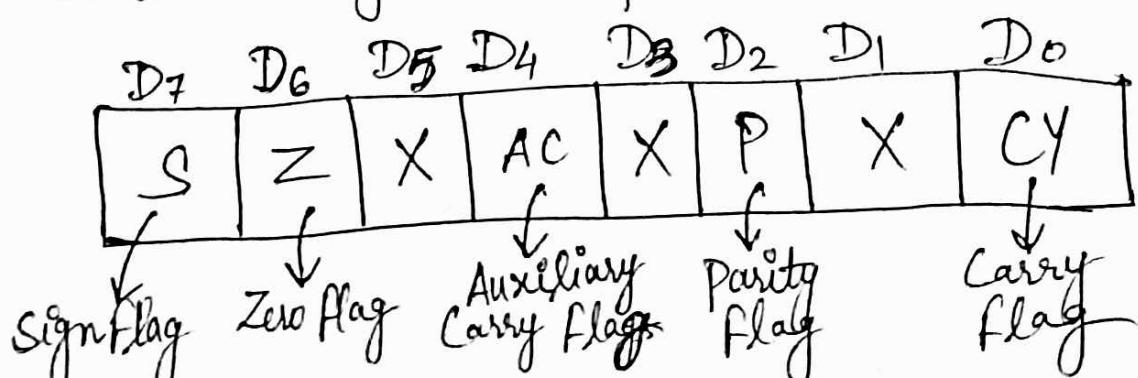
c) Three-byte instruction: In a 3-byte instruction, the first byte specifies the opcode, and the following 2-bytes specify the 16-bit address. In this, the second byte is the low-order address and the third byte is the high-order address.

Example: LDA, JMP, etc.

Table of Instruction Set

Notation	Meaning
M	Memory location pointed by HL register pair
x	8-bit register
rp	16-bit register pair
rs	Source register
rd	Destination register
addr	16-bit address / 8-bit address

Ans 9 flag Register: The ALU includes five flip-flops, which are set or reset after an operation according to data conditions of the result in the accumulator and other registers. There are 5 flags in 8085, they are organised in a 8-bit register as follows:



Bits marked with X mean no flags are assigned for those bits.

Sign Flag : After execution of some operation in ALU, if the result MSB is 1, it is interpreted as -ve value and hence sign flag is set ($S=1$).

Example: Subtract two numbers.

$$\begin{array}{r} 0110 \\ - 0001 \\ \hline 0101 \end{array}$$

MSB
(value of MSB becomes value of sign flag)

Zero Flag : The Z flag is set if the result of same operation in ALU is zero and similarly Z flag is reset if result is non-zero.

$Z=0$, is reset ; $Z=1$, is set

Example: We are adding two number

$$\begin{array}{r} 0110 \\ - 0110 \\ \hline 0000 \end{array}$$

\therefore result is a zero value hence $Z=1$

Auxiliary carry flag: This flag is set if there is an overflow out of bit 3, or if there is a carry from lower nibble to higher nibble then this flag becomes 1, else it remains zero.

Example: Add two numbers

$$\begin{array}{r}
 & 1 \rightarrow AC \\
 \begin{array}{r} 0001 \\ + 0010 \end{array} & \begin{array}{r} 1100 \\ 1000 \end{array} \\
 \hline
 & 0100
 \end{array}$$

Parity flag: Parity is defined by the number of ones present in the result.

If the result has even number of ones $P=1$

If the result has odd number of ones $P=0$

Example: A $\boxed{0110\ 0101}$
 No. of 1's = 4 (even)
 $P=1$

Carry flag: This flag is set if there is overflow out of bit 7 (MSB) of the result after some ALU operation.

Example: Adding two numbers

$$\begin{array}{r}
 1001\ 1011 \\
 + 0111\ 0101 \\
 \hline
 10001\ 0000
 \end{array}$$

$CY=1$
 carry \swarrow

Ans 10 PC and SP register of 8085 up
These are two 16-bit registers used to hold
memory addresses. The size of these registers is
16 bits because the memory addresses are 16 bits.
The up uses the PC register to sequence the
execution of the instructions. The function of PC
is to point to the memory address from which
the next byte is to be fetched. When a byte is
being fetched, the PC is incremented by one to point
to the next memory location.
The stack pointer (SP) is also a 16-bit register
used as a memory pointer. It points to a memory
location in R/W memory, called the stack. The beginning
of the stack is defined by loading a 16-bit
address in the stack pointer.

Ans 11 DAA : This instruction adjusts accumulator to
packed BCD after adding two BCD
numbers.

Instruction works as follows:

- i) If the value of the low order four bits ($D_3 - D_0$) in
the accumulator is greater than 9 or if auxiliary
carry flag is set, the instruction adds 6 to the
low-order four bits.
- ii) If the value of the higher-order four bits ($D_7 - D_4$)
in the accumulator is greater than 9 or if
carry flag is set, the instruction adds 6 to
the high-order four bits.

Example: If $A = 0011\ 1001 = 39 \text{ BCD}$
and $C = 0001\ 0010 = 12 \text{ BCD}$

ADD C

$$A = 0100\ 1011 = 4BH$$

DAA

$$\begin{aligned} &\text{add } 0110 = 6 \text{ BCD} \\ &\text{because } 1011 > 9 \end{aligned}$$

HLT

$$\therefore A = 0101\ 0001 = 51 \text{ BCD}$$

Ans 12

Opcode : It is also known as operation code. It is the one in which the task to be performed.

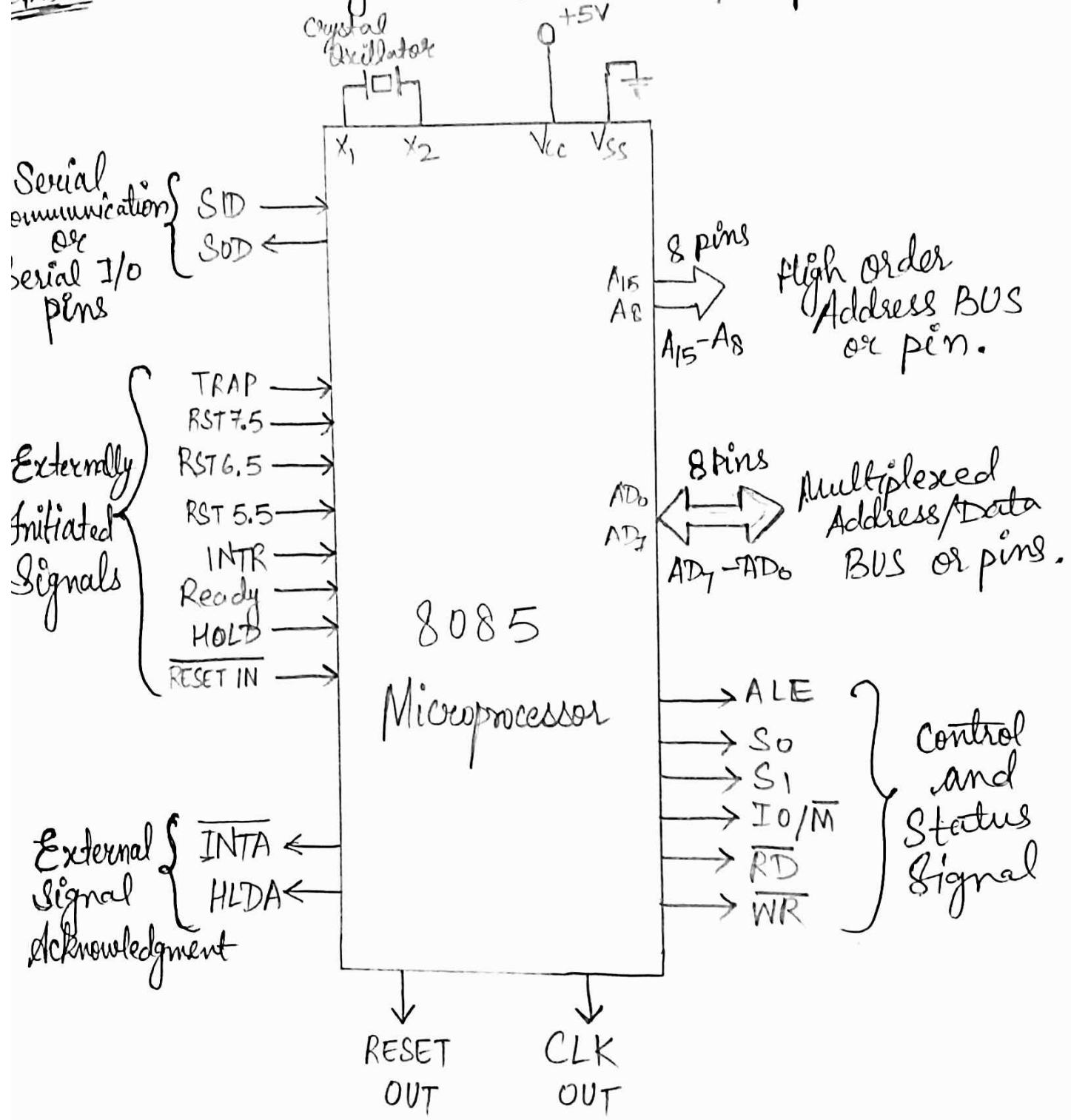
Operand : In this the data to be operated. It may include 8-bit or 16-bit data, an internal register, a memory location, or an 8-bit or 16-bit address.

Example: MOV H, L

Opcode \rightarrow MOV

Operand \rightarrow H, L

Ans 13 Pin diagram of 8085 microprocessor:



Total 40 pins in 8085 up

- * V_{cc} → power pin, +5V input voltage
 V_{ss} → Ground pin
- * X_1 and X_2 : These pins are used for microprocessor clock signal generation. A crystal oscillator of frequency 6 MHz is connected b/w X_1 and X_2 . This will generate a clock signal of 3 MHz inside 8085 microprocessor.
- * ALE signal is used to demultiplex the address/data lines by enabling the D-latch.
- * IO/M : This pin indicates IO/device operation or memory operation. When $IO/M = 1$, mean microprocessor is communicating with a IO device and when $IO/M = 0$ mean up is communicating with memory.
- * \overline{RD} : Active low read signal when $\overline{RD} = 0$ mean up wants to read data from memory or IO device.
- * \overline{WR} : Active low write signal when $\overline{WR} = 0$ means up wants to write data to memory or IO device.
- * SID : Serial input data pin. This pin accept serial data bits from external device.
- * SOD : Serial output data pin. This pin will send serial data bits to some external device.

Ans14) Logical Instruction

a) ANA r : This instruction logically ANDs the contents of the specified register with the contents of accumulator and stores the result in the accumulator. Each bit in the accumulator is logically ANDed with the corresponding bit in register r, i.e., D₀ bit in A with D₀ bit in register r, D₁ in A with D₁ in r, and so on upto D₇ bit. The register r is 8-bit general purpose register such as A, B, C, D, E, H & L.

Operation: $A \leftarrow A \text{ AND } r$

Example: ANA B
 $A \leftarrow (A) \text{ AND } (B)$

- i) LXI H, 2000H
ANA M
 $A \leftarrow A \text{ AND } (2000H)$
- ii) ANI 4FH
 $A \leftarrow A \text{ AND } 4FH$

b) XRA r : This instruction logically XORs the contents of the specified register with the contents of accumulator and stores the result in the accumulator. The register r is 8-bit general purpose register such as A, B, C, D, E, H & L.

Operation $A \leftarrow A \oplus r$

Example : i) XRA C

$$A \leftarrow A \oplus C$$

$$A = 1010\ 1010 \quad (\text{AAH})$$

$$\oplus \\ C = 0010\ 1101 \quad (2DH)$$

$$\Downarrow \\ A = 1000\ 0111 \quad (87H)$$

~~ii) XRA M~~

$$A \leftarrow A \oplus M$$

~~iii) XRI 4FH~~

$$A \leftarrow A \oplus 4FH$$

c) ORA r : This instruction logically ORs the contents of specified register with the contents of accumulator and stores the result in the accumulator. Each bit in the accumulator is ORed with corresponding bit in register r i.e., D₀ bit in accumulator is ORed with D₀ bit in register r, D₁ in A with D₁ in r and so on upto D₇ bit. The register r is 8-bit general purpose register such as A, B, C, D, E, H and L.

Operation : $A \leftarrow A \vee r$

Example :- i) OR A B

$$A \leftarrow A \vee B$$

$$\begin{array}{l} A = 1010\ 1010 \text{ (AAH)} \\ \swarrow \\ B = 0001\ 0010 \text{ (12H)} \end{array}$$

$$\begin{array}{l} \downarrow \\ A = 1011\ 1010 \text{ (BAH)} \end{array}$$

ii) OR A M

$$A \leftarrow A \vee M$$

iii) ORI 4FH

$$A \leftarrow A \vee 4FH$$

d) CMP r : This instruction subtracts the contents of the specified register from contents of the accumulator and sets the condition flags as a result of the subtraction. It sets zero flag if $A=r$ and sets carry flag if $A < r$.

Operation : $A - r$

Example :- i) CMP B

$$A - B$$

ii) CMP M

$$A - M$$

iii) CMP 4FH

$$A - 4FH$$

e) CMA : This instruction complements each bit of the accumulator.

Operation : $A \leftarrow \bar{A}$

Example : MVI A, 88H

CMA

$$\Rightarrow A = 1000 \quad 1000 \quad (\text{88H})$$
$$\bar{A} = 0111 \quad 0111 \quad (\text{77H})$$

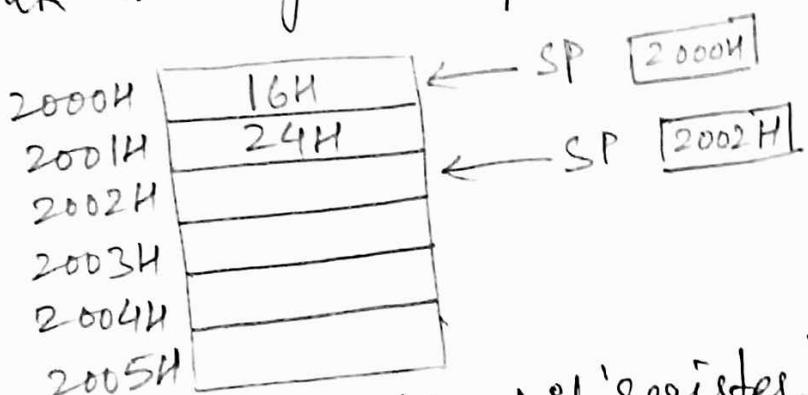
$$\therefore A \leftarrow \bar{A} \quad (\text{77H})$$

Ques 15 Stack Memory is that is a portion of read/write memory set aside by the user (or programmer) for the purpose of storing temporary data.

Stack data is organised in two ways:

- * FILO (First in Last out)
- * LIFO (Last in first out)

Stack memory is implemented in 8085 CPU.



Stack pointer (16-bit register)

PUSH B

In 8085 PUSH is the opcode for writing value in stack memory. The value to be stored in stack memory will always be a 16-bit value. We will always use register pair with PUSH instruction.

PUSH operation: Writing data onto stack memory.

POP operation: Reading data from stack memory.