8.15.1 Design of MOD-3 Counter

MOD-3 counter is one with three states. To design a counter with three states, the number of flip-flops required can be found using the equation $2^n \geq N \geq 2^{n-1}$, where n is the number of flip-flops required and N is the number of states present in the counter. For $N = 3$, from the above equation, $n = 2$, i.e. two flip-flops are required. Assume that the MOD-3 counter has three states a, b and c and its sequence is given by $a \rightarrow b \rightarrow c \rightarrow a \ldots$

Step 1 State diagram Now, the state diagram for the MOD-3 counter can be drawn as shown in Fig. 8.17. Here, it is assumed that the state transition from one state to another takes place when the clock pulse is asserted; when the clock is unasserted, the counter remains in the present state.

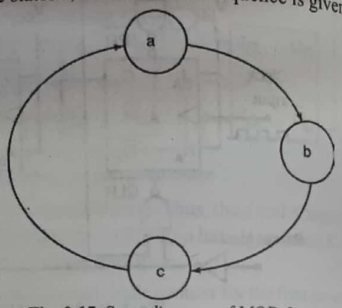

Fig. 8.17 State diagram of MOD-3 counter

Step 2 State table From the above state diagram, one can draw PS-NS table (Table 8.8).

Table 8.8 PS-NS table for MOD-3 counter

Present state (PS)	Next state (NS)
a	b
b	c
c	a

The state table given in Table 8.8 has no redundant state because no two states are equivalent. Hence, there is no modification required in the given state table.

Step 3 State assignment Let us assign two state variables to states a, b and c as follows: $a = 00$, $b = 01$ and $c = 10$. Then, the PS-NS table gets modified as shown in Table 8.9.

Table 8.9 PS-NS table for MOD-3 counter

Present state (PS)		Next state (NS)	
q_1	q_0	Q_1	Q_0
0	0	0	1
0	1	1	0
1	0	0	0
.....		.....	
1	1	d	d

Step 4 Excitation table Although any one of the four flip-flops, i.e. *SR*, *JK*, *T* and *D*, can be used , the selection of *J-K* flip-flop will result in a simplified circuit for synchronous counters. The excitation table having entries for flip-flop inputs (J_1K_1 and J_0K_0)

can be drawn from the above PS-NS table (and using the application table of *JK* Flip-flop given in Table 7.11) as shown in Table 8.10.

Table 8.10 Excitation table for MOD-3 counter

PS		NS		Excitation inputs			
q_1	q_0	Q_1	Q_0	J_1	K_1	J_0	K_0
0	0	0	1	0	d	1	d
0	1	1	0	1	d	d	1
1	0	0	0	d	1	0	d
.....							
1	1	d	d	d	d	d	d

In the first row of the above table, for the flip-flop 2 of the counter to change from present state ($q_1 = 0$) to next state ($Q_1 = 0$), the J_1K_1 inputs required are $0d$; for flip-flop 1 to change from $q_0 = 0$ to $Q_0 = 1$, the J_0K_0 inputs required are $1d$. Similarly, other entries are also made using the application table.

Step 5 Excitation maps The excitation maps for J_1, K_1, J_0 and K_0 inputs of the counter can be drawn as shown in Fig. 8.18 from the excitation table (Table 8.10).

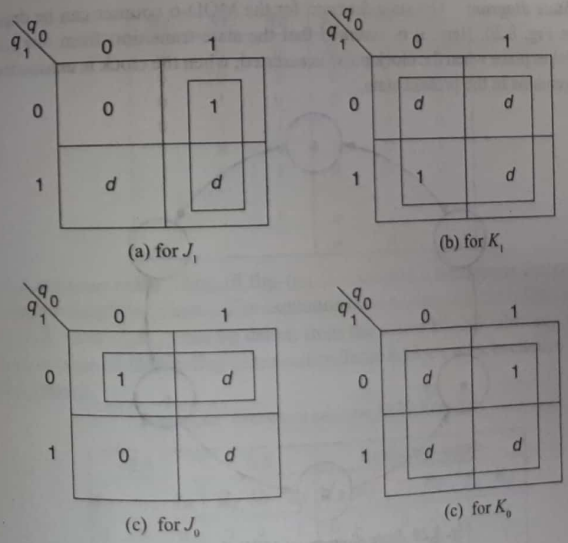

Fig. 8.18 Excitation maps

From the above excitation maps, the simplified excitation functions are :

$$J_1 = q_0,\ K_1 = 1;\ J_0 = \bar{q}_1 \text{ and } K_0 = 1$$

Step 6 Schematic diagram Using the above excitation equations, the circuit diagram for the MOD-3 counter can be drawn as shown in Fig. 8.19.

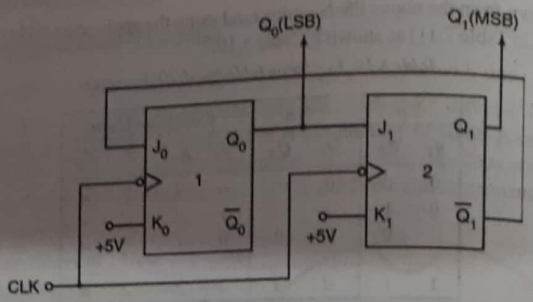

Fig. 8.19 Circuit diagram for MOD-3 synchronous counter

8.15.2 Design of MOD-6 Counter

In order to design a MOD-6 counter with six states, the number of flip-flops required is three. This is found from the equation $2^n \geq N \geq 2^{n-1}$, where $N = 6$, the number of states present in the MOD-6 counter. Let us assume that the MOD-6 counter has six states, viz. *a, b, c, d, e* and *f*.

Step 1 State diagram The state diagram for the MOD-6 counter can be drawn as shown in Fig. 8.20. Here, it is assumed that the state transition from one state to another takes place when the clock pulse is asserted; when the clock is unasserted, the counter remains in the present state.

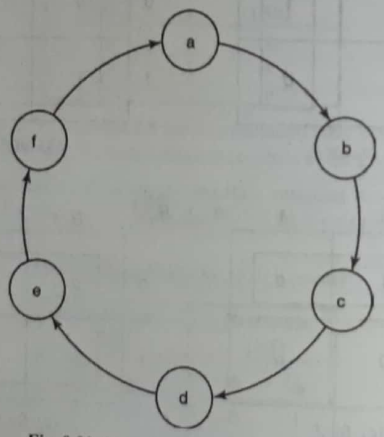

Fig. 8.20 State diagram of MOD-6 counter

Step 2 State table From the above state diagram, one can draw PS–NS table as shown in Table 8.11.

Table 8.11 PS–NS table for MOD-6 counter

Present state (PS)	Next state (NS)
a	*b*
b	*c*
c	*d*
d	*e*
e	*f*
f	*a*

The above state table does not have any redundant state because no two states are equivalent. So, there is no modification in the above state table.

Step 3 State assignment Let us assign three state variables to states *a, b, c, d, e* and *f* as follows: $a = 000, b = 001, c = 010, d = 011, e = 100$ and $f = 101$. Then, the PS–NS table gets modified as shown in Table 8.12.

Table 8.12 PS–NS table for MOD-6 counter

Present state (PS)			Next state (NS)		
q_2	q_1	q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	0
.....			.....		
1	1	0	*d*	*d*	*d*
1	1	1	*d*	*d*	*d*

Step 4 Excitation table The *JK* flip-flop is selected for the counter design because it results in a simplified circuit. The excitation table having entries for flip-flop inputs (J_2K_2, J_1K_1 and J_0K_0) can be drawn from the above PS–NS table and using the application table of *JK* flip-flop given earlier. Table 8.13 gives the excitation values of MOD-6 counter.

Table 8.13 Excitation table for MOD-6 counter

PS			NS			Excitation inputs					
q_2	q_1	q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	*d*	0	*d*	1	*d*
0	0	1	0	1	0	0	*d*	1	*d*	*d*	1
0	1	0	0	1	1	0	*d*	*d*	0	1	*d*
0	1	1	1	0	0	1	*d*	*d*	1	*d*	1
1	0	0	1	0	1	*d*	0	0	*d*	1	*d*
1	0	1	0	0	0	*d*	1	0	*d*	*d*	1
.....			.....			.....					
1	1	0	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	1	1	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*

Step 5 Excitation maps The excitation maps for J_2, K_2, J_1, K_1, J_0 and K_0 inputs of the counter can be drawn as shown in Fig. 8.21 from the excitation table (Table 8.13).

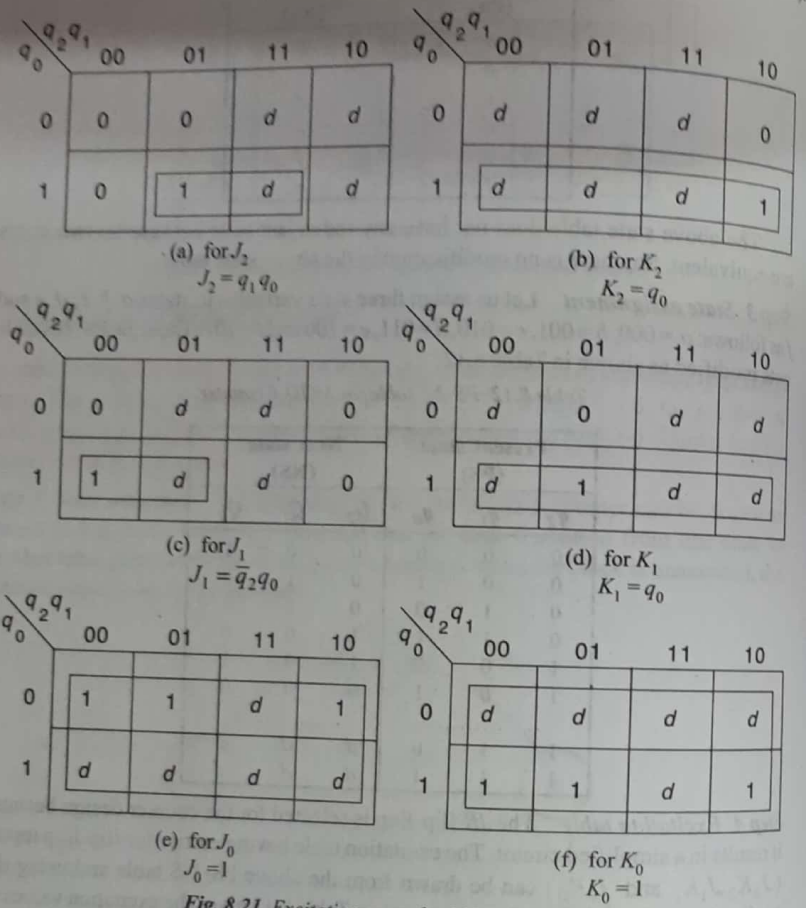

Fig. 8.21 Excitation maps for MOD-6 counter

Step 6 Schematic diagram Using the above excitation equations, the circuit diagram for the MOD-6 counter can be drawn as shown in Fig. 8.22.

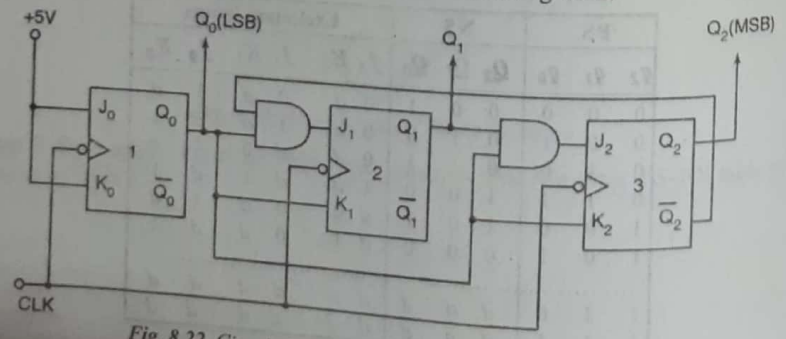

Fig. 8.22 Circuit diagram for MOD-6 synchronous counter

8.15.3 Design of BCD or Decade (MOD-10) Counter

To design a BCD or Decade (MOD-10) counter that has ten states i.e., 0 to 9 the number of flip-flops required is four. Let us assume that the MOD-10 counter has ten states, viz. *a, b, c, d, e, f, g, h, i* and *j*.

Step 1 State diagram Now the state diagram for the MOD-10 counter can be drawn as shown in Fig. 8.23. Here, it is assumed that the state transition from one state to another takes place when the clock pulse is asserted. When the clock is unasserted, the counter remains in the present state.

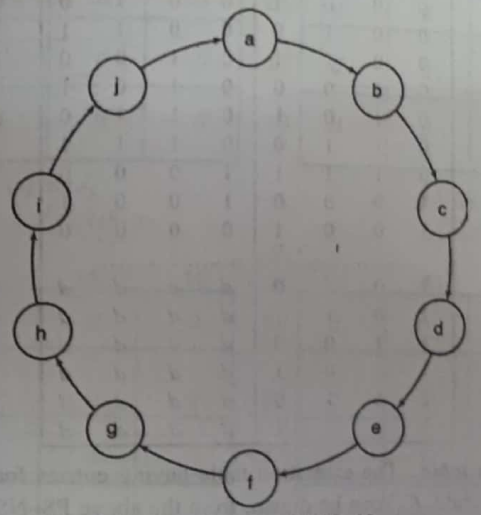

Fig. 8.23 State diagram of MOD-10 counter

Step 2 State table From the above state diagram, one can draw the PS-NS table as shown in Table 8.14.

Table 8.14 PS-NS table for MOD-10 counter

Present state (PS)	Next state (NS)
a	*b*
b	*c*
c	*d*
d	*e*
e	*f*
f	*g*
g	*h*
h	*i*
i	*j*
j	*a*

The above state table does not have any redundant state because no two states are equivalent. So, there is no modification required in the above state table.

Step 3 State assignment Let us assign four state variables to these states *a, b, c, d, e, f, g, h, i* and *j* as follows: $a = 0000, b = 0001, c = 0010, d = 0011, e = 0100, f = 0101, g = $

0110, $h = 0111$, $i = 1000$ and $j = 1001$. Then, the above PS–NS table can be modified as shown in Table 8.15.

Table 8.15 PS–NS table for MOD-10 counter

Present state (PS)				Next state (NS)			
q_3	q_2	q_1	q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0
.....				.....			
1	0	1	0	*d*	*d*	*d*	*d*
1	0	1	1	*d*	*d*	*d*	*d*
1	1	0	0	*d*	*d*	*d*	*d*
1	1	0	1	*d*	*d*	*d*	*d*
1	1	1	0	*d*	*d*	*d*	*d*
1	1	1	1	*d*	*d*	*d*	*d*

Step 4 Excitation table The excitation table having entries for flip-flop inputs (J_3K_3, J_2K_2, J_1K_1 and J_0K_0) can be drawn, from the above PS–NS table using the application table of *JK* flip-flop given earlier, as shown in Table 8.16.

Table 8.16 Excitation table for MOD-10 counter

PS				NS				Excitation inputs							
q_3	q_2	q_1	q_0	Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	0	1	0	*d*	0	*d*	0	*d*	1	*d*
0	0	0	1	0	0	1	0	0	*d*	0	*d*	1	*d*	*d*	1
0	0	1	0	0	0	1	1	0	*d*	0	*d*	*d*	0	1	*d*
0	0	1	1	0	1	0	0	0	*d*	1	*d*	*d*	1	*d*	1
0	1	0	0	0	1	0	1	0	*d*	*d*	0	0	*d*	1	*d*
0	1	0	1	0	1	1	0	0	*d*	*d*	0	1	*d*	*d*	1
0	1	1	0	0	1	1	1	0	*d*	*d*	0	*d*	0	1	*d*
0	1	1	1	1	0	0	0	1	*d*	*d*	1	*d*	1	*d*	1
1	0	0	0	1	0	0	1	*d*	0	0	*d*	0	*d*	1	*d*
1	0	0	1	0	0	0	0	*d*	1	0	*d*	0	*d*	*d*	1
.....				.....				.....							
1	0	1	0	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	0	1	1	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	1	0	0	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	1	0	1	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	1	1	0	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*
1	1	1	1	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*	*d*

Step 5 Excitation maps The excitation maps for $J_3, K_3, J_2, K_2, J_1, K_1, J_0$ and K_0 inputs of the counter can be drawn as shown in Fig.8.24 from the Excitation Table 8.16.

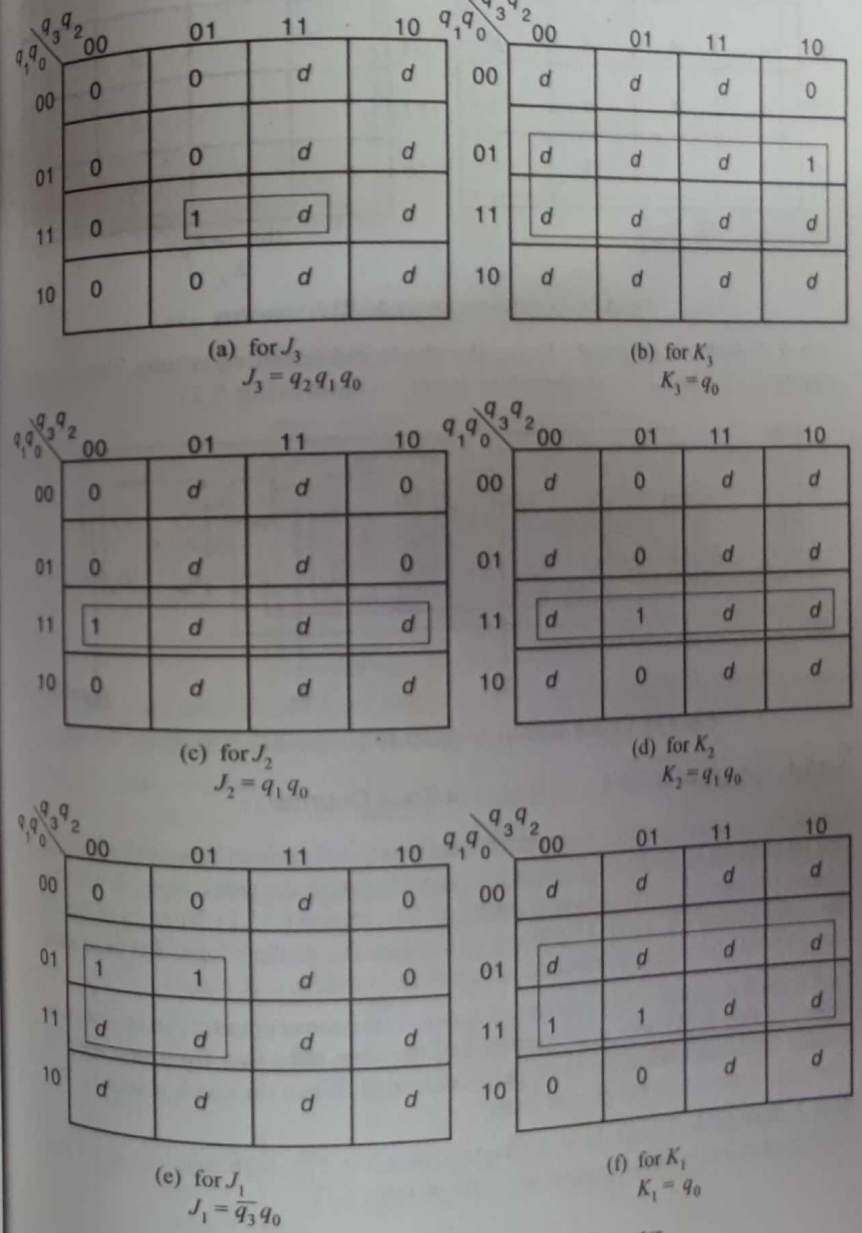

Fig. 8.24 *Excitation maps for MOD-10 counter*

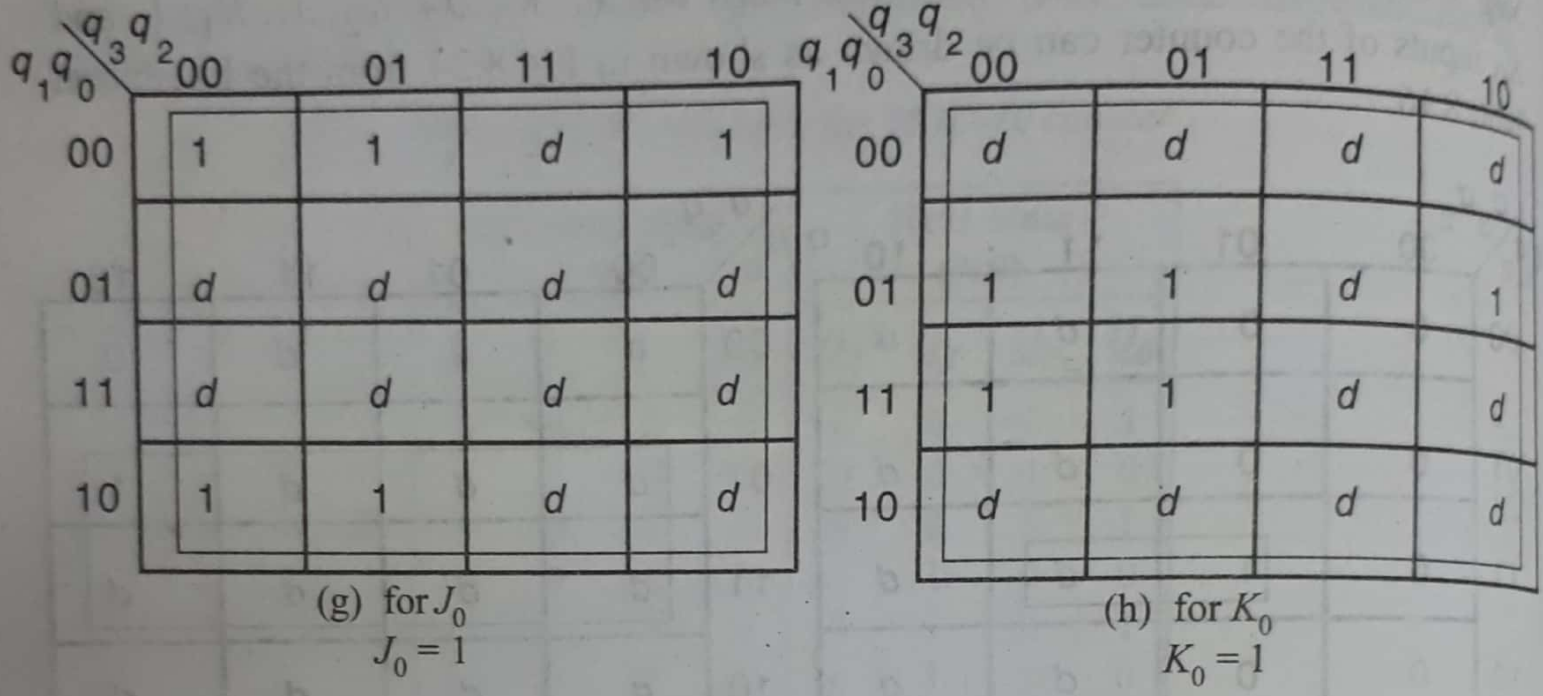

Fig. 8.24 *Excitation maps for MOD-10 counter*

Step 6 Schematic diagram Using the above excitation equations, the circuit diagram for the MOD-10 counter can be drawn as shown in Fig. 8.25.

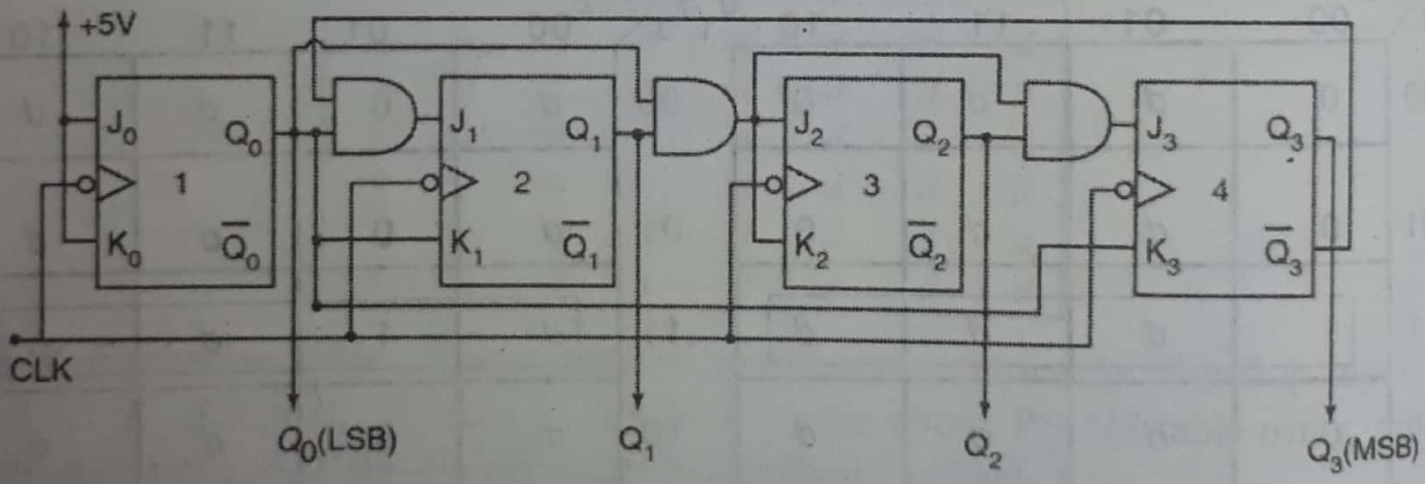

Fig. 8.25 *Circuit diagram for MOD-10 synchronous counter*