Page No.
Date

College Name :

DELHI GLOBAL INSTITUTE OF TECHNOLOG

Name : BAZGHA RAZI

Course Code : PCC-CSE-205G

Subject : Digital Electronics

Session : 2019-2023

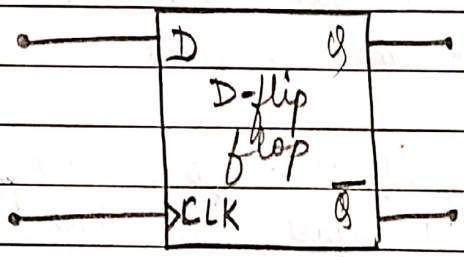
Page No.
Date

Ans 1a) In SR NAND gate circuit, the undefined input condition of set and reset is forbidden. It is the drawback of SR flip flop. To overcome this drawback an inverter is needed. Connect inverter between the set and reset inputs for producing another flip flop circuit called D flip flop.

The input data appears at the output at the end of the clock pulse. Thus the transfer of data from the input to the output is delayed and hence it is known as D (delay) flip flop.

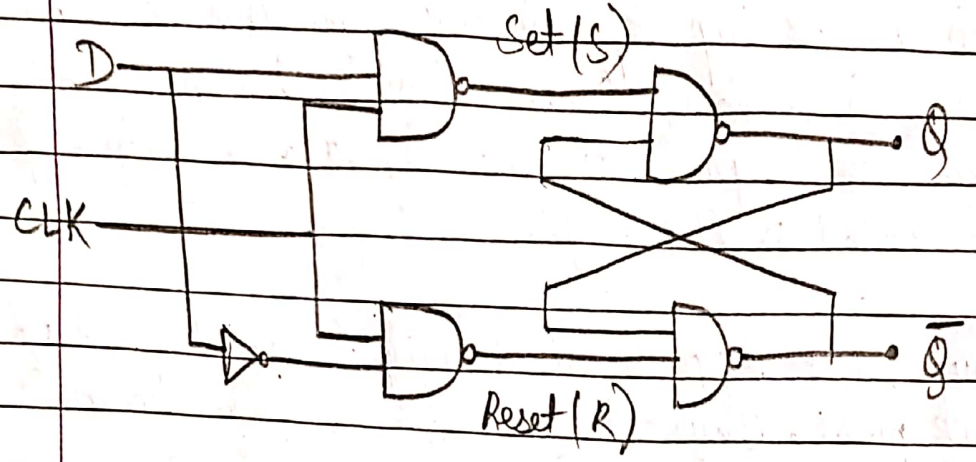
This flip flop ensures that at the same time, both the inputs are never equal to 1 i.e., (S=R≠1).

Block Diagram of D flip flop.



Page No.
Date

Circuit Diagram of D flip flop



SR flip flop requires two inputs. By using an inverter, we can set and reset the outputs with only one input. So, the two input signal complement each other.

In D flip flop, if D is set to 1, the flip flop would be set and when it is set to 0 the flip-flop become reset.

The CLK (clock signal) is used to avoid this for isolating the data input from the flip flop's latching circuitry.

Page No.
Date

Truth table for D flip flop

CLK	Input (D)	Output (Q_{n+1})
1	0	0
1	1	1
0	X.	(No change)

When the CLK is set to 1, then the Output (i.e., Q_{n+1}) is same as input D.

When the CLK is set to 0, then there is no change in the output.

Page No.
Date

Ans 1 b)

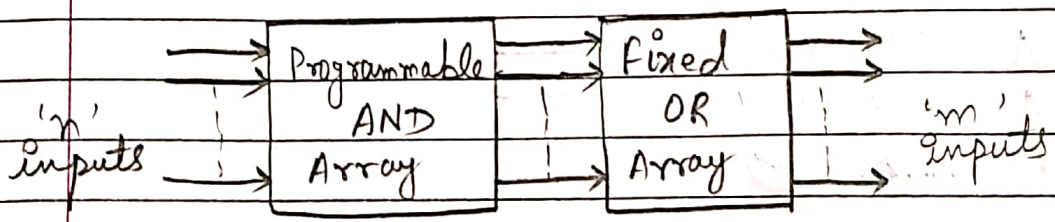
Latches	Flip Flops
• Latches are building blocks of sequential circuits and these can be built from logic gates.	Flip-flops are also building blocks of sequential circuits. But these can be built from the latches.
• Work with only binary inputs.	Work with binary inputs as well as the clock signal.
• It can not be used as a register.	It can be used as a register.
• Latch continously checks its inputs and changes its output correspondingly.	Flip-flop continously checks its inputs and changes its output corresponding only at times determined by clocking signal.
• It is level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is edge triggered, it means that the output and the next state input changes when there is a change in clockpulse whether it may a +ve or -ve clock pulse.
• The latch is sensitive to the duration of the pulse and can send or recieve the data when the switch is on.	Flip-flop is sensitive to a single change. They can transfer data only at the singal instant and data can't be changed until next signal change.

Page No.
Date

Ans 2b) Programmable Array Logic

PLD (Programmable logic device) are the components which don't have specific function with them. User can perform certain function on their need.
So, PAL (Programmable Array Logic) is the type of PLD.

PAL (Programmable Array Logic) is a programmable logic device that has programmable AND array and fixed OR array.
Block diagram of Programmable Array Logic:



Here, the inputs of AND gates are programmable. Each AND gate has both normal and complemented inputs of variables. So, according to our requirement, we can program any of those inputs. So, only the required product terms by using these AND gates are genetrated.

Now, the inputs of OR gates are not of programmable type. So, number of inputs to each OR gate will be of fixed type.

Page No.
Date

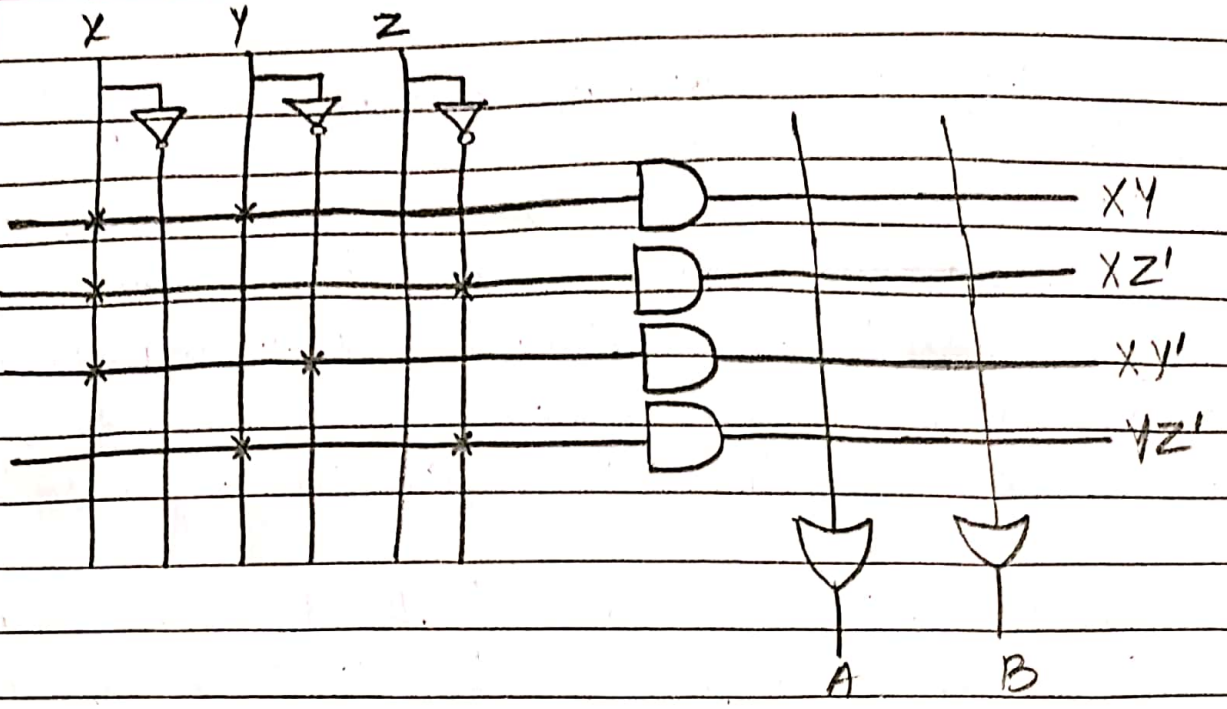
Hence, apply those required product terms to each OR gate as inputs. Therefore, the outputs of PAL will be in the form of sum of products form.
The advantage of PAL is that we can generate only the required product terms of Boolean function instead of generating all the min terms by using programmable AND gates.

Example:

Using PAL implement the following boolean functions.

$A = XY + XZ$
$A = XY' + YZ'$

The given functions are in sum of products form. There are two product terms present in each Boolean function. So, we require 4 programmable AND gates and two fixed OR gates for the above two function.



The programmable AND gates have the access of both normal and complemented inputs of variables. Inputs X, X'X', Y, Y'Y', Z and Z'Z' are available at the inputs of each AND gate. So program only the required literals in order to generate one product terms by each AND gate. The symbol x is used for programmable connections.

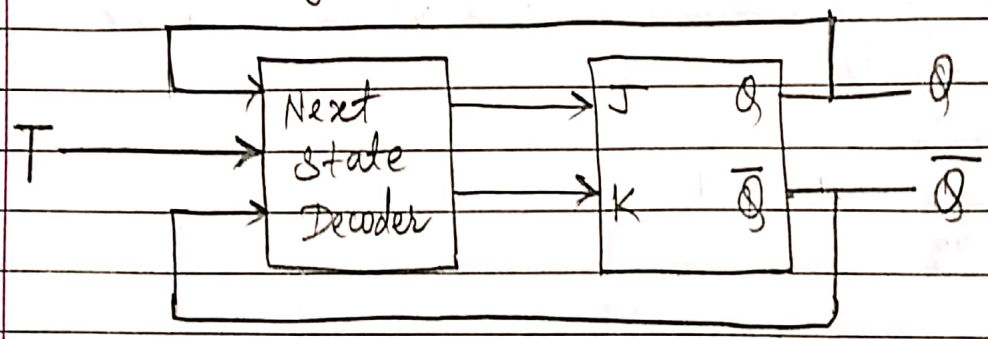
The inputs of OR gates are of fixed type. So, the necessary product terms are connected to inputs of each OR gate. So that the OR gates produce the respective boolean functions.

Page No.
Date

Ans 3a) Convert JK flip flop to T flip flop

Step 1: JK flip flop is basically a gated SR flip flop means a SR flip flop with added layer of feedback. This feedback enables one of the two set/reset inputs so they can't both carry an active signal to the multivibrator circuit.

Here the designed flip-flop is a T flip flop and the choosen one is a JK flip flop.
The block diagram is given below.



Step 2: Present State - Next State table for T flip flop

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Page No.
Date

Step3: Now, add excitation inputs in the present state-next state table i.e., inputs of JK flip flop.

T	Q_n	Q_{n+1}	Excitation inputs	
			J	K
0	0	0	0	d
0	1	1	d	0
1	0	1	1	d
1	1	0	d	1

Step4: Now using K-map, take simplified expressions for J and K. This k-map is called excitation map because it take value from excitation inputs.

Q_n \ T	0 ($\bar{T}$)	1 (T)
($\bar{Q}_n$) 0	0	1
(Q_n) 1	d	d

Excitation Map for J inputs

$\therefore J = T$

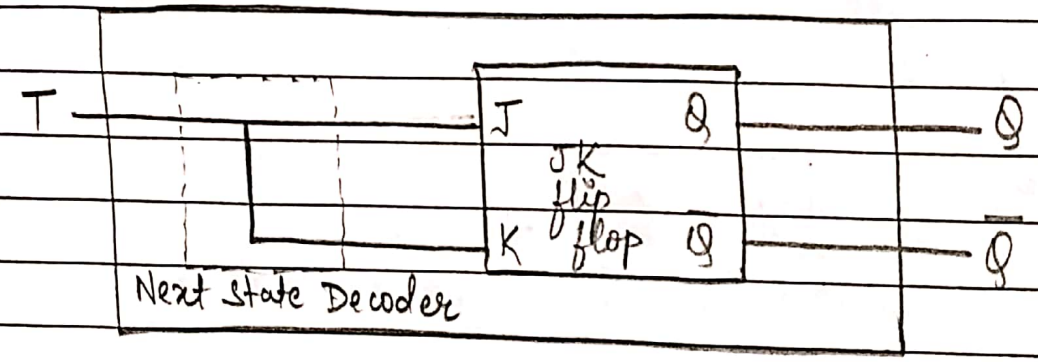
Date

Q_n \ T	0 ($\bar{T}$)	1 (T)
$\bar{Q}_n$ 0	d	d
Q_n 1	0	1

Excitation map for K inputs.

$\therefore K = T$

Step 5: Now, the circuit for T flip flop using JK flip flop when $J = T$ and $K = T$



$\Rightarrow$ T flip flop using JK flip flop