24/11/2021

8085 INTERRUPT

Hardware Interrupt

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Pins of 8085

↓

5 pins dedicated for 5 h/w interrupt.

- TRAP
- RST 7.5
- RST 6.5
- RST 5.5
- INTR

VECTOR ADDRESS

↓

Address predefined using internal ckt of µp

Software Interrupt.

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Invoked using instruction

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RESTART INSTRUCTION

↓

8 restart.

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RST 0
RST 1
RST 2
RST 3
RST 4
RST 5
RST 6
RST 7

Vectored Interrupt of 8085 with their vector address.

Hardware Vectored Interrupts.

TRAP → 0024H.

RST 7.5 → 003CH

RST 6.5 → 0034H

RST 5.5 → 002CH.

Software vectored Interrupts.

RST 0 → 0000H.

RST 1 → 0008H

RST 2 → 0010H

RST 3 → 0018H

RST 4 → 0020H

RST 5 → 0028H

RST 6 → 0030H

RST 7 → 0038H.

INTR → is a NON-VECTORED INTERRUPT.

↳ How the address for its ISR is determined?.

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Address of INTR is determined using external circuit.

MASKABLE INTERRUPT.

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RST 7.5 ; RST 6.5

RST 5.5 ; INTR

NON MASKABLE INTERRUPT.

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TRAP

EI → Enable. Interrupt.

DI → Disable Interrupt.

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OVERALL INTERRUPT.

If EI is given.

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Interrupt facility is enabled.

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TRAP is non-maskable.

BUT the remaining.

RST 7.5 RST 6.5

RST 5.5 INTR.

Can be masked individually

SIM → Set interrupt mask.

↳ use this to mask individual interrupts.

Interrupt type.	Trigger type	Priority	Maskable	Vector address.
TRAP	Edge/Level	1st (H)	NO	0024H
RST 7.5	Edge	2nd	Yes	003CH
RST 6.5	Level	3rd	Yes	0034H
RST 5.5	Level	4th	Yes	002CH
INTR	Level	5th (L)	Yes	Generate externally