



# MAHARSHI DAYANAND UNIVERSITY, ROHTAK

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Ans 1) Binary Number has only two digits 0 and 1. Hence its base is 2.

The maximum value of a single digit is 1. Each position of digit represents a specific power of the base 2.

This number system is used in computer.

Example of binary numbers :  $(11001)_2$

Uses of binary numbers

It is used for representing binary quantities which can be represented by any device that has only two operating states.

It is used in switches.

It is used in computer system to store the data.

Ans 11)

## Multiplexers

- It is a combinational circuit that select one digital information from several sources and transmits the selected information on a single output line.

- It is known as data selector.

- It is a digital switch.

- It has several data input lines & a single output lines.

- It works on many to one operational principle.

- Symbol:



## Demultiplexers

- It is a logic circuit that receives information on a single input & transmits the same information over one of the several  $2^m$  output lines.

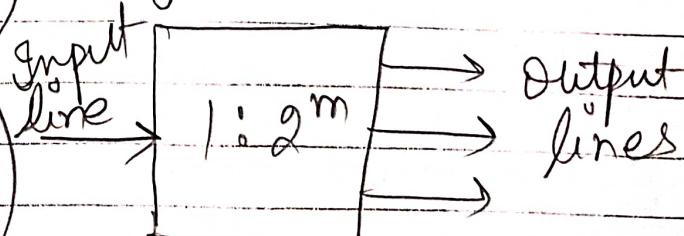
- It is known as data distributor.

- It is a digital circuit.

- It has single data input line &  $2^m$  output lines.

- It works on one to many operational principle.

- Symbol:

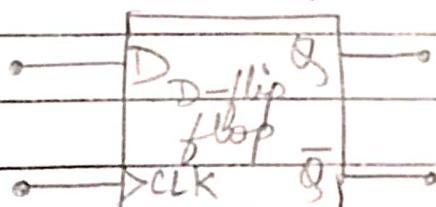


Ans(iii) D-flip flop

In SR NAND gate circuit, the undefined input condition of set & reset is forbidden. It is the drawback of SR flip flop. To overcome this drawback, an inverter is needed. Connect inverter b/w the set & reset inputs for producing another flip flop circuit called D-flip flop.

The input data appears at the output at the end of the clock pulse. Thus the transfer of data from the input to the output is delayed & hence it is also known as Delay flip flop.

## Block Diagram



## Truth table for D-flip flop

CLK	Input(D)	Output ( $S_{n+1}$ )
1	0	0
1	1	1
0	X	(No change)

When the CLK is set to 1, then output is same as input D.

When the CLK is set to 0, then there is no change in the output.

Ans 4) A/D converter.

Analog to digital converter converts the Analog signal to digital signal.

The input (analog) to this system can have any value in a range and are directly measured. But for output (digital) of N-bit A/D converter, it should have only  $2^N$  discrete values.

There are two steps involve in the process of conversion.

- i) Sample & Holding
- ii) Quantizing & Encoding.

Ans 5) CPLDs (Complex programmable logic devices)

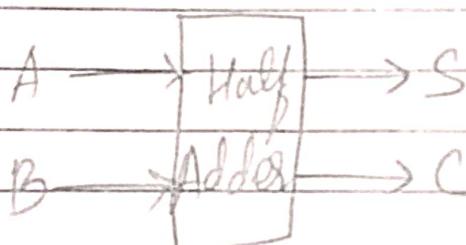
A CPLD is a logic device with completely programmable AND/OR arrays & macrocells. Macrocells are the main building blocks of a CPLD, which contain complex logic operations and logic for implementing algebraic normal form expressions. AND/OR arrays are completely reprogrammable & responsible for performing various logic functions.

Ans 1 vi) Half Adder

It is the simplest combinational circuit which performs the arithmetic addition of 2 binary digits is called half adder.

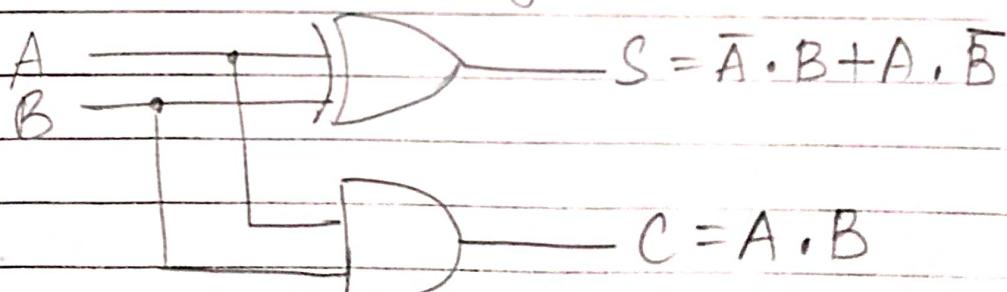
It has two inputs and two outputs. Inputs are 2 bits A & B, and outputs are sum (S) & carry (C).

Block Diagram      Truth Table.



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder using logic gates



Ans 3: Exclusive - OR gate also known as Ex-OR gate. This gate is a special type of gate used in different types of circuits. Ex-OR gate is not a basic gate. It is constructed by other logic gates.

Logic Symbol:



EX-OR gate

$$Y = (A \oplus B)$$

$$Y = (A'B + AB')$$

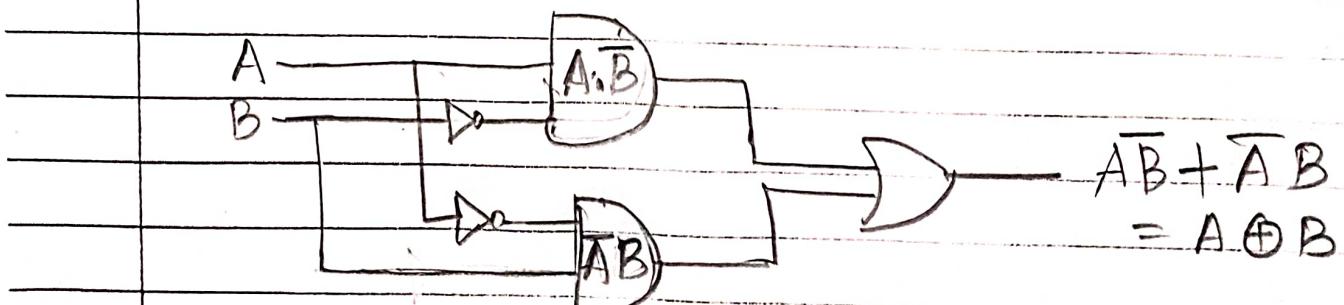
Truth table:

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

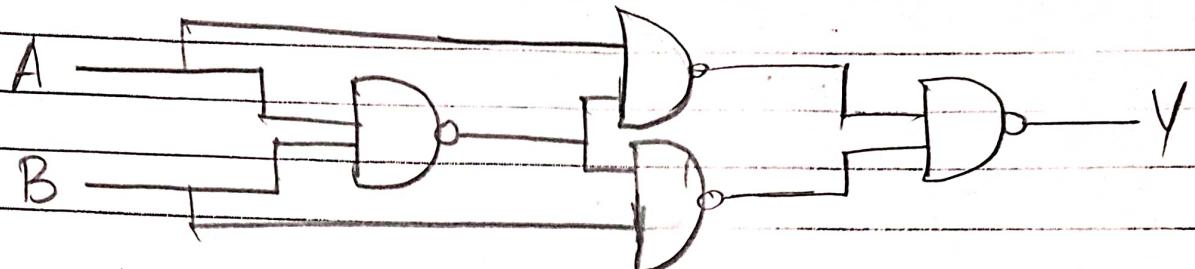
- When input A set to 0 & input B sets to 0 then the output is also zero.

- When input A set to zero & input B set to 1 then output should be 1.
  - When input A sets to 1 & Input B sets to 0 then output again comes one.
  - When both the input A & B set to 1 the output becomes 0.
- If any of the input is high then the output is also high.
- If both the input values are same then the output is ~~also~~ 0(zero).

### EX-OR gate construction using basic gates

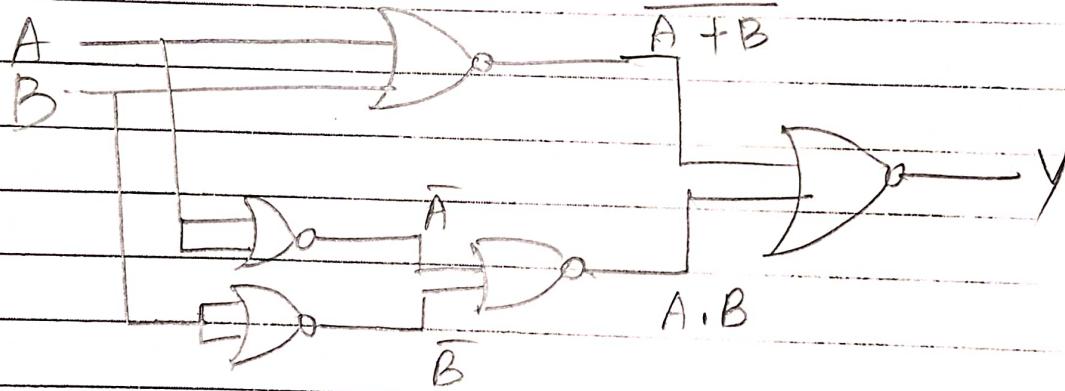


EX-OR gate using NAND gate



$$Y = \bar{A}B + A\bar{B} \Rightarrow Y = A \oplus B$$

EX-OR gate using NOR gate



$$Y = \bar{A}B + A\bar{B}$$

$$Y = A \oplus B$$

Boolean Algebra is used to analyze and simplify the digital circuits.

It uses only binary numbers i.e., 0 & 1.

It is also known as Binary Algebra.

### Rules in Boolean Algebra

- Variable used can have only 2 values.  
Binary 1 for high & 0 for low,
- Complement of a variable is represented by (-) or (').  
Example: Complement of A is  $\overline{A}$  or  $A'$
- OR of the variables is represented by (+) sign b/w them.  
Example:  $\overline{A} \text{ OR } \overline{B} = \overline{A} + \overline{B}$
- AND of the variable is represented by (.) sign b/w them.  
Example:  $\overline{A} \text{ and } \overline{B} = \overline{A} \cdot \overline{B}$

## Boolean Addition

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 1$$

It is same as the logical OR operation

## Boolean Multiplication

$$0 \cdot 0 = 0$$

$$0 \cdot 1 = 0$$

$$1 \cdot 0 = 0$$

$$1 \cdot 1 = 1$$

It is same as the logical AND operation.

## Properties of Boolean Algebra.

- Commutative property : It states that the interchanging of the order of operands in a boolean algebra/equation does not change its result

$$[A + B = B + A] \quad \text{and} \quad [A \cdot B = B \cdot A]$$

- Associative Property :

$$A + (B + C) = (A + B) + C$$

$$A \cdot (B \cdot C) = (A \cdot B) \cdot C$$

- Distributive property

$$A + BC = (A + B)(A + C)$$

$$A(B+C) = A \cdot B + A \cdot C$$

- Annulment law

$$A \cdot 0 = 0$$

$$A + 1 = 1$$

- Identity law :  $A \cdot 1 = A$

$$A + 0 = A$$

- Sidempotent law :  $A + A = A$

$$A \cdot A = A$$

- Complement law :  $A + A' = 1$

$$A \cdot A' = 0$$

- Double negation property :  $(\overline{\overline{A}}) = A$

- Census Law :  $AB + A'C + BC = AB + A'C$   
 $(A+B) + (A'+C)(B+C) = (A+B)(A+C)$

- De Morgan's Law :  $(A \cdot B)' = A' + B'$   
 $(A + B)' = A' \cdot B'$

4.

$$F(A, B, C, D) = \sum m(0, 2, 5, 7, 8, 10, 13, 15)$$

From the above function, we have given  
the minterms i.e.,  
 $\sum m(0, 2, 5, 7, 8, 10, 13, 15)$

Using the above terms, we construct  
a k-map:

		AB	$A\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
		CD	00	01	11	10
$\bar{C}\bar{D}$	00	1	0	4	12	8
	01		1	5	13	9
$C\bar{D}$	11		1	1	1	
	10	3	1	7	15	11
$C\bar{D}$	10		12	6	14	10

From the above k-map we can easily  
see that by using the minterms  
we form 2 quads.

First quad using  $\sum m(0, 2, 8, 10)$

Second quad using  $\sum m(5, 7, 13, 15)$

Now, from first quad  $\Sigma_m(0, 2, 8, 10)$   
we get,  $\bar{B}\bar{D}$

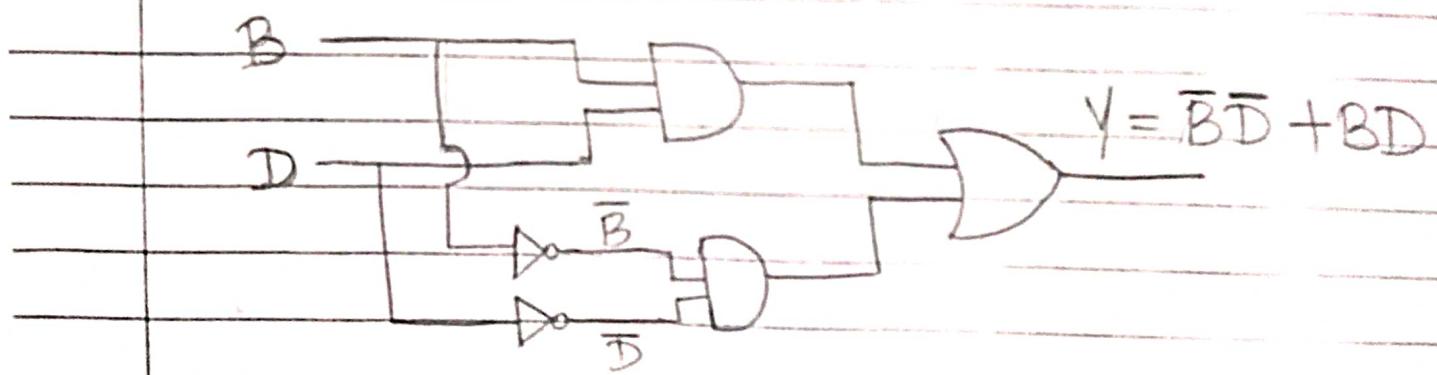
Now, from second quad  $\Sigma_m(5, 7, 13, 15)$   
we get,  $BD$

Now we ORed these terms so  
that we get the minimized expression:

$$Y = \bar{B}\bar{D} + BD$$

Here, Y is the Output

Now, using this simplified expression we  
design a circuit.

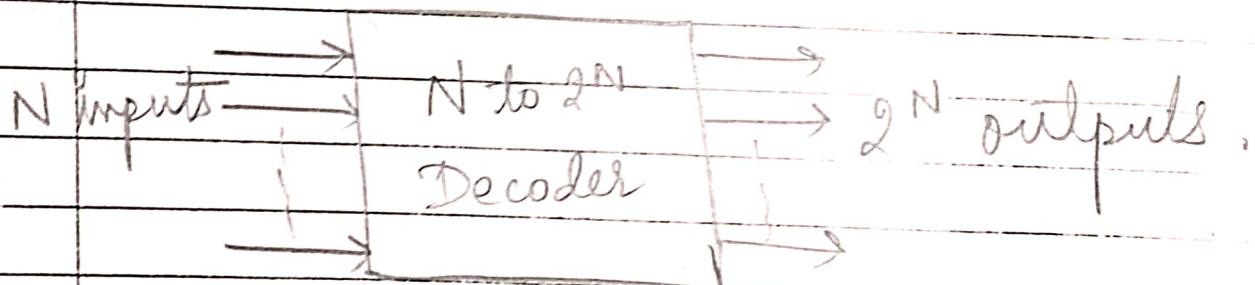


Here, we are using 2 AND gate, 2 NOT gate  
and one OR gate.

## Ans 5: Decoders

The combinational circuit that change the binary information into  $2^N$  output lines is known as Decoders. The binary information is passed in the form of  $N$  input lines. The output lines define the  $2^N$  bit code for the binary information. The Decoder perform the reverse operation of the encoders.

At a time, only one input line is activated for simplicity. The produced  $2^N$ -bit output code is equivalent to binary information.



A decoder is similar to demultiplexers but without any data input.

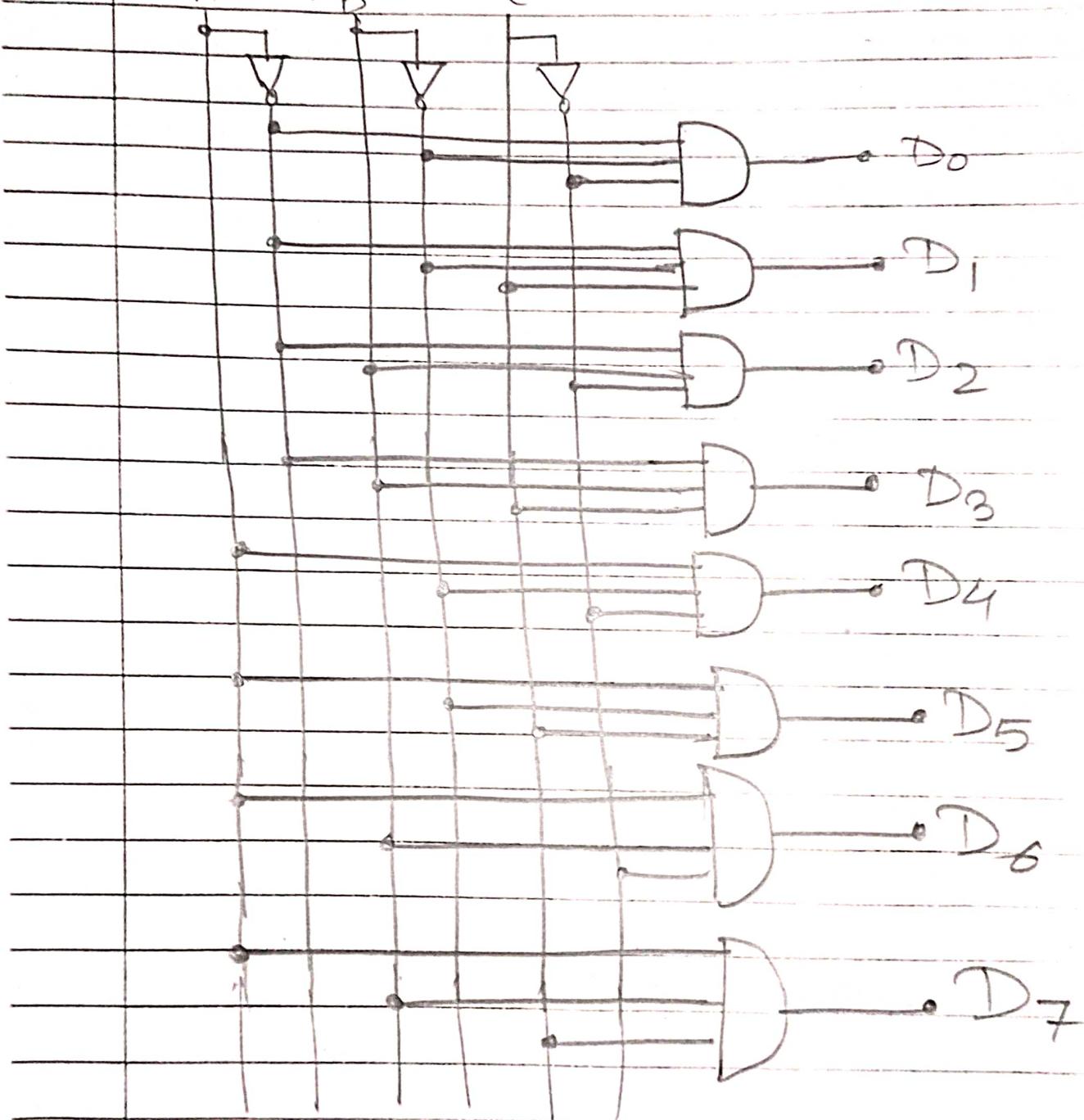
In decoder the no. of output is greater than the no. of inputs.

Example: 3 to 8 Decoder

A

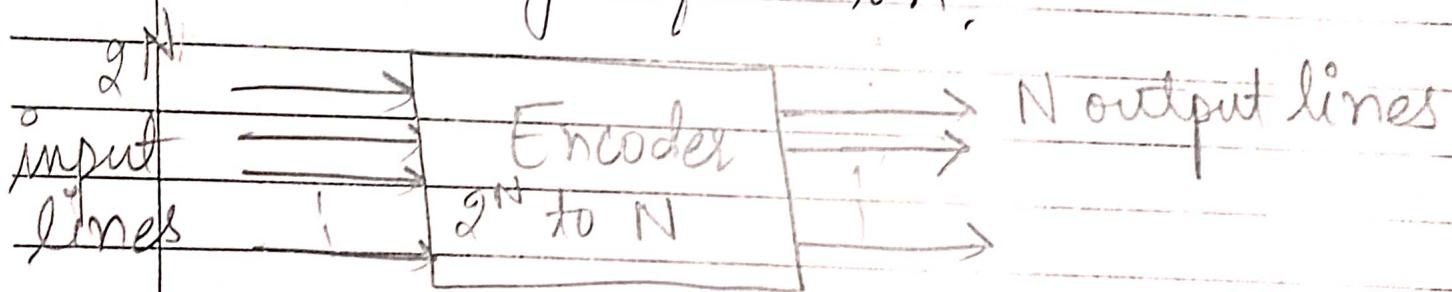
B

C



## Encoders

The combinational circuit that change the binary information to  $N$  output lines are known as Encoders. The binary info. is passed in the form of  $2^m$  input lines. The output lines define the  $N$ -bit code for the binary information. The Encoder performs the reverse operation of decoder. At a time, only one input line is activated for simplicity, the produced  $N$ -bit output code is equivalent to the binary information.



It is a combinational logic circuit that converts an active input signal into a coded ~~an~~ output signal.

In an encoder, the no. of output is less than the no. of inputs.

Example of Encoder:

$D_0$

$D_1$

$D_2$

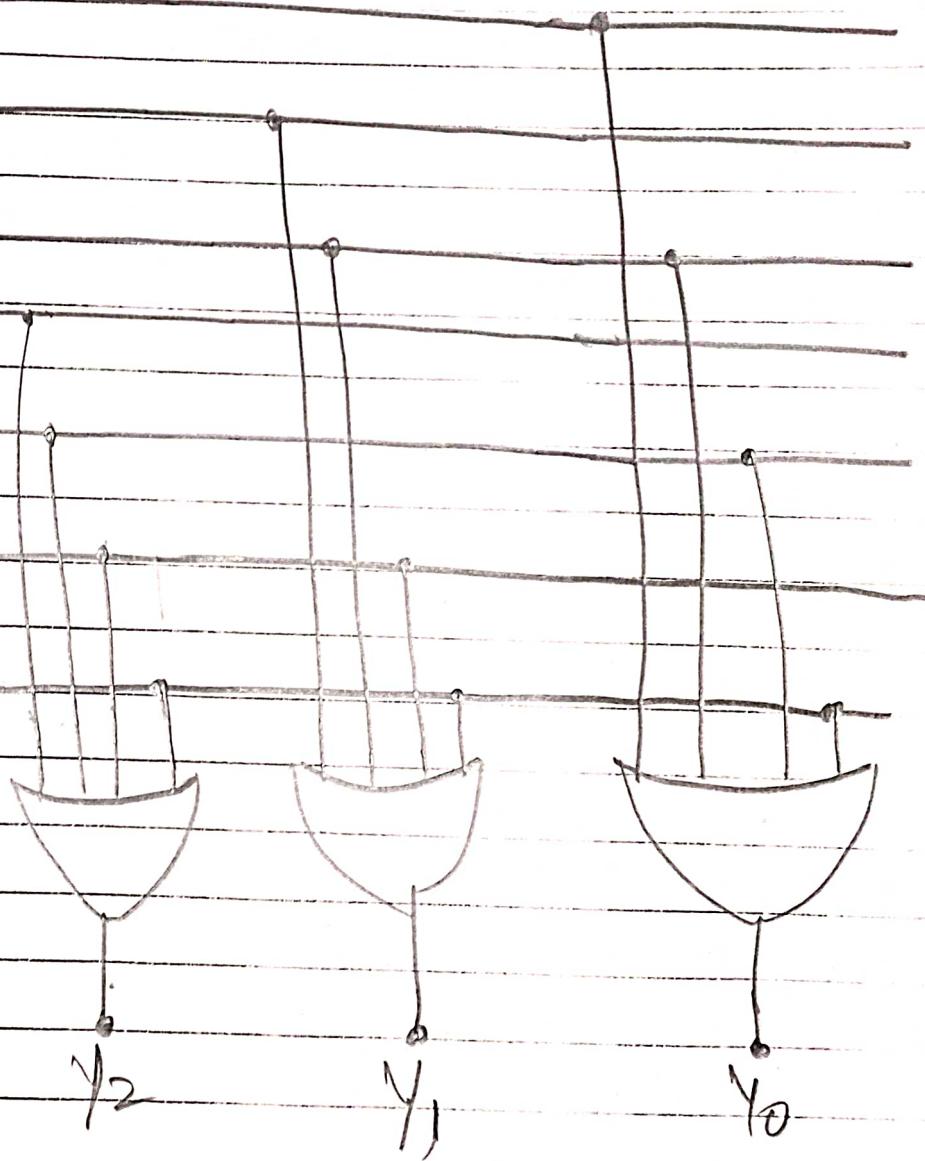
$D_3$

$D_4$

$D_5$

$D_6$

$D_7$



Octal to Binary  
Encoder.

### Ans 7a) RS flip-flop

RS and SR flip-flop are same.

So, SR flip flop having two inputs i.e., SET and RESET.

The SET input set the device, it produces output 1.

The RESET input reset the device, it produces output 0.

The RESET & SET inputs are denoted by R & S.

In SR flip-flop, the reset input is used to get back the flip flop to its original state from the current state with the output Q.

The output depends on the set and reset conditions, which is either at the logical level 0 or 1.

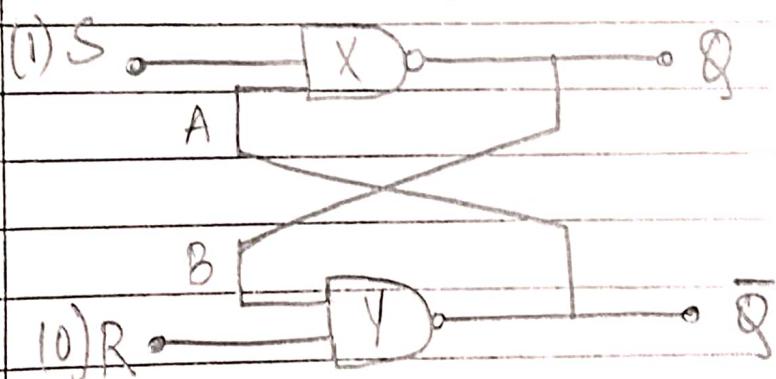
Block Diagram :



## NAND gate SR flip-flop

We can implement SR flip flop using OR by connecting 2 cross-coupled 2-input NAND gates together. In the SR flip flop circuit, from each output to one of the other NAND gate inputs, feedback is connected. So, the device has 2 inputs i.e., SET and RESET with two output  $Q$  &  $\bar{Q}$  respectively.

### Circuit - Diagram



### Truth - Table

State	S	R	Q	$Q'$	Description
Set	1	0	0	1	Set $Q' \gg 1$ No change
RESET	0	1	1	0	Reset $Q' \gg 0$ No change
Invalid	0	0	1	1	Invalid condition

## (Ans 7b) T flip-flop

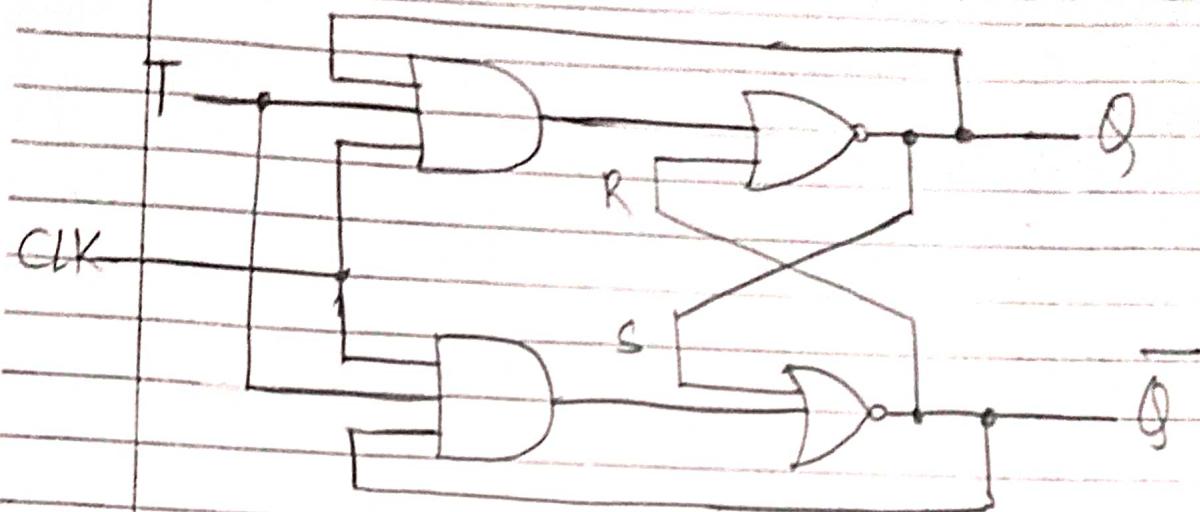
T flip-flop is also known as toggle flip-flop. This flip-flop works as a toggle switch whereas in SR flip flop, only a single input called toggle or trigger input is provided to avoid an intermediate state occurrence.

The next output state is changed with the complement of the present state output. This process is known as toggling.

T flip-flop has only one input, which is constructed by connecting the inputs of JK flip flop. Sometimes, the T flip flop is also known as single input JK flip flop.

### Construction of T flip flop using SR flip flop.

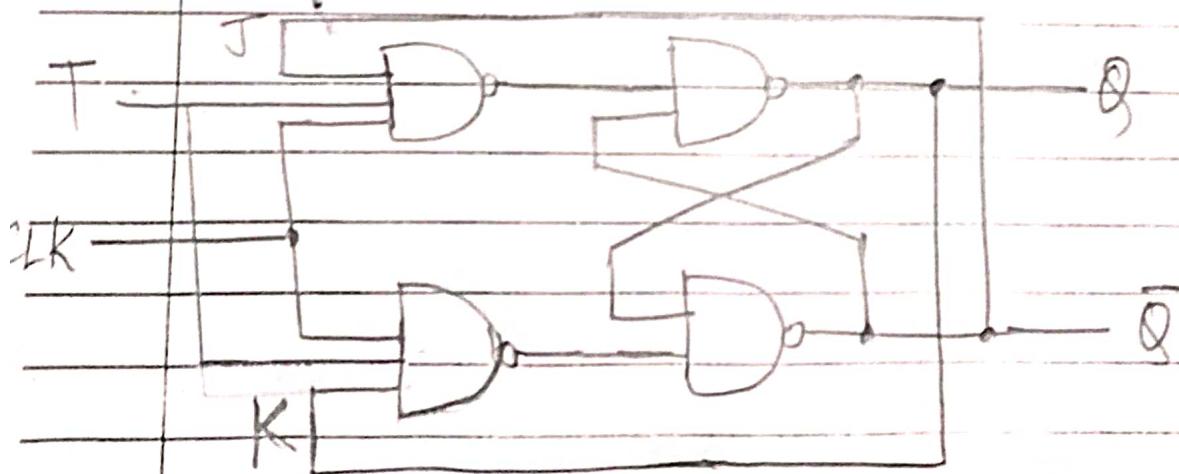
T flip flop is designed by passing the AND gates output as input to the NOR gate of SR flip flop. The inputs of the AND gates, the present output state  $Q$  &  $\bar{Q}$  are sent back to each AND gate. The toggle input is passed to the AND gates as input. These are connected to the CLK (i.e., clock signal).



→ T flip flop using SR flip flop

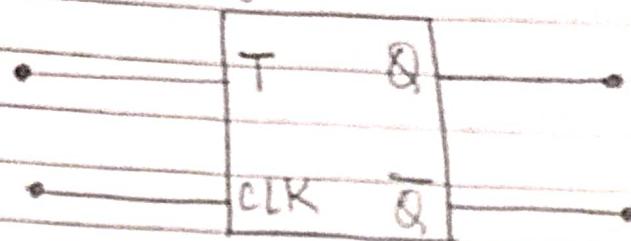
Construction of T-flip flop using JK flip flop

Both the inputs of the JK flip flop are connected to a single input T. It is the simplest construction of T-flip flop.

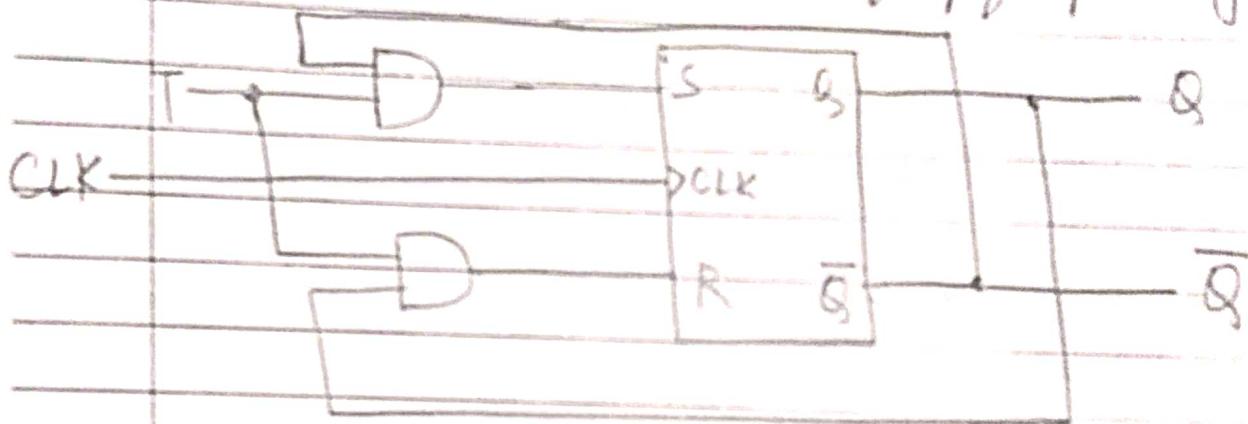


→ T flip flop using JK flip-flop.

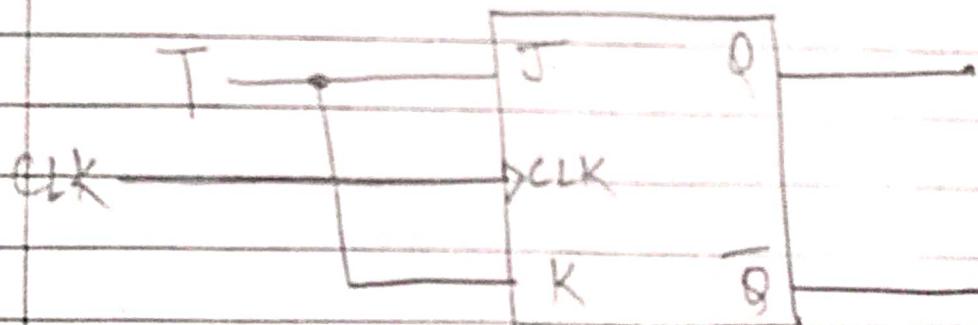
Block Diagram of T flip flop.



Block Diagram of T flip flop using SR flip flop.



Block Diagram of T flip flop using JK flip flop.



## Truth Table of T flip flop

T	Q	$Q_{n+1}$
0	0	0
0	1	1
1	0	1
1	1	0

When toggle (T) input set to 0.

- If T is set to 0 & Q is also 0, then next state ( $Q_{n+1}$ ) will be zero.
- If T is set to 0 & Q is set to 1, then  $Q_{n+1}$  will be 1.

When toggle (T) input set to 1.

- If T is set to 1 & Q is set to 0, then  $Q_{n+1}$  will be 1
- If T is set to 1 & Q is also 1, then  $Q_{n+1}$  will be 0.