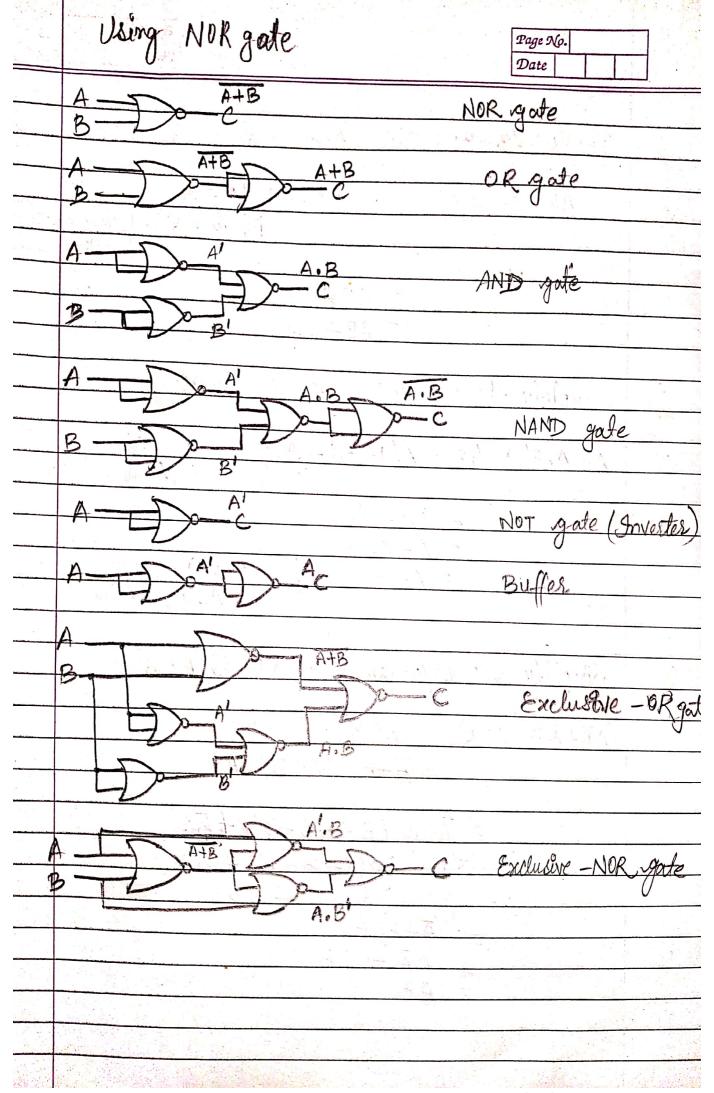
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	Collège Name:	
(o)	DELHI GLOBAL INSTITUTE	OF TECHNOLOGY
#	Name: BAZGHA RAZI	
	Course Code: PCC-CSE-2050	}
was in it.	Subject : Digital Electronics	
	Session: 2019 - 2023	4
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		r - The Property
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dns	a) Hand NAND and NOR are ralled universal gates. Because by using these gates we can implement any other gates.
	gates because by using these gates we can
	implement any other gates.
	To all his MAND gate we make
	For example by using NAND gate we make
ing 1	Y= A.B (NAND gale)
l I	
	A-Do-y= A (NOT gate) or Invertor
	Opportunities .
	A - Do A.B (AND gate)
	B-C
	$A - ID - (A \cdot B) = \overline{A} + \overline{B} = A + B$ (OR gate)
	B-DBT ATB
7 E	
<i>p</i> = 1	$A \rightarrow A \rightarrow$
	V-(AB+AB)=AAB
	PIDB (AB) / EXOR gate)
1.	ATTO
	B - V = A OB = A OB
	PEXNOR gate)
	EXNOR gate is the complemented form of EXOR gate.
	anto anto

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Ans 16	Combinational Circuits	Sequential Circuite
0	It is the circuits whose	1) It is the circuits whose
	output is determined by	output is defermined by
	the present values of its	the present values of the input
	input only.	the present values of the input as well as past values of the output.
7	It does not have a feedback path from output to input.	(2) It has a memory and a
	path from output to input.	(2) It has a memory and a feedback puth from output to input.
3	It does not have a clock signal.	
	Its action does not depend on	signal but must equal of
	It does not have a clock signal. Its action does not depend on clock transition.	3 It may or may not have clock signal but most sequential circuit have a clock signal.
<u> </u>	It's circuit is simpler than	(4) Its signiff is more
	that of segmential logic chariets.	Complex than that of
	arang.	combe national recruits
(3)	It is hill using bacic a to	
	It is built using basic gates i.e., NOT, AND, OR	and combinational riscuit
6	Example: Adder. subtractor	<u> </u>
	Example: Adder, subtractor, multiplexer, etc.	6 Example: Flip flops, counters, Shift regesters.
		myt regesters.

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			7:		7 -	4		da.		
On 2	e) De	Ma	4 9 a 1	is The	oum			- E		
	a) De Morgan's Theorem									
	It works on the principle of duality.									
	Duality states that inteschanging the operators									
	and hariables in a function, such as replacing									
	AND operator with O'R operator and OR operator									
	with	A	ND	operat	ol,	replo	wing	/ 0	with I and	الم
	1 m	ith_	0	•		1;	0	- /	• • • • • •	
	So,			tee th				:	· · · · · · · · · · · · · · · · · · ·	
			(1	1+B)	= A'.t	3'				
	**************************************			A.B)	= A'+	B'		,	- 1 - 1	49
				,			. 1	,		-
	Chou	The state of the s	not "	ABC	$=\overline{A}$	+B	+0			-
	• We	Description was	treu	th tak				An extend the last property of the		
	A	B	C	ABC	ABC	Ā	B	C	A+B+C	3
	0	0	0	0		•	1	1	1	
	0	0	1	0		1	1	0	1	
	0	1 :	0	0)	0		1	
	0	1		0	ľ	CHAPTE	0	0		
Marian y and a second of the s	1	0	0	0.	, , ,	0	a parties	11		<u> </u>
	1.	0	1	0		0	The state of the s	0	1	
		1	0	D		0	0	. 1	1.91	
ALE.			1-1-	1	0	0	0	0	0	
	0			·						
	Jo -	nom	-11	e ab	ove ta	ble	6			
	Colum	mn	0=	(AB	$\overline{c} =$	col	blm	n D	(A+B+C)	
	Hence, ABC = A+B+C									
4										
			1,832			4				
	是是由作事的。本									

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. '				

		- fin is						Dutt	
	Ne	w,	Sl	ron	that:	(A+B+C).	$D) = \overline{AE}$	3C +3	5
							,	. 11	11.1
y #	A	В	C	D	(A+B+C)	((A+B+C)D)	(A+B+C)D	ABC	T+58A
	0	0	0	0	0 .	140. 44	1	1	
	O	0	0	11	0	0	1 x x 1		#.
4-1	0	0		0	1	0		0	
1	, o	Đ.	1	3/3	W Y ; d	,-e, 199	0	0	10
	0	150%	0	Q	. 11 %	0	1 ATA 11	0	4)
	0	-1	O)	. 1	1 /	D	1 0 ,	0
	0	1	1	0	1	0	- \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0	
	0	1	1	1		to 1	0.	0	0
	1	0	0	D		18 -04	1 2 -1 1	0	
	1	0	υ	1	1		0	0	0
	1	D	1,	0	1	1 1 0	18 1: to	0	
	1	0	1		1	1 2	0	0	0
	1	1	0	0		D		0	.]
		1	0	,)	200	0	0	0
	1	1	1	0		Ð		0	1
	1	1	1	1			0	0	0
	-		1			The second secon			
	of the standard of the								had
	So, from the above table we can easily see that								
		. 0		10	(A LO LO)	J = colu	mm # 1 / 7	107-	47
	Folumn of $(\overline{A+B+C}D) = \text{column of } (\overline{A}\overline{B}\overline{C}+\overline{D})$								(1)
1									
	He	MC	11/4	h 1	12/2	ABC+D			r
t in			(4-	- K -	() () () ()	ABCTD			
2 2		1		4					
	4	1.2							
	4			100					
			£ .	-					
									<i>i</i> .
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dry 3. b)	F(A,B,C,D) = 5(0,1,2,3,6,7,9,13) + Ed(11,15)
K K	From the above function, we have given
	the mintures as well as don't care term
	$\sum_{m} = (0, 1, 2, 3, 6, 7, 9, 13)$
	$\sum_{k=1}^{\infty} \frac{1}{2} $
	Using the above torms, we construct a knowp
	, Ap
	00 01 11 10
	00 110 4 12 8
	1/ 1/3 1/7 0/15 0/1
The state of	10 13 1/6 14 10
	61 141 101
	From the above K-map we run easily see
	From the above K-map we san easily see that by using the minterms and clor't
	core termi use form 3 ands.
	First guad using = \(\int(0,1,2,3)\)
MA L	Second guard using = $5(2,3,6,7)$
	Third guad using = > (13,9)+ Zd = (11,15)
3	Now, from first quad we get,
	AB
	From second guard we get,
	AC '
	From third guad we get,
	AD
	None we OR ed these forms so that we get
	the minimized expression &

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	Y = AB + AC + AD	
	Here, Y is the output.	
	0 119 0 1011 1	
	Now using this simplified expression we	
	Now using this simplified expression we design a circuit.	
•	A NA AB	
1:	$y = A\bar{b} + \bar{A}C + AD$	
	B TO AC TO Y = ABTACTAD	
	AD	
		1.13
	Here we use using 2 NOT gate, 3-Nand Gate	
	and One 3-input OR gate.	
		7
		•
		10-15-14
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