28/10/2021

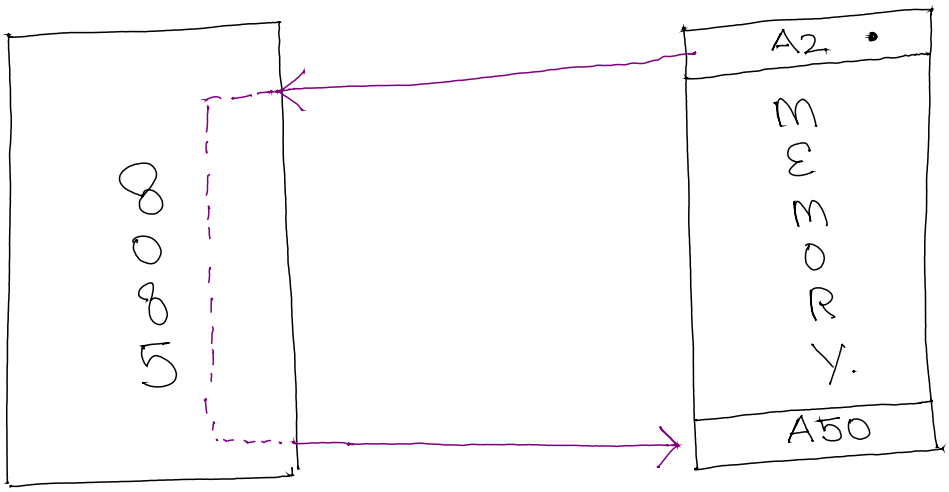
MICROPROCESSOR

DMA Signal :-

HOLD ; HLDA → Signal indicate μp that DMA wishes to use address and data line for data transfer.

DMA → Direct Memory Access

For example : For data transfer from one memory location to other memory location



Such transfer of data would be done through 8085 μp.

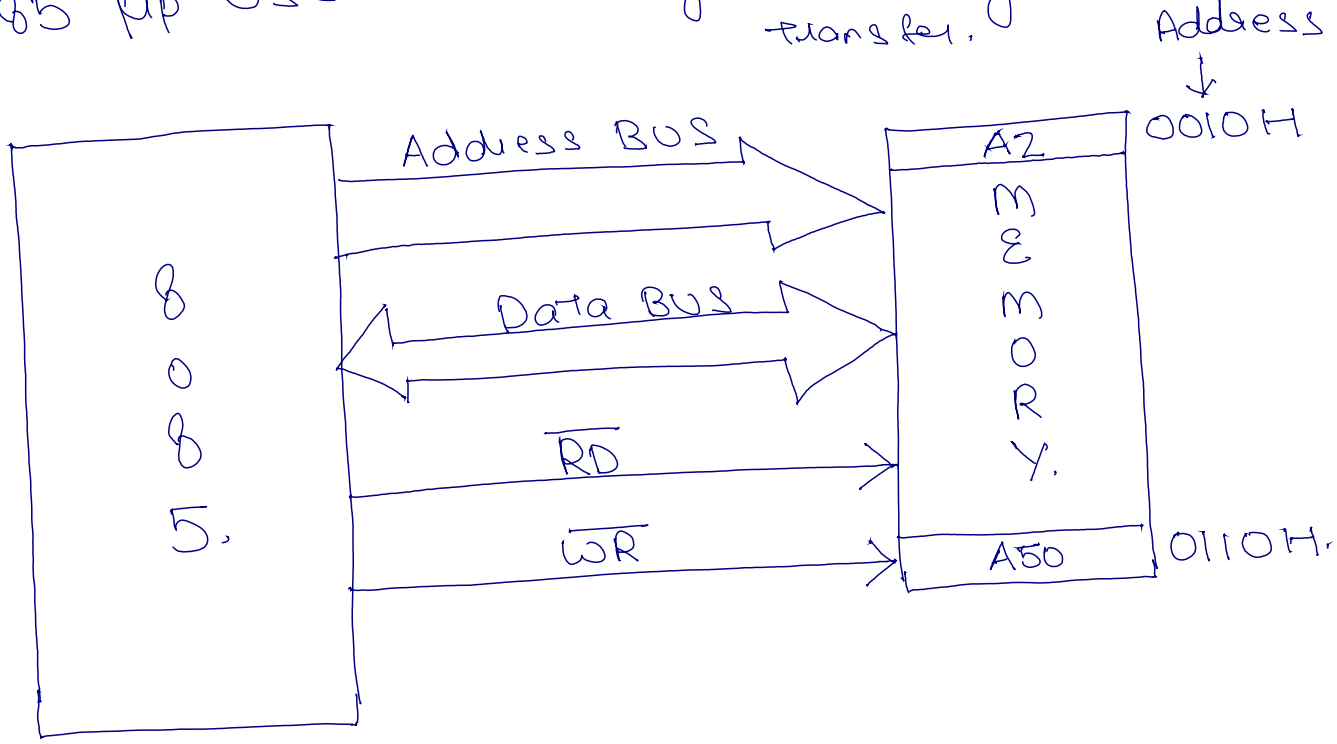
→ DMA is IC that can free μp from such data transfer.

→ How DMA is going to do this?

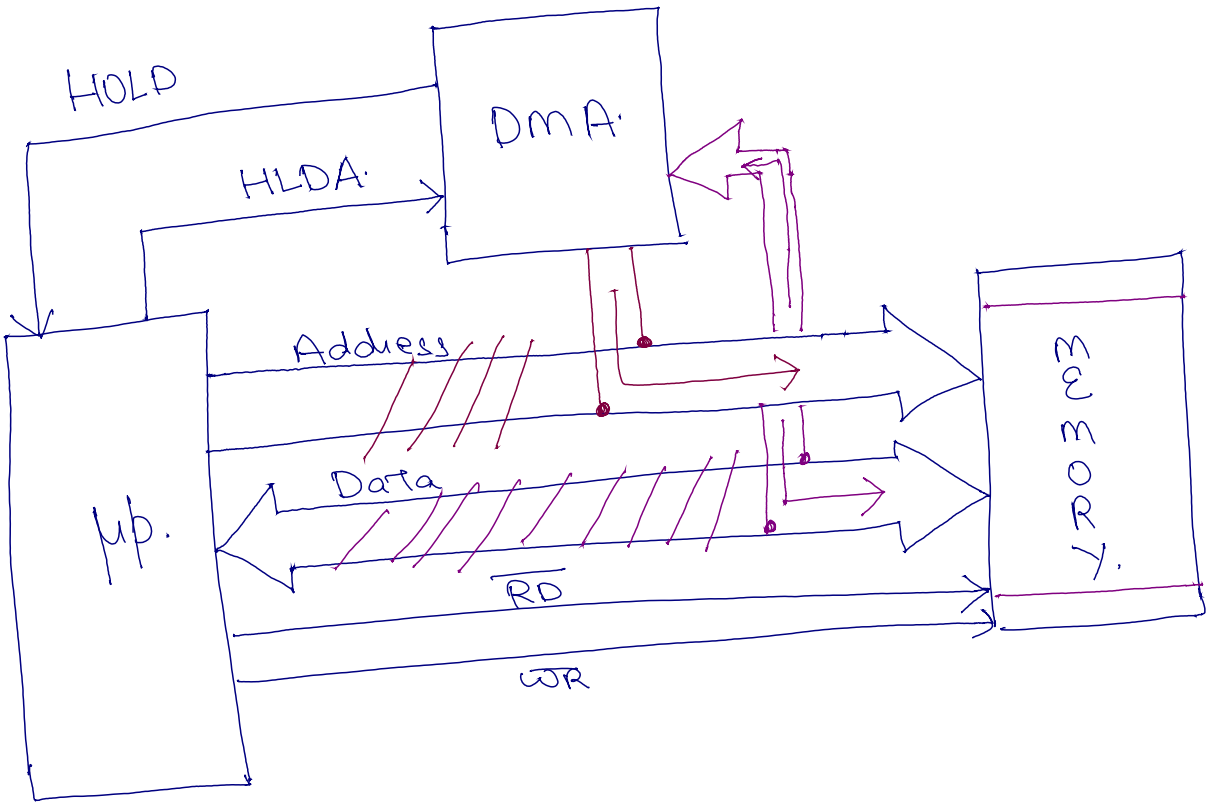
* DMA will use μp data and address lines.

After getting the request from DMA through HOLD signal for data and address bus, µp after finishing its current operation, will provide the control of its address and data bus to DMA by raising HLDA (Hold acknowledgement Signal).

8085 µp used for memory to memory data transfer.



① 8085 will send address 0010H to memory.
② 8085 will send $\overline{RD}$ signal.
③ memory will send the data A2 to µp using data bus.
④ 8085 will send address 0110H to memory.
⑤ 8085 will send $\overline{WR}$ signal ⑥ Data bus → m



Reset Signals

RESET IN → is used to reset the μp. On reset the value of PC register becomes 0000H. Also, the buses goes into tri-state (high impedance) Z (disconnected).

Active low

RESET OUT :- This is active high signal which indicates that the μp has been reset. Used to reset other device with μp.

Interrupt Signals :-

What is Interrupt in µp?.

↳ Due to certain condition, the normal processing of µp needs to be stopped to address the arised condition. This is refered as interrupt.

INTERRUPT CAN OCCUR IN TWO WAYS :-

① HARDWARE ② SOFTWARE

In 8085, Interrupt due to hardware :-

RST 5.5, RST 6.5, RST 7.5, INTR, TRAP

RST → Restart

TRAP → use in emergency power failure.

↓

highest priority

{ $\overline{INTA}$ = INTERRUPT ACKNOWLEGMEN. }

INSTRUCTION CYCLE :

The fetch, decode and execution of a single instruction is referred as one instruction cycle.