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MICROPROCESSORS

ADDRESSING MODES OF 8085

→ The different ways that a microprocessor can access data through an instruction is referred to as Addressing Modes.

→ The 8085 µp has 5 Addressing Modes :-

1. Immediate Addressing Mode
2. Register Addressing Mode
3. Direct Addressing Mode
4. Indirect Addressing Mode
5. Implied Addressing Mode

→ Immediate Addressing Mode : 8 or 16 bit data can be specified as a part of instruction. The instructions having 'I' letter fall under this category.

For Example :-

① MVI A, 24H

② LXI H, 2040H

③ ADI 24H

→ Register Addressing Mode : Source operand, destination operand or both are contained in 8085 internal register. The name of register is specified in the instruction.

For Example : ① MOV A, B ② ADD B

③ Direct Addressing Mode → Specifies 16 bit address of the operand which is stored in memory directly in the instruction.

For example : ① LDA 2000H
↓
16-bit address of memory from where data has to be copied to accumulator.

② LHLD 3000H
↓
16-bit address of memory.

④ Indirect Addressing Mode → The 16-bit memory address where the operand is stored is specified through contents of register pair.

For example : ① MOV A, M
↓
M means memory but the address of memory is indicated by HL register pair

② LDAX B
↓
BC register pair is indirectly specifying address of memory where operand is present.

(5) Implied Addressing Mode → NO operand is specified in the instruction. The operand on which operation has to be performed is hidden in the opcode itself.

For example : (1) CMA

↙ opcode is telling about data hence no operand needs to be specified.

↓ Complement of contents of accumulator.

(2) RAL (3) RLC (4) XCHG

Q Specify the addressing mode for each of the following 8085 instruction.

(i) SBB M → Indirect Addressing mode.

(ii) INR B → Register Addressing mode.

(iii) INX D → Register Addressing mode.

(iv) DAA → Implied Addressing mode.

(v) DAD D → Register Addressing mode.

BRANCHING INSTRUCTION → Control the sequence of execution of the program.

① Jump Instruction → Unconditional
→ Conditional.

→ Unconditional Jump Instruction: It goto the 16-bit address specified in instruction without any condition.

Syntax: JMP 16-bit address (LABEL).

for example: JMP 2000H.

2000H: MVI A, 00H. ← 2 byte instruction.
2002H: ADI 01H. ← 2 byte instruction.
2004H: JMP 2002H ← 3 byte instruction.
2007H: HLT

```
    MVI  A, 00H.
Repeat: ADI  01H.
    JMP  Repeat.
    HLT.
```

Repeat → LABEL given as memory address.