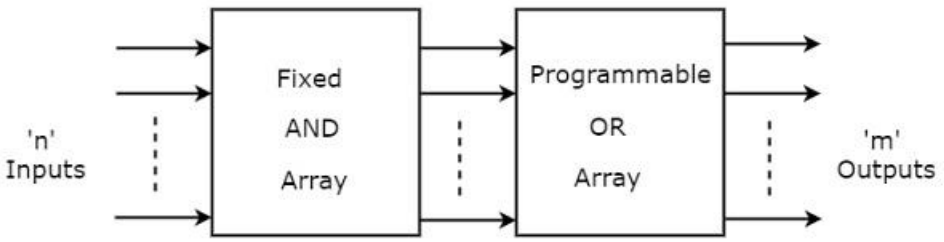
PLD(Programmable Logic Device)

A logic device is an electronic component which performs a definite function which is decided at the time of manufacture and will never change. For example, a not gate always inverts the logic level of the input signal and does/can-do-nothing else. On the other hand, Programmable Logic Devices (PLDs) are the components which do not have a specific function associated with them. These can be configured to perform a certain function by the user, on a need basis and can further be changed to perform some other function at the later point of time, i.e. these are re-configurable.

Programmable Read Only Memory PROM

Read Only Memory ROM is a memory device, which stores the binary information permanently. That means, we can't change that stored information by any means later. If the ROM has programmable feature, then it is called as Programmable ROM PROM. The user has the flexibility to program the binary information electrically once by using PROM programmer.

PROM is a programmable logic device that has fixed AND array & Programmable OR array. The block diagram of PROM is shown in the following figure:



Here, the inputs of AND gates are not of programmable type. So, we have to generate 2n product terms by using 2n AND gates having n inputs each. We can implement these product terms by using nx2n decoder. So, this decoder generates 'n' min terms.

Here, the inputs of OR gates are programmable. That means, we can program any number of required product terms, since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PROM will be in the form of sum of min terms.

Types of PLDs:

Programmable Logic Array (PLA)

This device comprises of programmable AND gate and OR gate arrays which are to be configured by the user to obtain the output.

Programmable Array Logic (PAL)

PALs use an OR gate array with fixed logic while an AND gate array which can be programmed as per the requirement of the user. As a result, these devices express the output as a combination of inputs in sum-of-products form.

Complex Programmable Logic Device (CPLD)

CPLDs are denser than PALs and comprise of a large number of programmable logical elements. The interconnection between these macro cells is to be established by the user through the interconnecting network. Here sum-of-product establishing logical elements are combined together to form structures in order to reduce the number of input-output (IO) pins. This facilitates the implementation of more complex logic design with slightly worse propagation time when compared to that of PALs. These offer predictable timing characteristics making them most suitable for critical control applications with high performance. CPLDs are preferred to implement combinational logic based designs.

Generic Logic Array (GLA)

These devices had their properties similar to those of PALs in addition to which they were electrically erasable and re-programmable. This important feature proved to be meritorious as it considerably eased the prototype design which in turn reduced the time to market.

Field Programmable Gate Array (FPGA)

These devices are capable of implementing state-machine based sequential designs along with the designs based on combinational logic. FPGAs are used to realize more complex designs when compared to CPLDs due to their high density. Moreover, FPGAs offer the customer the flexibility to design/re-design the logic even after being deployed in the work field which gives them the name field-programmable.

Examples of PLD applications

- Code converter, for instance from binary to gray code.
- BCD to 7 segment converters, supporting A-F letters.
- Quadrature decoders and counters.
- Parity checkers, checksums and error detection and correction.
- Different types of counters and registers.
- Memory and I/O controllers for microprocessors.
- Lookup tables.

Advantages of PLDs

1. Flexible, easy to implement.
2. Need less board space.
3. Lower power required.
4. Less costly for small quantities.
5. Higher reliability.

Disadvantaged of PLDs

6. Poor Performance.
7. Not flexible in terms of integrating analog blocks.
8. High cost for large quantities.