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Subject Name : Microprocessor

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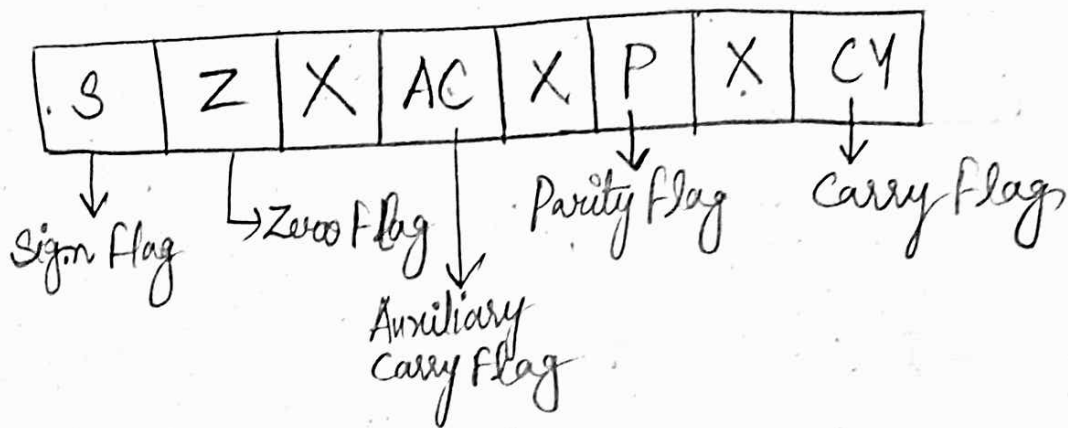
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Student Signature : Bazgha Razi

Date of Examination : 13/12/2021

Ans 1 i) Flag Register of 8085 Microprocessor

The ALU includes five flipflops, which are set or reset after an operation according to data conditions of the result in the accumulator and other register. There are five flags in 8085 microprocessor,



Bits marked with "X" means no flags are assigned for these bits.

Ans 1 ii) Register organisation of 8086 microprocessor

a) General purpose register : There are 8 general purpose register i.e.,
AH, AL, BH, BL, CH, CL,
DH and DL

These are used to store 8 bit data individually.

b) Flag register: There are 9 flag registers in 8086 microprocessor.

These are parity flag (PF), zero flag (ZF), sign flag (SF), carry flag (CF), auxiliary flag (AF), overflow flag (OF), Interrupt enable flag (IF), Direction flag (DF) and Trap flag (TF). Interrupt flag, direction flag, trap flag are also known as control flags.

c) Segment Register: There are 4 segment i.e., code segment, data segment, stack segment and extra segment.

d) Pointer and index register: Pointer register is associated with code segment.

Index register are used as offset indexed, base indexed and relative base index addressing modes.

AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL

General Purpose Register

CS
DS
ES
SS

Segment Registers

SP
BP
SI
DI
IP

Pointer Register and Index register

Ans 1v) Operand: It may include 8-bit or 16-bit data, an internal register, a memory location or an 8 bit or 16 bit address. In this the data to be operated.

Opcode: It is the one in which the task to be performed. It is also known as operation code.

In instruction MOV M, A :

Opcode: MOV

Operand: M, A

Ans 1iv) Difference b/w 8085 & 8086 microprocessor

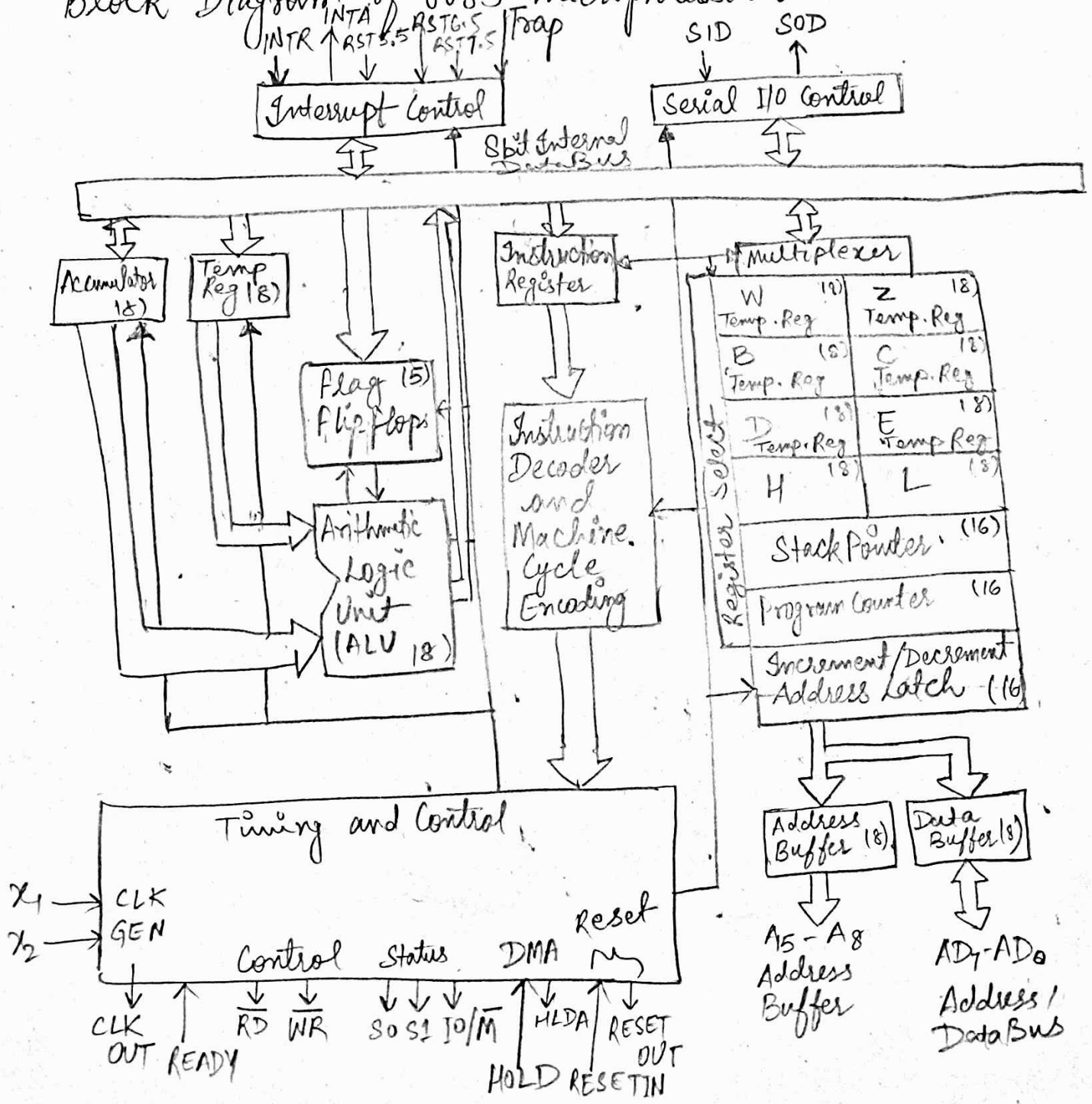
- 8085 is a 8bit microprocessor and 8086 is a 16 bit microprocessor.
- 8085 has 16-bit address line and 8086 has 20-bit address line.
- 8085 has 5 flag registers but in 8086, it has 9 flag registers.
- ~~8085~~ 8085 does not support pipelining but 8086 support pipelining.

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Ans 2b) 8085 microprocessor

Working: In memory instructions and data are stored, then from memory, microprocessor fetch instructions using address and data bus, decodes the instruction and then execute it.

Block Diagram of 8085 microprocessor:



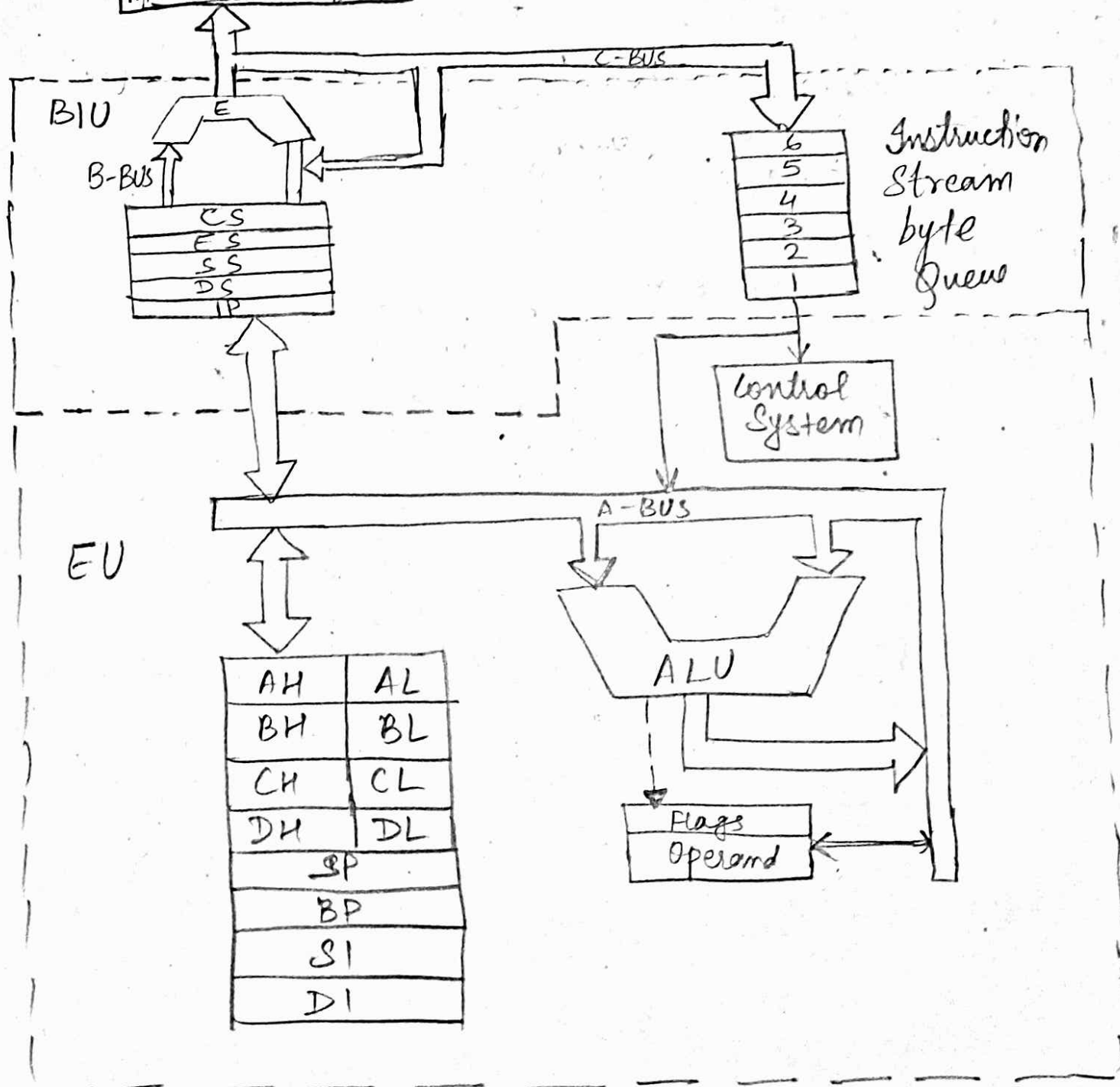
Block of 8085 microprocessors are described below:

- i) Accumulator: It is an 8-bit register that is part of ALU. It is used to store 8-bit data and to perform arithmetic and logical operations. The result of operation is stored in the accumulator. It is also known as A register.
- ii) Registers: There are six general purpose register to store 8-bit data. They are B, C, D, E, H and L registers.
- iii) Flags: It is combination of flip-flops. Based on result of ALU, flags indicate certain conditions. Some flags are zero (Z), carry (CY), sign (S), parity (P), Auxiliary carry (CY) flags. There are total five flag registers in 8085 μ p.
- iv) Instruction Decoder: After fetch instruction, instruction goes to instruction decoder.
- v) Program Counter (PC) and Stack Pointer (SP) are two 16-bit registers to hold the memory addresses. The size of these registers are 16-bit because the memory addresses are of 16 bits.

vi) Address Bus : Address bus used to carry address of memory. It is unidirectional and data bus is bidirectional.

Ans 3a) Architecture of 8086 microprocessor.

Memory Interface



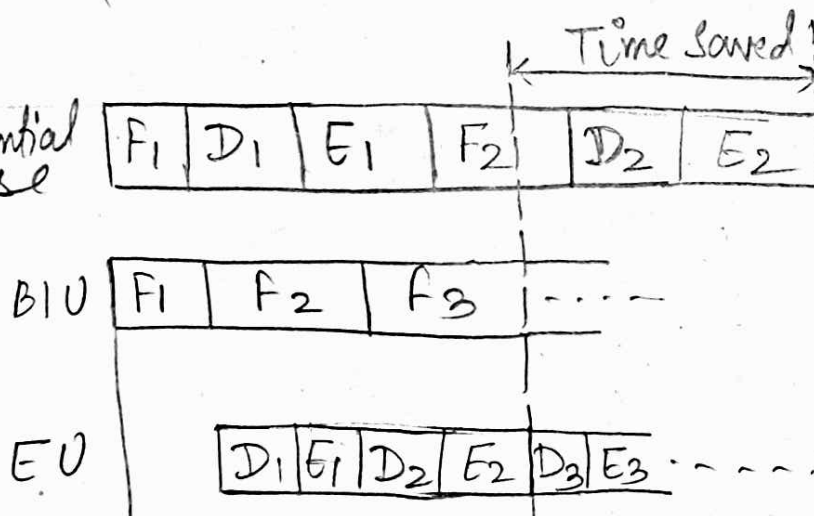
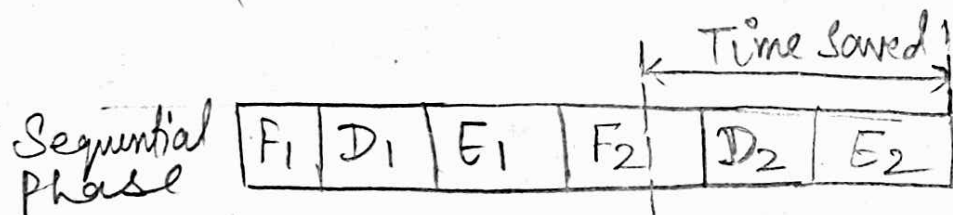
BIU: It is the 8086 interface to the outside world. It provides a full 16-bit bi-directional data bus and 20-bit address bus. It is responsible for performing all external bus operations. It is known as bus interface unit.

EU: Execution unit is EU. It tells the BIU from where to fetch instructions or data decoded instructions and executes instructions.

Pipelining in 8086 microprocessor

Pipelining: It is the process of fetching the next instruction when the current instruction is being executed. It helps us to save time.

← Time required for execution without Pipelining →



← Time Required for execution of two instructions because of pipelining →