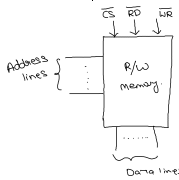


Address lines = n ✓

How many registers are there in memory chip?

→ 2^n ✓

Assume that each register can store 8-bit of data.

→ Memory size = no. of registers × Size of each register

$= 2^n \times m$

$= (2^n \times 8)$ bits

1 byte = 8 bits.

$= 2^n$ bytes.

Q A memory system of size 16 K bytes is required to be designed using memory chips having 12 address lines and 4 data lines each. How many such memory chips are required?.

Answer:

$$\text{Number of memory chips required} = \frac{\text{Required memory size in bits}}{\text{give memory chip size in bits}}$$

Required memory size = 16 K bytes = $(16K \times 8)$ bits

Give memory chip size = $(2^{12} \times 4)$ bits

→ If data lines = 4 that means each register can send or receive 4 bit data

$$\text{NO of memory chips} = \frac{16K \times 8}{2^{12} \times 4} = \frac{16 \times 1024 \times 8}{4096 \times 4}$$

$$= 8$$

→ 8 memory chips each having 12 address lines and 4 data lines are required to design 16 K byte memory system.

Q Three memory chips are of size 1 KB, 2 KB and 4 KB. Their address bus is 10 bits wide. What are the size of data bus for each memory chips?.

Ans: Size of memory = NO. of registers × Size of each register

$= 2^n \times$ size of data bus (bits)

$n \rightarrow$ Size of address bus (bits)

For 1 KB memory chip: $n = 10$; Size of memory = 1 K bytes = $1 \times 1024 \times 8$ bits

$1 \times 1024 \times 8 = 2^{10} \times$ Size of data bus

Size of data bus = 8 bits.

For 2 KB memory chip: $n = 10$; Size of memory = 2 K bytes = $2 \times 1024 \times 8$ bits

$2 \times 1024 \times 8 = 2^{10} \times$ Size of data bus

Size of data bus = 16 bits.

For 4 KB memory chip: Size of data bus = 32 bits.

Q For a microprocessor based system, how many memory chips are required if each chip is having 10 address lines and 8 data lines. The µp has 20 address lines.

Ans: The maximum memory addressing capability of given µp $= 2^{\text{Address lines}}$

$= 2^{20}$

$= 1$ MBytes

required memory size $= (1 \times 1024 \times 1024 \times 8)$ bits

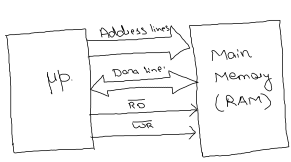
Given memory chip size $= 2^{\text{address lines}} \times$ data lines

$= (2^{10} \times 8)$ bits.

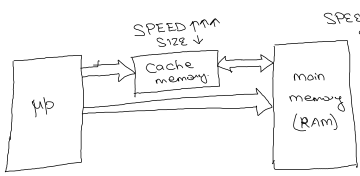
Memory chips required $= \frac{1 \times 1024 \times 1024 \times 8}{2^{10} \times 8} =$

1 K = 1024
1 M = 1024 × 1024
1 G = 1024 × 1024 × 1024
1 T = 1024 × 1024 × 1024 × 1024

CACHE MEMORY → Small high speed memory which is between µp and main memory (RAM)



RAM → SPEED ↑ COST ↑↑↑



Overall cost. (manageable.)

µp → GPR. Registers → CACHE → Main memory (RAM) → Secondary memory (Hard disk)