



NCEAC.FORM. 001-D

COURSE DESCRIPTION FORM

INSTITU:						
BS(CS)	-					
PROGRAM (S) TO BE						
EVALUATED						
A. Course Description						
В.						





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(Fill out the following table for each course in your computer science curriculum. A filled out form should not be more than 2-3 pages.)

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Course Code			
Course Title	Digital l	Logic Design (DLD)	
Credit Hours	3+1		
Prerequisites by Course(s) and Topics			
Assessment Instruments	Assessn	nent Tools (AT) & Criteria	
with Weights (homework,	AT	Description	Weight
quizzes, midterms,	1	Mid Term I and II	30
final,	2	Assignments	10
programming assignments,	3	Quizzes	10
lab work, etc.)	4	Final Examination	50

AT to CLO Mapping

	AT 1	AT 2	AT 3	AT 4	Weight
CLO 1	2			2	4
CLO 2	13	3	4	8	28
CLO 3	15	4	3	10	32
CLO 4		3	3	30	36

AT to PLO Mapping

	AT1	AT 2	AT 3	AT 4	Wei ght
PLO 1					
PLO 2	15	3	4	10	32
PLO 3	15	7	6	40	68





	PLO 4						
	DI O 5						
	PLO 6						
	PLO 7						
	PLO 8						
	PLO 9						
	PLO 10						
	PLO 11						
	PLO 12						
Course Coordinator	Rabia Tabassum						
URL (if any)							
Current Catalog Description					ls for the design of emputer science student		nic circuits using
Textbook (or Laboratory Manual for Laboratory Courses)	Digital Fundamentals , 11 th Edition, Floyd and Jain						
Reference Material	 Digital Systems Principles and Applications 8th Ed, Tocci, Widmer and Moss Digital Design by Moris Mano 						
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NCEAC.FORM. 001-D

Course Goals C

Course Learning Outcomes (CLO)

	Outcomes (CLO)	Domain	Taxonomy Level	PLO
1	Identify and explain fundamental concepts of digital logic design including basic and universal gates, number systems, binary coded system, basic components of combinational and sequence circuits.	Cognitive	2	2
2	Demonstrate the acquired knowledge to apply techniques related to the design and analysis of digital electronics circuits, including Boolean Algebra and Multi-variable Karnaugh map methods.	Cognitive	3	2
3	Analyze small –scale combinational digital circuits.	Cognitive	3	3
4	Design small-scale combinational and synchronous sequential digital circuit using Boolean Algebra and K-map.	Cognitive	3	3

Relevant Program Learning Outcomes (PLOs):

PLO 1	Computing Knowledge	Apply knowledge of mathematics, natural sciences, computing fundamentals, and a computing specialization to the solution of complex computing problems.
PLO 2	Problem Analysis	Identify, formulate, research literature, and analyse complex computing problems, reaching substantiated conclusions using first principles of mathematics, natural sciences, and computing sciences.
PLO 3	Design/Develop Solutions	Design solutions for complex computing problems and design systems, components, and processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations.
PLO 4	Investigation & Experimentation	Conduct investigation of complex computing problems using research based knowledge and research based methods
PLO 5	Modern Tool Usage	Create, select, and apply appropriate techniques, resources and modern computing tools, including prediction and modelling for complex computing problems.





PLO 6	Society Responsibility	Apply reasoning informed by contextual knowledge to assess societal, health, safety, legal, and cultural issues relevant to context of complex computing problems.
DI O 7	F 1	derstand and evaluate sustainability and impact of professional computing work he solution of complex computing problems
PLO 8	Ethics	Apply ethical principles and commit to professional ethics and responsibilities and norms of computing practice.
PLO 9	Individual and Team Work	Function effectively as an individual, and as a member or leader in diverse teams and in multi-disciplinary settings.
PLO 10	Communication	Communicate effectively on complex computing activities with the computing community and with society at large.
PLO 11	Project Mgmnt and Finance	Demonstrate knowledge and understanding of management principles and economic decision making and apply these to one's own work as a member or a team.
PLO 12	Life Long Learning	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological changes.

Relation between CLOs and PLOs (CLO: Course Learning Outcome, PLOs: Program Learning Outcomes)													
							PLC)s					
		1	2	3	4	5	6	7	8	9	10	11	12
	1		~										
CLO	2		~										
S	3			~									
	4			~									

Topics
Covered in
the Course,
with Number
of Lectures
on Each
Topic
(assume
15-week
instruction

Week No.	Course Contents/Topics	Chapter	CLOs	Tools
1	Decimal Numbers, Binary Numbers, Decimal-to-Binary Conversion, Binary Arithmetic, Complements of Binary Numbers, Signed Numbers, Arithmetic Operations with Signed Numbers, Hexadecimal Numbers, Octal Numbers,	2	1	A1, M1, F





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2	Fate, The NAND Gate, The INON Gate, The Exclusive-OR and Exclusive- NOR Gates	3	2	A2,Q1,M1,F
3	Boolean Operations and Expressions, Laws and Rules of Boolean Algebra, DeMorgan's Theorems,	4	2	A2,M1,F
4	Boolean Analysis of Logic Circuits, Logic Simplification Using Boolean Algebra, Standard Forms of Boolean Expressions, Boolean Expressions and Truth Tables.	4	2	A2,M1,F
	The Karnaugh Map, Karnaugh Map SOP Minimization, Karnaugh Map POS Minimization	4	2	A2,M1, F
6		Mid- Term I		
7	Basic Combinational Logic Circuits, The Universal Property of NAND and NOR gates, Pulse Waveform Operation	5	3	A3,M2, F
8	Half and Full Adders, Parallel Binary Adders,	6	3	A3,Q2,M2 ,F
	3 4 7	Boolean Operations and Expressions, Laws and Rules of Boolean Algebra, DeMorgan's Theorems, Boolean Analysis of Logic Circuits, Logic Simplification Using Boolean Algebra, Standard Forms of Boolean Expressions, Boolean Expressions and Truth Tables. The Karnaugh Map, Karnaugh Map SOP Minimization, Karnaugh Map POS Minimization Basic Combinational Logic Circuits, The Universal Property of NAND and NOR gates, Pulse Waveform Operation Half and Full Adders, Parallel Binary	Codes (Gray code with conversion) Logic gates, The Inverter, The AND iate, The NAND Gate, The Exclusive-OR and Exclusive-NOR Gates Boolean Operations and Expressions, Laws and Rules of Boolean Algebra, DeMorgan's Theorems, 4 Boolean Analysis of Logic Circuits, Logic Simplification Using Boolean Algebra, Standard Forms of Boolean Expressions, Boolean Expressions and Truth Tables. 4 The Karnaugh Map, Karnaugh Map SOP Minimization, Karnaugh Map POS Minimization Mid-Term I Basic Combinational Logic Circuits, The Universal Property of NAND and NOR gates, Pulse Waveform Operation 5 Half and Full Adders, Parallel Binary 6	Codes (Gray code with conversion) Logic gates, The Inverter, The AND iate, The NAND Gate, The Exclusive-OR and Exclusive-NOR Gates Boolean Operations and Expressions, Laws and Rules of Boolean Algebra, DeMorgan's Theorems, 4 2 Boolean Analysis of Logic Circuits, Logic Simplification Using Boolean Algebra, Standard Forms of Boolean Expressions, Boolean Expressions and Truth Tables. 4 The Karnaugh Map, Karnaugh Map SOP Minimization, Karnaugh Map POS Minimization The Karnaugh Map Circuits, The Universal Property of NAND and NOR gates, Pulse Waveform Operation 5 3 Half and Full Adders, Parallel Binary 6 3





	9	Comparators, Decoders, Encoders,	6	3	A3,M2,F		
	10	Code Converters, Multiplexers, Demultiplexers	6	3	A3,M2, F		
	11	Mid-Term II					
		Latches					
	12		7	4	,F		
	13	Flip-Flop	7	4	Q3, F		
	14	Asynchronous Counters, Synchronous Counters, Design of Synchronous Counters	9	4	Q3, F		
	15	Shift Register Operations, Types of Shift Register Data I/Os,	8	4	F		
	16	Revision					
		Final Examination					
Laboratory Projects/Exp eriments Done in the Course							
Programmin g Assignments Done in the Course							





NCEAC.FORM. 001-D

Class Time	Theory	Problem Analysis	Solution Design	Social and l				
Spent on (in credit hours)	30	10	5					
Oral and Written Communicat ions	typically10 minute's duration. Include only material that is graded for grammar, spelling, style, and so forth, as technical content, completeness, and accuracy.							

Instructor Name: Rabia Tabassum

Instructor Signature

Date 15-01-25