CLO # 1: Understanding and implementation of the adder/subtractor/multiplier circuits for real-world application.

Q1. Design Full Adder using decoders and use minimum number of gates. **[10 marks]**

CLO # 2: Identify the use case of binary comparators in real-world systems and applications.

Q2. Design and construct an 1 x 16 DEMUX with 1 x 4 DEMUX in Logic Works. Draw the truth table of 1 x 16 DEMUX. **[10 marks]**

CLO # 3: Understand how computers store data using latches and flip flops, how counters operate with respect to incrementing and decrementing values.

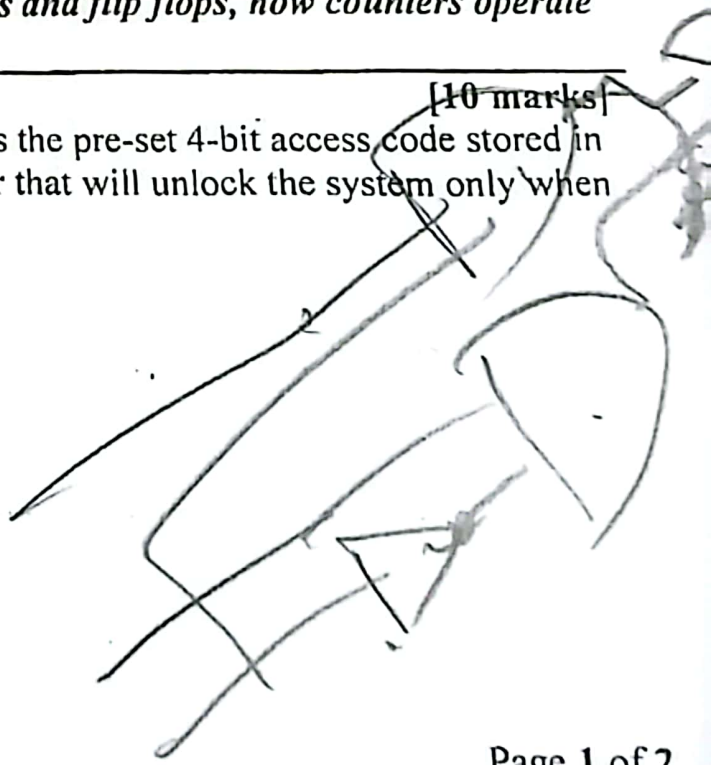
[10 marks]

Q3. A digital lock opens only when a 4-bit input code matches the pre-set 4-bit access code stored in memory. Question: Design a digital circuit using a comparator that will unlock the system only when the input code is equal to the stored code.

Use EN → Enable (1 = Compare, 0 = No output)

- Based on the comparison:
  - **(A > B)** Lock.
  - **(A < B)** Lock.
  - **A = B)** OPEN.

- A3 A2 A1 A0 → 4-bit
- B3 B2 B1 B0 → 4-bit



CLO # 3: Understand how computers store data using latches and flip flops, how counters operate with respect to incrementing and decrementing values.

[20 Marks]

Q4: Design a circuit using **D flip-flops** to generate a **binary counting sequence**. The sequence should represent decimal numbers from **0 to 7**, progressing in binary as follows:

This sequence should repeat after every **eight clock pulses**, cycling back to 000. The design must ensure the flip-flops count in proper binary order from 0 to 7, then restart the sequence automatically.

Hint:
Use three D flip-flops to create a 3-bit binary counter. Each flip-flop output corresponds to one bit of the binary number.

Binary Sample Output and Decimal Sample Output: