Digital Logic Design

(EL-1005)

LABORATORY MANUAL

Spring-2025

LAB 06

Binary Comparator

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STUDENT NAME	ROLL NO	SEC

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INSTRUCTOR SIGNATURE& DATE

MARKS AWARDED: /10

Lab Session 06: Binary Comparator

OBJECTIVES:

- To learn and understand how to design a multiple output combinational circuit
- To learn and understand the working of 2-bit binary comparator
- To learn and understand the working and usage of Exclusive-OR and Exclusive-NOR gates

APPARATUS: Logic trainer, Logic probe

COMPONENTS: ICs 74LS08, 74LS32, 74LS04, 74LS86, 74LS02

THEORY:

Binary comparator is a combinational circuit that compares magnitude of two binary data signals A & B and generates the results of comparison in the form of three output signals A>B, A=B, A<B. Binary comparator is a multiple input and multiple output combinational circuit. When a combinational circuit has two or more than two outputs then each output is expressed separately as a function of all inputs. Separate K-map is made for each output.

One-bit comparator:

One-bit comparator compares magnitude of two numbers A and B, 1 bit each, and generates the comparison result. The result consists of three outputs let us say L, E, G, so that

$$L = 1 \; if \; A < B$$

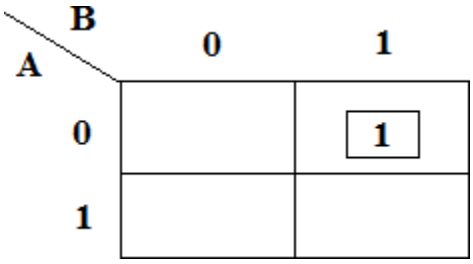
$$E = 1 \; if \; A = B$$

$$G = 1 \; if \; A > B$$

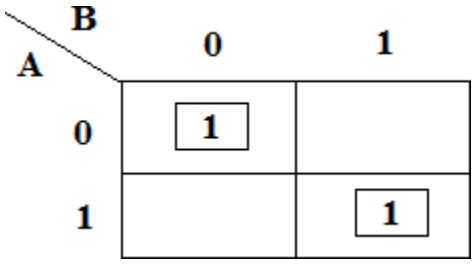
Truth Table:

Inputs		Outputs		
A	**B**	**L**	**E**	**G**
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

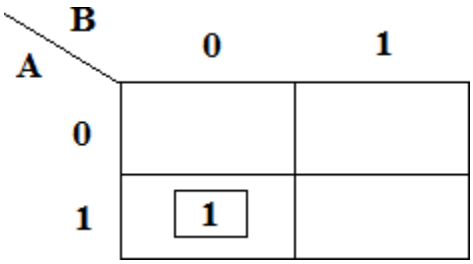
K-Maps for Outputs:



K-Map for Output **L**



K-Map for Output **E**



K-Map for Output **G**

Boolean Expressions of Outputs:

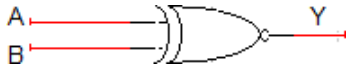
L: $\bar{A}B$

E: $AB + \bar{A}\bar{B}$

G: $A\bar{B}$

Exclusive-OR & Exclusive-NOR gates:

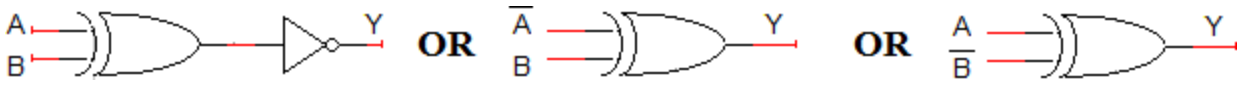
The figure given below shows the symbol of Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates.



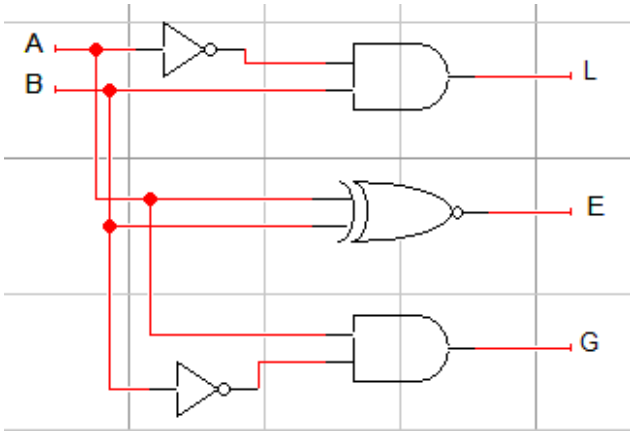
XNOR gate

XOR gate

Boolean expression of XNOR gate is $AB + \bar{A}\bar{B}$ and Boolean expression of XOR is $\bar{A}B + A\bar{B}$. Boolean expression of XNOR gate can be implemented using XOR gate as shown in figure below:



Circuit Diagram for one-bit comparator:



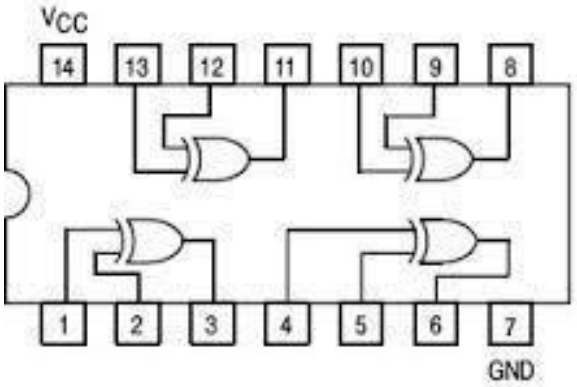
In this experiment 74LS86 IC will be used for implementation of XOR gate function. 74LS86 IC contains four 2-input XOR gates. The function table and connection diagram for this IC are shown below:

Function Table:

Inputs		Output
A	**B**	**Y**
L	**L**	**L**
L	**H**	**H**
H	**L**	**H**
H	**H**	**L**

H= Logic High, L= Logic Low

Connection Diagram:



Lab Task #1

Design a combinational circuit that compares two 2-bit numbers and generates the comparison result. The result consists of three outputs let us say L, E, G, so that (i.e. 10 and 01 but can vary)

$$L = 1 \; if \; A < B$$

$$E = 1 \; if \; A = B$$

$$G = 1 \; if \; A > B$$

1. Write truth table on copy and demonstrate the circuit you made for a 2-bit comparator.

Lab Task #2

2. Create a circuit that does two operations (i.e. multiplication/addition/subtraction your choice). Consider an input (10 and 01 must be two bits) which when performed will generate some output to which you would have to compare the results. Do not make a truth table of the circuit just the diagram and implementation would be sufficient.

Lab Task #3

Take the above scenario and modify it such that you now have three operations (add/subtract/multiply) and three bits this time but you will need to create a circuit such that for a given input of three bits (A and B) there should an equal stage such that you can achieve it by subtracting/adding/multiplying the inputs. You can also do a stage i.e. 100 and 010 are added to yield 110 but if we multiply the inputs we get 1000 and subtract it by 010 to get an equal output. This might seem tricky at first, and it is that's the reason you can implement this in logism no need to create a H.W implementation of this.