

DLD Assignment-3

1. If the waveforms in Fig-1 are applied to an active-Low S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume that Q starts Low.

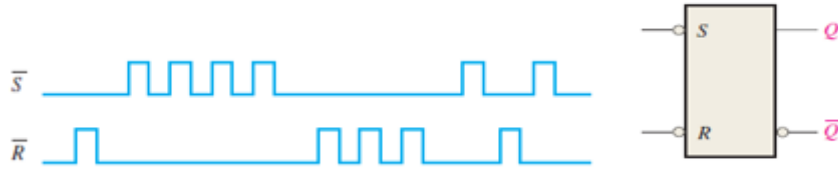


Fig-1

2. Solve problem -1 for the input waveform in Fig-2 applied to an active –High S-R latch.

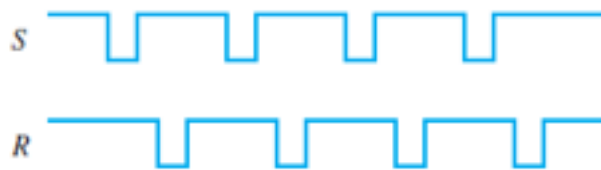


Fig-2

3. Solve problem -1 for the input waveform in Fig-3.



Fig-3

4. For a gated S-R latch, determine the Q and Q' output for the inputs in Fig-4. Show them in proper relation to the enabled input. Assume that A starts LOW.

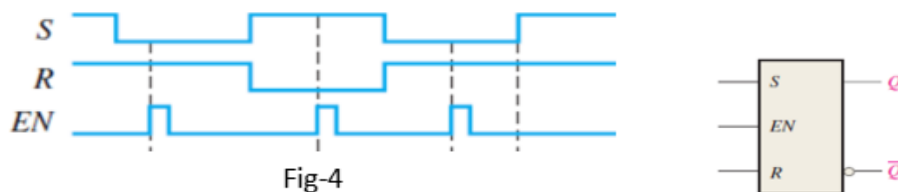


Fig-4

5. Determine the output of the gated D latch for the inputs in Fig-5 and Fig-6.

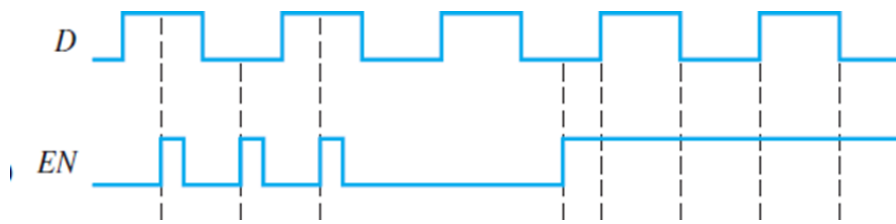


Fig-5



Fig-6

6. The Q output of an edge-triggered D flip-flop is shown in relation to the clock signal in Fig-7. Determine the input waveform on the D input that is required to produce this output if the flip-flop is a positive edge-triggered type.

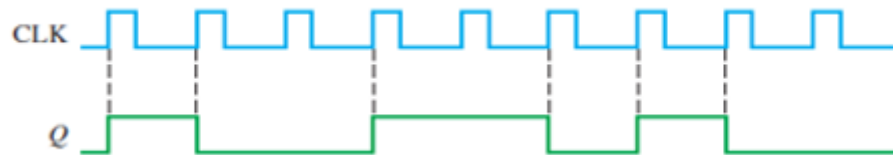


Fig-7

7. Determine the Q waveforms relative to the clock if the signal shown in Fig -8 are applied to the input of the J-K flip-flop. Assume that Q initially LOW.

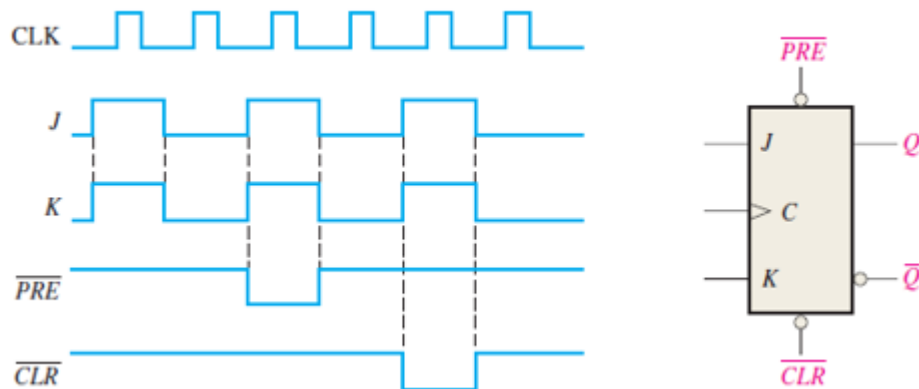


Fig-8

8. For negative edge-triggered J-K flip-flop with the input in Fig-9, develop the Q output waveform relative to the clock. Assume that Q is initially LOW.

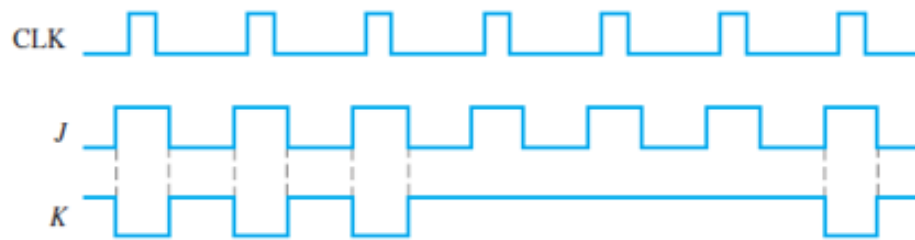


Fig-9

9. For the circuit in Figure -10, complete the timing diagram in Fig-1` by showing the Q output (which is initially LOW). Assume PRE and CLR remain HIGH.

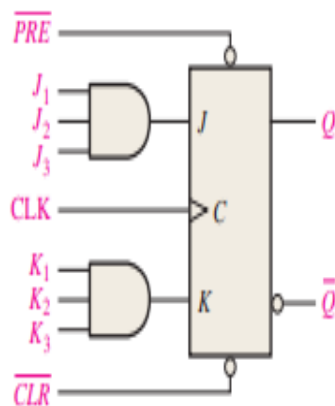
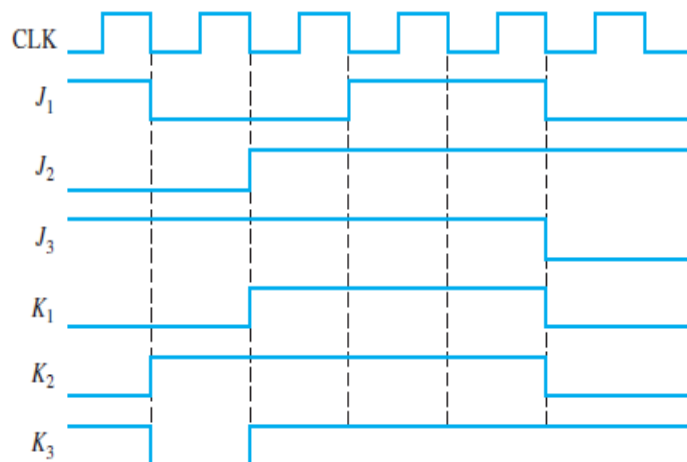


Fig-11

Fig-10

10. A D flip-flop is connected as shown in Fig-12. Determine the Q output in relation to the clock. What specific function does this device perform?

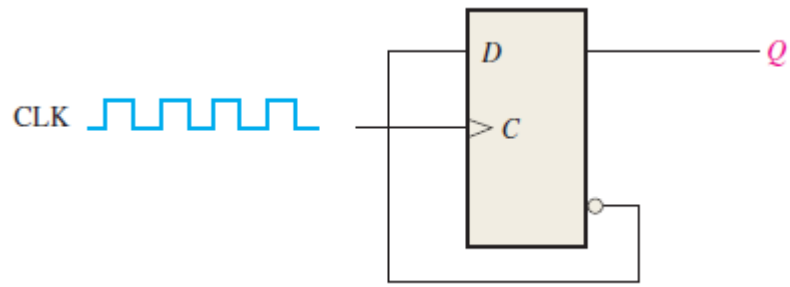


Fig-12