EC605: Computer Engineering Fundamentals Fall 2016
Lab 5: Single Cycle ARM Datapath

Goals

- Gain experience with digital design and Verilog.
- Gain understanding of computer organization via hands-on implementation of an ARM datapath.

Overview

In this lab you will design a single-cycle ARM-like datapath, with supports variation on a sub-set of the LEGv8 instructions. The structure of the datapath should follow the one described in the textbook and lectures. The movk instruction implementation is not specified in the textbook, and you may implement the datapath to support it as you see fit.

The simplified ARM instruction format is as follows:

R-format:

opcode		Rm		shamt		Rn		Rd	
31	21	20	16	15	10	9	5	4	0

I-format:

opcode		ALU Immedate		Rn		Rd	
31	21	20	10	9	5	4	0

D-format:

opcode		DT address		Rn		Rt	
31	21	20	10	9	5	4	0

CB-format:

opcode		COND BR address		Rt	
31	21	20	5	4	0

IM-fortat:

opcode		MOV address		Rd	
31	21	20	5	4	0

Following is the simplified subset of instructions to be supported:

Instruction	**Opcode**
BRANCH	11'h0A0

AND	11'h450
ADD	11'h458
ORR	11'h550
CBZ	11'h5A0
SUB	11'h658
MOVK	11'h794
STUR	11'h7C0
LDUR	11'h7C2

Tasks

Task 1: Datapath Components

1. **Instruction Memory**
   The instruction memory, with sample instructions is provided in IMem.v. Note that the instruction memory is read-only. Simulate the instruction memory module and make sure that it operates correctly.

2. **Register File**
   The register file module, Register_File.v is provided. Simulate the instruction memory module and make sure that it operates correctly.

3. **Data Memory**
   Implement and test a data memory module. This module can be similar in structure to the register file.

4. **ALU**
   Implement and test a 64-bit ALU, supporting the following operations:

Opcode	Operation
1	AND
2	OR
3	NOT
4	MOVA: Out <= A
5	MOVB: Out <=B
6	Add
7	Subtract

The ALU also has a Zero output flag.

5. **Control logic**
   Implement and test a unified control unit, which combines the functionality of the central control unit and the ALU control unit. The input should be an instruction, and the outputs are the control inputs to all the datapath elements.

Task 2: Integrated Datapath

1. In a new project, implement and test a working datapath that instantiates and connects all the datapath components.
2. Modify the content of the instruction memory to include a complete test assembly program, and demonstrate the workings of your datapath with a waveform.

First Milestone

Completed modules and working testbenches for the following portions of the datapath:

- Register file - read and write operations
- Data memory - read and write operations
- ALU - all operations and zero flag
- Incrementing PC counter and branch selection control

Deliverables

- Submit your Verilog code and testbench for each datapath component and the integrated datapath. Also submit a pdf with a waveform and a description of the tests done for each component, and a description of your implementation of the movk instruction, and any other design choices that you made.
- Sign-up to demo your design to a TA. Come prepared to answer questions on your design.