

EC605 LAB 1 Report

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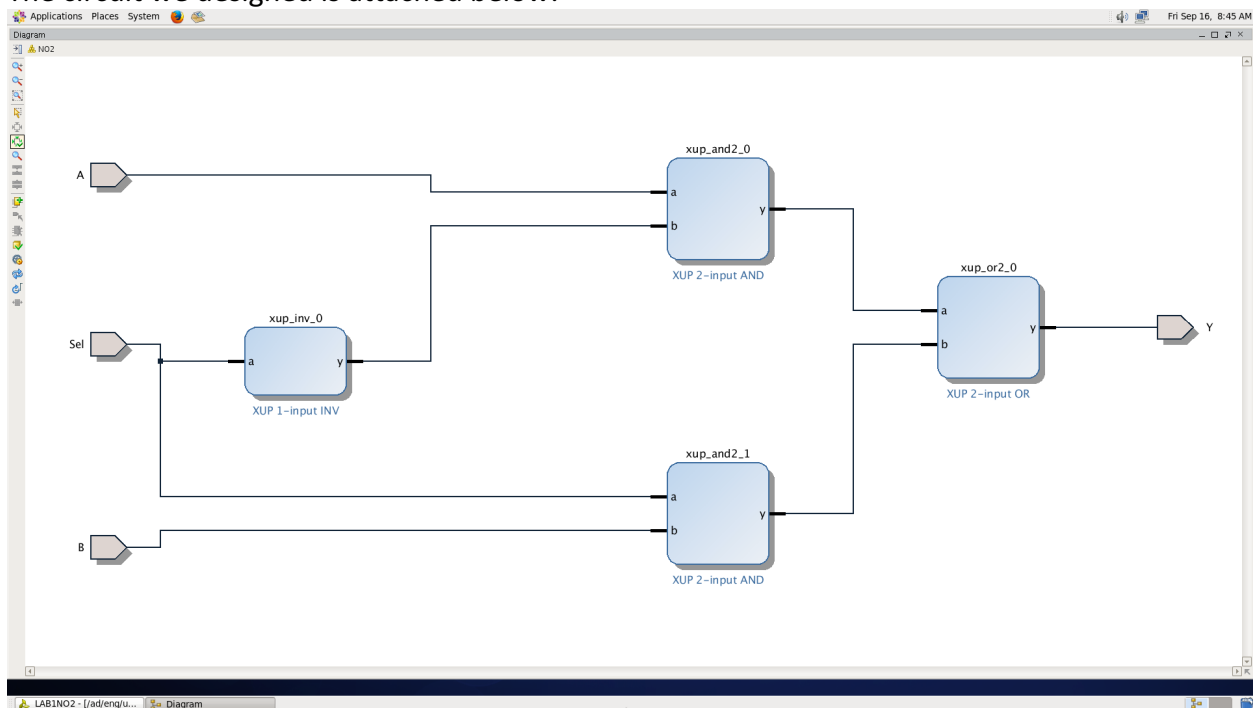
Task (2): 2:1 Multiplexer

At first we figure out the output table when we manage selection of the data.

The output table is listed as follows:

S	Y
0	A
1	B

The circuit we designed is attached below:



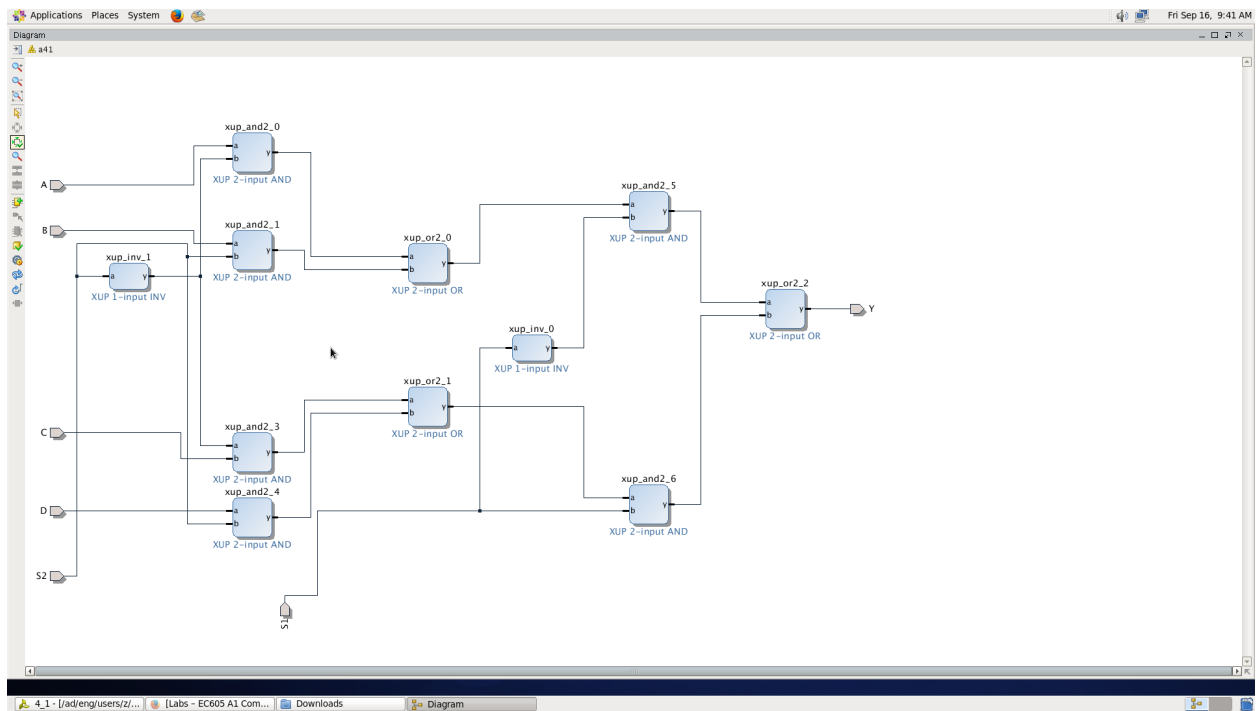
Task (3): 8:1 Multiplexer

First we managed the output list of 4:1 Multiplexer.

The output list is:

S1	S2	Y
0	0	A
0	1	B
1	0	C
1	1	D

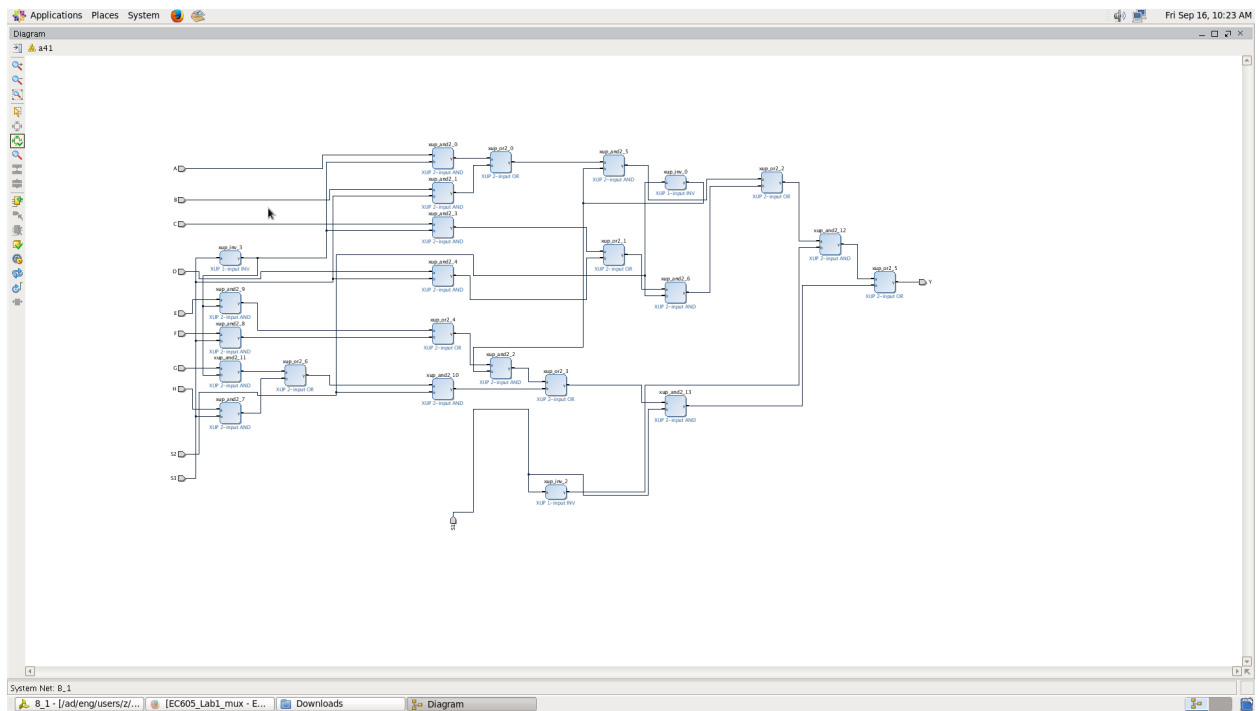
We can use 3 2:1 mux to build this 4:1 mux.



After that, we used the same principle to build a 8:1 mux with 2 4:1 mux. The output table of the 8:1 mux is shown below:

S1	S2	S3	Y
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H

The circuit of this 8:1 mux is:



We modified the circuit to run the time test. The circuit is shown below:

