



PayTrans_POS Terminal Communications Specification

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5/5/16	2.0	C. Meaney	Corrections to typos, formatted to new template

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Introduction

This specification document provides details for the VISA 2nd Generation Terminal Communications Protocol. The following flow charts depict the protocol level for messages sent between the terminal and the processor.

The purpose of this document is to help provide information necessary to develop a communications interface for transmitting transaction information to and from a POS terminal and an acquirer/processor. The flow charts include the modes of normal operation as well as conditions that may be recoverable or result in cancelled transactions.

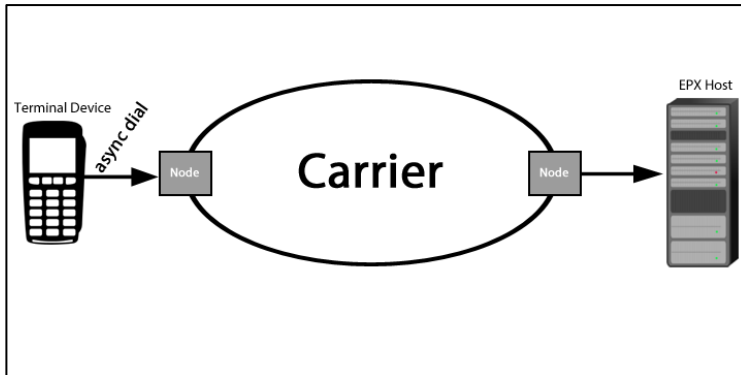
This document was created under the assumption that the reader already possesses current knowledge of POS processing and data communications.

Access Options

Dial Access

Figure 1 depicts the initial communication between the Terminal device and the EPX host.

Figure 1: Dial Access



Message Format Structure

General Format Structure

Figure 2 depicts a general message format and flow used for Visa 2nd generation messaging. A "message" refers to a data frame starting with a start-of-text (STX), followed by information characters and ending with an end-of-text (ETX) and an LRC (or Longitudinal Redundancy Check).

Figure 2: General Message Format

STX	Data Frame	ETX	LRC
-----	------------	-----	-----

Longitudinal Redundancy Check (LRC)

A Longitudinal Redundancy Check or LRC is depicted in *Figure 3*. An LRC helps ensure the data integrity of information messages. An LRC character is generated and added to all data messages in order to detect and recover from any resulting errors during transmission. An LRC is calculated by doing an exclusive OR of each byte in the message, starting with the first byte after the STX and including the ETX.

Figure 3: Longitudinal Redundancy Check (LRC)

STX	Data Frame	ETX	LRC
	← LRC Calculation →		

For more detailed description of the LRC algorithm see:

https://en.wikipedia.org/wiki/Longitudinal_redundancy_check

Character Sets

Data link character set

The VISA 2nd Generation protocol uses characters defined within the ASCII character set. [Table 1](#) provides a partial listing of the special-use characters used by this protocol.

Table 1: Control-character summary

Character	DEC	HEX	Name
STX	2	02	Start of Text
ETX	3	03	End of Text
EOT	4	04	End of Transmission
ENQ	5	05	Enquiry
ACK	6	06	Acknowledgement
BEL	7	07	Bell, Affirmative Acknowledgement
DLE	16	10	Data Link Escape
NAK	21	15	Negative Acknowledgement
ETB	23	17	End of Transmission Block

Figure 4: ASCII Character Set

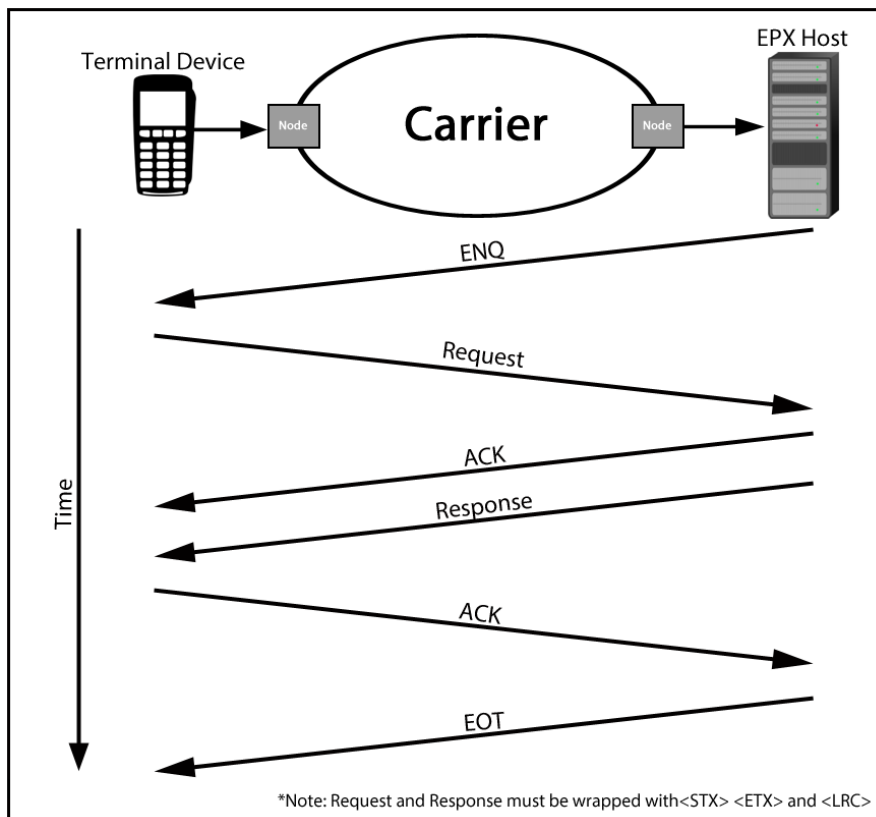
<div> <div> <div>b₇</div> <div>b₆</div> <div>b₅</div> </div> <div> <div>→</div> <div>→</div> <div>→</div> </div> </div> <div> <div>Bits</div> <div>b₄</div> <div>b₃</div> <div>b₂</div> <div>b₁</div> <div> <div>Column →</div> <div>Row ↓</div> </div> </div>					0	0	0	0	1	0	1	1	0	1	1	1
					0	0	0	1	0	1	0	1	0	1	0	1
					0	1	2	3	4	5	6	7				
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p				
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q				
0	0	1	0	2	STX	DC2	"	2	B	R	b	r				
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s				
0	1	0	0	4	EOT	DC4	\$	4	D	T	d	t				
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u				
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v				
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w				
1	0	0	0	8	BS	CAN	(8	H	X	h	x				
1	0	0	1	9	HT	EM)	9	I	Y	i	y				
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z				
1	0	1	1	11	VT	ESC	+	;	K	[k	{				
1	1	0	0	12	FF	FC	,	<	L	\	l					
1	1	0	1	13	CR	GS	-	=	M]	m	}				
1	1	1	0	14	SO	RS	.	>	N	^	n	~				
1	1	1	1	15	SI	US	/	?	O	_	o	DEL				

Modes of Normal Operation (Flowcharts)

Credit Card, Debit Card, EBT Single-transaction mode

Figure 5 depicts a normal single-transaction cycle between a terminal and the host processor during a credit card authorization request.

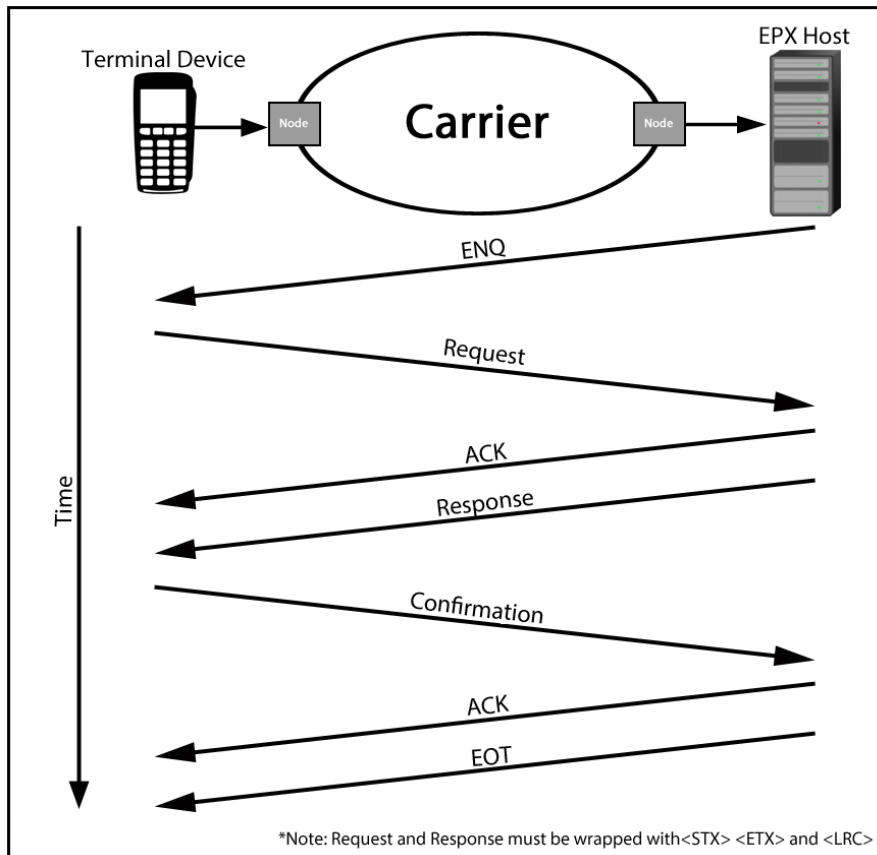
Figure 5: Credit Card Single-Transaction



ATM Single-Transaction mode

Figure 6 depicts a normal single-transaction cycle between a terminal and the host processor during a debit card authorization request.

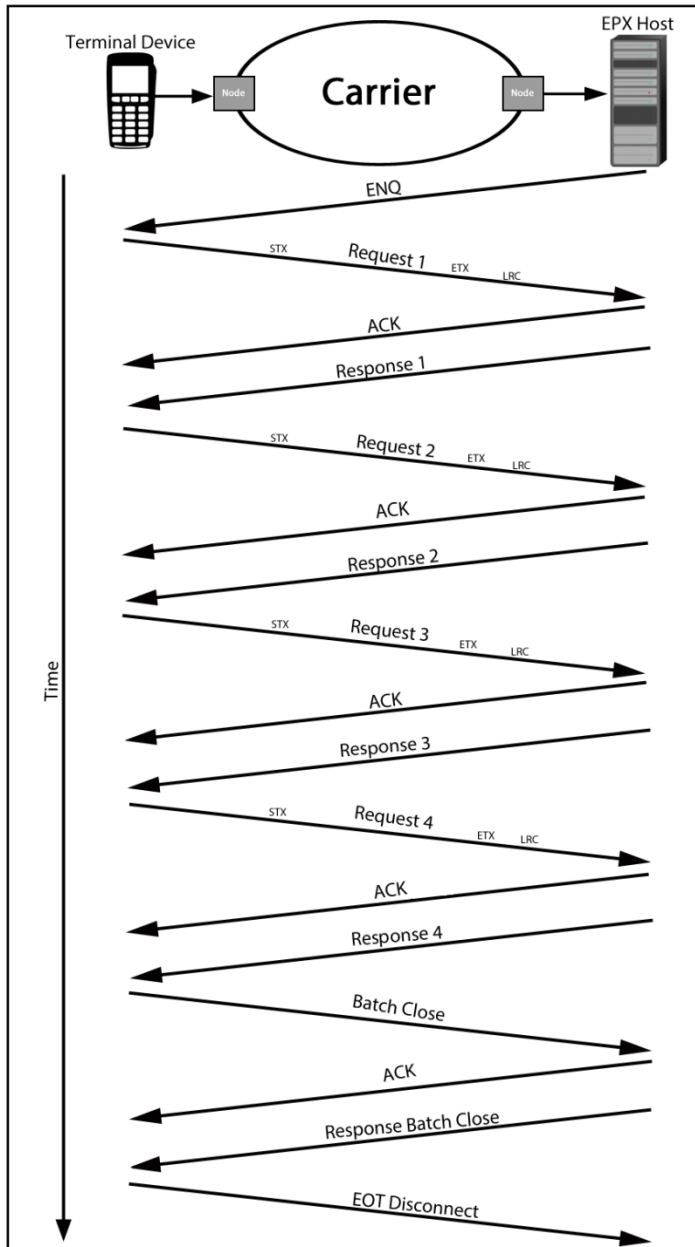
Figure 6: Debit Card Single-Transaction



Single-batch mode

Figure 7 depicts a single-batch cycle between a terminal and the host processor during settlement.

Figure 7: Single-Batch Mode

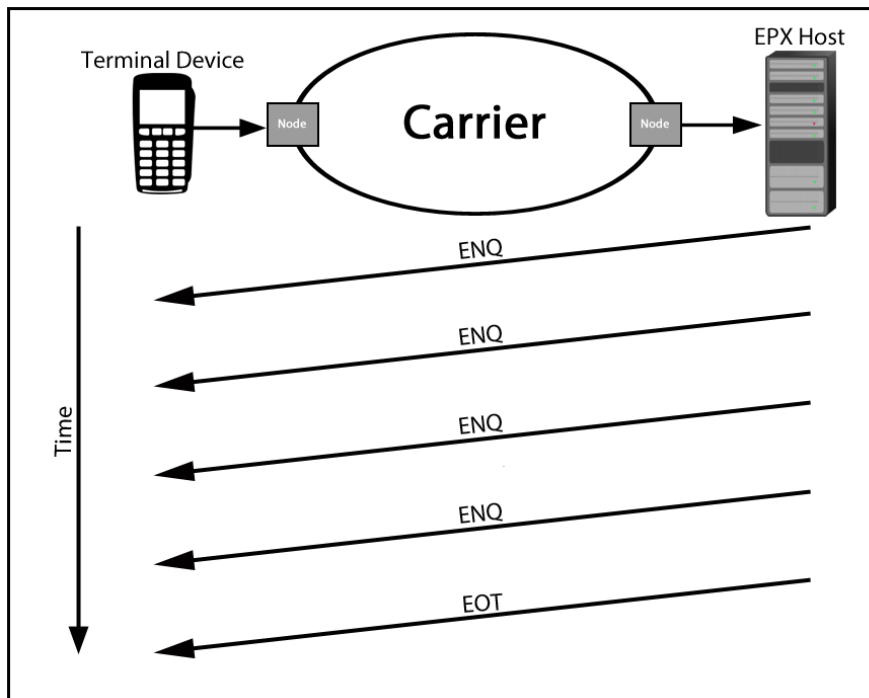


Error Flow Diagrams

No response to host ENQ

Figure 8 depicts protocol for when the terminal does not respond to the Host's enquiry. The host will send at least 4 ENQ before disconnecting.

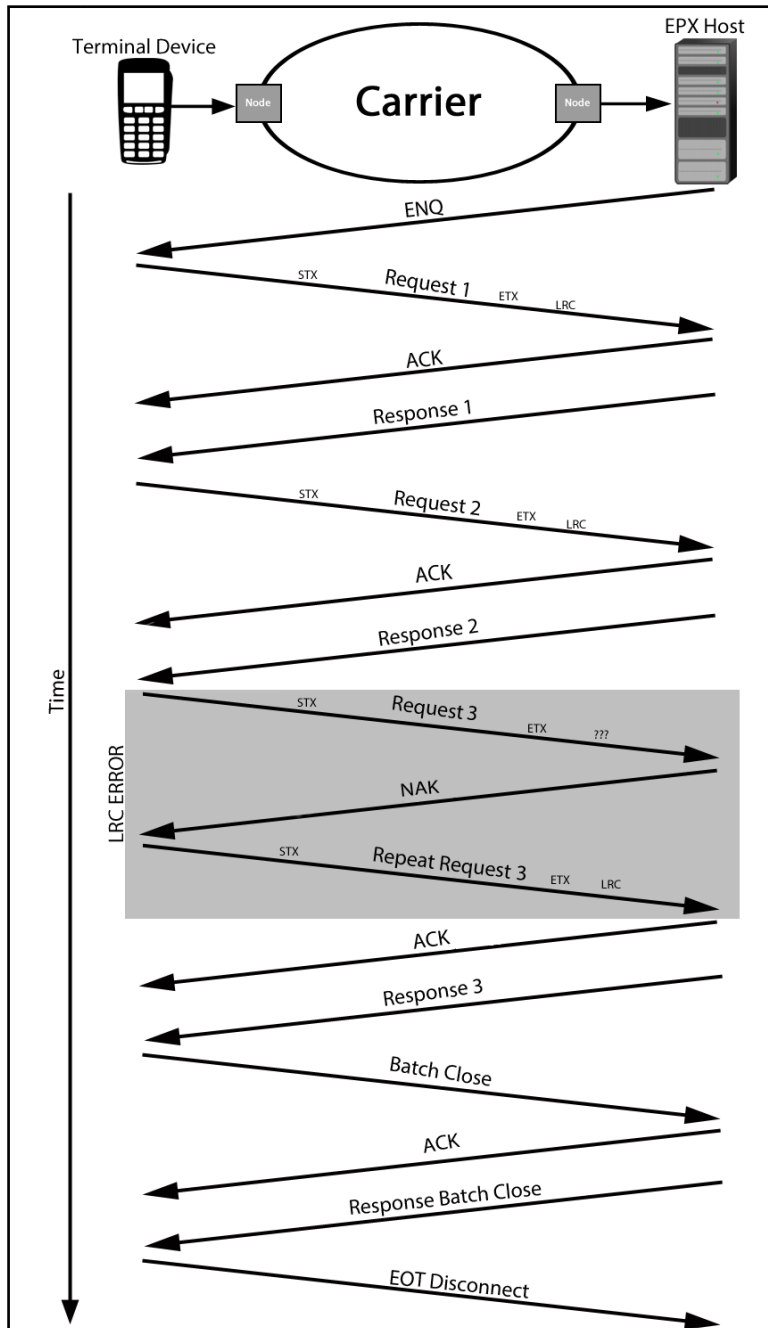
Figure 8: No Response



Recoverable LRC or parity error in batch-settlement process

Figure 9 depicts a scenario in which the terminal receives an error in a batch response message and sends a NAK and request for retransmission, eventually receiving a response without error.

Figure 9: Recoverable LRC Error in Batch Response



Unrecoverable LRC or parity error in batch-settlement process

Figure 10 depicts a scenario in which the terminal receives an error in a batch response message. The host will make three attempts before disconnection.

Figure 10: Unrecoverable LRC Error in Batch

