TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Integrated Masters in Aerospace Engennering, Técnico, University of Lisbon

Laboratory Report 4- Group 28

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1 Introduction

The aim of this laboratory assignment was to create an audio amplifier circuit. To do so, both the gain and the output stages were designed. This amplifier receives an audio maximum input of 10mV and connects to an 8 Ohm speaker. The source has an impedance of 100 Ohms and the circuit is supplied by a 12V Voltage DC source (vcc).

In the gain stage mentioned above, a NPN transistor and a common emitter amplifier with degeneration were used. It allows us to have a high Z_i and a high A_V. Nevertheless, Z_o is also very high, which consitutes a problem. Hence, this situation has to be adressed in the output stage. Consequently, in this second stage, it was used a common collecter amplifier and a PNP transistor. Not only does it allow to remain a high A_V but it also reduces the value of (Z_o) significantly. Therefore, the gain is ≈ 1, which is the desired result.

The quality of the audio amplifier is evaluated by the following expression:

$$MERIT = \frac{VoltageGain * Bandwidth}{Cost * LowerCutOffFrequency} \tag{1}$$

The circuit is shown below.

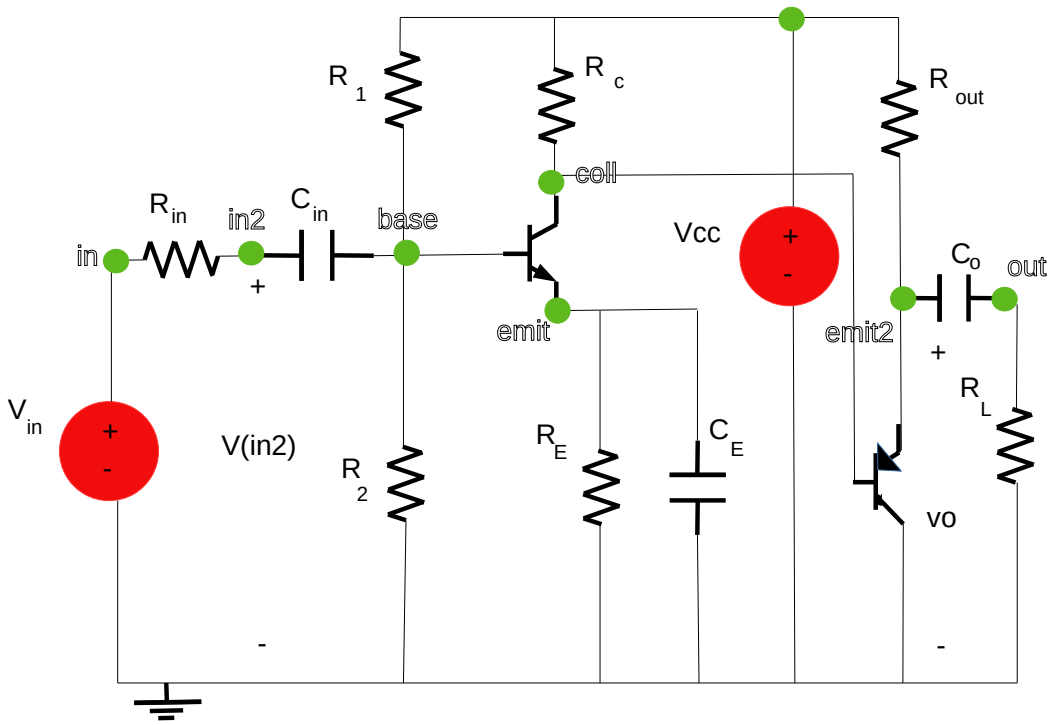

Figure 1: Circuit i analysis.

2 Theoretical Analysis

In this section, a theoretical analysis of the circuit was conducted. In the introduction, we can see analysed circuit.

First of all we got to keep in mind that that our circuit is divided in two different stages. The first one corresponds to the gain stage with a NPN transistor and the second is the output stage with a PNP transistor. The components and their functions of each stage has already been described in the Simulation Analysis as well as the goal of each stage.

In order to analyse a stage we need to study both Operating point and incremental analysis. First, we shut down the AC independent sources and and compute a simple analysis of the circuit. This way we obtain Z_i and Z_o. Moreover, to compute the DC response we can say the capacitors behave like open circuits because there is only DC.

To analyse the incremental response we have to create a model of the transistor (and the rest of the gain stage) similar to Fig.2. Studying the circuit we get $v_{o1} = -g_m * (r_o || R_c) * v_\pi$ and $v_\pi = \frac{R_B || r_\pi}{R_B || r_\pi + R_s} * v_s$ which lead us to $A_{v1} = \frac{v_{o1}}{v_s} = -g_m * (r_o || R_c) * \frac{R_B || r_\pi}{R_B || r_\pi + R_s}$

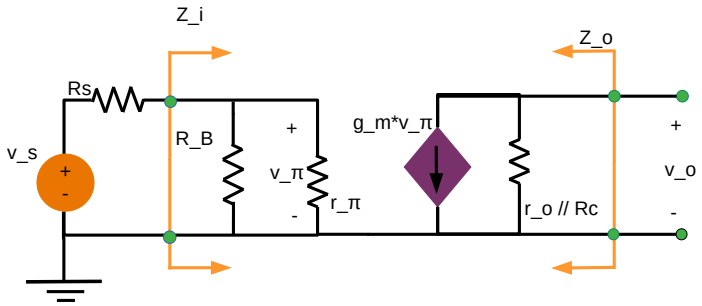

Figure 2: Model for the gain stage incremental analysis

For the DC response of the output stage, we follow the same logic of the gain stage and we easily get Z_{i2} and Z_{o2}. On the other hand, to get the incremental response we have to create another model like Fig.3. Using nodal analysis we end up with $Av2 = \frac{v_{o1}}{v_i} = \frac{g_\pi + g_m}{g_\pi + g_z + g_o + g_m}$ for the gain.

Finally, we calculated i_o to then compute $Z_o = \frac{v_o}{i_o}$ using the provided equations. $Z_i = Z_{i1}$. The gain is given by $A_V = A_{V1} * AV2$ All the important results obtained are shown in the tables and in the figure bellow.

Name	Value
IB1	5.044933e-06
IC1	9.015296e-04
IE1	9.065745e-04
VO1	3.002734e+00

Table 1: Operating point currents and Vcoll.

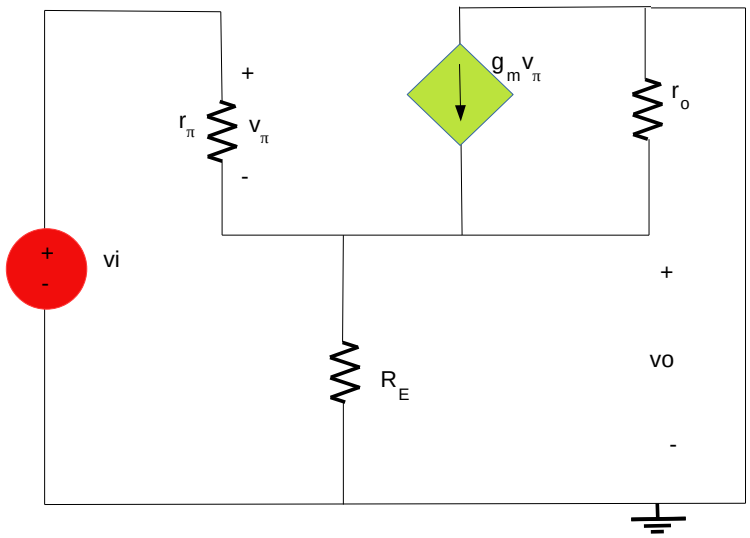

Figure 3: Model for the output stage incremental analysis

Name	Value

Table 2: Impedences of both stages and of the full circuit.

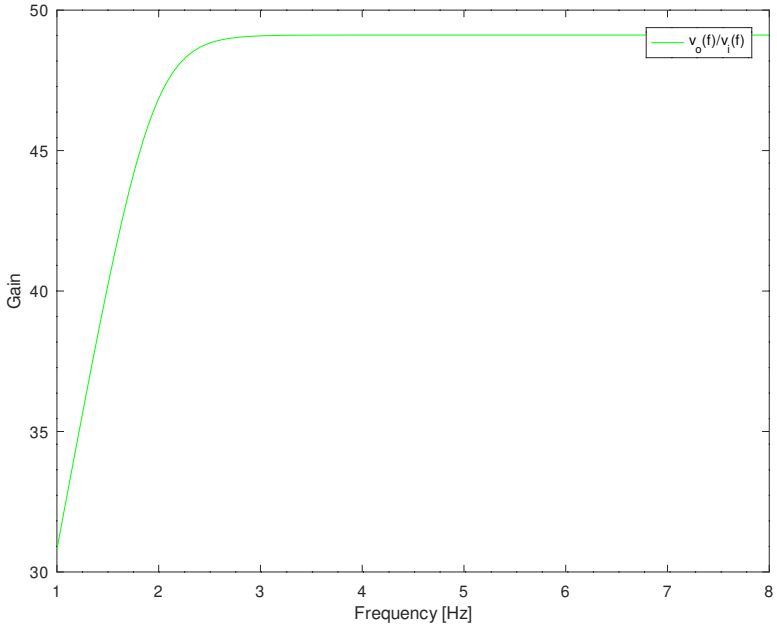

Figure 4: Voltage Gain of the circuit

Name	Value
Gain stage- AV1	2.865758e+02 V
Output stage stage -AV2	9.963314e-01 V
Bandwidth	9.999902e+06 Hz
Cut Off Frequency	9.770100e+01 Hz

Table 3: Gain, bandwidth and cutoff frequency.

3 Simulation Analysis

In this section, the several steps taken using ngspice in order to conduct the simulation of the audio amplifier, as requested, will be described. In fact, the group proceded as follows:

1. Design of the circuit, having as a starting point the circuit given by the professor.
2. Verification of the operation of the transistors in the F.A.R mode. The results are shown below.

Vce ¿ Vbe	Correct F.A.R

Table 4: Verification of the F.A.R mode in the NPN transistor

Vec ¿ Veb	Correct F.A.R

Table 5: Verification of the F.A.R mode in the NPN transistor

3. OP Analysis Then, the OP values of the currents and nodal voltages were computed. These are key to calculate the incremental parameters.
4. In the frequency domain, measure of the output voltage gain, using the function .meas as well as the lower and upper cut off frequencies and the bandwidth.

   The quantities obtained are desribed in the table 7. The first conclusion to be taken from the results are that the main goal of the assignment was achieved, since the voltage gain in the passband is considerable. However, the bandwidth is not as substancial as desired. As so, we conclude the following:

   - The coupling capacitors' main porpuse is to block the DC signals. If studying an incremental model of an audio amplifier, all values that are constant must be eliminated so the transistors are alwaywas fowardly conducting. One of the reasons for the bandwidth obtained to be small is that, these capacitors also cut some low frequencies. These means that the cut off- frequency is high in our circuit. Nevertheless, due to the weight of the cut off frequency in the calculus of the merti, we were able to obtained a good figure of merit.
   - As studied in the lectures, the resistor Re has the funciton of stabelizing the effect of the temperature in the DC voltage. Howerver, it has also a negative effect on the gain, once it lowers it. In order to solve the problem, a bypass capacitor Ce is placed in parallel with the resistor, so that the capacitor bypasses the resistor. In DC mode, the resistor plays its effect in the temperature. In AC, the resistor will not affect the gain. To sum up, the capacitor is a short-circuit for higher frequencies (AC) and a open-circuit for low frequencies (DC).
   - IC is the most important current in the circuit because it determines gm, and so directly influences the gain. So, after making some calculations, Rc is of extremely importance.

5. Determination of the imput impedance, seen from the imput voltage source.

   The result obtained for the imput impedance, considering the value in Kohm, is high. Tis is benefitial for the gain, because the voltage in the node In 2 must be as similiar to Vin as possible. Using a voltage dividir, the only way to achieve this was to have a very high resistance value.

6. Determination of the output impedance, using a different set up, seen from the load resistance.

   Conserning the output impedance, an opposite deduction to the one made for the output impedance is mandoratory. Considering a voltage divider, the output impedance must be as low as possible, in order to the output voltage to be as high as possible. Having said that, an analysing tables 8 9, the difference needed between the two is confirmed.

7. Compute of the cost and figure of merit

Name	Value [V,A]
@cb[i]	0.000000e+00
@ci[i]	0.000000e+00
@cout[i]	0.000000e+00
@q1[ib]	5.121431e-06
@q1[ic]	9.425191e-04
@q1[ie]	-9.47641e-04
@q1[is]	5.956431e-12
@q2[ib]	3.362255e-04
@q2[ic]	5.222856e-02
@q2[ie]	-5.25648e-02
@q2[is]	-5.95738e-12
@r1[i]	1.519829e-03
@r2[i]	1.514712e-03
@rc[i]	6.055066e-04
@re[i]	9.468490e-04
@rin[i]	0.000000e+00
@rl[i]	0.000000e+00
@rout[i]	-5.25648e-02
base	1.969126e+00
coll	5.957044e+00
emit	1.325589e+00
emit2	6.743522e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
vbe	6.435374e-01
vcc	1.200000e+01
vce	4.631455e+00
veb	7.864784e-01
vec	6.743522e+00

Table 6: Simulation nodal voltage results. All variables are expressed in V or A.

V Gain	27.6695
Bandwidth	1.34524E+06
Cut Off Freq	3235.26

Table 7: Results for ngspice

Zin	-887.134 + 65.2407 j

Table 8: Input impedance in KOhm

Zo	41.4899 + -1.33584 j
Zo(arg)	41.5114

Table 9: Output impedance in KOhm

Cost	100.08
merit	114.96

Table 10: Output impedance in KOhm

4 Comparison

In this section, a comparison between Octave and Ngspice results will be made. Firstly, the operating point was computed using the theoretical DC model. In the tables below, the three current values (I_A, I_B, I_C) are presented as well as the voltage in the coll.

Calculus	Value [A or V]
@cb[i]	0.000000e+00
@ci[i]	0.000000e+00
@cout[i]	0.000000e+00
@q1[ib]	5.121431e-06
@q1[ic]	9.425191e-04
@q1[ie]	-9.47641e-04
@q1[is]	5.956431e-12
@q2[ib]	3.362255e-04
@q2[ic]	5.222856e-02
@q2[ie]	-5.25648e-02
@q2[is]	-5.95738e-12
@r1[i]	1.519829e-03
@r2[i]	1.514712e-03
@rc[i]	6.055066e-04
@re[i]	9.468490e-04
@rin[i]	0.000000e+00
@rl[i]	0.000000e+00
@rout[i]	-5.25648e-02
base	1.969126e+00
coll	5.957044e+00
emit	1.325589e+00
emit2	6.743522e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
vbe	6.435374e-01
vcc	1.200000e+01
vce	4.631455e+00
veb	7.864784e-01
vec	6.743522e+00

Table 11: Operating point using DC model. Variables are expressed in Ampere or Volt. (Ngspice)

Name	Value [A or V]
IB1	5.044933e-06
IC1	9.015296e-04
IE1	9.065745e-04
VO1	3.002734e+00

Table 12: Operating point using DC model. Variables are expressed in Ampere or Volt.(Octave)

As one may observe, some discrepancies are noticeable. These may be due to....

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Moreover, the importance of this calculations must be highlighted. In fact, the theoretical gain expression is dependent on the value of the current I_C. This relation can be understood by the expression below. Since this incremental parameter is also present in the gain expression, this may be one of the reasons why some discrepancies may be observed when comparing Octave and Ngspice gain resuts.

$$MERIT = \frac{I_C}{V_T} \tag{2}$$

For both stages, input and output impedances were also computed and the results are shown in the following table.

Calculus	Value [V]
Zin	-887.134 + 65.2407 j

Table 13: Results for the voltage regulator. All variables are expressed in Volt. (Ngspice)

Calculus	Value [V]
Zo	41.4899 + -1.33584 j
Zo(arg)	41.5114

Table 14: Results for the voltage regulator. All variables are expressed in Volt. (Ngspice)

Name	Value [A or V]

Table 15: Results for the voltage regulator. All variables are expressed in Volt.(Octave)

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Aditionally, the gain, bandwidth and cut off frequency results were also computed and compared.

Calculus	Value
V Gain	27.6695
Bandwidth	1.34524E+06
Cut Off Freq	3235.26

Table 16: Gain, bandwidth and cut off frequency. (Ngspice)

Name	Value
Gain stage- AV1	2.865758e+02 V
Output stage stage -AV2	9.963314e-01 V
Bandwidth	9.999902e+06 Hz
Cut Off Frequency	9.770100e+01 Hz

Table 17: Gain, bandwidth and cut off frequency. (Octave)

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5 Conclusion

As discussed in the introduction, the main goal of this assignment was to project an audio amplifier that allowed maximum voltage gain, spending the less possible on the components used. As so, both theorical analysis and simulation analyses were conducted.

Despite strong efforts to match the results obtained in the different analysis, it was concluded that, due to the non-linearity of the components of the circuit, particularly the transistors, it was impossible to obtain the exact same quality using both tools. In fact, the complexity of the parameters of the transistors is believed to be the main reason for this outcome.

Nevertheless, with the believe that the ngspice model is the most similiar to reality, the figure of merit was 60.4168, with a cost of 123.208. That said, the model used can be validated, dispate the discrepancies already explained.