TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Integrated Masters in Aerospace Engengnering, Técnico, University of Lisbon

Laboratory Report 4- Group 28

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Contents

1 Introduction

The aim of this laboratory assignment was to create an audio amplifier circuit. To do so, both the gain and the output stages were designed. This amplifier receives an audio maximum input of 10mV and connects to an 8 Ohm speaker. The source has an impedance of 100 Ohms and the circuit is supplied by a 12V Voltage DC source (vcc).

In the gain stage mentioned above, a NPN transistor and a common emitter amplifier with degeneration were used. It allows us to have a high Z_i and a high A_V. Nevertheless, Z_o is also very high, which consitutes a problem. Hence, this situation has to be adressed in the output stage. Consequently, in this second stage, it was used a common collecter amplifier and a PNP transistor. Not only does it allow to remain a high A_V but it also reduces the value of (Z_o) significantly. Therefore, the gain is ≈ 1, which is the desired result.

The quality of the audio amplifier is evaluated by the following expression:

$$MERIT = \frac{VoltageGain * Bandwidth}{Cost * LowerCutOffFrequency} \tag{1}$$

The circuit is shown below.

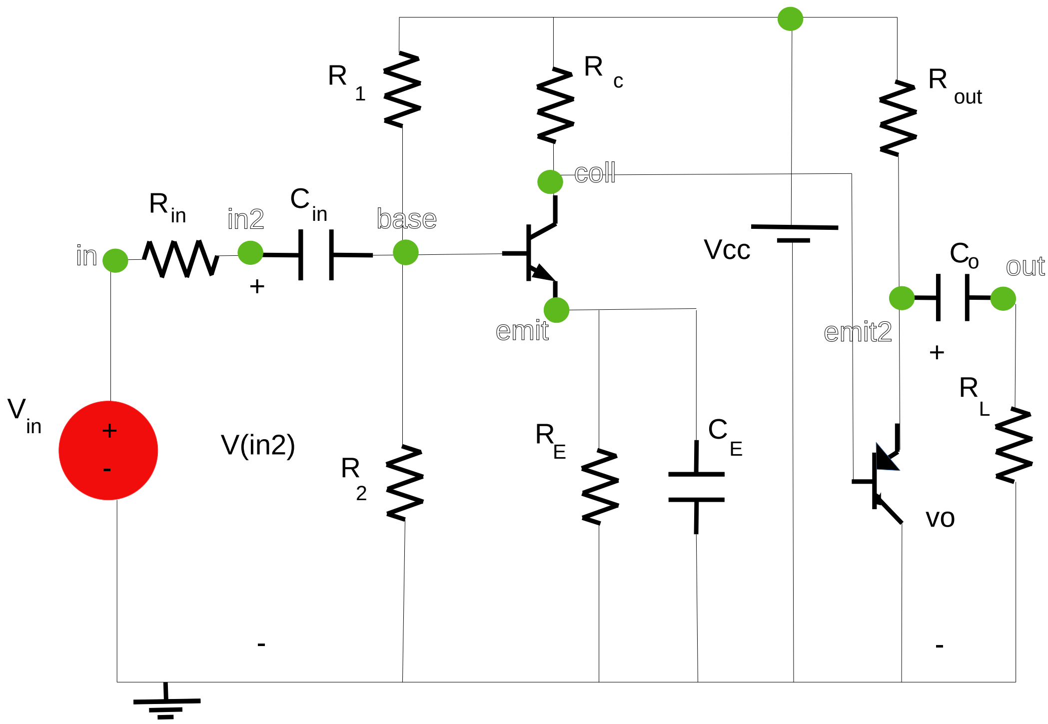

Figure 1: Circuit i analysis.

2 Theoretical Analysis

In this section, a theoretical analysis of the circuit was conducted. In the introduction, we can see analysed circuit.

First of all we got to keep in mind that that our circuit is divided in two different stages. The first one corresponds to the gain stage with a NPN transistor and the second is the output stage with a PNP transistor. The components and their functions of each stage has already been described in the Simulation Analysis as well as the goal of each stage.

In order to analyse a stage we need to study both Operating point and incremental analysis. First, we shut down the AC independent sources and and compute a simple analysis of the circuit. This way we obtain Z_i and Z_o. Moreover, to compute the DC response we can say the capacitors behave like open circuits because there is only DC.

To analyse the incremental response we have to create a model of the transistor (and the rest of the gain stage) similar to Fig.2. Studying the circuit we get $v_{o1} = -g_m * (r_o||R_c) * v_\pi$ and $v_\pi = \frac{R_B||r_\pi}{R_B||r_\pi + R_s} * v_s$ which lead us to $A_{v1} = \frac{v_{o1}}{v_s} = -g_m * (r_o||R_c) * \frac{R_B||r_\pi}{R_B||r_\pi + R_s}$

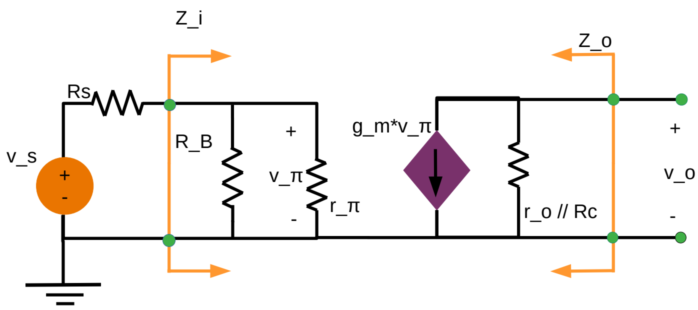

Figure 2: Model for the gain stage incremental analysis

For the DC response of the output stage, we follow the same logic of the gain stage and we easily get Z_{i2} and Z_{o2}. On the other hand, to get the incremental response we have to create another model like Fig.3. Using nodal analysis we end up with $Av2 = \frac{v_{o1}}{v_i} = \frac{g_\pi + g_m}{g_\pi + g_z + g_o + g_m}$ for the gain.

Finally, we calculated i_o to then compute $Z_o = \frac{v_o}{i_o}$ using the provided equations. $Z_i = Z_{i1}$. The gain is given by $A_V = A_{V1} * AV2$ All the important results obtained are shown in the tables and in the figure bellow.

Name	Value
IB1	1.975467e-05
IC1	3.530160e-03
IE1	3.549915e-03
VColl	1.409519e+00
VBase	1.090909e+00
VEmit	3.549915e-01

Table 1: Operating point currents and Vcoll.

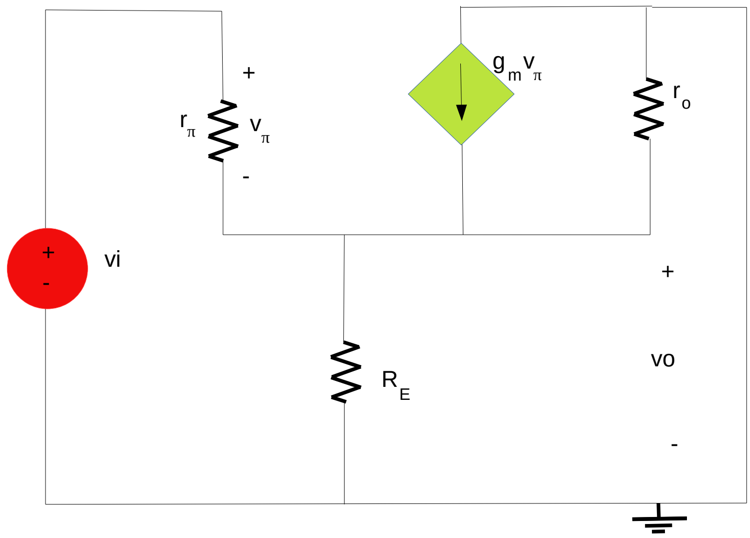

Figure 3: Model for the output stage incremental analysis

Name	Value

Table 2: Impedences of both stages and of the full circuit.

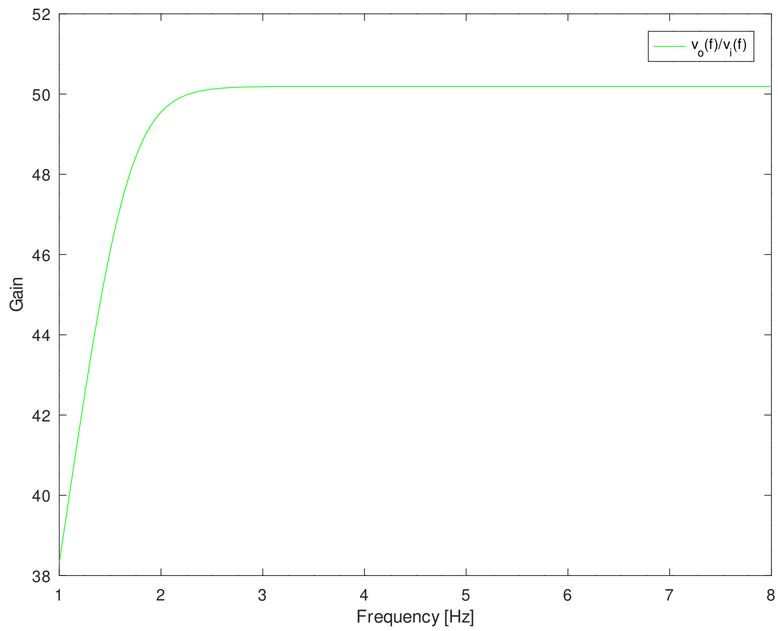

Figure 4: Voltage Gain of the circuit

Name	**Value**
Total Gain (AV)	3.035752e+02 V
Bandwidth	1.348349e+06 Hz
Lower Cut Off Frequency	5.094138e+01 Hz

Table 3: Gain, bandwidth and cutoff frequency.

3 Simulation Analysis

In this section, the several steps taken using ngspice in order to conduct the simulation of the audio amplifier, as requested, will be described. The main focus of the simulation was to determine and optimize de values of the gain, the cut off frequencies, both lower and upper and the bandiwidth. The quality and overall figure of merit will then be analysed. The group proceded as follows:

1. Design of the circuit, having as a starting point the circuit given by the professor.
2. Verification of the operation of the transistors in the forward Active region, the called F.A.R mode. The results are shown below.

Vce	1.57786
Vbe	0.682323
Vce greater than Vbe	Correct F.A.R

Table 4: Verification of the F.A.R mode in the NPN transistor

Vec	2.72908
Veb	0.781397
Vec greater than Veb	Correct F.A.R

Table 5: Verification of the F.A.R mode in the NPN transistor

3. OP Analysis Then, the OP values of the currents and nodal voltages were computed. These are key to calculate the incremental parameters.
4. In the frequency domain, measure of the output voltage gain, using the function .meas as well as the lower and upper cut off frequencies and the bandwidth.

   The quantities obtained are desribed in the table 7. The results obtained allowed the group to understand the functions of the different components of the circuit. The conclusions will be outlined.

   EFFECT OF THE COUPLING CAPACITORS

   The coupling capacitors' main porpuse is to block the DC signals. If studying an incremental model of an audio amplifier, all values that are constant must be eliminated so the transistors are always fowardly conducting. As so, two coupling capacitors were used. Once the capacitors may also block some low frequencies, they have a direct influence in the bandwidth.

   EFFECT OF THE BYPASS CAPACITOR

   As studied in the lectures, the resistor Re has the funciton of stabelizing the effect of the temperature in the DC voltage. However, it has also a negative effect on the gain, once it lowers it. In order to solve the problem, a bypass capacitor Ce is placed in parallel with the resistor, so that the capacitor bypasses the resistor. In DC mode, the resistor plays its effect in the temperature. In AC, the resistor will not affect the gain. To sum up, the capacitor is a short-circuit for higher frequencies (AC) and a open-circuit for low frequencies (DC).

   EFFECT OF RC

   IC is the most important current in the circuit because it determines gm, and so directly influences the gain, by increasing it.

   GRAPHICAL REPRESENTATION

   In the graphics **??** and **??**, a graphic representation of the effect pf the components above mentioned can be observed. In fact, in the plot **??** is extremely enligtenment as one can intuitevely notice the high bandwidth, the stabilization of the gain, and the gain itself.

Name	Value [V,A]
@cb[i]	0.000000e+00
@ci[i]	0.000000e+00
@cout[i]	0.000000e+00
@q1[ib]	2.132105e-05
@q1[ic]	3.676881e-03
@q1[ie]	-3.69820e-03
@q1[is]	1.945288e-12
@q2[ib]	3.261073e-04
@q2[ic]	4.602851e-02
@q2[ie]	-4.63546e-02
@q2[is]	-1.94801e-12
@r1[i]	5.473928e-04
@r2[i]	5.260718e-04
@rc[i]	3.350773e-03
@re[i]	3.698202e-03
@rin[i]	0.000000e+00
@rl[i]	0.000000e+00
@rout[i]	-4.63546e-02
base	1.052144e+00
coll	1.947680e+00
emit	3.698202e-01
emit2	2.729077e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
vbe	6.823234e-01
vcc	1.200000e+01
vce	1.577860e+00
veb	7.813967e-01
vec	2.729077e+00

Table 6: Simulation nodal voltage results. All variables are expressed in V or A.

5. Determination of the imput impedance, seen from the imput voltage source.

   The result obtained for the imput impedance, considering the value in Kohm, is high. This is benefitial for the gain, because the voltage in the node In 2 must be as similiar to Vin as possible. Using a voltage dividir, the only way to achieve this was to have a very high resistance value.

6. Determination of the output impedance, using a different set up, seen from the load resistance.

   Conserning the output impedance, an opposite deduction to the one made for the output impedance is mandoratory. Considering a voltage divider, the output impedance must be as low as possible, in order to the output voltage to be as high as possible. Having said that, an analysing tables 8 9, the difference needed between the two is confirmed. The output impedance obtained is favorable to the 8 ohm load resistance.

7. Compute of the cost and figure of merit To finally understand the efficency of the amplifier, the cost and figure of merit were calculated

   Analysing table 10, the results obtained may be considered satisfying.

V Gain	36.3869
Bandwidth	1.27868E+06
Lower Cut Off Freq	53.0031

Table 7: Results for ngspice

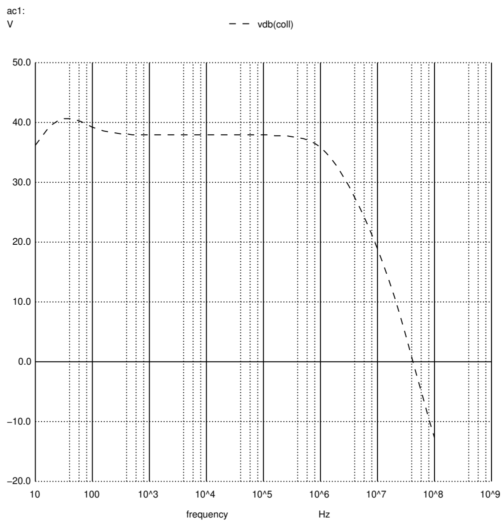

Figure 5: Input Voltage

Zin	-738.418 + 125.718 j

Table 8: Input impedance in Ohm

Zo	22.5223 + 0.359649 j
Zo(arg)	22.5252

Table 9: Output impedance in Ohm

Cost	1225.6
merit	716.238

Table 10: Cost and Figure of merit

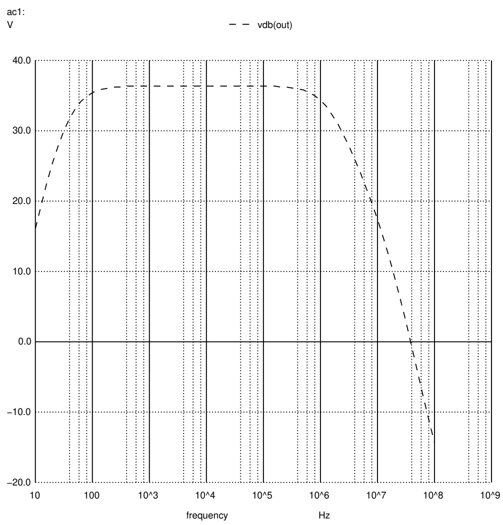

Figure 6: Output voltage

4 Comparison

In this section, a global comparison between Octave and Ngspice results will be made. Firstly, one should bear in mind that, in the previous sections, an Operating Point Analysis was performed to find the necessary values for the Incremental Analysis. Therefore, in the table below, the voltages in the collector, base and emitter of the transistor are presented as well as the currents in each terminal (I_B, I_C, I_E).

Calculus	Value [A or V]
@cb[i]	0.000000e+00
@ci[i]	0.000000e+00
@cout[i]	0.000000e+00
@q1[ib]	2.132105e-05
@q1[ic]	3.676881e-03
@q1[ie]	-3.69820e-03
@q1[is]	1.945288e-12
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@rc[i]	3.350773e-03
@re[i]	3.698202e-03
@rin[i]	0.000000e+00
@rl[i]	0.000000e+00
@rout[i]	-4.63546e-02
base	1.052144e+00
coll	1.947680e+00
emit	3.698202e-01
emit2	2.729077e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
vbe	6.823234e-01
vcc	1.200000e+01
vce	1.577860e+00
veb	7.813967e-01
vec	2.729077e+00

Table 11: Operating point using DC model. Variables are expressed in Ampere or Volt. (Ngspice)

Name	Value [A or V]
IB1	1.975467e-05
IC1	3.530160e-03
IE1	3.549915e-03
VColl	1.409519e+00
VBase	1.090909e+00
VEmit	3.549915e-01

Table 12: Operating point using DC model. Variables are expressed in Ampere or Volt.(Octave)

In the Ngspice table, the only parameters in comparison are $@q1[ib]$, $@q1[ic]$, $@q1[ie]$, $base$, $coll$ and $emit$.

As one may observe, some discrepancies in the voltage values are noticeable. Nevertheless, the values of the currents flowing are are within reasonable intervals of similarity. Therefore, the gain computed in Octave should not be severely affected by this. It is important to highlight that the theoretical gain expression is dependent on the value of the current I_C because of the incremental parameter g_m.

Aditionally, the gain, bandwidth and cut off frequency results were also computed. As predicted, the voltage gain in the theoretical approach is greater than in the Ngspice computation. Moreover, since we do not have the theoretical high cut frequency, we can only compare the results for the low cut frequency, which are very

Calculus	Value
V Gain	36.3869
Bandwidth	1.27868E+06
Lower Cut Off Freq	53.0031

Table 13: Gain, bandwidth and cut off frequency. (Ngspice)

Name	Value
Total Gain (AV)	3.035752e+02 V
Bandwidth	1.348349e+06 Hz
Lower Cut Off Frequency	5.094138e+01 Hz

Table 14: Gain, bandwidth and cut off frequency. (Octave)

similar as far as the order of magnitude is concerned.. For this reason, as the bandwidth is the subtraction between high and low cut frequencies, it should not be compared.

5 Conclusion

As discussed in the introduction, the main goal of this assignment was to project an audio amplifier that allowed maximum voltage gain, spending the less possible on the components used. As so, both theorical analysis and simulation analyses were conducted.

Despite strong efforts to match the results obtained in the different analysis, it was concluded that, due to the non-linearity of the components of the circuit, particularly the transistors, it was impossible to obtain the exact same quality using both tools. In fact, the complexity of the parameters of the transistors used in ngspice is believed to be the main reason for this outcome.

Nevertheless, once the ngspice model is the most similiar to reality, the the model used can then be validated, dispate the discrepancies already explained.