

74VHC373

Octal D-Type Latch with 3-STATE Outputs

General Description

The VHC373 is an advanced high speed CMOS octal D-type latch with 3-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input (OE). The latches appear transparent to data when latch enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is LATCHED. When the OE input is HIGH, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

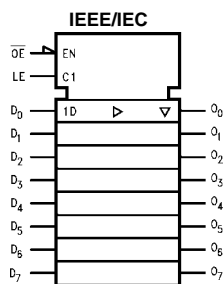
- High Speed: $t_{PD} = 5.0 \text{ ns (typ) @ } V_{CC} = 5V$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (Min)}$
- Power Down Protection is provided on all inputs
- Low Noise: $V_{OLP} = 0.6V \text{ (typ)}$
- Low Power Dissipation: $I_{CC} = 4 \mu A \text{ (Max) @ } T_A = 25^\circ C$
- Pin and Function Compatible with 74HC373

Ordering Code:

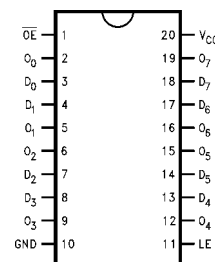
Order Number	Package Number	Package Description
74VHC373M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC373SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ –D ₇	Data Inputs
LE	Latch Enable Input
\overline{OE}	Output Enable Input
O ₀ –O ₇	3-STATE Outputs

Truth Table

Inputs			Outputs
LE	\overline{OE}	D _n	O _n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O ₀

H = HIGH Voltage Level

L = LOW Voltage Level

Z = High Impedance

X = Immaterial

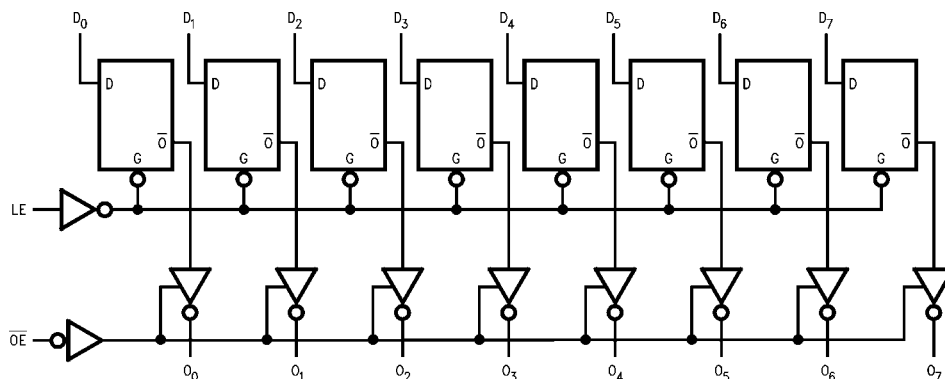
O₀ = Previous O₀ before HIGH-to-LOW transition of Latch Enable

Functional Description

The VHC373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW tran-

sition of LE. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to + 7.0V
DC Input Voltage (V_{IN})	-0.5V to + 7.0V
DC Output Voltage (V_{OUT})	-0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	-20 mA
Output Diode Current	± 20 mA
DC Output Current (I_{OUT})	± 25 mA
DC V_{CC} /GND Current (I_{CC})	± 75 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to + 5.5V
Input Voltage (V_{IN})	0V to + 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 3.3V \pm 0.3V$	0 ~ 100 ns/V
$V_{CC} = 5.0 \pm 0.5V$	0 ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V _{IH}	HIGH Level Input Voltage	2.0 3.0 – 5.5	1.50 0.7 V _{CC}			1.50 0.7 V _{CC}		V		
V _{IL}	LOW Level Input Voltage	2.0 3.0 – 5.5			0.50 0.3 V _{CC}	0.50 0.3 V _{CC}		V		
V _{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA
		3.0	2.9	3.0		2.9				I _{OH} = -4 mA
		4.5	4.4	4.5		4.4		V		I _{OH} = -8 mA
		3.0	2.58			2.48				I _{OL} = 50 μA
V _{OL}	LOW Level Output Voltage	4.5	3.94			3.80		V	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA
		2.0		0.0	0.1		0.1			V
		3.0		0.0	0.1		0.1	V		
		4.5			0.36		0.44			
I _{OZ}	3-STATE Output Off-State Current	5.5			±0.25	±2.5	μA	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		
I _{IN}	Input Leakage Current	0 – 5.5			±0.1	±1.0	μA	V _{IN} = 5.5 or GND		
I _{CC}	Quiescent Supply Current	5.5			4.0	40.0	μA	V _{IN} = V _{CC} or GND		

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.6	0.9	V	$C_L = 50 \text{ pF}$
V_{OLV} (Note 3)	Quiet Output Minimum Dynamic V_{OL}	5.0	-0.6	-0.9	V	$C_L = 50 \text{ pF}$
V_{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50 \text{ pF}$
V_{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50 \text{ pF}$

Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
t _{PLH}	Propagation Delay Time (LE to O _n)	3.3 ± 0.3		7.0	11.0	1.0	13.0	ns		C _L = 15 pF
t _{PHL}				9.5	14.5	1.0	16.5			C _L = 50 pF
		5.0 ± 0.5		4.9	7.2	1.0	8.5	ns		C _L = 15 pF
				6.4	9.2	1.0	10.5			C _L = 50 pF
t _{PLH}	Propagation Delay Time (D to O _n)	3.3 ± 0.3		7.3	11.4	1.0	13.5	ns		C _L = 15 pF
t _{PHL}				9.8	14.9	1.0	17.0			C _L = 50 pF
		5.0 ± 0.5		5.0	7.2	1.0	8.5			C _L = 15 pF
				6.5	9.2	1.0	10.5			C _L = 50 pF
t _{PZL}	3-STATE Output Enable Time	3.3 ± 0.3		7.3	11.4	1.0	13.5	ns	R _L = 1 kΩ	C _L = 15 pF
t _{PZH}				9.8	14.9	1.0	17.0			C _L = 50 pF
		5.0 ± 0.5		5.5	8.1	1.0	9.5	ns		C _L = 15 pF
				7.0	10.1	1.0	11.5			C _L = 50 pF
t _{PLZ}	3-STATE Output	3.3 ± 0.3		9.5	13.2	1.0	15.0	ns	R _L = 1 kΩ	C _L = 50 pF
t _{PHZ}	Disable Time	5.0 ± 0.5		6.5	9.2	1.0	10.5			C _L = 50 pF
t _{OSLH}	Output to	3.3 ± 0.3			1.5		1.5	ns	(Note 4)	C _L = 50 pF
t _{OSHL}	Output Skew	5.0 ± 0.5			1.0		1.0			C _L = 50 pF
C _{IN}	Input Capacitance			4	10		10	pF	V _{CC} = Open	
C _{OUT}	Output Capacitance			6				pF	V _{CC} = 5.0V	
C _{PD}	Power Dissipation Capacitance			27				pF	(Note 5)	

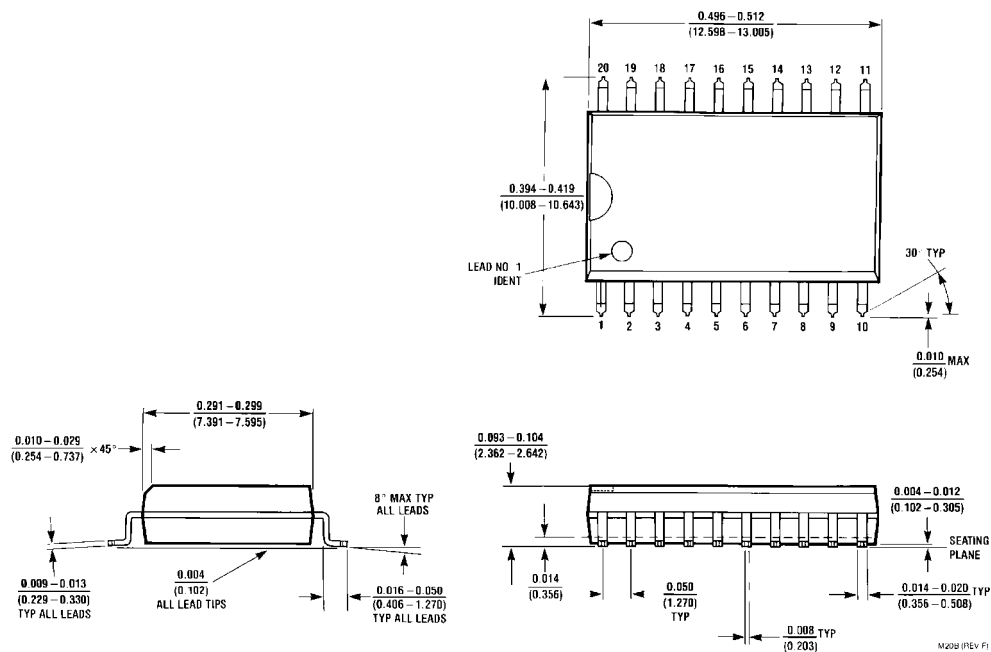
Note 4: Parameter guaranteed by design. t_{OSLH} = |t_{PLH max} - t_{PLH min}|; t_{OSHL} = |t_{PHL max} - t_{PHL min}|

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC (opr.)} = C_{PD} • V_{CC} • f_{IN} + I_{CC}/8 (per Latch). The total C_{PD} when n pcs. of the Latch operates can be calculated by the equation: C_{PD(total)} = 14 + 13n.

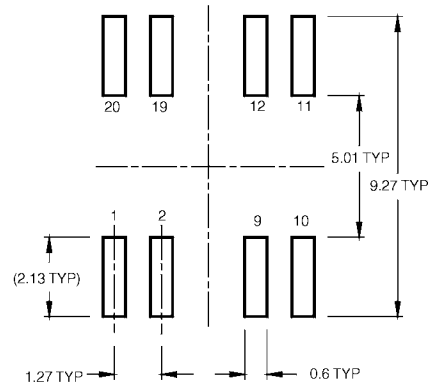
AC Operating Requirements

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units
			Min	Typ	Max	Min	Max	
t _{W(H)}	Minimum Pulse Width (LE)	3.3 ± 0.3	5.0			5.0		ns
		5.0 ± 0.5	5.0			5.0		
t _S	Minimum Set-Up Time	3.3 ± 0.3	4.0			4.0		ns
		5.0 ± 0.5	4.0			4.0		
t _H	Minimum Hold Time	3.3 ± 0.3	1.0			1.0		ns
		5.0 ± 0.5	1.0			1.0		

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B



Technical drawing of a 12-pin D-sub connector. The drawing includes front and side views with the following dimensions and tolerances:

- ALL LEAD TIPS**: Indicated by a symbol with a tolerance of 0.1 and a material specification C .
- 2.1 MAX.**: Dimension for the overall height of the connector.
- 1.8±0.1**: Dimension for the height of the lead tips.
- 0.15±0.05**: Dimension for the thickness of the lead tips.
- 0.35-0.51**: Dimension for the width of the lead tips.
- 1.27 TYP**: Dimension for the pitch between pins.
- C-**: Dimension for the width of the connector body.
- Symbol**: A circular symbol with a crosshair, indicating a specific feature or tolerance.
- 0.12**: Dimension for the width of the lead tips.
- M**: Material specification for the lead tips.
- C**: Material specification for the connector body.
- A**: Material specification for the lead tips.

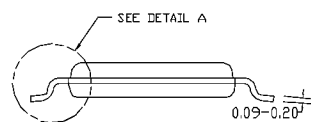
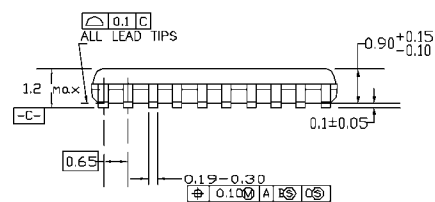
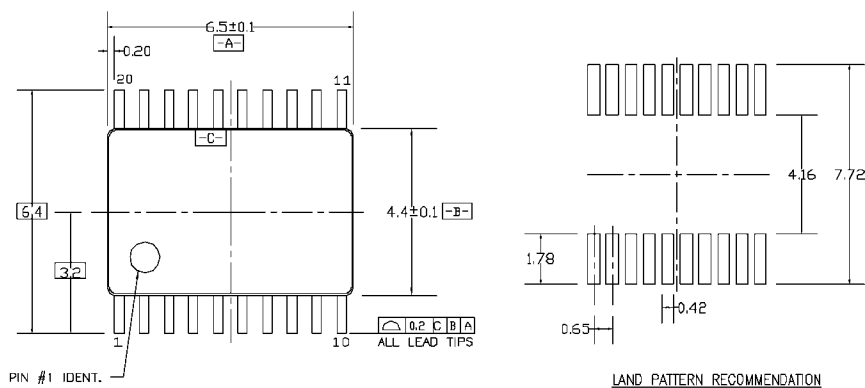
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

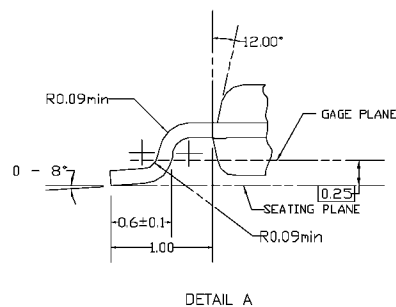
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

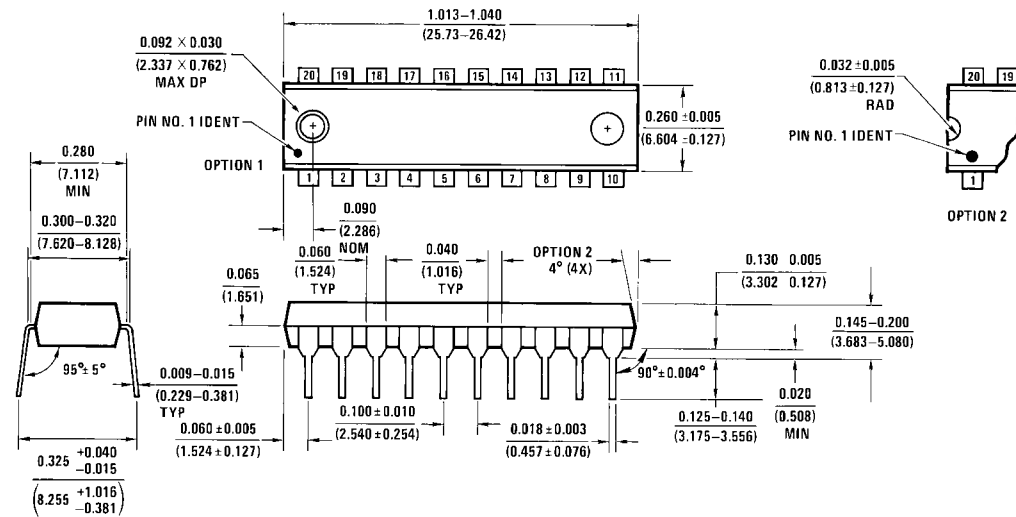
- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



MTC20REVD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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