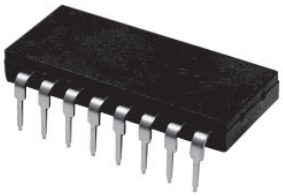
ADNS-2030
Low Power Optical Mouse Sensor

AVAGO TECHNOLOGIES

Data Sheet



Description
The ADNS-2030 is a low-power optical mouse sensor used to implement a non-mechanical tracking engine for computer mice. With a 3.3V power supply and power-saving sleep functions, this sensor is particularly suited to cordless mouse applications.

It is based on optical navigation technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The sensor is housed in a 16-pin staggered dual inline package (DIP) that is designed for use with the HDNS-2100 Lens and HDNS-2200 Clip and HLMP-ED800-xx000 (639 nm LED illuminator source). There are no moving parts, and precision optical alignment is not required, facilitating high volume assembly.

The output format is two channel quadrature (X and Y direction) which emulates encoder photo-transistors. The current X and Y information are also available in registers accessed via a serial port.

Default resolution is specified as 400 counts per inch, with rates of motion up to 14 inches per second. Resolution can also be programmed to 800 cpi.

The part is programmed via a two wire serial port, through registers.

Theory of Operation
The ADNS-2030 is based on Optical Navigation Technology. It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP) and a two channel quadrature output, and a two wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system provided by the HDNS-2100, 2200, and HLMP-ED800-xx000. These images are processed by the DSP to determine the direction and distance of motion. The DSP generates the Δx and Δy relative displacement values that are converted to two channel quadrature signals.

Features
- Precise optical navigation technology
- No mechanical moving parts
- Complete 2D motion sensor
- Serial interface and/or quadrature interface
- Smooth surface navigation
- Programmable frame speed up to 2300 frames per sec (fps)
- Accurate motion up to 14 ips
- 800 cpi resolution
- High reliability
- High speed motion detector
- Wave solderable
- Single 3.3 volt power supply
- Shutdown pin for USB suspend mode operation
- Power conservation mode during times of no movement
- On chip LED drive with regulated current
- Serial port registers
  - Programming
  - Data transfer
- 16-pin staggered dual inline package (DIP)

Applications
- Cordless optical mice
- Mice for desktop PCs, workstations, and portable PCs
- Trackballs
- Integrated input devices

Pinout of ADNS-2030 Optical Mouse Sensor

Pin Number	Pin	Description
1	SCLK	Serial port clock (input)
2	XA	XA quadrature output
3	XB	XB quadrature output
4	YB	YB quadrature output
5	YA	YA quadrature output
6	XY_LED	LED control
7	REFA	Internal reference
8	REFB	Internal reference
9	OSC_IN	Oscillator input
10	GND	System ground
11	OSC_OUT	Oscillator output
12	GND	System Ground
13	V_{DD}	3.3 volt power supply
14	R_BIN	LED current bin resistor
15	PD	Power Down Pin, active high
16	SDIO	Serial data (input and output)

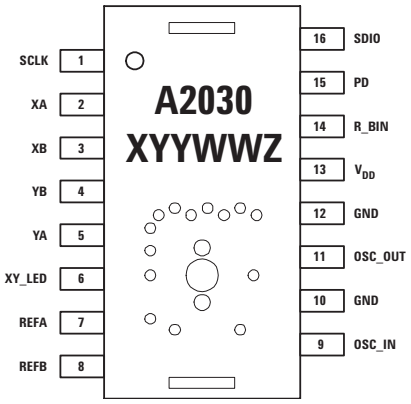


Figure 1. Top view.

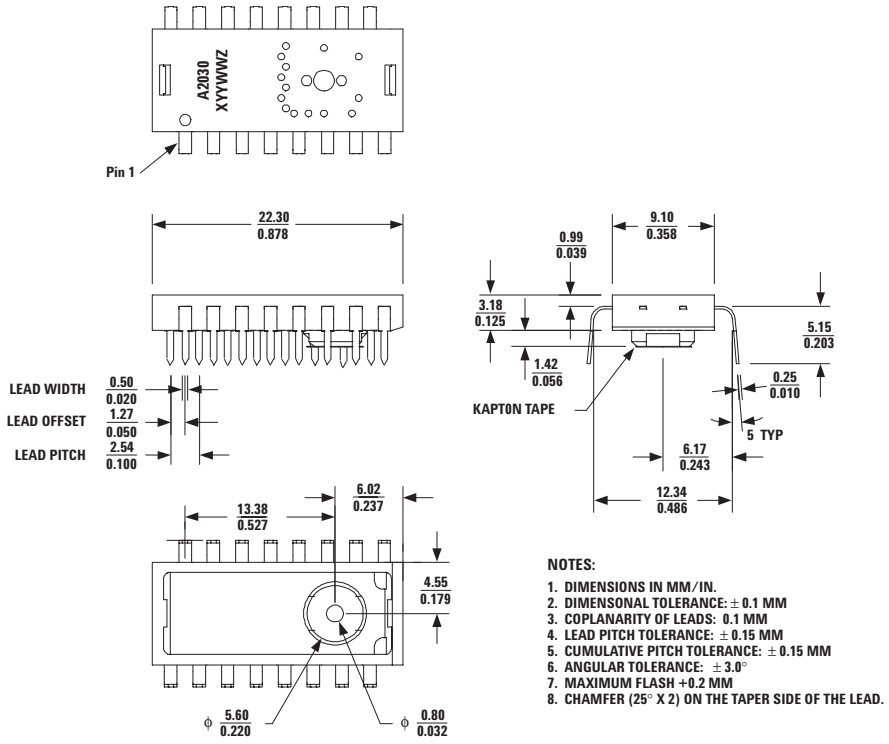


Figure 2. Package outline drawing of ADNS-2030 optical mouse sensor.

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Overview of Optical Mouse Sensor Assembly

2D Assembly Drawing of ADNS-2030

Figures 3 and 4, shown with HDNS-2100, HDNS-2200 and HLMP-ED800-xx000.

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment

These components interlock as they are mounted onto defined features on the base plate.

The ADNS-2030 sensor is designed for mounting on a through hole PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The HDNS-2100 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor, base plate, and clip with the LED. The lens also has a large round flange to provide a long creepage path for any ESD events that occur at the opening of the base plate.

The HDNS-2200 clip holds the LED in relation to the lens. The LED must be inserted into the clip and the LED's leads formed prior to loading on the PCB. The clip interlocks the sensor to the lens, and through the lens to the alignment features on the base plate.

The HLMP-ED800-xx000 LED is recommended for illumination. If used with the bin table, sufficient illumination can be guaranteed.

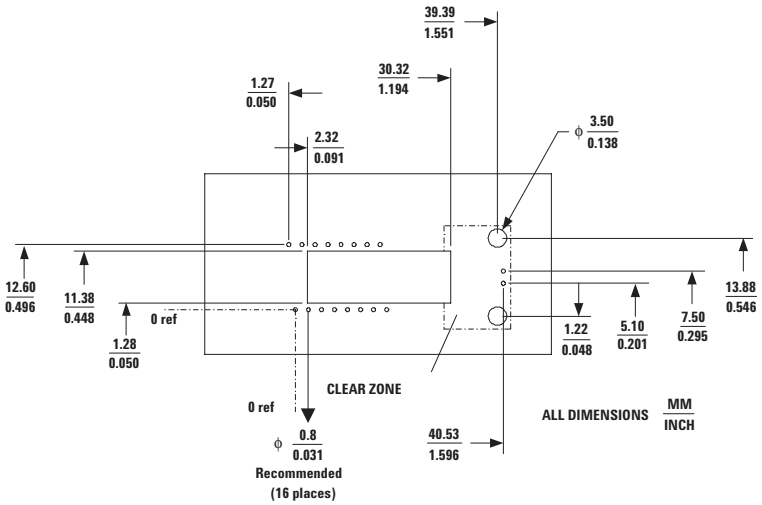


Figure 3. Recommended PCB mechanical cutouts and spacing (top view).

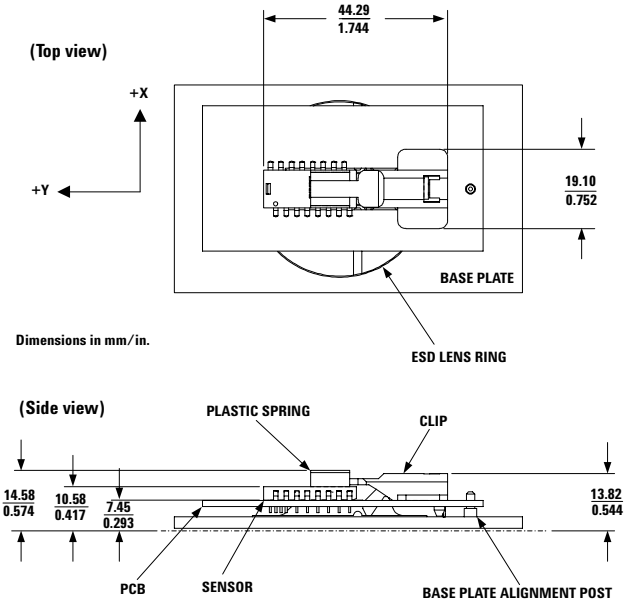


Figure 4. 2D assembly drawing of ADNS-2030 (top and side view).

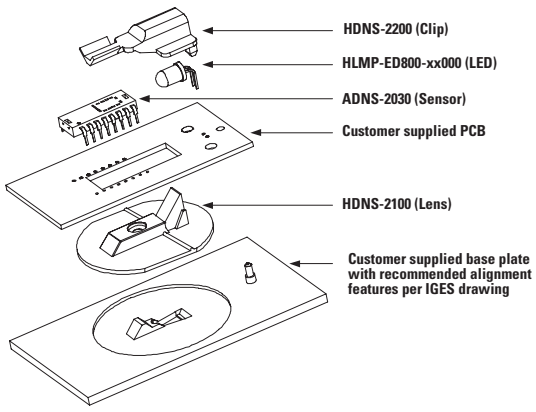


Figure 5. Exploded view drawing.

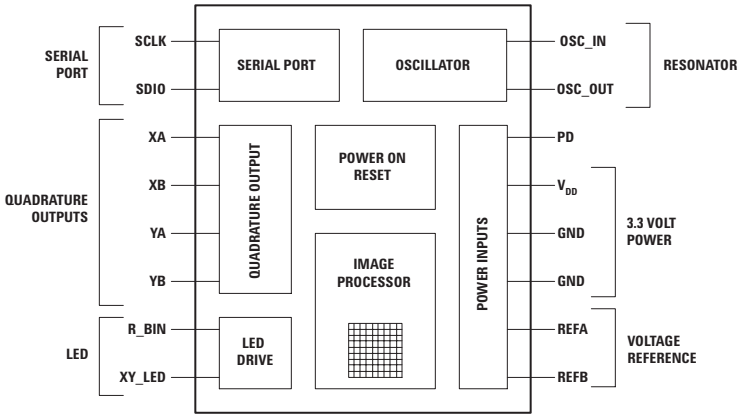


Figure 6. Block diagram of ADNS-2030 optical mouse sensor.

PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB.
2. Bend the LED leads 90° and then insert the LED into the assembly clip until the snap feature locks the LED base.
3. Insert the LED/clip assembly into PCB.
4. Wave Solder the entire assembly in a no-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact. The solder fixture is also used to set the reference height of the sensor to the PCB top during wave soldering (Note: DO NOT remove the kapton tape during wave soldering).
5. Place the lens onto the base plate.
6. Remove the protective kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. It is recommended not to place the PCB facing up during the entire mouse assembly process. The PCB should be held vertically during the kapton removal process.
7. Insert PCB assembly over the lens onto the base plate aligning post. The sensor aperture ring should self-align to the lens.
8. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
9. Install mouse top case. There must be a feature in the top case to press down onto the clip to ensure all components are interlocked to the correct vertical height.

Design Considerations for Improving ESD Performance

The flange on the lens has been designed to increase the creepage and clearance distance for electrostatic discharge. The table below shows typical values assuming base plate construction per the Avago supplied IGES file and HDNS-2100 lens flange.

Typical Distance	Millimeters
Creepage	16.0
Clearance	2.1

For improved ESD performance, the lens flange can be sealed (i.e. glued) to the base plate. Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should **NOT** be used.

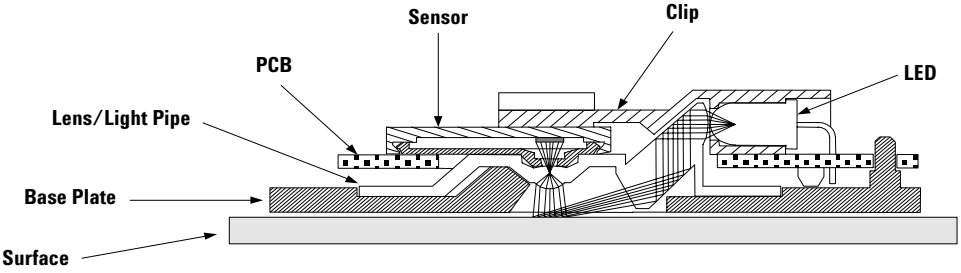
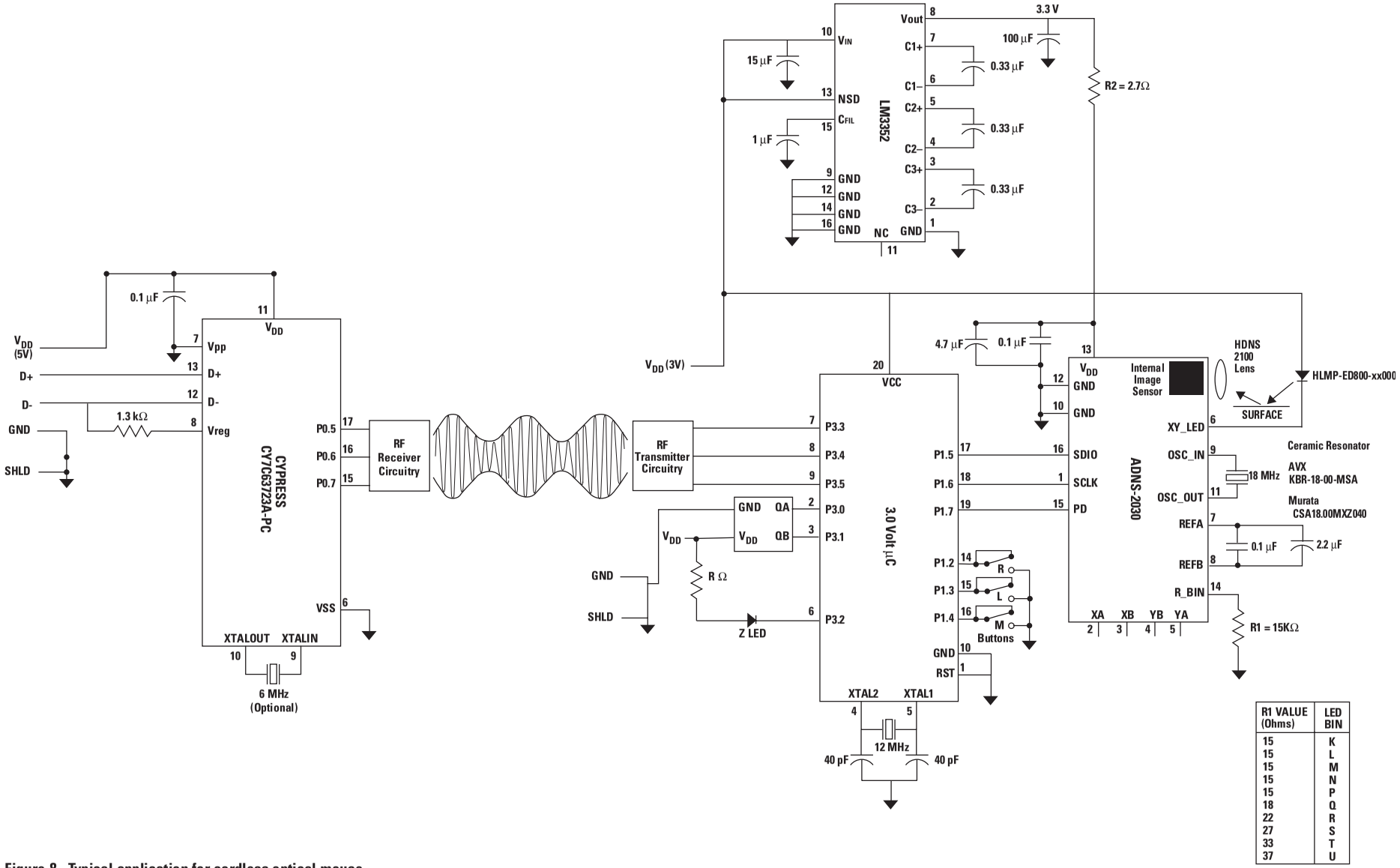


Figure 7. PCB assembly.

Recommended Typical Application (Receiver side)

Recommended Typical Application (Transmitter side)



R1 VALUE (Ohms)	LED BIN
15	K
15	L
15	M
15	N
15	P
18	Q
22	R
27	S
33	T
37	U

Figure 8. Typical application for cordless optical mouse.

Notes on Bypass Capacitors

- Caps for pins 7, 8 and 12, 13 *MUST* have trace lengths *LESS* than 5 mm.
- The 0.1 µF caps must be ceramic.
- Caps should have less than 5 nH of self inductance.
- Caps should have less than 0.2Ω of ESR.
- Surface mount parts are recommended.

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with unshielded cable and following Avago recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with unshielded cable and following Avago recommendations.
- UL flammability level UL94 V-0.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15kV when assembled into a mouse according to usage instructions above.
- For eye safety consideration, please refer to the document, Eye Safety Calculation AN1228 available on the web site, http://www.Avago.com/view/opticalnavigation.
- The 15.0 kΩ resistor is determined by the absolute maximum rating of 50 mA for the HLMP-ED800-xx000. The other resistor values for brighter bins will guarantee sufficient intensity with reduced power.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_A	-15	55	°C	
Lead Solder Temp			260	°C	For 10 seconds, 1.6 mm below seating plane
Supply Voltage	V_{DD}	-0.5	3.6	V	
ESD			2	KV	All pins, human body model MIL 883 Method 3015
Input Voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	All I/O pins

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	Volts	
Power Supply Rise Time	V_{RT}			100	ms	
Supply Noise	V_N			30	mV	Peak to peak @27 MHz bandwidth
Clock Frequency	f_{CLK}	17.4	18.0	18.7	MHz	Set by ceramic resonator
Serial Port Clock Frequency	SCLK			$f_{CLK}/4$	MHz	
Resonator Impedance	X_{RES}			55	Ω	
Distance from Lens Reference Plane to Surface	Z	2.3	2.4	2.5	mm	Results in ±0.2 mm DOF (See Figure 9.)
Speed	S	0		14	in/sec	@ frame rate = 1500 fps
Acceleration	A			0.15	g	@ frame rate = 1500 fps
Light Level onto IC	IRR_{INC}	80 100		25,000 30,000	mW/m^2	λ = 639 nm λ = 875 nm
SDIO Read Hold Time	t_{HOLD}	100			µs	Hold time for valid data (Refer to Figure 27.)
SDIO Serial Write-write Time	t_{SWW}	100			µs	Time between two write commands (Refer to Figure 30.)
SDIO Serial Write-read Time	t_{SWR}	100			µs	Time between write and read operation (Refer to Figure 31.)
SDIO Serial Read-write Time	t_{SRW}	120			ns	Time between read and write operation (Refer to Figure 32.)
SDIO Serial Read-read Time	t_{SRR}	120			ns	Time between two read commands (Refer to Figure 32.)
Data Delay after PD ↓	$t_{COMPUTE}$	3.2			ms	After $t_{COMPUTE}$, all registers contain data from first image after PD ↓. Note that an additional 75 frames for AGC stabilization may be required if mouse movement occurred while PD was high. (Refer to Figure 11.)
SDIO Write Setup Time	t_{SETUP}	60			ns	Data valid time before the rising of SCLK (Refer to Figure 25.)
PD Pulse Width (to power down the chip)	t_{PDW}	700			µs	Pulse width to initiate the power down cycle @1500 fps (Refer to Figure 13.)
PD Pulse Width (to reset the serial port)	t_{PD}	100			µs	Pulse width to reset the serial port @1500 fps (but may also initiate a power down cycle) (Refer to Figure 11.)
Frame Rate	FR		1500		frames/s	See Frame_Period register section
Bin Resistor	R1	15K	15K	37K	Ω	Refer to Figure 8

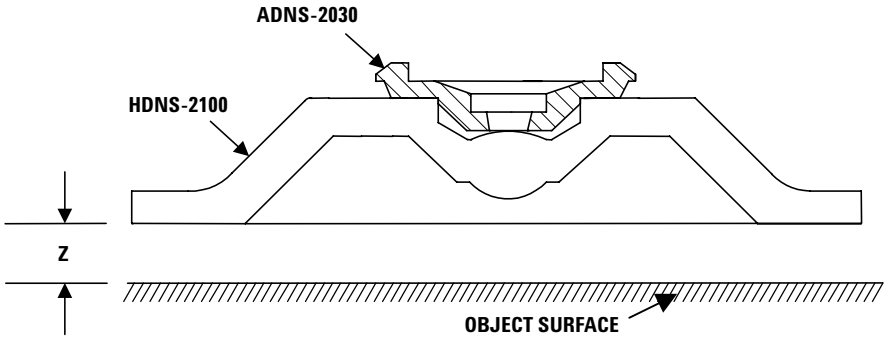


Figure 9. Distance from lens reference plane to surface.

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 3.3 V, 18 MHz, 1500 fps.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Power Down	t_{PD}		700		µs	From PD ↑ Time uncertainty due to firmware delay (Refer to Figure 11).
Power Up from PD ↓	t_{PUPD}			50	ms	From PD ↓ to valid quad signals 705 µsec + 75 frames (Refer to Figure 11).
Power Up from V_{DD} ↑	t_{PU}			30	ms	From V_{DD} ↑ to valid quad signals 705 µsec + 40 frames
Rise and Fall Times						
SDIO	t_r		15		ns	C_L = 30 pF (the rise time is between 10% to 90%)
	t_f		12		ns	C_L = 30 pF (the fall time is between 10% to 90%)
XA, XB, YA, YB	t_r		30		ns	C_L = 30 pF (the rise time is between 10% to 90%)
	t_f		22		ns	C_L = 30 pF (the fall time is between 10% to 90%)
ILED between	t_r		35		ns	With HLMP-ED800-xx000 LED (the rise time is 10% to 90%).
between	t_f		170		ns	With HLMP-ED800-xx000 LED (the fall time is 10% to 90%).
Serial Port Transaction Timer	t_{SPTT}	0.7	0.9	1.0	s	Serial port will reset if current transaction is not complete within t_{SPTT} (Refer to Figure 35).
Transient Supply Current	I_{DDT}		18	37	mA	Max supply current during a V_{DD} ramp from 0 to 3.3V with > 500 ms rise time. Does not include charging current for bypass capacitors.

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 3.3 V, 18 MHz.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
DC Supply Current (mouse moving)	$I_{DD\ AVG}$		13	23	mA	No load on XA, XB, YA, YB, SCLK, SDIO. Excluding LED current.
Peak Supply Current (mouse moving)	$I_{DD\ PEAK}$		18		mA	No load on XA, XB, YA, YB, SCLK, SDIO. Excluding LED current.
DC Supply Current (mouse not moving)	I_{DD}		10	23	mA	No load on XA, XB, YA, YB, SCLK, SDIO. Excluding LED current.
DC Supply Current (Power Down)	I_{DDPD}		4	30	µA	PD = V_{DD}, SCLK, SDIO = GND or V_{DD}
SCLK, SDIO, PD						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	0.65 * V_{DD}			V	
Output Low Voltage	V_{OL}			0.45	V	@ I_{OL} = 2 mA (SDIO only)
Output High Voltage	V_{OH}	0.6 * V_{DD}			V	@ I_{OH} = 2 mA (SDIO only)
Output Low Voltage (XA, XB, YA, YB)	V_{OL}			0.6	V	@I_{OL} = 0.5 mA
Output High Voltage (XA, XB, YA, YB)	V_{OH}	0.6 * V_{DD}			V	@I_{OH} = 0.5 mA
Output Low Voltage (XY_LED)	V_{OL}			0.5	V	Refer to Figure 10.
XY LED Current	I_{LED}	Typ –20% Typ –15%	614/R1 614/R1	Typ +20% Typ +15%	A A	Recommended operating conditions @25°C, V_{DD} = 3.3 V (Refer to Figure 10 and table below).
XY LED Current (Fault Mode)	I_{LED}			1000	µA	R1 < 200Ω
Powerup XY LED Current	I_{LED}			500	µA	V_{DD} < 2.5 V

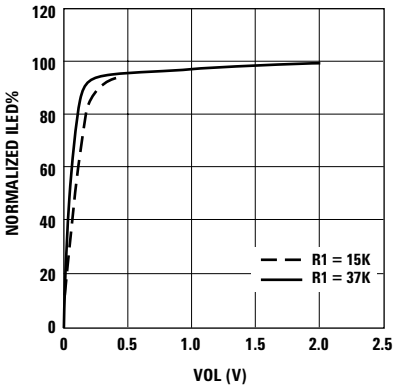


Figure 10. Typical I-V characteristic of ADNS-2030 XY_LED pin.

Typical LED Current Table

R1 value	kΩ	15	18	22	27	33	37
LED current (Typical)	mA	41	34	28	23	19	17

PD Pin Timing

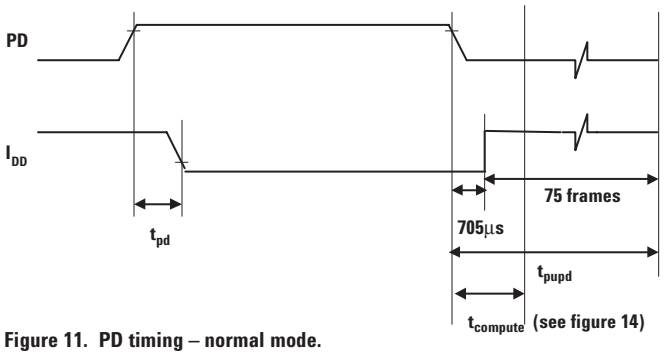


Figure 11. PD timing – normal mode.

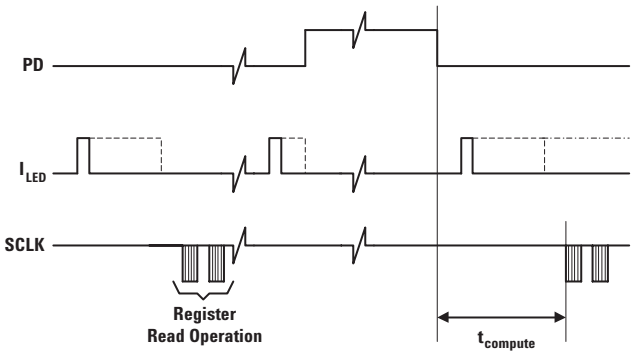


Figure 12. PD timing – sleep mode.

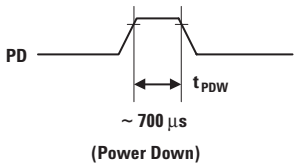


Figure 13. PD minimum pulse width.

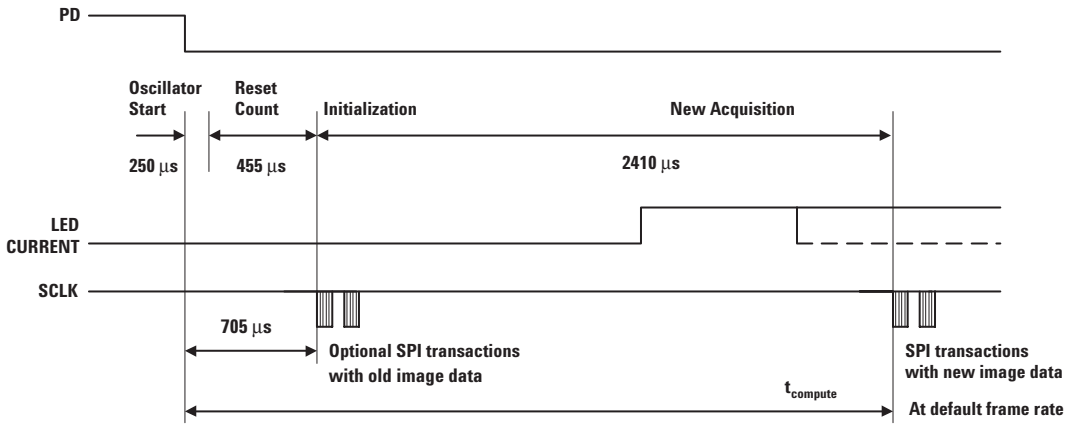


Figure 14. Detail of PD falling edge timing.

Quadrature Mode Timing

The output waveforms emulate the output from encoders. With the resolution set to 400 cpi, from one to five quadrature states can exist within one frame time. The minimum state time is 133 µs. If the resolution is 800 cpi, then up to ten quadrature states can exist within a frame time. If the motion within a frame is greater than these values, the extra motion will be reported in the next frame. The following diagrams (see Figures 15, 16 and 17) show the timing for positive X motion, to the right, or positive Y motion, up. If a power down via the PD pin occurs during a transfer, the transfer will resume after PD is de-asserted. The timing for that quadrature state will be increased by the length of the PD time.

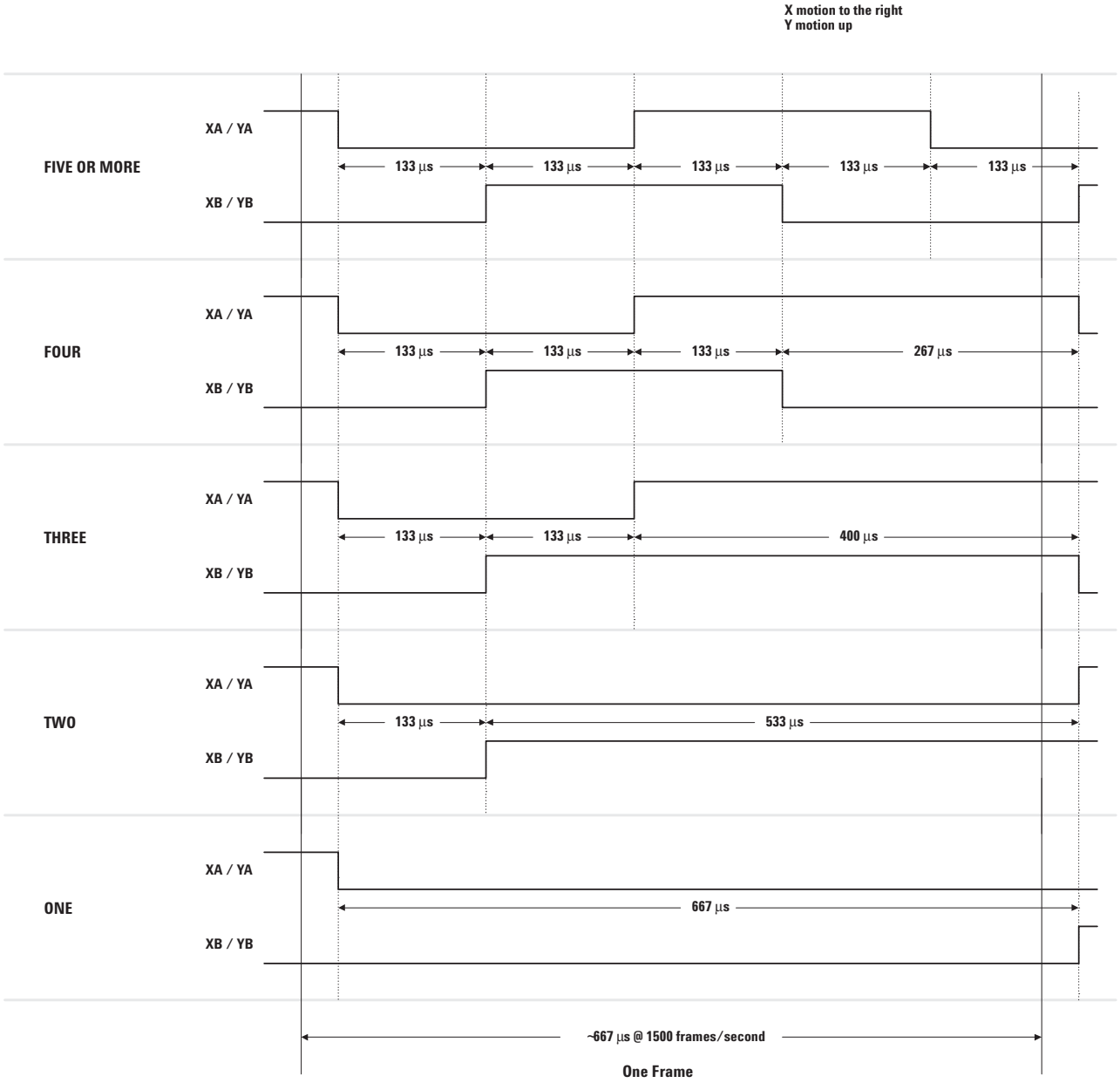


Figure 15. Quadrature states per frame (400 cpi mode).

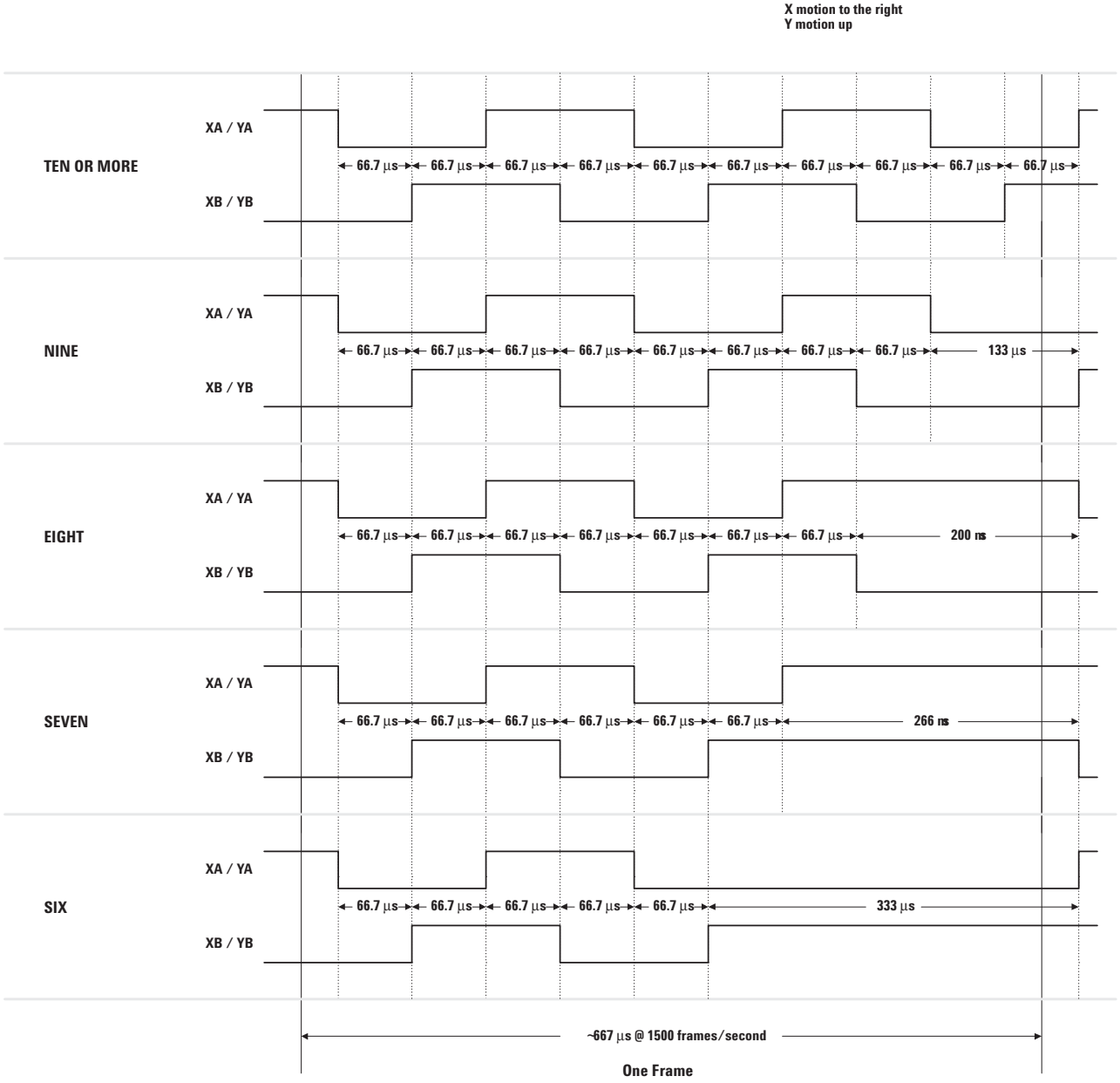


Figure 16. Quadrature states per frame (800 cpi mode).

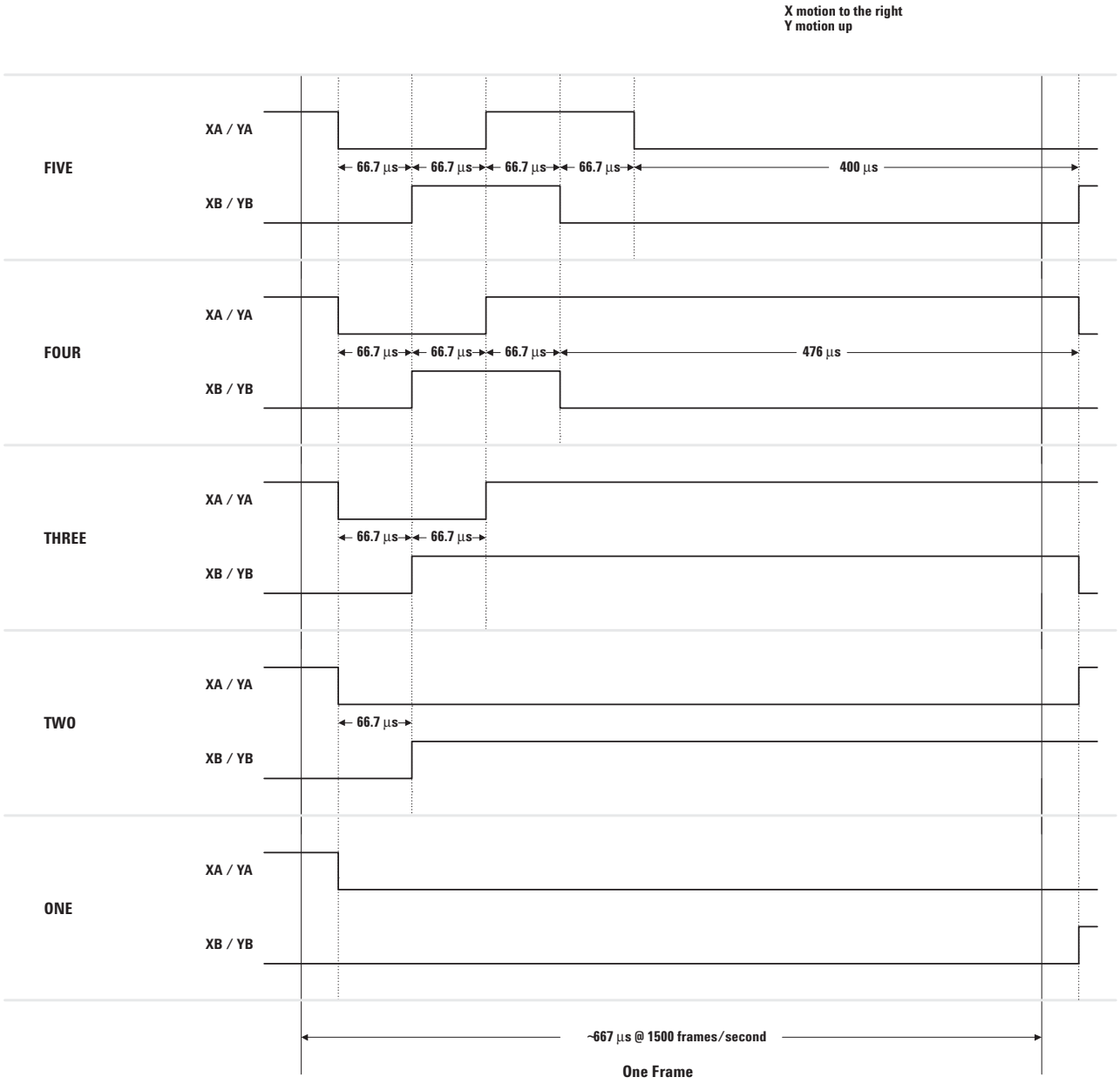
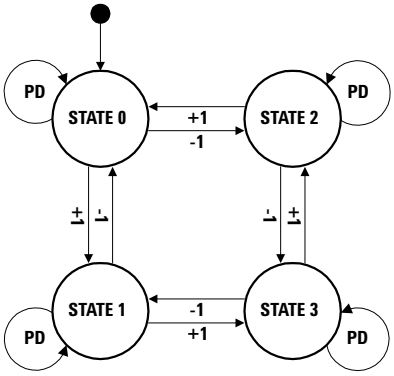


Figure 17. Quadrature states per frame (800 cpi mode).

Quadrature State Machine

The following state machine shows the states of the quadrature pins. The two things to note are that while the PD pin is asserted, the state machine is halted. Once PD is de-asserted, the state machine picks up from where it left off. State 0 is entered after a power up reset.



STATE	X and Y OUTPUT	
	A	B
0	0	0
1	0	1
2	1	0
3	1	1

Figure 18. Quadrature state machine.

Quadrature Output Waveform

The two channel quadrature outputs are 3.3 volt CMOS outputs. The Δx count is used to generate the XA and XB signals, and Δy count is used for the YA and YB signals.

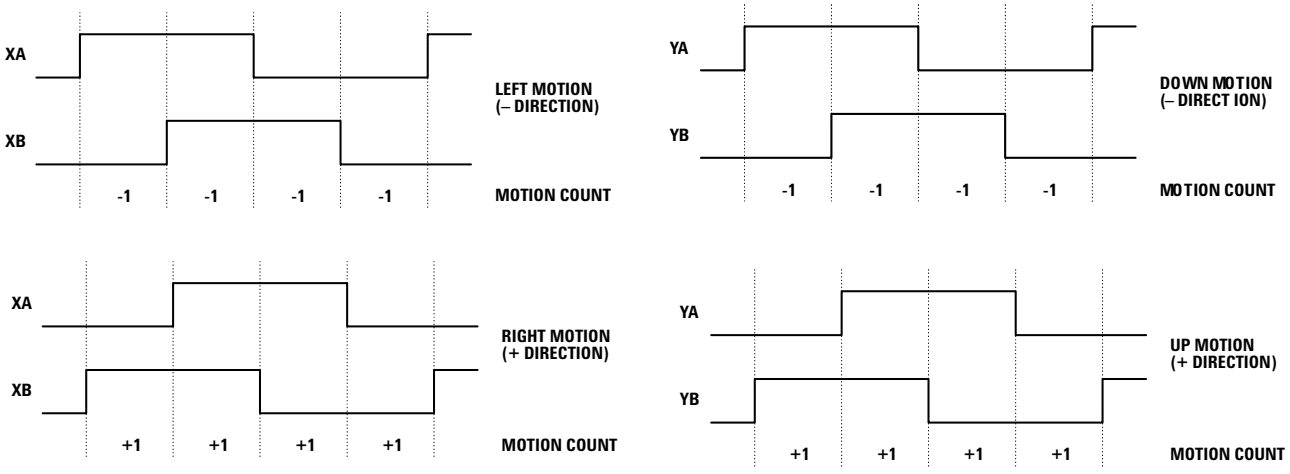


Figure 19. Quadrature output waveform.

Typical Performance Characteristics

Performance characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 3.3 V, 18 MHz.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Path Error (Deviation)	P_{Error}		0.5		%	Path Error (Deviation) is the error from the ideal cursor path. It is expressed as a percentage of total travel and is measured over standard surfaces.

The following graphs (Figs 20–23) are the typical performance of the ADNS-2030 sensor, assembled as shown in the 2D assembly drawing with the HDNS-2100 Lens/Prism, the HDNS-2200 clip, and the HLMP-ED800-xx000 LED (See Figure 5).

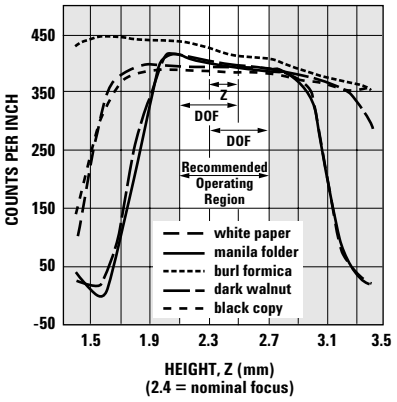


Figure 20. Typical Resolution vs. Height, Z. (Comparative Surfaces)

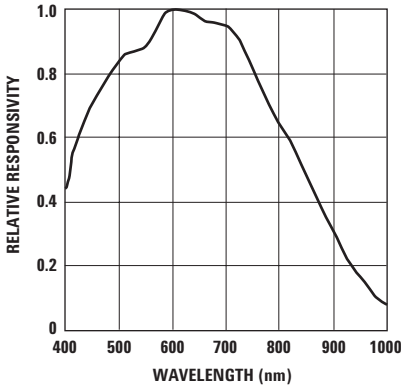


Figure 16. Wavelength Responsivity[1].

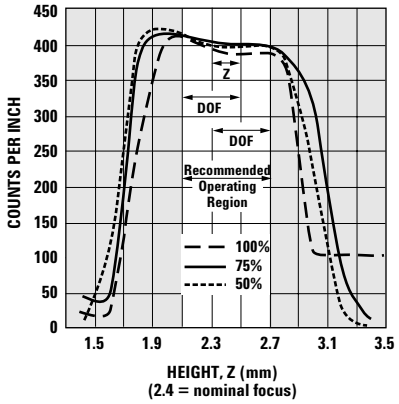


Figure 22. Typical Resolution vs. Height, Z. (Manila folder and LED variation)[2,3]

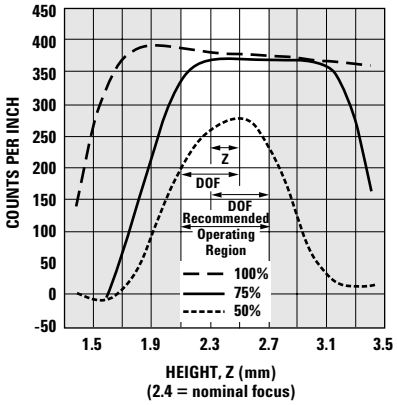


Figure 23. Typical Resolution vs. Height, Z. (Black copy and LED variation)[2,3]

Notes :

1. The ADNS-2030 is designed for optimal performance when used with the HLMP-ED800-xx000 (Red LED 639nm). For use with other LED colors (ie. blue, green), please consult factory. When using alternate LED's there may also be performance degradation and additional eye safety consideration.
2. Z = Distance from Lens Reference Plane to Surface.
3. DOF = Depth of Field

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-2030, and can be used to read out the motion information instead of the quadrature data pins.

The port is a two wire, half duplex port. The host microcontroller always initiates communication; the ADNS-2030 never initiates data transfers.

SCLK: The serial port clock. It is always generated by the master (the microcontroller).

SDIO: The data line.

PD: A third line is sometimes involved. PD (Power Down) is usually used to place the ADNS-2030 in a low power mode. PD can also be used to force re-synchronization between the microcontroller and the ADNS-2030 in case of an error.

Write Operation

A write operation, which means that data is going from the microcontroller to the ADNS-2030, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The transfer is synchronized by **SCLK**. The microcontroller changes **SDIO** on falling edges of **SCLK**. The ADNS-2030 reads **SDIO** on rising edges of **SCLK.**

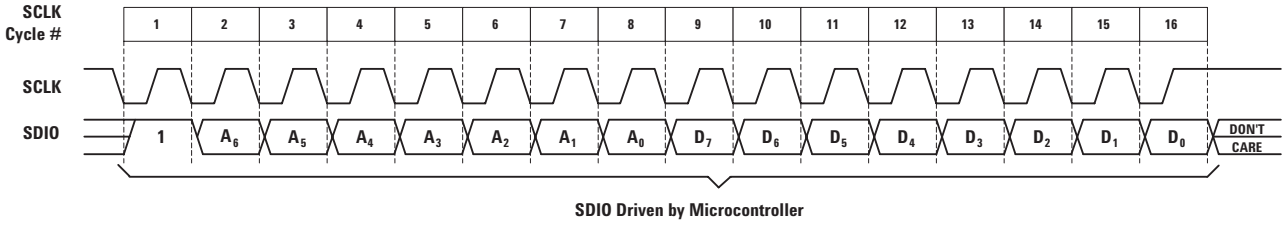


Figure 24 . Write operation.

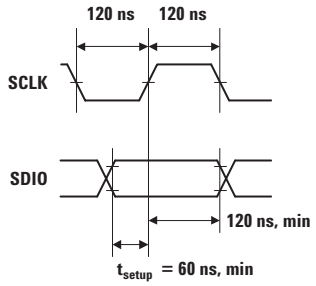


Figure 25. SDIO setup and hold times SCLK pulse width.

Read Operation

A read operation, which means that data is going from the ADNS-2030 to the microcontroller, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address, is written by the microcontroller, and has a “0” as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-2030. The transfer is synchronized by **SCLK**. **SDIO** is changed on falling edges of **SCLK** and read on every rising edge of **SCLK**. The microcontroller must go to a high Z state after the last address data bit. The ADNS-2030 will go to the high Z state after the last data bit. (see detail “B” in Figure 29). One other thing to note during a read operation is that SCLK will need to be delayed after the last address data bit to ensure that the ADNS-2030 has at least 100 µs to prepare the requested data. This is shown in the timing diagrams below.

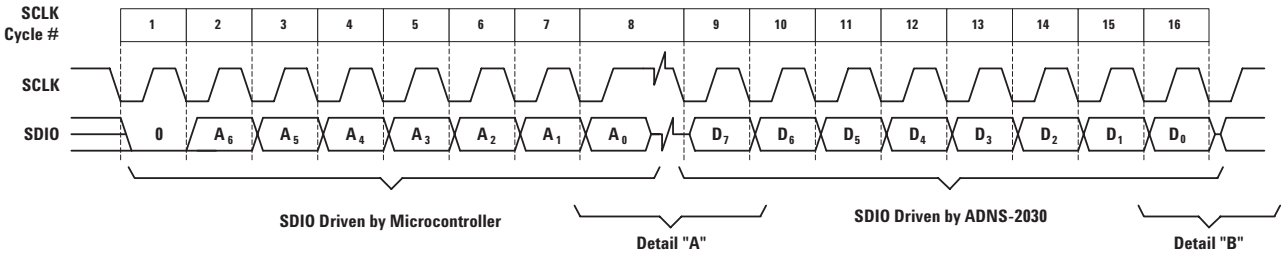


Figure 26. Read operation.

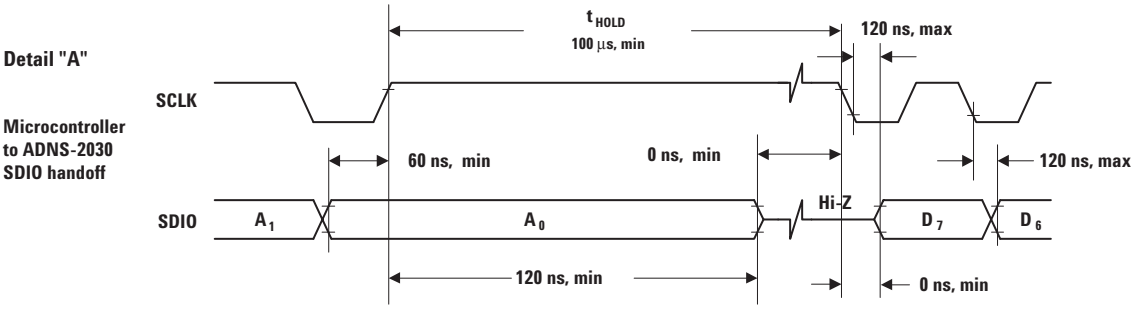


Figure 27. Microcontroller to ADNS-2030 SDIO handoff.

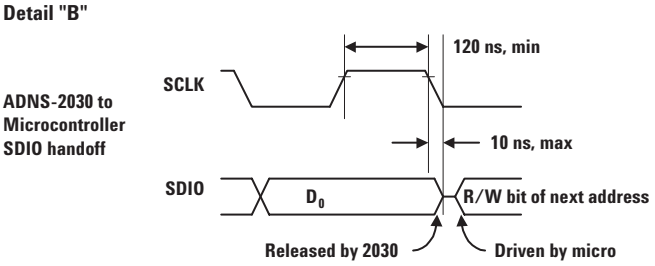


Figure 28. ADNS-2030 to microcontroller SDIO handoff.

NOTE: The 120 ns high state of SCLK is the minimum data hold time of the ADNS-2030. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-2030 will hold the state of D_0 on the SDIO line until the falling edge of SCLK. In both write and read operations, SCLK is driven by the microcontroller.

Serial port communications is not allowed while PD (Power Down) is high. See “Error Detection and Recovery” regarding re-synchronizing via PD.

Forcing the SDIO Line to the Hi-Z State

There are times when the SDIO line from the ADNS-2030 should be in the Hi-Z state. If the microprocessor has completed a write to the ADNS-2030, the SDIO line is Hi-Z, since the SDIO pin is still configured as an input. However, if the last operation from the microprocessor was a read, the ADNS-2030 will hold the D0 state on SDIO until a falling edge of SCLK.

To place the SDIO pin into the Hi-Z state, first raise the PD pin for 100 µs (min). The PD pin can stay high, with the ADNS-2030 in the shutdown state, or the PD pin can be lowered, returning the ADNS-2030 to normal operation. In either case, the SDIO line will now be in the Hi-Z state.

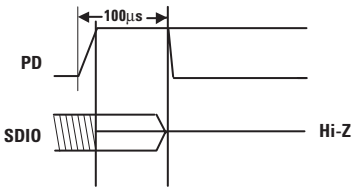


Figure 29. SDIO Hi-Z state and timing.

Required Timing Between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port. See Figure 30.

If the rising edge of SCLK for the last data bit of the second write command occurs before the 100 microsecond required delay, then the first write command may not complete correctly. See Figure 31.

If the rising edge of SCLK for the last address bit of the read command occurs before the 100 microsecond required delay, then the write command may not complete correctly. See Figure 32.

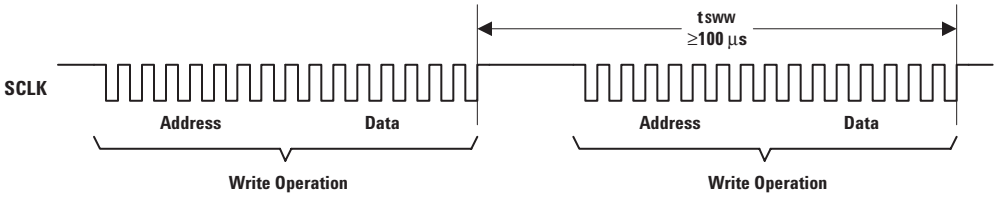


Figure 30. Timing between two write commands.

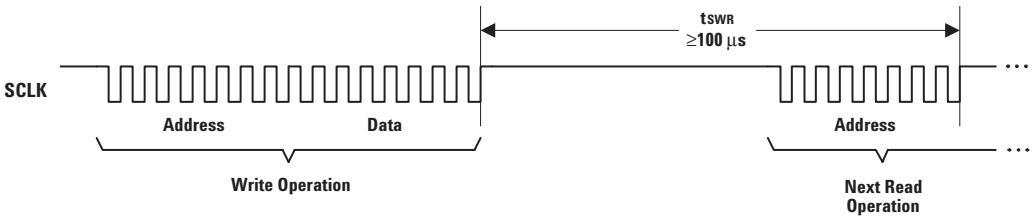


Figure 31. Timing between write and read commands.

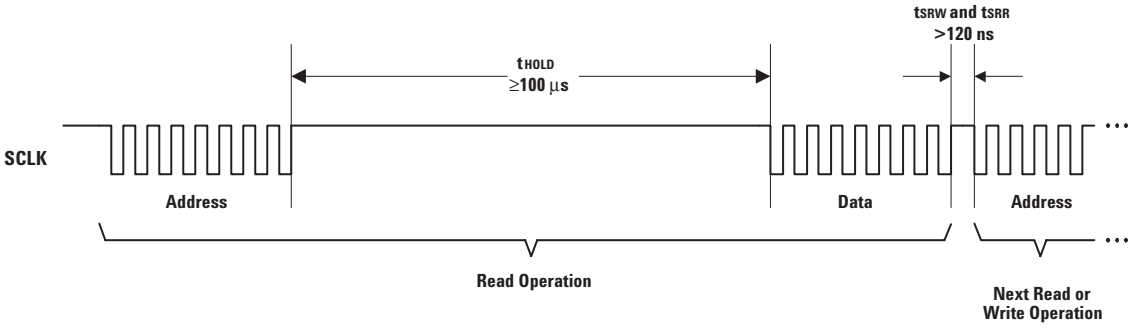


Figure 32. Timing between read and either write or subsequent read commands.

The falling edge of SCLK for the first address bit of either the read or write command must be at least 120 ns after the last SCLK rising edge of the last data bit of the previous read operation.

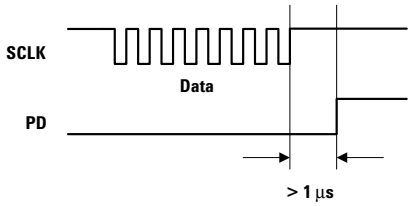


Figure 33. Timing between SCLK and PD rising edge.

Error Detection and Recovery

1. The ADNS-2030 and the microcontroller might get out of synchronization due to ESD events, power supply droops or microcontroller firmware flaws. In such a case the microcontroller should raise PD for 100 µs. The ADNS-2030 will reset the serial port but will not reset the registers, and be prepared for the beginning of a new transmission.

2. The ADNS-2030 has a transaction timer for the serial port. If the 16th SCLK rising edge is spaced more than approximately 0.9 seconds from the first SCLK edge of the current transaction, the serial port will reset.

3. Invalid addresses:
   Writing to an invalid address will have no effect. Reading from an invalid address will return all zeros.

4. Collision detection on SDIO:
   The only time that the ADNS-2030 drives the SDIO line is during a READ operation. To avoid data collisions, the microcontroller should relinquish SDIO before the falling edge of SCLK after the last address bit. The ADNS-2030 begins to drive SDIO after the next rising edge of SCLK. The ADNS-2030 relinquishes SDIO within 120 ns of the falling SCLK edge after the last data bit. The microcontroller can begin driving SDIO any time after that. In order to maintain low power consumption in normal operation or when the PD pin is pulled high, the microcontroller should not leave SDIO floating until the next transmission (although that will not cause any communication difficulties).

5. In case of synchronization failure, both the ADNS-2030 and the microcontroller may drive SDIO. The ADNS-2030 can withstand 30 mA of short circuit current and will withstand infinite duration short circuit conditions.

6. Termination of a transmission by the microcontroller may sometimes be required (for example, due to a USB suspend interrupt during a read operation). To accomplish this the microcontroller should raise PD. The ADNS-2030 will not write to any register and will reset the serial port (but nothing else) and be prepared for the beginning of future transmissions after PD goes low.

7. The microcontroller can verify success of write operations by issuing a read command to the same address and comparing written data to read data.

8. The microcontroller can verify the synchronization of the serial port by periodically reading the product ID register.

Notes on Power up and the Serial Port

The sequence in which V_{DD}, PD, SCLK and SDIO are set during powerup can affect the operation of the serial port. The diagram below shows what can happen shortly after powerup when the microprocessor tries to read data from the serial port.

This diagram shows the V_{DD} rising to valid levels, at some point the microcontroller starts its program, sets the SCLK and SDIO lines to be outputs, and sets them high. It then waits to ensure that the ADNS-2030 has powered up and is ready to communicate. The microprocessor then tries to read from location 0x00, Product_ID, and is expecting a value of 0x03. If it receives this value, it then knows that the communication to the ADNS-2030 is operational.

The problem occurs if the ADNS-2030 powers up before the microprocessor sets the SCLK and SDIO lines to be outputs and high. The ADNS-2030 sees the raising of the SCLK as a valid rising edge, and clocks in the state of the SDIO as the first bit of the address (sets either a read or a write depending upon the state).

In the case of SDIO low, then a read operation has started. When the microprocessor begins to actually send the address, the ADNS-2030 already has the first bit of an address. When the 7th bit is sent by the micro, the ADNS-2030 has a valid address, and drives the SDIO line high within 120 ns (see detail "A" in Figure 26 and Figure 27). This results in a bus fight for SDIO. Since the address is wrong, the data sent back will be incorrect.

In the case of SDIO high, a write operation is started. The address and data are out of synchronization, and the wrong data will be written to the wrong address.

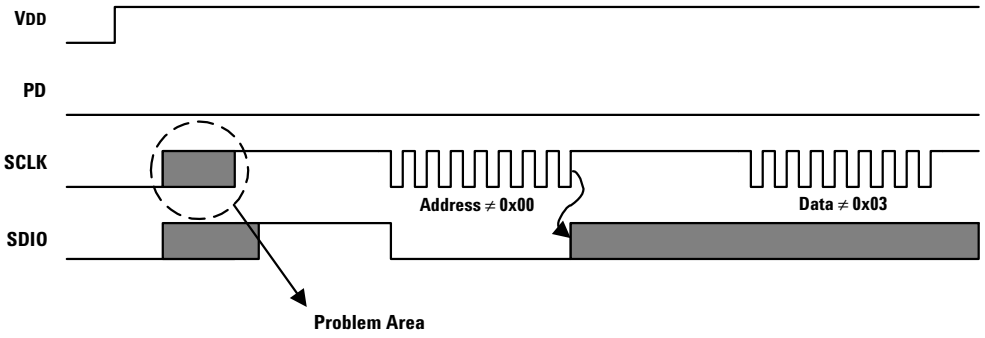


Figure 34. Power up serial port sequence.

Two Solutions

There are two different ways to solve the problem: (1) waiting for the serial port watchdog timer to time out, or (2) using the PD line to reset the serial port.

1. Serial port watchdog timer timeout

(Refer to Figure 35.)

If the microprocessor waits at least t_{SPTT} from V_{DD} valid, it will ensure that the ADNS-2030 has powered up and the watchdog timer has timed out. This assumes that the microprocessor and the ADNS-2030 share the same power supply. If not, then the microprocessor must wait t_{SPTT} from ADNS-2030 V_{DD} valid. Then when the SCLK toggles for the address, the ADNS-2030 will be in sync with the microprocessor.

2. PD Sync

(Refer to Figure 36.)

The PD line can be used to resync the serial port. If the microprocessor waits for 4 ms from V_{DD} valid, and then outputs a valid PD pulse (Refer to Figure 14), then the serial port will be ready for data.

Resync Note

If the microprocessor and the ADNS-2030 get out of sync, then the data either written or read from the registers will be incorrect. An easy way to solve this is to output a PD pulse to resync the parts after an incorrect read.

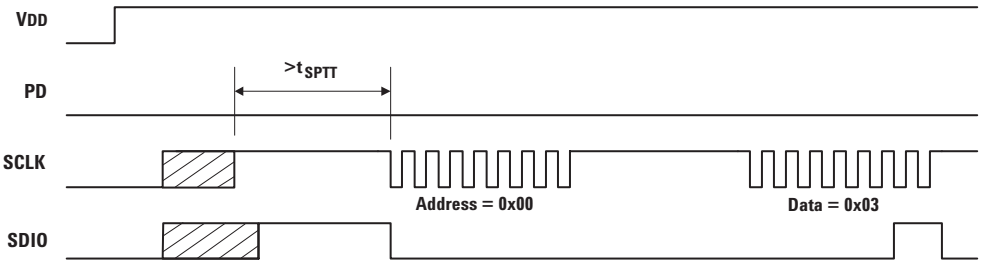


Figure 35. Power up serial port watchdog timer sequence.

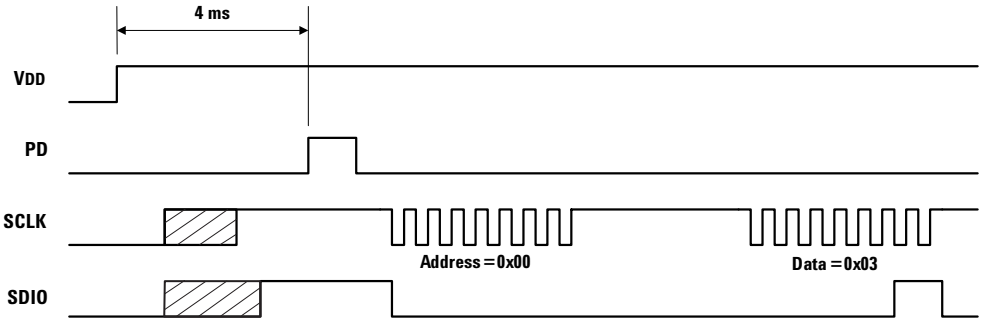


Figure 36. Power up serial port PD sync sequence.

Registers

The ADNS-2030 can be programmed through registers, via the serial port, and configuration and motion data can be read from these registers.

Address	Register
0x00	Product_ID
0x01	Revision_ID
0x02	Motion
0x03	Delta_X
0x04	Delta_Y
0x05	SQUAL
0x06	Average_Pixel
0x07	Maximum_Pixel
0x08	Reserved
0x09	Reseved
0x0a	Configuration_bits
0x0b	Reserved

Address	Register
0x0c	Data_Out_Lower
0x0d	Data_Out_Upper
0x0e	Shutter_Lower
0x0f	Shutter_Upper
0x10	Frame_Period_Lower
0x11	Frame_Period_Upper

Product_ID Address: 0x00
Access: Read Reset Value: 0x03

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type**:** Eight bit number with the product identifier.

USAGE: The value in this register does not change; it can be used to verify that the serial communications link is OK.

Revision_ID Address: 0x01
Access: Read Reset Value: 0xNN

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: Eight bit number with current revision of the IC.

USAGE : NN is a value between 00 and FF which represent the current design revision of the device.

IC Revision	NN
Rev. 1.0	0x10
Rev. 2.0	0 x 20

Motion Address: 0x02
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	FAULT	OVFY	OVFX	Reserved	Reserved	RES

Data Type**:** Bit field

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If so, then the user should read registers 0x03 and 0x04 to get the accumulated motion. It also tells if the motion buffers have overflowed and whether or not an LED fault occurred since the last reading. The current resolution is also shown.

Field Name	Description
MOT	Motion since last report or PD **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers
Reserved	Reserved for future
FAULT	LED Fault detected – set when RBIN is too low or too high, shorts to V_{DD} or Ground **0 = No fault** 1 = Fault detected
OVFY	Motion overflow Y, ΔY buffer has overflowed since last report **0 = No overflow** 1 = Overflow has occurred
OVFX	Motion overflow X, ΔX buffer has overflowed since last report **0 = No overflow** 1 = Overflow has occurred
Reserved	
Reserved	Reserved for future
RES	Resolution in counts per inch **0 = 400** 1 = 800

Notes for Motion:

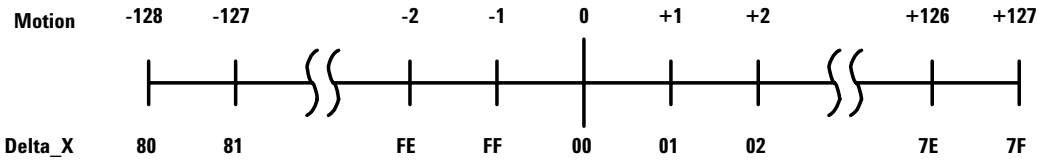
1. Reading this register freezes the Delta_X and Delta_Y register values. Read this register before reading the Delta_X and Delta_Y registers. If Delta_X and Delta_Y are not read before the motion register is read a second time, the data in Delta_X and Delta_Y will be lost.
2. Avago RECOMMENDS that registers 0x02, 0x03 and 0x04 be read sequentially.
3. Internal buffers can accumulate more than eight bits of motion for X or Y. If either one of the internal buffers overflows, then absolute path data is lost, and the OVFX or OVFY bit is set. To clear these bits (OVFX and OVFY), read the Motion, Delta_X and Delta_Y registers consecutively. Repeat until the motion bit (MOT) is cleared. Until MOT is cleared, the Delta_X or Delta_Y registers will read either positive or negative full scale, except possibly the last read. If the motion register has not been read for long time, at 400 cpi it may take up to 16 read cycles to clear the buffers, at 800 cpi, up to 32 cycles.
4. The FAULT bit signifies that an LED fault has occurred since the last time the motion register was read. An LED fault occurs if RBIN has a low resistance connection to ground. When this is detected the LED is turned off. The FAULT bit is set after a fault occurs. The FAULT bit remains set until the fault condition is cleared and the motion register is read. This bit is updated only when the motion register is read. Once an LED fault has cleared, the hardware will drive the LED normally.

Delta_X Address: 0x03
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number.

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.

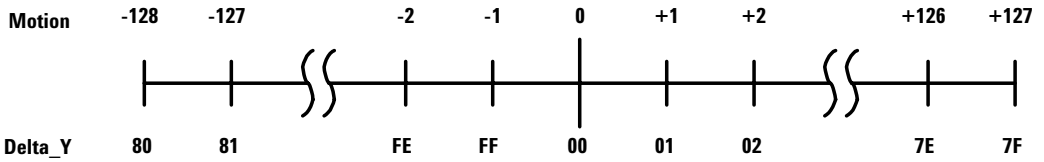


Delta_Y Address: 0x04
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number.

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register

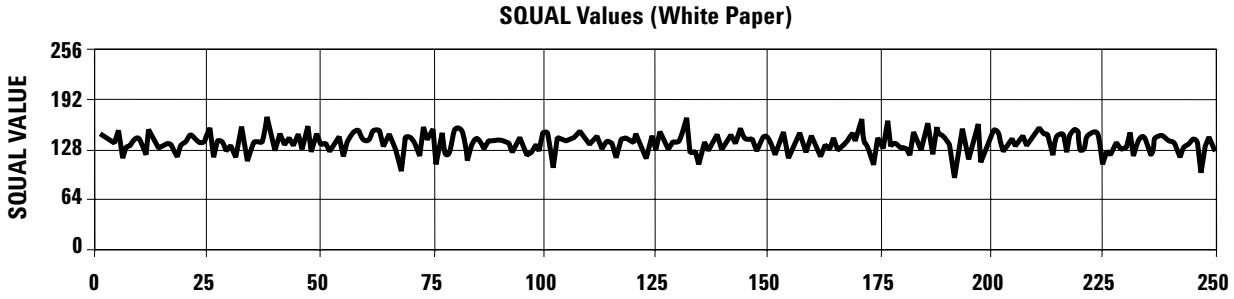


SQUAL Address: 0x05
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Eight bit number.

USAGE: SQUAL (Surface QUALity) is a measure of the number of features visible by the sensor in the current frame. The maximum value is 255. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 250 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor.



The focus point is important and could affect the SQUAL value. Figure 37 shows another setup with various Z-height. This graph clearly shows that the SQUAL count is dependent on focus distance. The data is obtained by getting multiple readings over different heights.

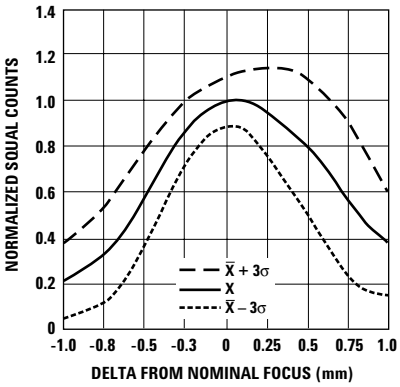


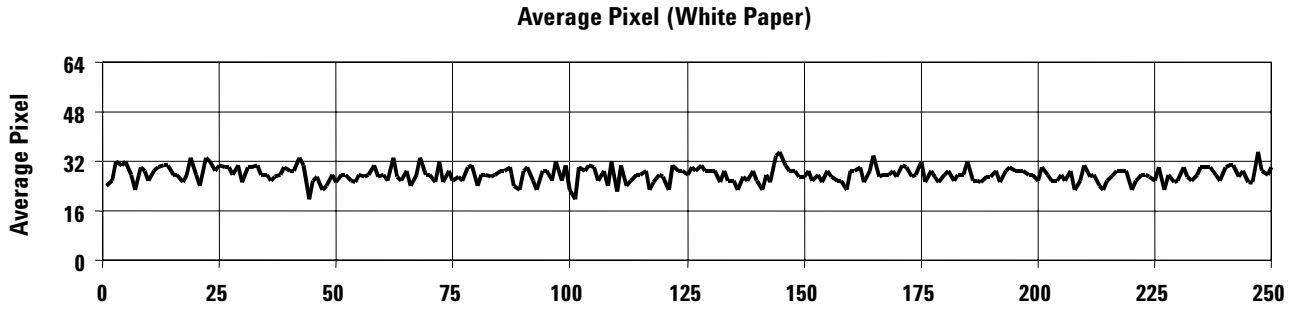
Figure 37. Typical SQUAL vs. Height, Z. (white paper)

Average_Pixel Address: 0x06
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	0	0	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type: Six bit number.

USAGE: Average Pixel value in current frame. Minimum value = 0, maximum = 63. The average pixel value may vary from frame to frame. Shown below is a graph of 250 sequentially acquired average pixel values, while the sensor was moved slowly over white paper.

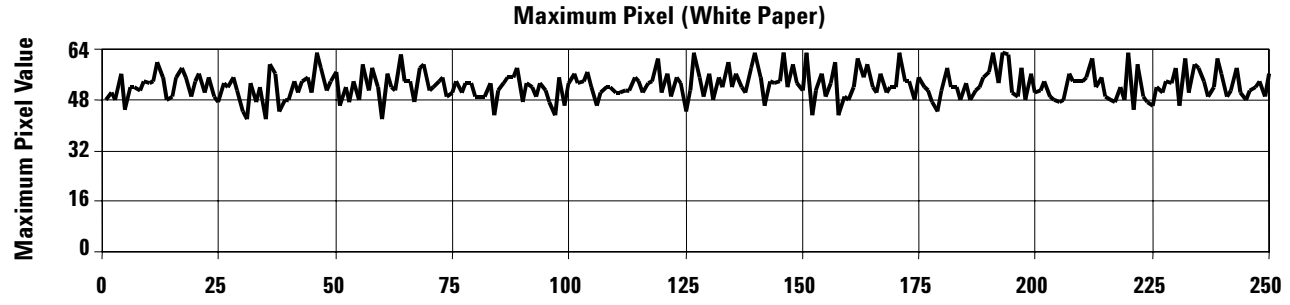


Maximum_Pixel Address: 0x07
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	0	0	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Six bit number.

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 63. The maximum pixel value may vary from frame to frame. Shown below is a graph of 250 sequentially acquired maximum pixel values, while the sensor was moved slowly over white paper.



Reserved Address: 0x08

Reserved Address: 0x09

Configuration_bits Address: 0x0a
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RESET	LED_MODE	Self Test	RES	PixDump	Reserved	Reserved	Sleep

Data Type**:** Bit field

USAGE: Register 0x0a allows the user to change the configuration of the sensor. Shown below are the bits, their default values, and optional values.

Field Name	Description
RESET	Power up defaults (bit always reads 0) **0 = No effect** 1 = Reset registers and bits to power up default settings (bold entries)
LED_MODE	LED Shutter Mode **0 = Shutter mode off (LED always on, even if no motion up to 1 sec)** 1 = Shutter mode on (LED only on when electronic shutter is open)
Self Test[1]	Self Tests (bit always reads 0) **0 = No tests** 1 = Perform all self tests, output 16 bit CRC via Data_Out_Upper and Data_Out_Lower registers.
RES	Resolution in counts per inch **0 = 400** 1 = 800
Pix Dump	Dump the pixel array through Data_Out_Upper and Data_Out_Lower, 256 bytes each **0 = Disabled** 1 = Dump pixel array
Reserved	
Reserved	
Sleep	Sleep Mode **0 = Normal, falls asleep after one second of no movement (1,500 frames/s)** 1 = Always awake

Note:

1. Since part of the self test is a RAM test, the RAM will be overwritten with the default values when the test is done. If any configuration changes from the default are needed for operation, make the changes AFTER the self test is run. This operation requires substantially more time to complete than other register transactions.

Reserved Address: 0x0b

Data_Out_Lower Address: 0x0c
Access: Read Reset Value: undefined

Bit	7	6	5	4	3	2	1	0
Field	DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0

Data_Out_Upper **Address: 0x0d**
Access: Read Reset Value: undefined

Bit	7	6	5	4	3	2	1	0
Field	DO_{15}	DO_{14}	DO_{13}	DO_{12}	DO_{11}	DO_{10}	DO_9	DO_8

Data Type: Sixteen bit word.

USAGE: Data from the system self test or the pixel dump command can be read out with these registers. The data can be read from 0x0d only, or from 0x0d followed by 0x0c.

	Data_Out_Upper	Data_Out_Lower	Notes
Self Test result 1:	DB	FD	One of two results returned.
Self Test result 2:	20	D6	These values are subject to change with each device design revision.
Pixel Dump command:	Pixel Address	Pixel Data (bits 0-5) and Pixel Data Status (bit 7)	

Once the pixel dump command is given, the sensor writes the address and the value for the first pixel into the Data_Out_Upper and Data_Out_Lower registers. The MSB of Data_Out_Lower is the status bit for the data. If the bit is high, the data are NOT valid. Once the MSB is low, the data for that particular read are valid and should be saved. The pixel address and data will then be incremented on the next frame. Once the pixel dump is complete, the PixDump bit in register 0x0a should be set to zero. To obtain an accurate image to get the Pixel Dump image, the LED needs to be turned on by changing the sleep mode of the configuration register 0x0a to always awake.

Pixel Address Map (looking through the HDNS-2100 lens)

Last Pixel

FF	FE	FD	FC	FB	FA	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
EF	EE	ED	EC	EB	EA	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
DF	DE	DD	DC	DB	DA	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CF	CE	CD	CC	CB	CA	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
BF	BE	BD	BC	BB	BA	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
AF	AE	AD	AC	AB	AA	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
9F	9E	9D	9C	9B	9A	99	98	97	96	95	94	93	92	91	90
8F	8E	8D	8C	8B	8A	89	88	87	86	85	84	83	82	81	80
7F	7E	7D	7C	7B	7A	79	78	77	76	75	74	73	72	71	70
6F	6E	6D	6C	6B	6A	69	68	67	66	65	64	63	62	61	60
5F	5E	5D	5C	5B	5A	59	58	57	56	55	54	53	52	51	50
4F	4E	4D	4C	4B	4A	49	48	47	46	45	44	43	42	41	40
3F	3E	3D	3C	3B	3A	39	38	37	36	35	34	33	32	31	30
2F	2E	2D	2C	2B	2A	29	28	27	26	25	24	23	22	21	20
1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00

First Pixel

Top X-ray View of Mouse

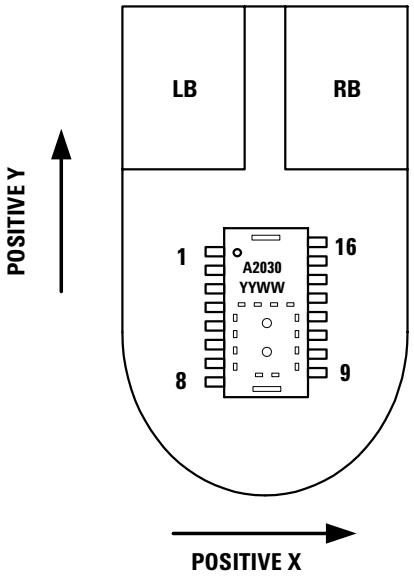
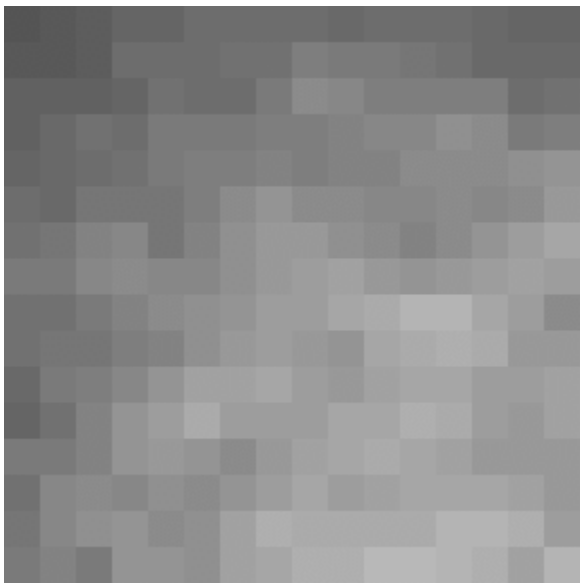


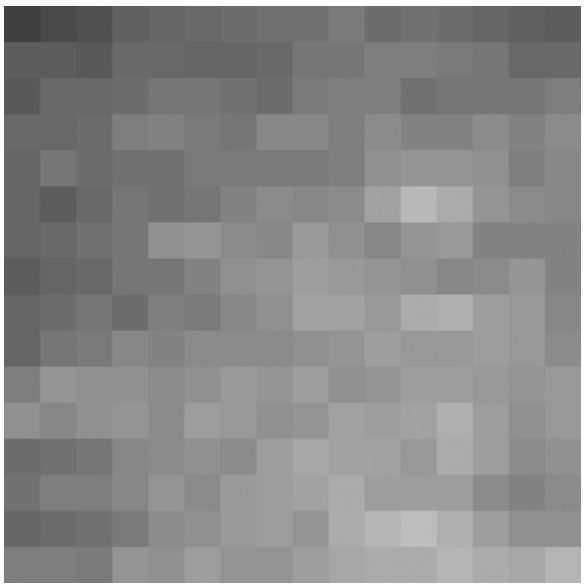
Figure 38. Directions are for a complete mouse, with the HDNS-2100 lens.

Pixel Dump Pictures

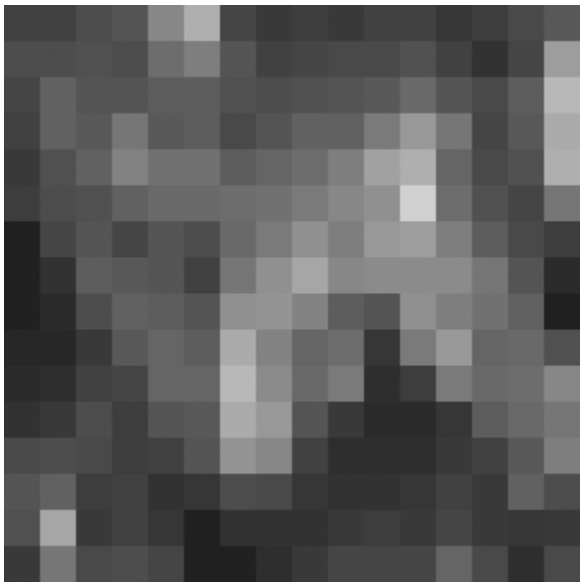
The following images are the output of the pixel dump command. The data ranges from zero for complete black, to 63 for complete white. An internal AGC circuit adjusts the shutter value to keep the brightest feature (max pixel) in the mid 50's.



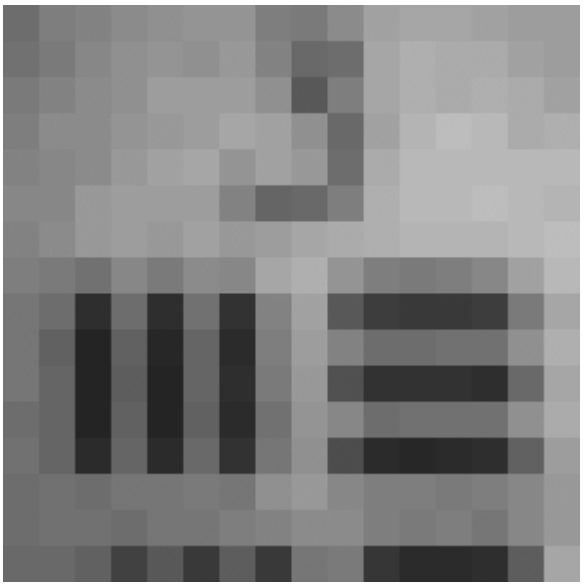
(a) White Paper



(b) Manila Folder



(c) Neoprene Mouse Pad (Gray)



(d) USAF Test Chart Group 3, Element 1, 8 line pairs per mm

Figure 39. Pixel dump pictures.

Shutter_Lower Address: 0x0e
Access: Read Reset Value: 0x64

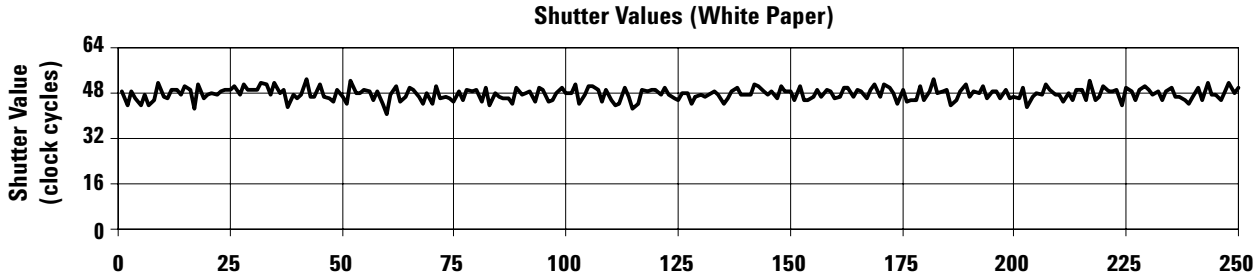
Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Shutter_Upper Address: 0x0f
Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Data Type: Sixteen bit word.

USAGE: Units are clock cycles; default value is 64. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value may be different on every frame. For each frame, the shutter can only change by ± 1/16 of the current value. Shown below is a graph of 250 sequentially acquired shutter values, while the sensor was moved slowly over white paper.



The focus point is important and could affect the shutter value. Figure 40 shows another setup with various Z-heights. This graph clearly shows that the shutter value is dependent on focus distance. It shows average readings over different heights.

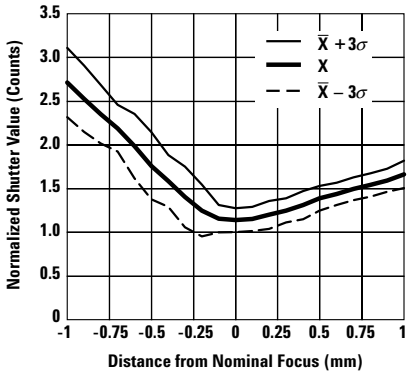


Figure 40. Typical shutter vs. Z (white paper).

The maximum value of the shutter is dependent upon the frame rate and clock frequency.

The formula for the maximum shutter value is:

$$\text{Max shutter value} = \frac{\text{clock freq}}{\text{frame rate}} - 2816$$

For a clock frequency of 18 MHz, the following table shows the maximum shutter value. 1 clock cycle is 55.56 nsec.

Frames/second	Max Shutter		Shutter		
	Decimal	Hex	Upper	Lower	
2300*	5010	0x1392	13	92	
2000*	6184	0x1828	18	28	
1500	9184	0x23E0	23	E0	← Default Max Shutter
1000	15184	0x3B50	3B	50	
500	33184	0x81A0	81	A0	

* **Note:** To optimize tracking performance on dark surfaces, it is recommended that an adaptive frame rate based on shutter value be implemented for frame rates greater than 1500.

Frame_Period_Lower Address: 0x10
Access: Read/Write Reset Value: 0x20

Bit	7	6	5	4	3	2	1	0
Field	FP_7	FP_6	FP_5	FP_4	FP_3	FP_2	FP_1	FP_0

Frame_Period_Upper Address: 0x11
Access: Read/Write Reset Value: 0xd1

Bit	7	6	5	4	3	2	1	0
Field	FP_{15}	FP_{14}	FP_{13}	FP_{12}	FP_{11}	FP_{10}	FP_9	FP_8

Data Type: Sixteen bit 2's complement word.

USAGE: Sets the frame rate. The frame period counter counts up until it overflows. Units are clock cycles.

The formula is: $\frac{\text{clock rate}}{\text{frame rate}} = \text{counts}$ (2's complements hex)

For an 18 MHz clock, below are the Frame_period values for popular frame rates.

Frames/second	Counts			Frame_Period		
	Decimal	Hex	2's comp	Upper	Lower	
2300*	7826	0x1E92	0xE16E	E1	6E	
2000*	9000	0x2328	0xDCD8	DC	D8	
1500	12000	0x2EE0	0xD120	D1	20	← Default Frame Period
1000	18000	0x4650	0xB9B0	B9	B0	
500	36000	0x8CA0	0x7360	73	60	← Minimum Frame Period

***Note:** To optimize tracking performance on dark surfaces, it is recommended that an adaptive frame rate based on shutter value be implemented for frame rates greater than 1500.

Changing the frame rate results in changes in the maximum speed, acceleration limits, and dark surface performance.

IC Register State after Reset (power up or setting bit 7, register 0x0a)

Address	Register	Default Value	Meaning
0x00	Product_ID	0x03	Product ID = 3 (Fixed value)
0x01	Revision_ID	0xNN	Revision of IC (Fixed value) (For each device design revision)
0x02	Motion	0x00	No Motion LED = No fault No X data overflow No Y data overflow Resolution is 400 counts per inch
0x03	Delta_X	0x00	No X motion
0x04	Delta_Y	0x00	No Y motion
0x05	SQUAL	0x00	No image yet to measure
0x06	Average_Pixel	0x00	No image yet to measure
0x07	Maximum_Pixel	0x00	No image yet to measure
0x08	Reserved		
0x09	Reserved		
0x0a	Configuration_bits	0x00	Part is not Reset LED Shutter Mode is off No Self Tests Resolution = 400 counts per inch Pixel Dump is disabled Sleep mode is enabled
0x0b	Reserved	—	
0x0c	Data_Out_Lower	undefined	No data to read
0x0d	Data_Out_Upper	undefined	No data to read
0x0e	Shutter_Lower	0x64	Initial shutter value
0x0f	Shutter_Upper	0x00	Initial shutter value
0x10	Frame_Period_Lower	0x20	Initial frame period value (corresponds to 1500 fps)
0x11	Frame_Period_Upper	0xd1	Initial frame period value (corresponds to 1500 fps)

Optical Mouse Design References
Application Note AN1179
Eye Safety Calculation AN1228

Ordering Information
Specify part number as follows:
ADNS-2030 = Sensor IC in a 16-pin staggered DIP, 20 per tube.
HDNS-2100 = Round Optical Mouse Lens
HDNS-2100#001 = Trimmed Optical Mouse Lens
HDNS-2200 = LED Assembly Clip (Black)
HDNS-2200#001 = LED Assembly Clip (Clear)
HLMP-ED800-xx000 = LED

For product information and a complete list of distributors, please go to our web site:
www.avagotech.com

Obsoletes 5988-5686EN
5988-8421EN June 1, 2006

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