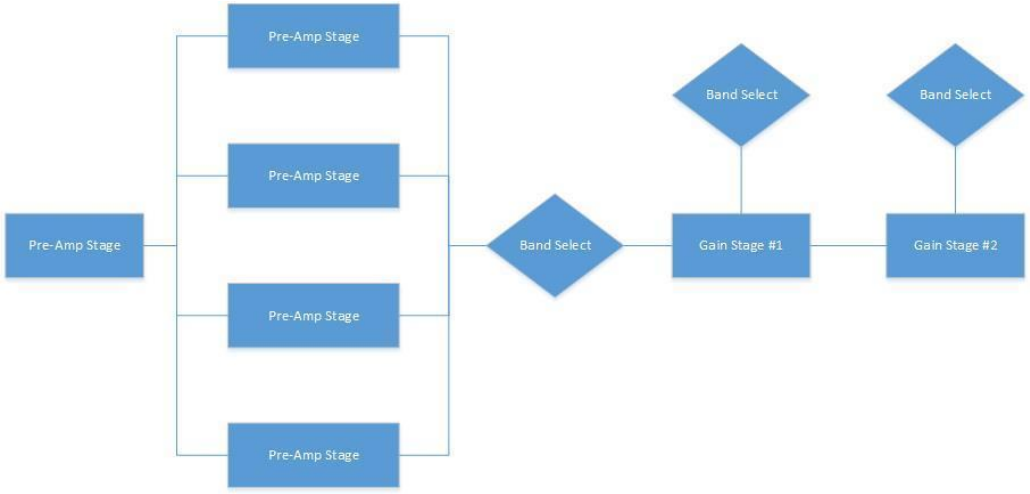
Filter Design Doc

Please note: this document is one section of a design project “Test Tank Automation for Beam Pattern Analysis” that is taken out to showcase the work on the filter amplifier. For confidentiality, the company name and IC names and specific passive component values of the design were removed from the document.

2.3 Amplifier Design

2.3.1 Amplifier Design Overview

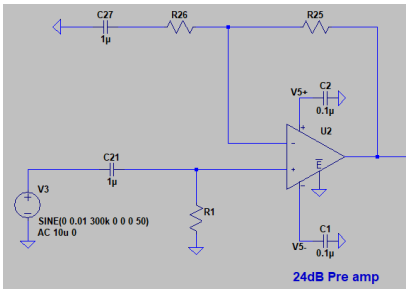
The amplifier design had to have selectable gains from 24-60dB with 6dB of increment, selectable bandwidths of 40-90kHz, 150-250kHz, 250-350kHz and 350-500kHz (these bands will be referred to as Bands 1-4, respectively) and capable of amplifying input signals as low as 10µV from a high impedance ceramic with acceptable noise cancellation. To achieve this, the filter was broken down to behave as the block diagram seen below in filter block diagram. The whole filter is powered of ±12V battery supply for adequate power and noise reduction with the signal outputting to the oscilloscope. The behaviour of the circuit was designed and simulated in LTspice circuit simulating software.



filter block diagram

2.3.2 Pre-Amplifying Stage

This stage is a low noise, 24dB boost for the front end of the filter that can be seen below in Pre-amp stage. Here the filter uses an amplifier designed for low noise applications. The particular component cannot handle the 12V input from the battery thus the rails use a ±5V input that feed off low noise voltage regulators which will be discussed further in *Peripheral Components* in *section 2.3.7*.

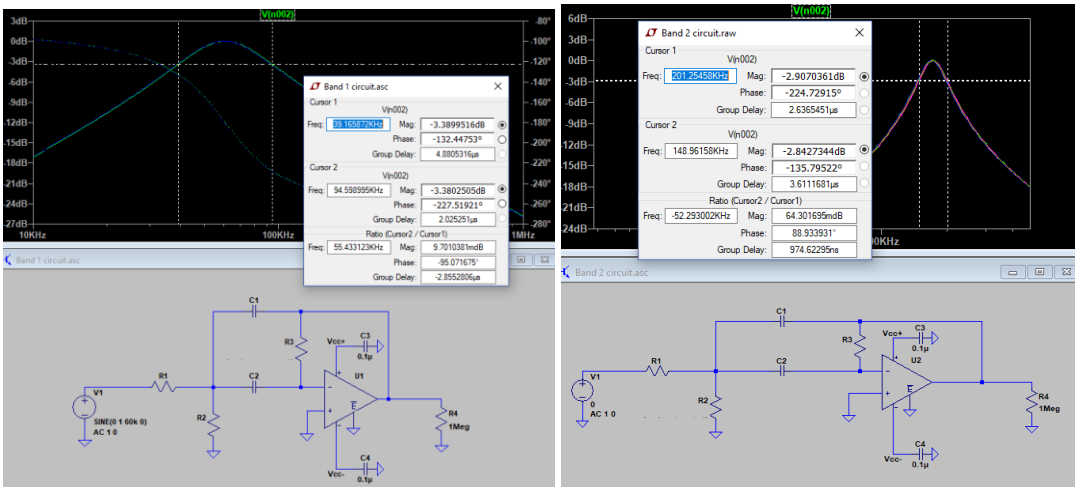


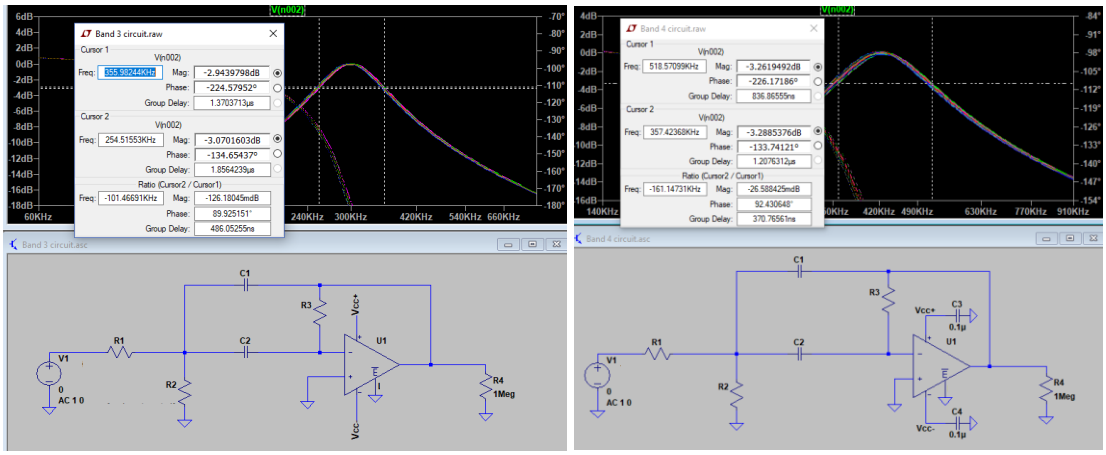
Pre-amp stage

The amplifier is used in a non-inverting op amp configuration such that there can be large input resistance into the amplifier from the ceramic while having small resistance values to reduce noise and to prevent parasitic capacitance from causing a lowpass filter. The low resistance feedback resistor configuration gives a 24dB gain without causing significant noise and eliminates effects of parasitic capacitance on the circuit. At the input of the amplifier, there is a 1µF AC-coupling capacitor in series with a high value resistor. The additional AC-coupling capacitor C_{27} was implemented due to DC offset. To prevent DC offset from being seen at the output, a AC-coupling capacitor is used to eliminate the DC component. Although the DC offset is eliminated at the input to the next stage, the capacitor C_{27} was desired to prevent unequal power draw from the batteries.

2.3.3 Filter Stage

The filter design of the bandpass stage was done using Friend bandpass filters with specifications assisted through the TI Filter design open software tool made by Texas Instrument. Once these were found the filters were tested in LTspice to check for performance with adjustments made to component values to give desired performance. Each Band was designed to give a unity gain. The images below in Bandpass Filters 1-4 show the circuits with the frequency response curves showing the -3dB cut-offs and their respective circuits. Each filter uses the same op amp described in the previous section. The output of each band leads into a 4:1 multiplexer that will allow the user to select the desired bandwidth. More on this will be discussed in the *Peripheral Components* in *section 2.3.7*. The resistors are chosen to be low value, 0.1% tolerance resistors in order to reduce noise as well as the parasitic capacitance of the circuit and for greater consistency.

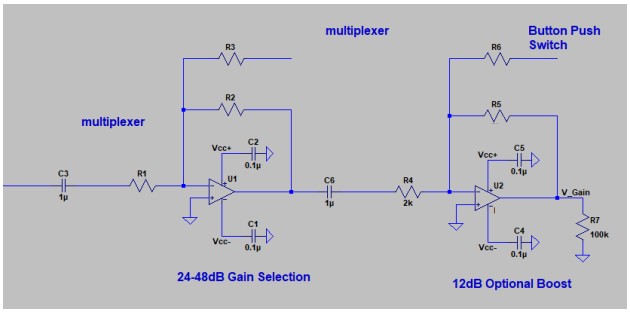




Bandpass Filters 1-4

3.2.4 Gain Stage

In this stage, an op amp with higher rail-to-rail capability as well as good gain response was needed. For this reason, the higher power amplifier with a 12V, rail-to-rail voltage was used. Since the input voltage to this gain stage has been amplified to 24dB greater than the voltage output by the receiver and filtered out with the desired bandwidths, constraints of noise could be relaxed more. With a very large gain requirement of 24-60dB, it was not reasonable in terms of stability to use a single op amp for the gain. It was found that the chosen amplifier would begin to lose significant gain when amplifying greater that 24dB, individually. For this reason, the gain was achieved with 2 stage inverting amplifiers. The first op amp selects user desired gains from 24-48dB by changing resistor R_3 as seen in Gain Stage below. The last stage is the "boost" stage which is either 0dB or 12dB to allow for 60dB to be achieved without gain attenuation in the upper frequencies. The 1µF capacitors in the circuit are used at the input of each stage to prevent drift voltage, caused by op-amp off-set current, from getting amplified and causing unwanted DC offset.



Gain Stage

For choosing the correct gain values, we can use equation Gain Stage Amplification below to solve for the values of R_3. Here, it is taken into account the 24dB pre-amp stage by multiplying it by corresponding linear value of 24dB.

$$Atotal = R2||R3R1 * 102420$$

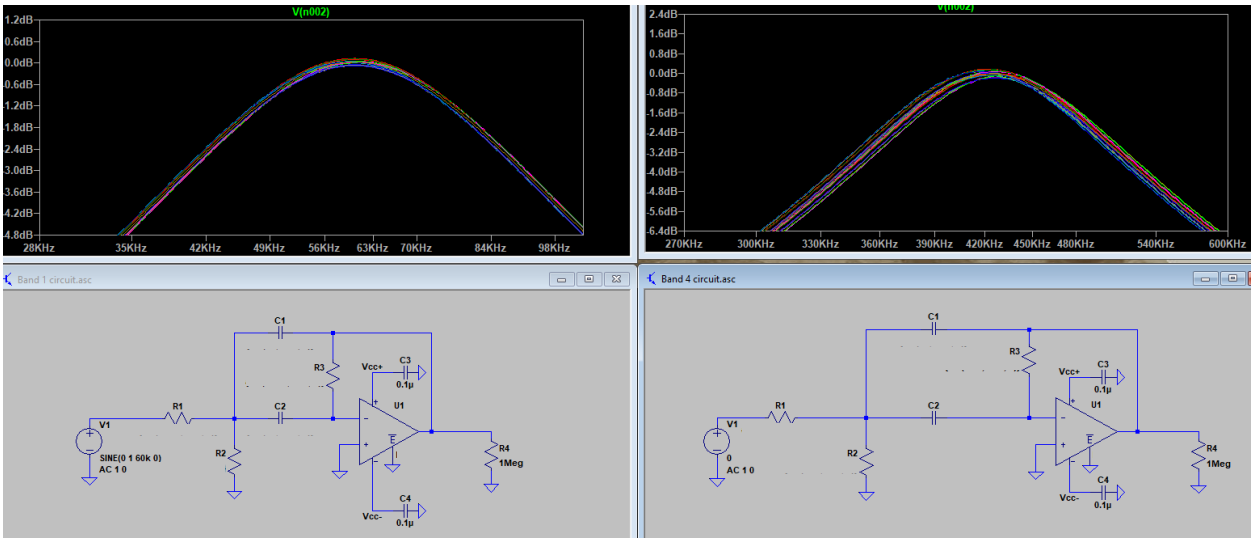
Gain Stage Amplification

By using this, the resistor values seen in Desired Gain vs R_3 Values correspond to the desired gains. In practice, this will be done using (5) inputs of an 8:1 multiplexer that will be discussed further in *Peripheral Components in section 2.3.7*

In the boost stage, the resistor R_6 seen in Gain Stage, is switched on and off to change the boost gain. When R_6 is connected to the circuit, the gain is 0dB. When R_6 is disconnected from the circuit, the gain is 12dB. The allows for gains of 54 and 60dB to be achieved without high frequency gain attenuation.

3.2.5 Filter Sensitivity

To test the sensitivity of the filters, a function in the LTspice simulation software was used to run multiple simulations at the maximum tolerances of each component. This gives an example of the worst-case scenario when the components are at their maximum tolerances. An example of these simulation can be seen in filter Sensitivity below where band 1 and band 4 are tested.



filter Sensitivity

When these filter sensitivity tests are run, the resulting filter sensitivity characteristics can be seen in table Bandwidth Filter Sensitivity below. The gains of each are measured in the center of the sensitivity analysis with the gain variations referring to max/min gain above/below average gain. When viewing filter Sensitivity, it can be seen that the width of the curve is thinner at the center frequency and becomes wider outside of the center frequency. For this reason, the filter sensitivities were tested at the center frequency f_0 and the upper and lower cut-off frequencies f_1 and f_2 to see how they differed. This is done with resistor tolerances at 0.1% and capacitor tolerances at 1%. When viewing the table 2, it can be seen that the higher frequency bandwidths have larger component sensitivity and benefit from having low tolerances.

Bandwidth Filter Sensitivity

	Band 1	Band 2	Band 3	Band 4
f_0 gain (dB)	0	0	0	0
f_0 variation (dB)	0.12	0.14	0.1	0.2
f_1 gain (dB)	-3	-3	-3	-3
f_1 variation (dB)	0.04	0.4	0.3	0.5

f_2 gain (dB)	-3	-3	-3	-3
f_2 variation (dB)	0.08	0.3	0.25	0.33

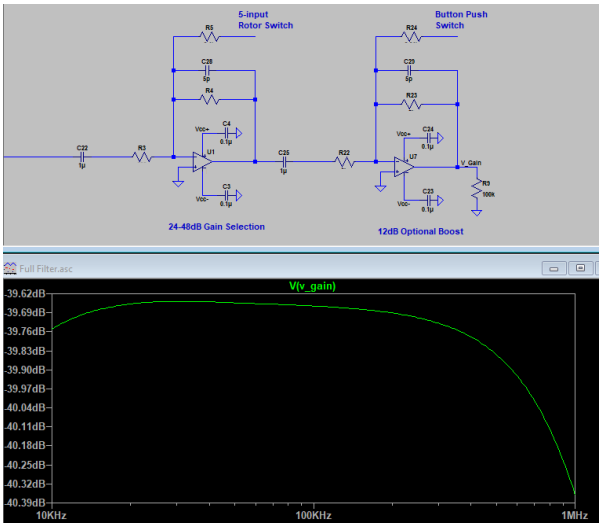
3.2.6 Gain Sensitivity

Using the same functions described in "*Filter Sensitivity*," the sensitivity of the circuit can be tested for component tolerances. Here, only resistors are needed, and the resistor sensitivity is 1%. Table Gain Circuit Sensitivity below shows the sensitivity of the circuit for component values as well as frequency sensitivity. Component sensitivity look a specific frequency and lists the average actual gain and variations while the frequency sensitivity looks at variation from 40-500kHz.

Gain Circuit Sensitivity

Parallel R_3 Resistance (kΩ)	Desired Gain (dB)	Average Gain (dB) (at 40kHz)	Component Gain Variation (dB)	Frequency drop (dB) (at 500kHz)
A	24	23.90	0.35	0.047
B	30	30.16	0.34	0.046
C	36	36.09	0.35	0.045
D	42	42.08	0.36	0.049
X	48	47.93	0.36	0.077
Y	54	54.11	0.35	0.06
Z	60	60.11	0.35	0.1

As can be seen in the table there is minimal variation in gain from the component sensitivity as well as across the frequencies. This variation is also negligible when the circuit is simulated with 5pF parasitic capacitances from the PCB across the feedback resistors as seen in Parasitic Capacitance below. This is because the resistors have been made small enough such that they do not have a large effect on the frequency response. When the total circuit is implemented with parasitic capacitance and a gain of 60dB, it is found that there is 0.2dB drop from 40-500kHz. This shows that the desired gain can be achieved.



Parasitic Capacitance

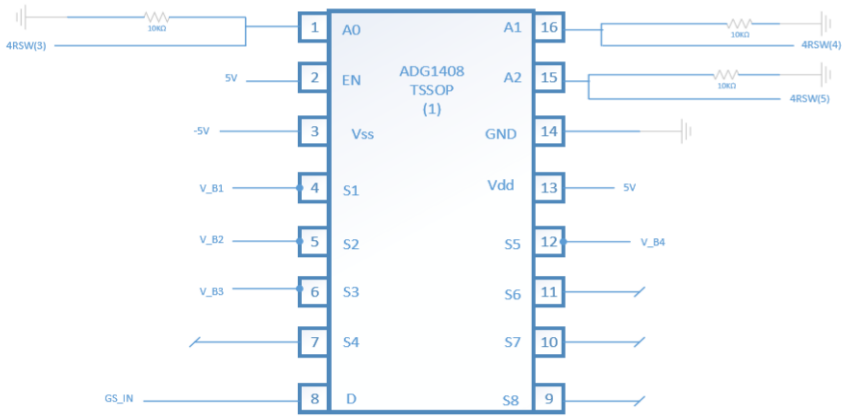
3.2.7 Peripheral Components

To make this filter realizable and selectable by the user, a few extra components are needed. In terms of user interface, the user interacts with a 4-input rotary switch to select the desired band width, a 5-input rotary switch to select the desired gain and a push button switch to activate/deactivate the 12dB boost.

For the bandwidth selection, the user will interact with an Alpha rotary switch. The pinout of the alpha rotary switch can be seen below in rotary switch.

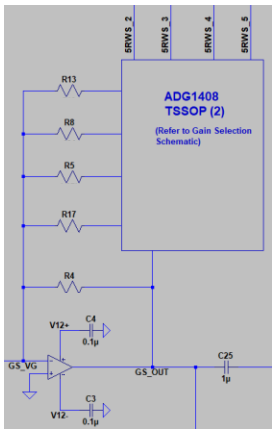
rotary switch (Left 5 position, Right 4 position)

However, since rotary switches can have antenna properties that can result in increased noise into the circuit, this is used to interact with a multiplexer. The multiplexer is an 8:1 multiplexer that will have the outputs of each bandpass filter enter into one of the (4) terminals with the output leading to the selectable gain stage. The part is not available on LTspice thus the circuit for the filter selection and a circuit drawing can be seen below in Bandwidth Selection. “V_Bandx” corresponds to the output of the each filter stage and “GS_in” corresponds to the input of the gain selection stage. The select pins A_0, A_1 and A_2 on the multiplexor connector to the (4) position rotary as seen in the left hand side of rotary switch.



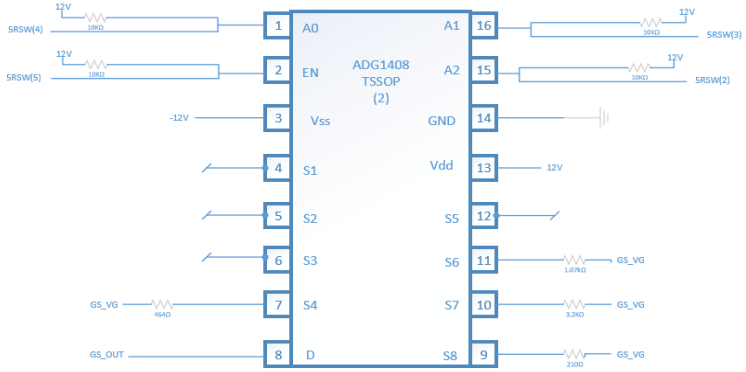
Bandwidth Selection

For the gain selection, the same 8:1 multiplexer is used but with a (5) input rotary switch to switch between the resistors found in table 1. This is placed in the gain selection stage as seen in multiplexor placement below where the multiplexer is placed between V_{G1} and V_{Go}.



Bandwidth Selection

With the multiplexor placed in the circuit, the (5) position rotary, seen in on the right side of rotary switch, will connect ground to either A_0, A_1, A_2, EN or an open line as seen below in gain select. This will either ground the specified select pin or leave them all high, which selects the desired gain. If EN is grounded, then the multiplexer is shut off and nothing is output, resulting in maximum gain to be selected. The truth table illustrating desired behaviour can be seen in MAX4538 Truth Table below.



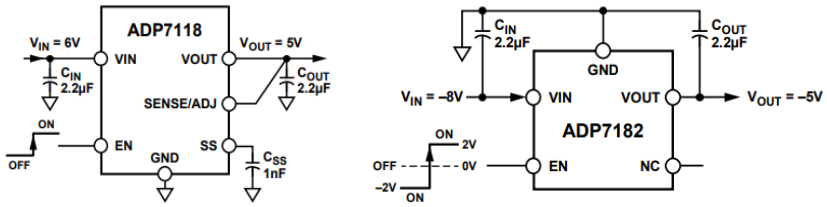
gain select

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

MAX4538 Truth Table

To toggle the 12dB boost, a push button switch toggles connection of resistor R_6 seen in Gain Stage. Finally, the 5V op-amps require a low noise voltage regulator to output 5V to the system. The voltage regulator for this will be a ADP7118ARDZ-5.0-R7 positive voltage regulator. This particular regulator is chosen for its 50dB PSRR at 1MHz, 200mA max current output, 30nV/√Hz noise spectrum and 190-320µA operating current. The circuit for implementation can be seen below in Voltage Regulator Circuits (+5 left, -5 Right). For the -5V portion, a ADP7182 voltage regulator is used. This particular regulator is chosen for its noise ranting from 30-10nV/√Hz noise spectrum, -200mA output current and 100-650µA

operating current. The operating circuit from the datasheet can be seen in Voltage Regulator Circuits (+5 left, -5 Right) below. Additionally, the reglator requires a -2V activating voltage. For this, a voltage divider is used with a 390kΩ resistor from V_{in}-EN and a 100kΩ resistor from EN-GND to keep a -2V activating signal. A bill of materials of all components involved in the circuit minus standard resistor and capacitor components can be found in the Appendix A. Total cost of components is $80.34.



MAX4538 Truth Table

3.2.8 Noise

The noise of the circuit has been largely mitigated by reducing the resistor values at each stage of the amplifier. Putting the whole circuit together and testing the noise simulations at 60dB through the different bands yields table Noise Per Spectrum below. This table lists the noise spectrum in the passband of the frequency spectrum followed by the total noise based on the bandwidth of each band followed by the minimum predicted signal to noise ratio (SNR) based on the signal voltage projected to be ≥10µV.

Noise Per Spectrum

Band	Noise (µV/√(Hz))	Total Input Noise (µV)	Minimum SNR (10µV/Noise)
1	5.5	1.23	8.13
2	6.74	1.5	6.63
3	6.08	1.922	5.2
4	5.87	2.27	4.4

From the table, it can be seen that the voltage produced by the signal should be at least 4.4 time larger than the noise within the circuit. However, this circuit does not include potential noise that may occur from other sources. LTspice does not have circuit models for the voltage regulator and multiplexer mentioned in the previous section. The low noise voltage regulator is listed as having a noise spectrum of 30nV/√Hz thus can be neglected for noise in the circuit. The MAX4638EUE+, 8:1 multiplexer is listed as having a maximum on resistance of 3.5Ω. By using equation Thermal Noise Equation seen below, the noise created by this multiplexer can be estimated to be ≤107.7nV/√Hz with a bandwidth of 150kHz (the equation as found on https://electronics.stackexchange.com/questions/106368/how-much-is-the-noise-of-a-multiplexer-for-analog-inputs (need to site separately)). This noise level can also be neglected as it is 100 less than the simulated noise of the entire circuit.

$$vn=4kBTRfb$$

Thermal noise equation

3.2.9 Power consumption

Through performing transient simulations, it was found that the (5) early stage op amps consume 5.2mA. Meanwhile, the two gain amplifiers use a total of 12.58mA from both the positive and negative supply. Since the datasheets for the voltage regulator and multiplexer each list the ambient current draw to be in the micro-amp range, we can neglect these from our battery requirements. This means that the total amperage requirements for the circuit is 35.7mA or 17.85mA per battery. Given that the requested battery time is 48 hours between charge, this means that each battery needed a capacity of

$$48h*0.01785A=0.8568Ah$$

When looking at the gain stage op amps within the system, it is found that each op amp has about 150mW or less of power dissipation. Since the Junction-Ambient rating of the component is 130°C/W, and the T_{JMax} is 150° the power consumption of the circuit is acceptable. When looking at the early stage op amp, it found that the pre-amplifier has about 8.5mW of power dissipation while the filter stage op amps each have about 10.5mW of power dissipation. Since the JA rating of the component is 250°C/W, and the T_{JMax} is 150° the power consumption of the circuit is acceptable. With everything put together, the total circuit schematic is seen in the pdf following this file.