**Lab 2: Signal Conditioning Circuitry**

# Introduction

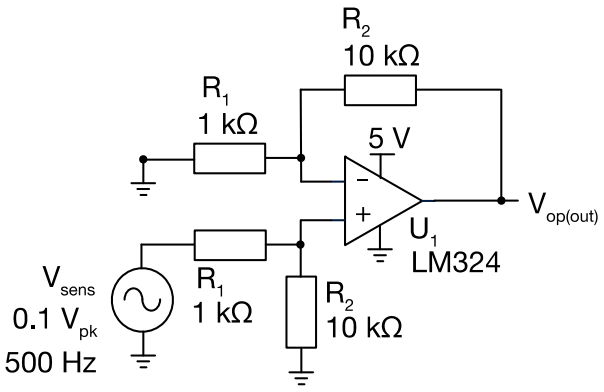
In this lab assignment, we will continue designing, modelling, simulating, and verifying the rest of your analogue circuitry. During the first part of the lab, you will explore the operating principles of a differential amplifier. You will then use this knowledge to develop the circuitry required to level-shift and amplify the signals obtained from the current sensing and voltage sensing circuits developed during Lab 1. The second part of the lab introduces you to filters, and how to use LTspice to explore the frequency response of a filter circuit. Using this understanding, a suitable 1st order low pass filter circuit is designed and validated. In the final part of this lab, we will design the 5V power supply that is required to power your OpAmps, Bluetooth module and the display.

We will now start using more realistic device models in our LTspice simulation. Unfortunately, the LTspice library does not include a model of the LM324 OpAmps we will use to implement our signal conditioning circuitry. Therefore, we are using a 3rd party OpAmp model of the LM324. The LTspice file provided to you via GitHub is already setup correctly to include this device. If you wish to learn how to setup your own 3rd party models, you may follow the video from Analog Devices on '[Adding Third-Party Models]'.

**Read the entire lab manual before you start.** This lab should take you approximately **4 hours**. There are five compulsory parts and an optional activity. Before starting the lab, pull the ee209-2021-labs repository from GitHub as it contains the LTspice model(s) and a script that may be used to write your final answers to the lab questions. Remember to commit and push your saved work to the ee209-2021-labs repository on GitHub after completing each task.

# Part 1: Differential Amplifiers

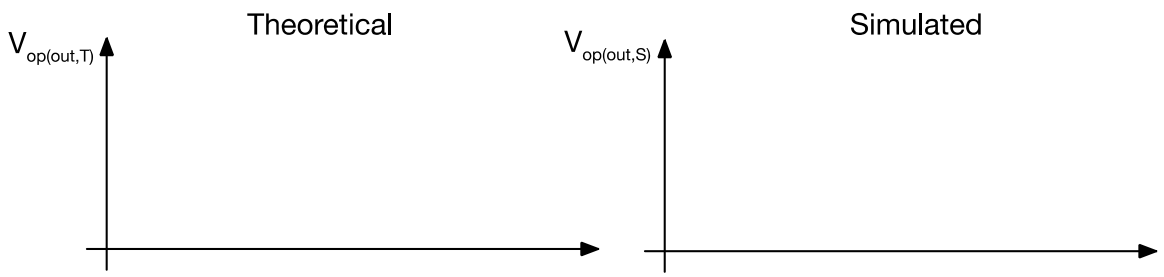
For simplicity and cost reasons, your design is going to utilise a single-rail 5V power supply instead of a dual-rail ±5V power supply. Thus, all signals in your circuit have to be constrained to be within 0V-5V. This means that the AC signals obtained from the current sensor ($V_{is}$) and the voltage sensor ($V_{vs}$), which you designed during Lab 1, need to be level-shifted. These signals may also need to be amplified, especially in the case of $V_{is}$. The LM324 based differential amplifier circuit shown below could be used to amplify the signals obtained from your voltage and current sensing circuits:



This differential amplifier circuit also allows you to easily add a DC bias to the AC signal derived from the sensors, thus ensuring the output of the OpAmp is within 0V and 5V. Since a differential amplifier measures the difference between the signals applied across its input, it has the added advantage of rejecting common mode noise. Therefore, in this project, we recommend you to use two differential amplifiers, one to level-shift and amplify $V_{is}$ while the other one is used to level-shift (and if needed amplify) $V_{vs}$. Let's start by first revising how a differential amplifier, especially one that can also work as a level-shifter, works.

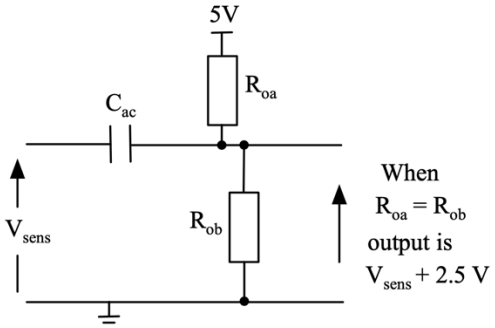
*Q 1.1: Analyse the OpAmp circuit in the figure above using your theoretical knowledge and sketch the theoretically expected output voltage waveform ($V_{op(out)}$). Simulate this circuit on LTspice using the model provided (labelled Part 1A) and verify your theoretically obtained results. Note that the LM324.lib has to be in the same folder as the LTspice simulation file, as we call this LM324 OpAmp model from within LTspice.*

Transfer function of $V_{op(out)}$ =




*Q 1.2: Why is your theory and simulation showing that the output is distorted/clipped (i.e., the output is not an exactly amplified AC waveform)?*

The clipping of the output waveform can be fixed using a number of methods. One obvious solution is to use a dual-rail ±5V power supply. However, creating a -5V rail requires extra components and adds to the cost as well the complexity of the design. Also, it does not help much since the ADC unit of the microcontroller only accepts signals between 0V and 5V anyway. Another option is to level-shift the $V_{sens}$ signal using a "passive" circuit before passing it through the OpAmp circuit. "Passive" circuits are circuits made-up of resistors, capacitors and inductors. We can use an AC coupling capacitor and a voltage divider to create a passive level-shifting circuit as shown by:



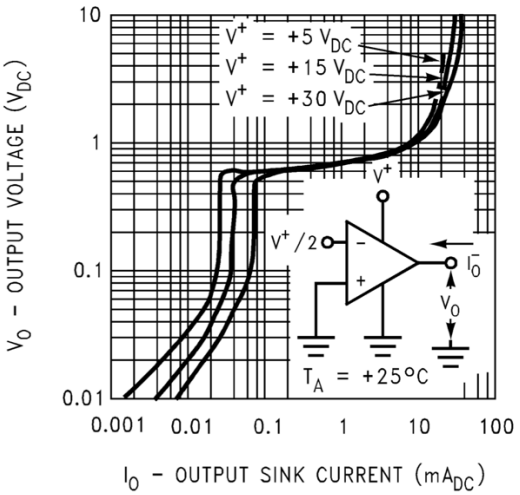

Using a passive level-shifting circuit prior to the OpAmp has a few disadvantages. Firstly, the OpAmp will amplify the offset introduced by the passive level-shifting circuit. Secondly, the impedance of the passive level-shifting circuit can impact the functionality of the OpAmp circuit following it and often require a buffer amplifier (also referred to as a unity gain or a voltage follower OpAmp circuits) to avoid this. Finally, an unwanted phase error to the signal can be introduced as the passive level-shifting circuit behaves like a high-pass filter.
The clipping of the output waveform can also be fixed by feeding a DC voltage to $R_2$, which is connected to the non-inverting terminal of the differential amplifier. The amplifier could then produce a signal that has a level-shift equal to this DC voltage fed. This is the preferred solution as it does not have the drawbacks of the two methods we discussed previously. Before we modify our differential amplifier circuit to achieve this, lets first determine what is a good level-shift (or an offset) we can apply to our signals. To do this we need to understand the maximum and the minimum voltage an LM324 can produce at its output.

*Q 1.3: Based on the LM324 datasheet provided on Canvas, what is the maximum output voltage an LM324 can produce when it is supplied by a single-rail 5V source? In the datasheet this is usually referred to as the "High-level output voltage" or $V_{OH}$. This would change with operating temperature and the current supplied through the output pin of the OpAmp (i.e., the load supplied by the OpAmp). Assume $25^0$C and a 2k$\Omega$ load. Can the simulation model mimic this behaviour? To check this, increase the amplitude of the signal labelled $V_{sens}$ (in the simulation model provided this is set by the AC source V3 found in the section labelled Power/Signal sources) to 0.5V. See if the high-level output voltage of the OpAmp circuit clips close to the level indicated in the datasheet.*

| |
|---|
| From datasheet $V_{OH}$ when OpAmp supplied by 5V = |
| $V_{OH}$ observed in simulation = |

When you completed Q1.1, you would have noticed that the LM324 model used in LTspice can produce a low-level output voltage ($V_{OL}$) that is very close to 0V (in the range 5-10mV). This agrees with what is summarised in the table found on page 7 of the datasheet. However, this is only true if the output of the OpAmp is connected to a purely resistive load. In our case, the output of the OpAmp connects to a filter circuit, which you will develop later in this lab. Filters use capacitors (and inductors in some cases). In such a situation, the OpAmp not only

has to supply (source) current to charge the capacitor in the filter, but also has to draw (sink) current to discharge capacitor in the filter. The need to sink current limits the low-level voltage an LM324 can produce as shown by the following plot taken from the datasheet:

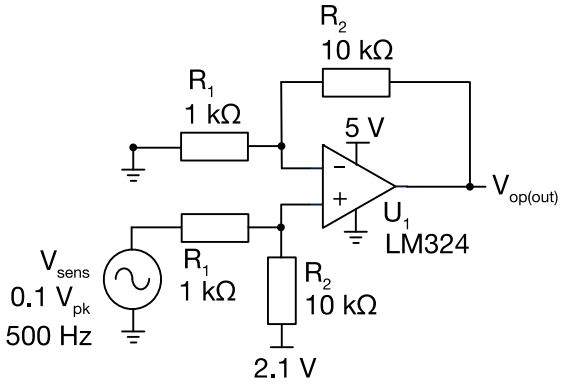



*Q 1.4: Based on the plot provided above, what is the minimum output voltage an LM324 can produce when it is supplied by a single-rail 5V source? Assume that the LM324 has to sink 1mA.*

| Minimum $V_{OL}$ from plot = |
|---|

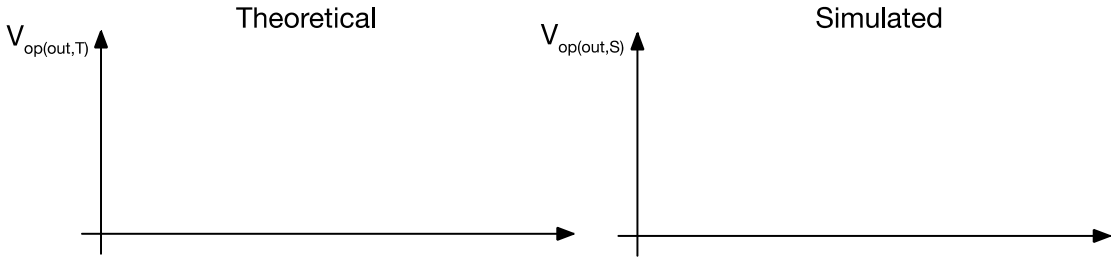
The **LTspice model of the LM324 cannot simulate** the impact of the OpAmp output current on $V_{OL}$. If you had tried to simulate a scenario where the LM324 is sinking 1mA, LTspice will tell you that the output voltage of the LM324 can reach almost 0V. Remember, results given by LTspice are only as reliable as the details captured in your circuit model. And in this case our model is not comprehensive enough to capture some of the information.

There are simple design techniques that may be used to lower $V_{OL}$ below what you noted above. You are encouraged to think about this and improve your design. For now, let's work with the numbers you worked out as answers to Q1.3 and Q1.4. Based on these answers, we could deduce that the level-shift (or the offset) should be about 2.1V (roughly midpoint between $V_{OH}$ and $V_{OL}$). Let's now modify the differential amplifier circuit to produce a 2.1V level-shift:



*Q 1.5: Analyse the OpAmp circuit in the figure above using your theoretical knowledge and sketch the theoretically expected output voltage waveform ($V_{op(out)}$). Simulate this circuit on LTspice using the model provided (labelled Part 1B) and verify your theoretically obtained results.*

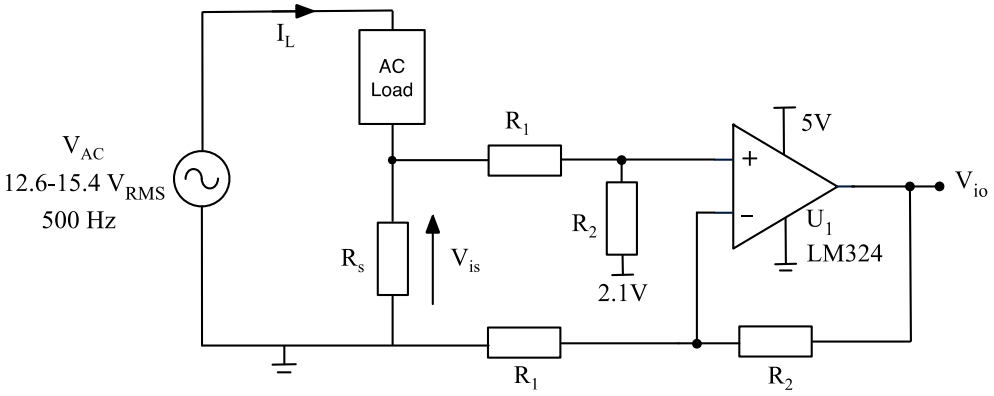
Transfer function of $V_{op(out)}$ =




## Part 2: Conditioning Current Measurement

Now that you have some understanding of how a differential amplifier functions, you should extend the current sensor design from Part 3 of Lab 1 by adding an LM324 based differential amplifier to amplify and level shift the signal. Note that the AC voltage induced across the current sensor ($V_{is}$) was in milli-volts and is a function of load current. Since the differential amplifier gain is fixed, we must design the gain so that the output of the amplifier will not clip (i.e. saturate) when $V_{is}$ is at its largest value.

The current sensor circuit, that combines the $R_s$ from Lab 1 and the LM324 based differential amplifier will look like:




*Q 2.1: Determine the resistor values $R_1$ and $R_2$ required to produce an output voltage signal ($V_{io}$) that has an offset of 2.1V and a peak-peak voltage of 2V when the AC load current is a maximum. Make sure to select resistors from the E12 series. The value of the shunt resistor ($R_s$) should be what you determined in Q3.4 of Lab 1. Note that you have already calculated and validated the minimum and maximum values of $I_L$ as well as $V_{is}$ in Lab 1. So, refer to lab 1 to extract this information.*

$R_1$ –

$R_2$ –

*Q 2.2: Modify the simulation model provided (sections of the model labelled 'Part 2' and 'AC Source, Load and Sensors') to verify that you have calculated the correct resistor values in Q2.1. As you did in Lab 1, you can validate the design by changing load resistance/supply voltage to vary the VA drawn by the AC load, while keeping it within 7.5VA to 2.5VA and observing the sensed voltage ($V_{is}$) as well as the output voltage ($V_{io}$).*

Summarise key findings (theoretical vs simulated) in the table below. Here we are analysing the circuit under 3 possible scenarios, including the two extreme cases (i.e. minimum and maximum load current). We are assuming that L is exactly 4mH and $R_L$ is changed to simulate varying load conditions. You should extract the values you have calculated in Lab 1 (Q3.2) to complete part of this table.

| Source VA | $V_{ac(rms)}$ | $R_L$ | $I_{L(rms)}$ | $V_{is(pk)}$ Theo | $V_{is(pk)}$ Sim | $V_{io(pk)}$ Theo | $V_{io(pk)}$ Sim |
|---|---|---|---|---|---|---|---|
| 7.5VA | 12.6V | | | | | | |
| 7.5VA | 15.4V | | | | | | |
| 2.5VA | 15.4V | | | | | | |

Comments (state if OpAmp output may clip or not):

*Q 2.3: What will happen if the corresponding resistor pairs of the differential amplifier are not equal to each other (e.g. $R_1$ in each arm differ slightly from each other)?*

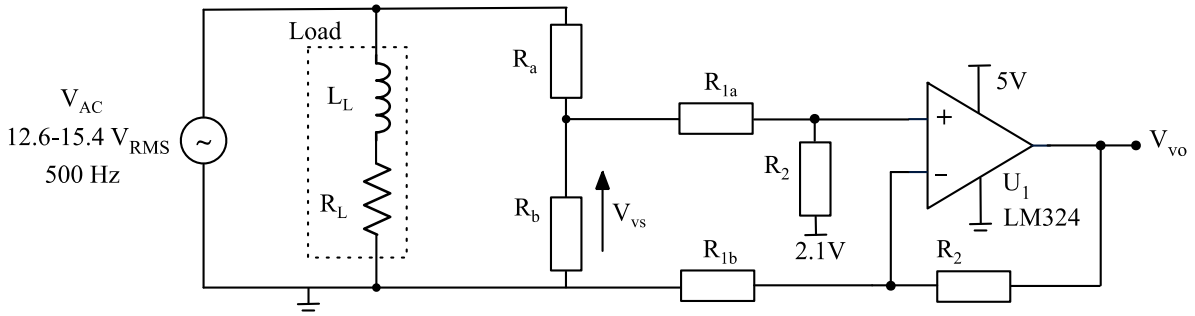
*Q 2.4: What could you do to improve the accuracy of current measurement under light loads? Under light load $I_L$ reach the minimum load current you determined during Lab 1. Since the differential amplifier gain is fixed, $V_{io}$ can be quite small.*

Note that the PCB traces have some inductance and resistance. These components will introduce a small voltage drop as you move along the trace (think of a PCB trace as many small series connected resistors and inductors). Thus, measuring the voltage at the top end of the shunt resistor with respect to a common ground (that's far away from the ground end of the shunt resistor) will introduce significant errors due to the voltage drop along the ground plane/trace. This is an example of common mode noise affecting measurements, which in your design can be avoided by taking a measurement across the shunt resistor using the differential amplifier.

## Part 3: Conditioning Voltage Measurement

You will now develop another differential amplifier circuit to level-shift the AC voltage derived from the voltage sensing circuit developed in Part 4 of Lab 1. Note that the voltage divider was designed to produce a voltage of $2V_{pk\text{-}pk}$ at maximum input voltage. Therefore, the gain of the differential amplifier can be 1, and it is mainly used to add an offset to ensure that the signal is constrained to be within 0V and 5V. As explained in the previous task, using a differential amplifier has the added advantage of rejecting common mode noise when used properly.

The voltage sensor circuit, that combines the voltage divider from Lab 1 and the LM324 based differential amplifier will look like:




*Q 3.1: Determine the resistor values $R_{1a}$, $R_{1b}$, and $R_2$ required to produce an output voltage signal that has an offset of 2.1V and a peak-peak voltage of about $2V_{pk\text{-}pk}$ when the AC source voltage is a maximum. Make sure to select resistor values from the E12 series. The values of the voltage divider resistors ($R_a$ and $R_b$) are what you determined in Q4.3 of Lab 1. Note that you have already calculated and*

*validated the minimum and maximum values of $V_{vs}$ in Lab 1. So, refer to Lab 1 to extract this information.*

$R_{1a}$ –

$R_{1b}$ –

$R_2$ –

*Q 3.2: Modify the simulation model provided (sections of the model labelled 'Part 3' and 'AC Source, Load and Sensors') to verify that you have calculated the correct resistor values in Q3.1. As you did in Lab 1, you can validate the design by changing supply voltage (within the specified range) and observing the sensed voltage ($V_{vs}$) as well as the output voltage ($V_{vo}$).*

Summarise key findings (theoretical vs simulated) in the table below. Here we are analysing the circuit under 3 possible scenarios including the two extreme cases (i.e. minimum and maximum AC voltage). We are assuming that L is exactly 4mH and $R_L$ is changed to simulate varying load conditions. You should extract the values you have calculated in Lab 1 (Q4.2) to complete part of this table.

| Source VA | $V_{ac(rms)}$ | $R_L$ | $I_{L(rms)}$ | $V_{vo(pk)}$ Theo | $V_{vo(pk)}$ Sim |
|---|---|---|---|---|---|
| 7.5VA | 12.6V | | | | |
| 7.5VA | 15.4V | | | | |
| 2.5VA | 15.4V | | | | |

Comments (state if OpAmp output may clip or not):

*Q 3.3: State why $V_{vs}$ has an offset (i.e. it is not a pure AC waveform) once you connect the voltage divider with the differential amplifier?*

*Q 3.4: When selecting the resistors for your differential amplifier circuits, would you pick them to be in the ohms, Kilo-ohms, or Mega-ohms range? State issues relating to using resistor values that are too small (ohms) or too large (Mega-ohms).*

| |
|---|
| Reasons not to use very small resistor values (e.g. ohms):<br><br><br>Reasons not to use very large feedback resistor values (e.g. Mega-ohms): |

*Q 3.5: Assume that LM324 OpAmps become unavailable (products get discontinued very often in real life) and you had to order a different OpAmp. What device parameters would you need to consider? Is there a minimum and/or maximum rating for each of these parameters that need to be observed? Complete the following table – we have given you an example.*

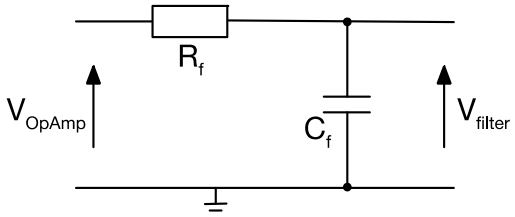
| Parameter | Max and/or Min Specification |
|---|---|
| Single rail supply voltage | Min rating < 5V < Max rating |
| | |
| | |
| | |
| | |
| | |

You should note that using a differential OpAmp to level-shift $V_{vs}$ is only one design option out of a few. For example, alternatively, as discussed in Part 1 of this lab, a passive level-shifting circuit may be used to avoid having to use an OpAmp. As you become an experienced designer, you will learn to explore different options and select the best that suits your design specifications.

# Part 4: Filters

The signals derived from the voltage and current sensing circuits will contain a significant amount of high-frequency electrical noise. As a result, the two signals generated at the output of the 2 differential amplifier circuits designed in previous

tasks will also contain high-frequency electrical noise. If these two signals are directly fed into 2 ADC channels, due to aliasing, the noise will introduce error in the digital values obtained by your C program. Therefore, it is common practice to use 1st or 2nd order antialiasing filters to filter high-frequency electrical noise from signals before feeding them to ADC channels. In more sensitive designs, they may employ multiple cascaded filters to obtain very clean signals. However, since our design measures a very low frequency signals (500Hz) and the electrical noise is typically at high frequencies (100s of kHz), it is sufficient to use a 1st order low-pass RC filter circuit to filter $V_{io}$ and another 1st order low-pass RC filter circuit to filter $V_{vo}$ before passing these 2 signals from the OpAmps into 2 ADC channels of the microcontroller. Remember, a 1st order low-pass RC filter looks like:

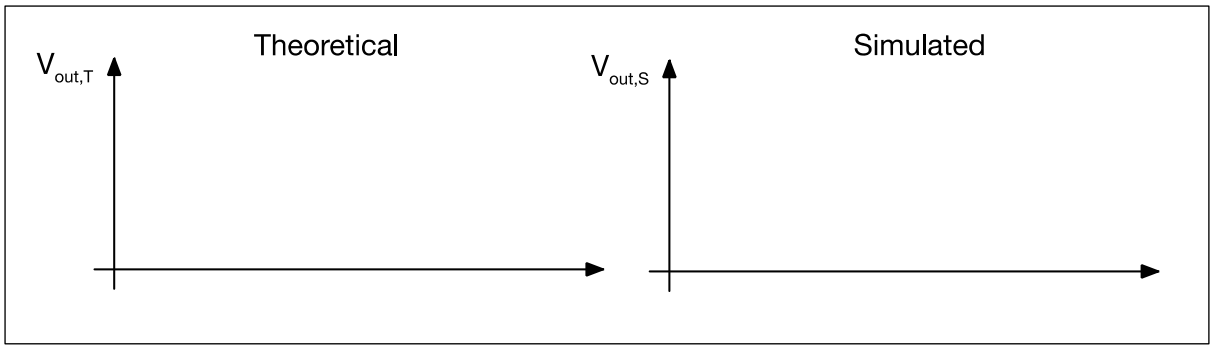



Here, $V_{OpAmp}$ represents the signal coming from one of the level-shifting OpAmps (i.e., either $V_{io}$ or $V_{vo}$). $V_{filter}$ represents the output of the filter going into one of the ADC channels of the microcontroller. Therefore, the capacitor in each RC filter will be connected directly from an ADC pin to the ground of the circuit. Since a capacitor looks like almost a short circuit for very high-frequency signals, the noise would be shunted to ground, and a reasonably clean signal will be passed to the ADC. This capacitor also helps improve the accuracy as well as the speed of the sample and hold circuit that is used inside the ADC module of the microcontroller. So, this filter circuitry has two very important functions.

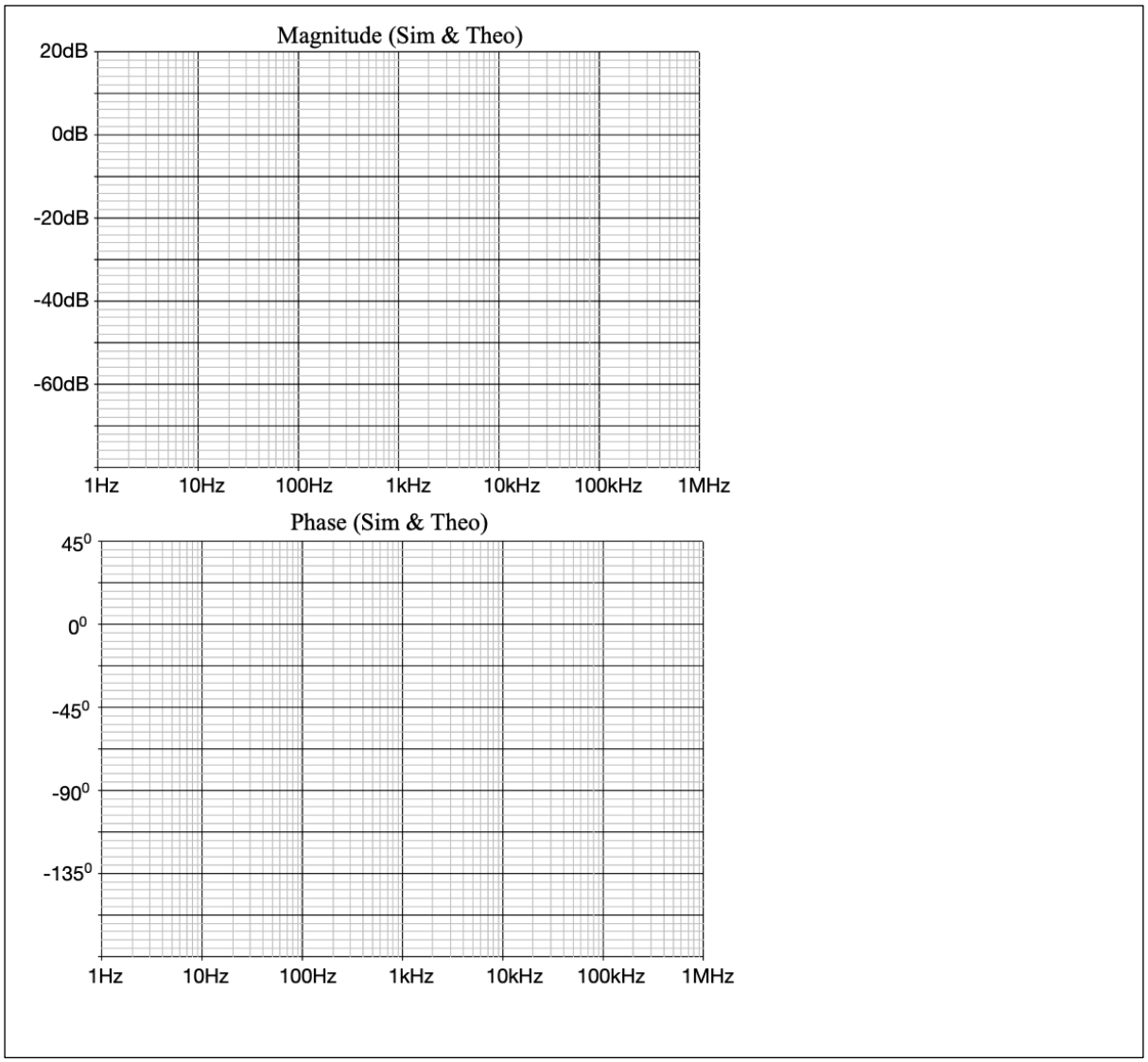
*Q 4.1: Derive the transfer function ($V_{filter}/V_{OpAmp}$) of the RC filter shown above to show that it functions as a 1st order low-pass filter. Determine the values of $C_f$ and $R_f$ required to ensure a -3dB cut-off frequency of 10kHz. Note that, the AC source is expected to generate a significantly strong noise components at frequencies 100kHz and beyond. As such, it is a good decision to place the filter cut-off frequency at 10kHz, which is significantly lower than noise frequency but still considerably higher than the 500Hz signal frequency.*

| |
|---|
| Transfer function $V_{filter}/V_{OpAmp}$ = |
| $C_f$ and $R_f$ = |

*Q 4.2: Sketch the theoretically expected output voltage waveform ($V_{filter}$) of the RC filter if the input is a $2V_{pk\text{-}pk}$ AC signal that has an offset of 2.1V. Modify the simulation model provided by editing $C_f$ and $R_f$ values as per Q4.1 (section of the model labelled 'Part 4') and verify your theoretically obtained results.*




*Q 4.3: Sketch the theoretically expected bode magnitude and phase plots of the filter transfer function ($V_{filter}/V_{OpAmp}$). Using AC analysis option provided in LTspice, simulate the frequency response of the RC filter circuit (section of the provided model labelled 'Part 4') and verify your theoretically obtained results. To assist, the simulation command required is provided in the comments under 'Simulation Commands'.*




*Q 4.4: What will be the impact of shifting the filter cut-off frequency closer to 500Hz or 100kHz? Validate your answer using LTspice.*

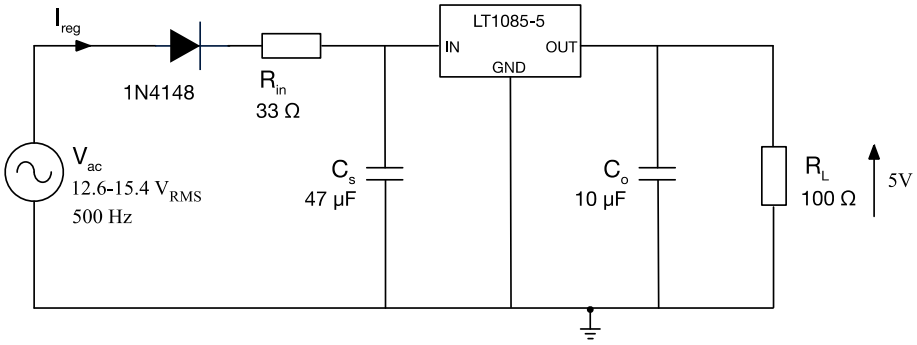
A cut-off frequency closer to 500Hz results in:

A cut-off frequency closer to 100kHz results in:

Note, to emulate noise in your circuit you may add a source that generates a 100kHz signal in series with V4 (i.e. the source that generates the $2V_{pk-pk}$ AC signal that has an offset of 2.1V) in the simulation model. We encourage you to try this and observe the reduction in the 100kHz noise signal at the output of the filter.

## Part 5: DC Regulator Circuit

The OpAmps used in our design need to be powered using a DC power supply. Similarly, the Bluetooth module and the display requires a DC power supply. As discussed previously, we are going to use a single-rail 5V DC power supply to power these devices. There are many ways to obtain a 5V DC supply, including using a battery pack. However, it is convenient to use the AC source itself to derive this 5V DC supply. This can be achieved using a half-wave rectifier and 5V linear regulator IC as shown in the figure:




*Q 5.1: The smoothing capacitor $C_s$ in the regulator circuit above is selected in order to make sure the voltage ripple at the input ($\Delta V_{in}$) to the regulator is acceptable. Note that the worst case line regulation of the LT1085 regulator IC according to the datasheet is 0.5%. Thus, a certain $\Delta V_{in}$ will result in an output ripple of $\Delta V_{in}$x0.5%. If $C_s$ is chosen to be 47$\mu$F, stating your assumptions, determine the approximate value of $\Delta V_{in}$. Simulate the operation of regulator circuit using the LTspice model provided (labelled 'Part 5') and verify your answer.*

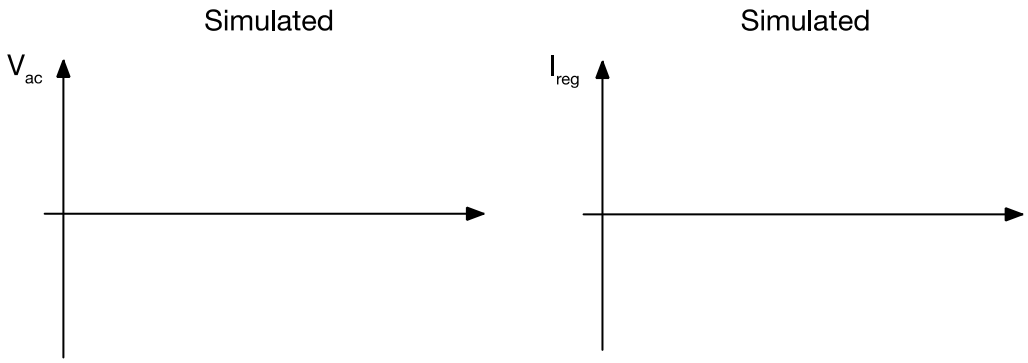
Assumptions –

Theoretical $\Delta V_{in}$ =

Simulated $\Delta V_{in}$ =

The minimum value of $C_o$ required to ensure stable operation of the LT1085 IC is indicated in the datasheet as 10μF. Therefore, the design above uses a 10μF capacitor. It should be also noted that $R_L$ models the average current consumed by your OpAmps, the Bluetooth module and the display. Therefore, in this example, we are assuming that the total current consumption of your analogue circuitry is 50mA (i.e. 5V/100Ω). This can be different in practice (though in a real design we should accurately estimate the current consumption of the circuit before designing the regulator circuit, in ELECTENG 209 due to limited time you have, we are assuming it is about 50mA as a first try. Later may find that this approximation might be too optimistic/pessimistic and improve your design).

*Q 5.2: On LTspice, observe $V_{ac}$ and $I_{reg}$ waveforms, and sketch them here. State why the current waveform looks like short-duration bursts.*




$I_{reg}$ looks like short-duration bursts because:

*Q 5.3: The half-wave rectifier employs a current limiting resistor ($R_{in}$) to avoid large current spikes been drawn from the AC source to charge $C_s$. However, this also limits the maximum current the LT1085 can supply at the output. Assume that the current consumption of your analogue circuitry has increased to 100mA. To emulate this increase in current, modify the simulation model (labelled 'Part 5') by changing $R_L$ to 50Ω. Run the simulation to show that the regulator fails to maintain a constant 5V output when $V_{ac}$ is 14$V_{rms}$. Reduce $R_{in}$ to fix this issue, simulate and observe the significant increase in current draw from the AC source.*

*Q 5.4: What are the benefits and disadvantages of using a half-wave rectifier opposed to a full-wave rectifier in your design?*

Advantages of a half-wave rectifier

Disadvantages of a half-wave rectifier

*Q 5.5: How can you derive the 2.1V offset required for the differential amplifiers from the 5V DC supply that you just designed? Sketch a suitable circuit, simulate and verify the answer. Hint: Using just a simple voltage divider is not the best solution. You need extra circuitry in addition to the voltage divider to derive a stable and clean 2.1V signal.*

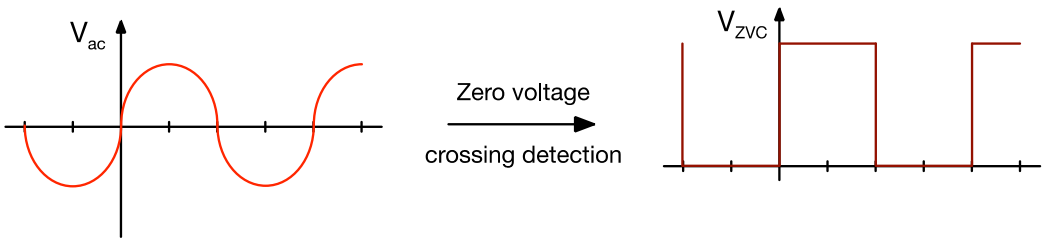
Sketch a circuit that would provide the 2.1V offset signal

## Optional Tasks: Integration & Improvements

During your progress review, you must show us a simulation model that verifies the viability of your proposed analogue design for the energy monitor. You have already designed, developed and validated most of your analogue design during Lab 1 and Lab 2. So, let's combine the following circuits you have already designed,

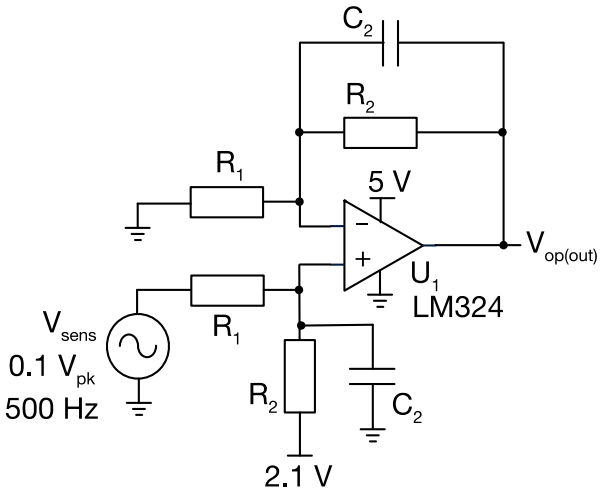
1. Current and voltage sensors
2. The two differential amplifier circuits used to level-shift (and amplify) the sensed current and voltage signals
3. The two 1$^{st}$ order low pass filters to filter the output of each differential amplifier circuit
4. The 5V DC regulator
5. The 2.1V offset generation circuit

The only component left for you to design on your own is a circuit that can detect the zero voltage crossings of the AC source voltage ($V_{ac}$). This circuit will produce a square wave output ($V_{ZVC}$). The rising and the falling edges of this square wave should correspond to the zero voltage crossings of $V_{ac}$ as shown by:




As you did during the lab exercises, make sure to validate the design by changing the supply voltage (within the specified range), and observing the correct behaviour of the design.

After completing the basic design of your analogue circuitry, you may start thinking about improvements. As mentioned earlier, we can achieve a lower $V_{OL}$ with a simple modification. This could be a good starting point to improve your design. Earlier in this lab, we also asked you to think about how to improve the accuracy of the current measurement under light load conditions (i.e., when $R_L$ is closer to 105Ω). You could also improve the filter design and turn it in to a 2nd order filter. When you start working on the software, you will learn that the ADC conversion rate needs to be limited to 10kHz (to meet the design specifications). This means, to avoid errors due to aliasing you should try to lower the cut-off frequency of the filters further below 5kHz. However, lowering the cut-off frequency closer to 500Hz can introduce measurement errors. A 2nd order filter, can attenuate noise much faster than a 1st order filter. As a result it can help these contradicting requirements to some extent. As shown below, it is also possible to configure a differential amplifier to function as a 1st order filter:




Cascading two 1st order filters perform as a 2nd order filter. You can try this as another improvement. There are many more improvements you could do. However, it is not a requirement to do any of these improvements. These are all optional activities you could attempt on your own time. If you require support with these optional activities, we will be happy to help.

**To get signed off for the lab:**

- Record all the workings in hardcopy or in digital format so we can give you marks for workings if final answers are not correct
- Modify the simulation models provided as per the lab tasks and save
- Commit and push your saved work to the uoa-ece209-2021-labs repository on GitHub after completing each task and make sure it is up to date
- Complete this document/Lab2_AnswerScript.md summarising your final answers, commit and push to the uoa-ece209-2021-labs repository on GitHub
- Update logbook indicating yours and teams progress, meeting notes, etc.
- Go to your assigned interview session to check-in with a TA who will check your solutions and ask a few questions
- Report on your weekly progress