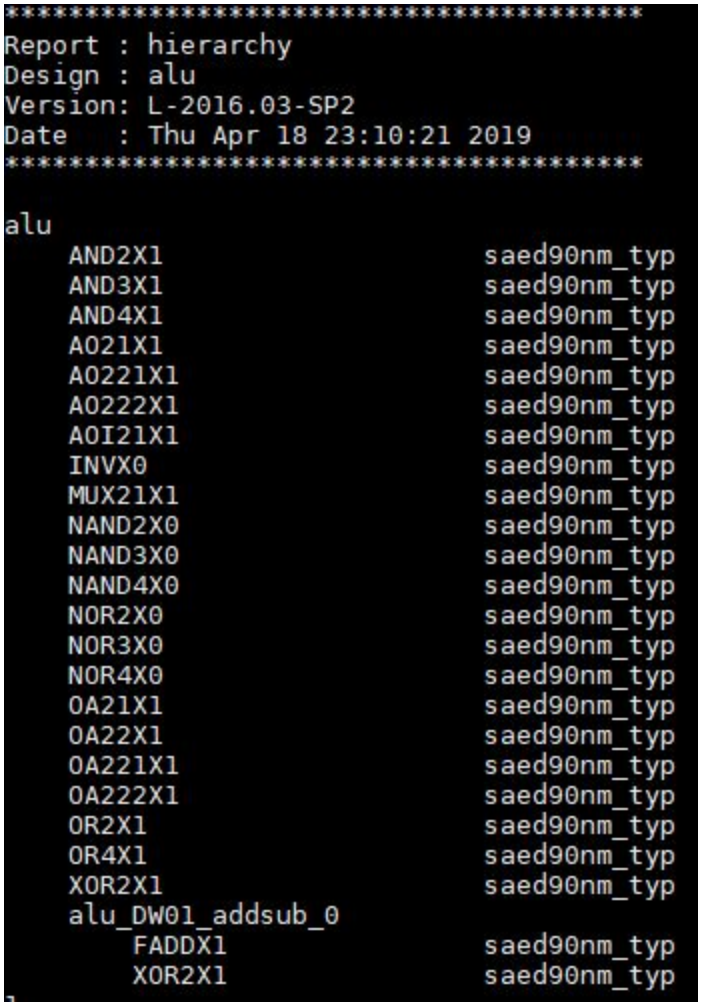
John Behman
ECE 474 HW #2 Responses

4:

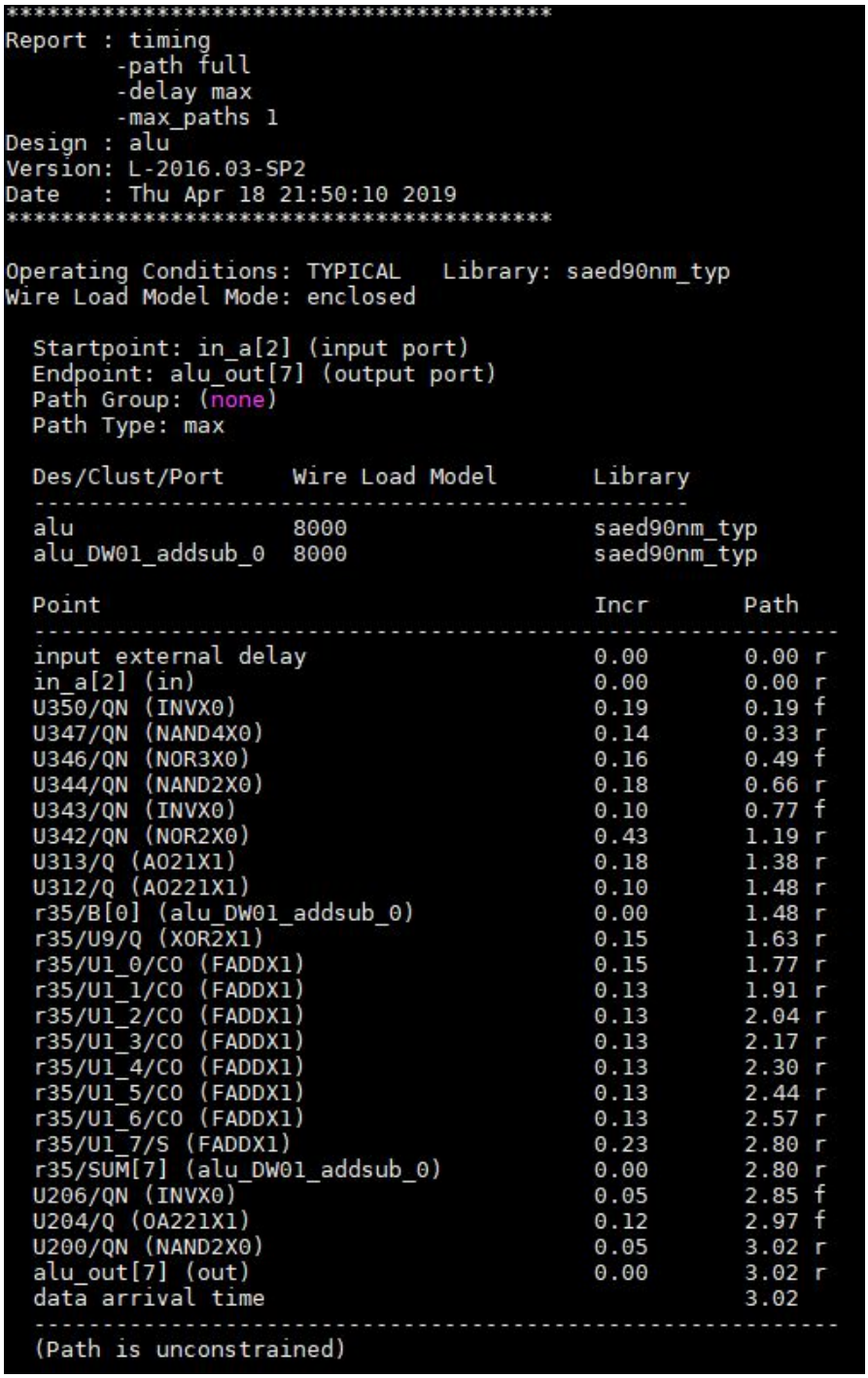
a. Using the report_area command, I found that the total cell area was 1,808.24 micrometers squared and the total area was 1,911.5 micrometers squared.
b. Using the report_hierarchy command, I found that my design used a total of 24 different types of gates. This can be seen in the graphic below.



c. The size of a NAND2X1 was found to be 5.5296 micrometers squared. Given this value, the amount of gates can be calculated with 1911.5/5.5296. This results in a calculated gate amount of approximately 346 total gates.
d. Using the hierarchy image from question b, it can be seen that Design Vision added a hierarchical block labeled alu_DW01_addsub_0. This block is used to implement portions of the design allowing for a more efficient gate level design. The style it

implemented by the synthesis tool included add and subtract functionality within the hierarchical block as seen in the name.

e. The total delay through the ALU was 3.02. The path traveled to create this delay began at input a_in and finished at the output alu_out. This image below highlights this information in greater detail.



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****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : alu
Version: L-2016.03-SP2
Date   : Thu Apr 18 21:50:10 2019
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

  Startpoint: in_a[2] (input port)
  Endpoint: alu_out[7] (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  alu                8000                  saed90nm_typ
  alu_DW01_addsub_0  8000                  saed90nm_typ

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  in_a[2] (in)                             0.00       0.00 r
  U350/QN (INVX0)                          0.19       0.19 f
  U347/QN (NAND4X0)                        0.14       0.33 r
  U346/QN (NOR3X0)                         0.16       0.49 f
  U344/QN (NAND2X0)                        0.18       0.66 r
  U343/QN (INVX0)                          0.10       0.77 f
  U342/QN (NOR2X0)                         0.43       1.19 r
  U313/Q (AO21X1)                          0.18       1.38 r
  U312/Q (AO221X1)                         0.10       1.48 r
  r35/B[0] (alu_DW01_addsub_0)             0.00       1.48 r
  r35/U9/Q (XOR2X1)                        0.15       1.63 r
  r35/U1_0/CO (FADDX1)                     0.15       1.77 r
  r35/U1_1/CO (FADDX1)                     0.13       1.91 r
  r35/U1_2/CO (FADDX1)                     0.13       2.04 r
  r35/U1_3/CO (FADDX1)                     0.13       2.17 r
  r35/U1_4/CO (FADDX1)                     0.13       2.30 r
  r35/U1_5/CO (FADDX1)                     0.13       2.44 r
  r35/U1_6/CO (FADDX1)                     0.13       2.57 r
  r35/U1_7/S (FADDX1)                      0.23       2.80 r
  r35/SUM[7] (alu_DW01_addsub_0)           0.00       2.80 r
  U206/QN (INVX0)                          0.05       2.85 f
  U204/Q (OA221X1)                         0.12       2.97 f
  U200/QN (NAND2X0)                        0.05       3.02 r
  alu_out[7] (out)                         0.00       3.02 r
  data arrival time                                   3.02
  -----------------------------------------------------------
  (Path is unconstrained)
```