65816 Microprocessor Quick Reference

Jeff Tranter <tranter@pobox.com>

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Registers:

<table>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8" rowspan="3">Data Bank Register (DBR)</td><td colspan="8">Accumulator (B)</td><td colspan="8">Accumulator (A)</td></tr>
<tr><td colspan="16">X Index Register (X)</td></tr>
<tr><td colspan="16">Y Index Register (Y)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="16">Direct Page Register (D)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="16">Stack Pointer (S)</td></tr>
<tr><td colspan="8">Program Bank Register (PBR)</td><td colspan="16">Program Counter (PC)</td></tr>
<tr><td colspan="8"></td><td colspan="15">Processor Status Register (P)</td><td>E</td></tr>
<tr><td colspan="8"></td><td colspan="8"></td><td>N</td><td>V</td><td>M</td><td>X</td><td>D</td><td>I</td><td>Z</td><td>C</td></tr>
</table>

Notes:
1. Accumulator is 16-bit (C) when M=0, 8-bit (A and B) when M=1.
2. Index registers are 16-bit when X=0, 8-bit when X=1.

Processor Status Register:

N - Negative (1=negative)
V - Overflow (1=overflow)
M - Memory/Accumulator Select (1=8-bit, 0=16-bit)
X - Index Register Select (1=8-bit, 0=16-bit)
D - Decimal Mode (1=decimal, 0=binary)
I - IRQ Disable (1=disabled)
Z - Zero (1=zero result)
C - Carry (1=carry)
E - Emulation (0=native mode)

Switching Modes:

Go to native mode:

```
CLC
XCE
```

Go to emulation mode:

```
SEC
XCE
```

Select 16-bit memory and 16-bit index registers:

```
REP #%00110000
```

Select 8-bit memory and 8-bit index registers:

```
SEP #%00110000
```

Select 16-bit memory and 8-bit index registers:

```
REP #%00100000
SEP #%00010000
```

Select 8-bit memory and 16-bit registers:

```
SEP #%00100000
REP #%00010000
```

Emulation Mode Features:

1. Emulation mode is default on power up/reset.
2. Separate 8-bit accumulators (A and B).
3. 8-bit index registers (X and Y).
4. Stack is limited to page 1.
5. Direct page indexing wraps.
6. B flag in PSR reflects BRK status (instead of X).
7. Uses 6502 interrupt vectors.

New Addressing Modes:

Addressing Mode	Example
Program Counter Relative Long	BRL JMPLABEL
Stack Relative	LDA 3,S
Stack Relative Indirect Indexed with Y	LDA (5,S),Y
Block Move	MVP 0,0
Absolute Long	LDA $02F000
Absolute Long Indexed with X	LDA $12D080, X
Absolute Indirect Long	JMP [$2000]
Direct Page Indirect Long	LDA [$55]
Direct Page Indirect Long Indexed with Y	LDA [$55], Y

New Instructions:

BRL	Branch always long	REP	Reset status bits
COP	Co-processor empowerment	RTL	Return from subroutine long
JML	Jump long	SEP	Set status bits
JSL	Jump to subroutine long	STP	Stop the processor
MVN	Block move negative	TCD	Transfer 16-bit accumulator to direct page register
MVP	Block move positive	TCS	Transfer accumulator to stack pointer
PEA	Push effective absolute address onto stack	TDC	Transfer direct page register to 16-bit accumulator
PEI	Push effective indirect address onto stack	TSC	Transfer stack pointer to 16-bit accumulator
PER	Push effective PC relative address onto stack	TXY	Transfer index registers X to Y
PHB	Push data bank register onto stack	TYX	Transfer index registers Y to X
PHD	Push direct page register onto stack	WAI	Wait for interrupt
PHK	Push program bank register onto stack	WDM	Reserved for future two-byte opcodes
PLB	Pull data bank register from stack	XBA	Exchange the B and A accumulators
PLD	Pull direct page register from stack	XCE	Exchange carry and emulation bits

Interrupt Vector Locations:

Vector	Emulation Mode	Native Mode
IRQ	$FFFE, $FFFF	$FFEE, $FFEF
RESET	$FFFC, $FFFD	-
NMI	$FFFA, $FFFB	$FFEA, $FFEB
ABORT	$FFF8, $FFF9	$FFE8, $FFE9
BRK	-	$FFE6, $FFE7
COP	$FFF4, $FFF5	$FFE4, $FFE5

Notes: All locations are in bank zero.