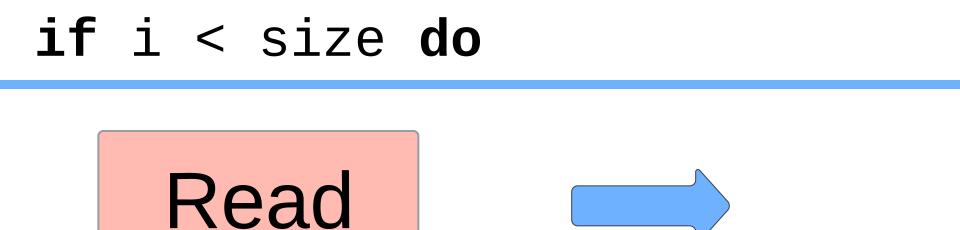
```
// Engine: ENGINE_CSR_SEQ_1, Number of entries: 10
0x0000001
// entry_0 < 5b>:
// increment[0:0]=1 || decrement[1:1]=0
// mode_sequence[2:2]=0 || mode_buffer[3:3]=0 || mode_break[4:4]=0
0x0000000
// entry_1 <32b>:
// index_start[0:31]=0x0000000
0x0000000
// entry_2 <32b>:
// index_end[0:31]=0x0000000
0x0000001
// entry 3 <32b>:
// stride[0:31]=0x0000001
0x0000000
// entry_4 <32b>:
// shift.amount[0:30]=0 || shift.direction[31:31]=0
0x0000120
// entry_5 <29b>:
// cmd[0:6]=CMD_ENGINE || buffer[7:12]=STRUCT_ENGINE_SETUP
// id_module[13:20]=0x00 || id_engine[21:28]=0x00
0x01030201
// entry_6 <32b>:
// id_cu[0:7]=0x01 || id_bundle[8:15]=0x02 ||
// id_lane[16:23]=0x03 || id_buffer[24:31]=0x01
0x0000000
// entry_7 <32b>:
// array_pointer[0:31]=0x0000000
0x0000000
// entry_8 <32b>:
//array_pointer[0:31]=0x0000000
0x0000000
// entry_9 <32b>:
//array_size[0:31]=0x00000000
```

Bundle F

CU Setup Engine

Program Mode	
Operation 7 Bits	MEM_READ
Size 32 Bits	overlay_program
array_pointer 64	overlay_program
Result 4 Bytes	entry[i]=BFS,PR,





Memory

CU Cache

GLay

Bundle 0-3

Cast Bits

Cast Bits

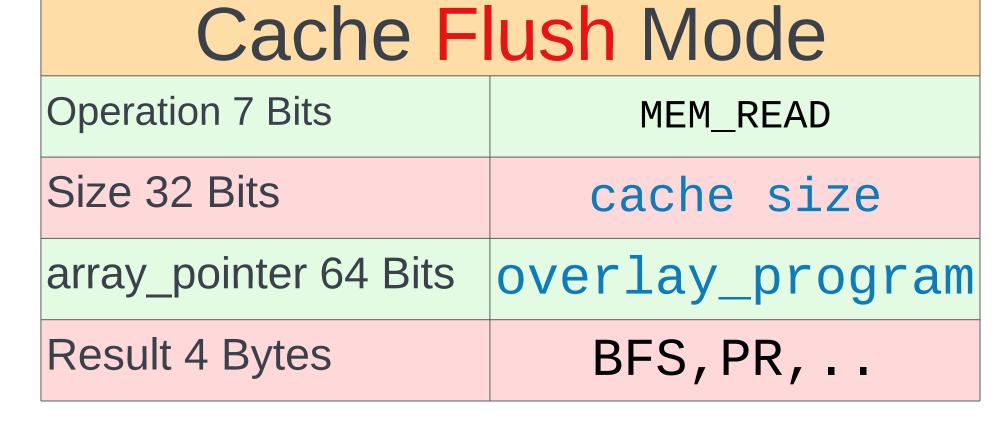
Lane 0 0

Lane 0 1

Lane 1

Lane 2

Lane 3



if i < size do</pre>

