

2025 Digital IC Design Homework 4

NAME	章元豪		
Student ID	N26132314		
ATCONV Simulation Result			
Functional simulation	Pass	Pre-Layout simulation	Pass
<pre># ----- SUMMARY ----- # # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # # terminate at 50181 cycle # ----- # # ** Note: \$finish : C:/Users/Beethovenjoker/Desktop/CONV/ATCONV/testfixture.sv(224) # Time: 2509050 ns Iteration: 0 Instance: /testfixture # # # ----- SUMMARY ----- # # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # # terminate at 50181 cycle # ----- # # ** Note: \$finish : C:/Users/Beethovenjoker/Desktop/CONV/ATCONV/testfixture.sv(224) # Time: 2509050 ns Iteration: 0 Instance: /testfixture # # # ----- SUMMARY ----- # # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # # terminate at 50181 cycle # ----- # # ** Note: \$finish : C:/Users/Beethovenjoker/Desktop/CONV/ATCONV/testfixture.sv(224) # Time: 2509050 ns Iteration: 0 Instance: /testfixture # #</pre>		<pre># ----- SUMMARY ----- # # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # # terminate at 50181 cycle # ----- # # ** Note: \$finish : C:/Users/Beethovenjoker/Desktop/CONV/ATCONV/testfixture.sv(224) # Time: 2509058470 ps Iteration: 0 Instance: /testfixture # # ----- SUMMARY ----- # # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # # terminate at 50181 cycle # ----- # # ** Note: \$finish : C:/Users/Beethovenjoker/Desktop/CONV/ATCONV/testfixture.sv(224) # Time: 2509058470 ps Iteration: 0 Instance: /testfixture # # ----- SUMMARY ----- # # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # # terminate at 50181 cycle # ----- # # ** Note: \$finish : C:/Users/Beethovenjoker/Desktop/CONV/ATCONV/testfixture.sv(224) # Time: 2509058470 ps Iteration: 0 Instance: /testfixture # #</pre>	
System Simulation Result			
Functional simulation	Pass	Pre-Layout simulation	Pass
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ATCONV Synthesis Result			
Total logic elements	410/55856 (<1%)		
Total memory bits	0/2,396,160 (0%)		
Total registers	147		
Embedded multiplier 9-bit elements	2/308 (<1%)		
Total Cycle used	50,181		

Flow Summary

 <<Filter>>

Flow Status	Successful - Tue May 27 00:22:42 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	410 / 55,856 (< 1 %)
Total registers	147
Total pins	124 / 325 (38 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

System Synthesis Result

Total logic elements	538/55,856 (<1%)
Total memory bits	0/2,396,160 (0%)
Total registers	147
Embedded multiplier 9-bit elements	2/308 (<1%)
Total Cycle used	50181

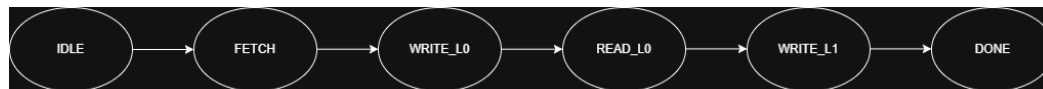
Flow Summary

 <<Filter>>

Flow Status	Successful - Tue May 27 00:42:56 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	top
Top-level Entity Name	top
Family	Cyclone IV E
Device	EP4CE55F23A7
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Total logic elements	538 / 55,856 (< 1 %)
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Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

ATCONV:



起始狀態為 IDLE，接著進入 FETCH 階段從 ROM 取得卷積所需的資料。由於每次卷積需進行九次乘法與一次加法，我用單一 Buffer 依序從 ROM 擷取資料，並將結果累加至另一個 Buffer 中。因為我這學期有修人工智慧晶片，因此我有想說設計重複利用的 filter 以降低 cycle 數。然而，這樣雖然提升了運算效率，但也讓控制邏輯變得更複雜，導致整體硬體面積增加，所以後來就保持原樣。

接著進入 READ_L0 階段，從 Layer 0 的 SRAM 中讀取卷積結果，進行 MaxPooling，然後進入 WRITE_L1 階段，將 MaxPooling 後的結果寫入 Layer 1 的 SRAM。最後系統進入 DONE 狀態，完成整個運算流程。

System:

這次要按照簡化版 AXI-Protocol 來撰寫，其實沒有到很複雜，只是將線包成 AXI Interface 讓 Master 和 Slave 進行溝通。

