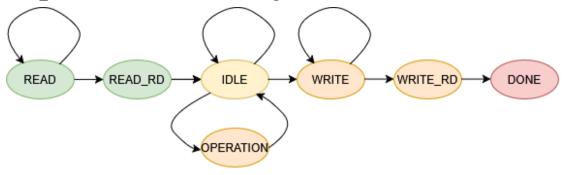
2025 Digital IC Design Homework 2

NAME	章元豪	ar ie Design ii			
Student ID	N26132314				
		ional Simulation	Result		
Pattern1					
Pass	Pass	Pass	Pass	Pass	
Pattern 1					
VSIM 2> run -all					
# All data have b	een generated succe	ssfully!			
• ////////////////////////////////////					
# / _ # / Congratulations !! / / 0.0					
# / / /					
# / ^ ^ ^ w # /////////////////////////////////					
Į.	///////////////////////////////////////	////////////// \m <u> </u>			
<pre># # ** Note: \$finish : D:/file/testfixture.sv(162)</pre>					
# Time: 1345 ns Iteration: 0 Instance: /testfixture					
<pre># 1 # Break in Module testfixture at D:/file/testfixture.sv line 162</pre>					
Pattern 2					
VSIM 2> run -all # All data have been generated successfully!					
# # ///////////////////////////////////					
į.	1	/ 1_			
# #	/ Congratulatio	ns!! / /0.			
*	/ Simulation PA	ss !! / / / / / / / / / / / / / / / / /			
1	'mmmmmm	//////// \mm			
#					
* ** Note: \$finish : D:/file/testfixture.sv(162) * Time: 1405 ns Iteration: 0 Instance: /testfixture					
# 11me: 1405 ns	s Iteration: U Ins	tance: /testilxture			
# Break in Module	testfixture at D:/f	ile/testfixture.sv l	ine 162		
Pattern 3					
VSIM 2> run -all	n generated successful	101			
#	ā.				
*		/ 1_11			
:	/ Congratulations !	/ /			
÷	/ Simulation PASS !	i / /^ ^ ^ w			
:	111111111111111111111111111111111111111	///// \mm_l_l			
# ** Note: Sfinish	: D:/file/testfixtu	re.sv(162)			
	Iteration: 0 Instanc				
The second secon	estfixture at D:/file/	testfixture.sv line 16	2		
		Pattern 4			
		1 4110111 4			

```
VSIM 2> run -all
 All data have been generated successfully!
                     Congratulations !!
                        Simulation PASS !!
# ** Note: $finish
                     : D:/file/testfixture.sv(162)
    Time: 1565 ns Iteration: 0 Instance: /testfixture
# Break in Module testfixture at D:/file/testfixture.sv line 162
                                                Pattern 5
VSIM 2> run -all
# All data have been generated successfully!
                     Congratulations !!
                     Simulation PASS !!
                   Note: $finish : D:/file/testfixture.sv(162)
Time: 1605 ns Iteration: 0 Instance: /testfixture
# ** Note: $finish
# Break in Module testfixture at D:/file/testfixture.sv line 162
```

LCD_CTRL Finite-State Machine Design:



這個狀態機從 READ 狀態開始,會不斷由位址遞增讀取 IROM 直到到達最後一筆;為了確保最尾端的第 64 筆資料也能讀入,特地在讀取結束後多留一個週期進入 READ_RD 狀態,讓最後一筆完成寫入`ImageBuffer。接著進入IDLE,在這裡可根據使用者指令切換到 OPERATION(進行Shift/Max/Min/Average 等運算)或進入 WRITE (把結果寫回 IRAM)。同樣地,寫到最後一筆(位址 63)後,會進到 WRITE_RD 狀態,確保最尾端資料也能穩定寫入 IRAM,最後再進入 DONE 表示整個流程結束。