2025 Digital IC Design Homework 5

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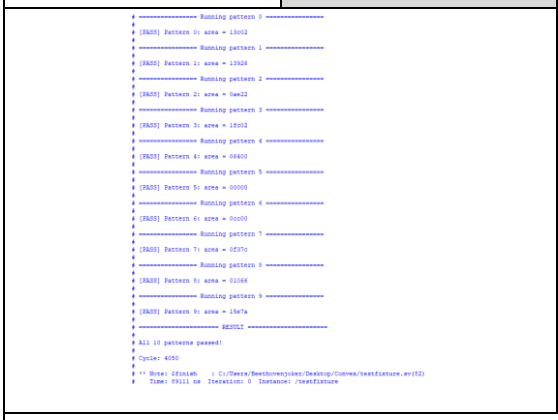
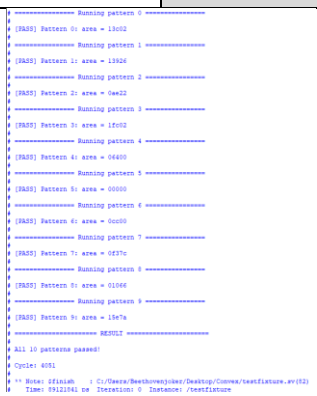
Simulation Result

Functional simulation	Pass	Pre-Layout simulation	Pass





Synthesis Result

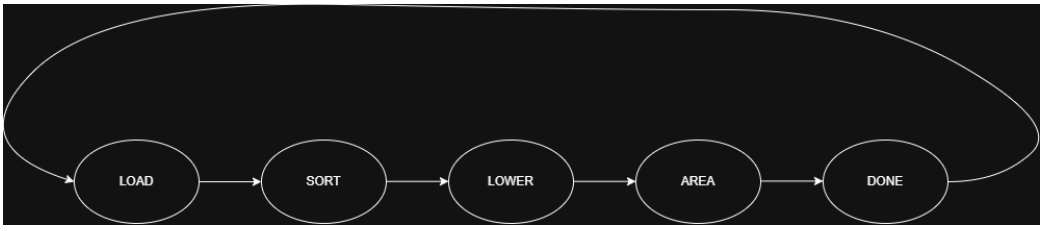
Total logic elements	3,290/55,856 (6%)
Total memory bits	0/2,396,160 (0%)
Total registers	497
Embedded multiplier 9-bit elements	6/308 (2%)
Clock period (ns)	22
Total Cycle used	4051

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Jun 03 04:09:20 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	MCH
Top-level Entity Name	MCH
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	3,290 / 55,856 (6 %)
Total registers	497
Total pins	36 / 325 (11 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	6 / 308 (2 %)
Total PLLs	0 / 4 (0 %)

Description of your design



我是照講義中的演算法來實作。首先，在 LOAD 階段會輸入 20 個點的座標，接著從中找出 Y 座標最小、X 座標最小的那個點作為 Anchor。接下來，利用 Anchor 當作基準，計算每個點的極角座標，並使用泡排序（Bubble Sort）將所有點依照極角大小排列。排序完成後，進入 LOWER 階段，也就是 Graham Scan 的主體：透過外積（Cross Product）來判斷是否是左轉，只有形成左轉的點才會被保留在 Stack 中，從而構成一個正確的凸包（Convex Hull）。最後，在 AREA 階段使用 Shoelace Formula 計算多邊形的面積，計算完成後進入 DONE 狀態並輸出結果。