

2025 Digital IC Design Homework 5

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Student ID	N26132314		
Simulation Result			
Functional simulation	Pass	Pre-Layout simulation	Pass
<pre>##### Building pattern 0 ##### # (F805) Pattern 0: a0a = 130d2 ##### Building pattern 1 ##### # (F805) Pattern 1: a0a = 130d4 ##### Building pattern 2 ##### # (F805) Pattern 2: a0a = 0a4d2 ##### Building pattern 3 ##### # (F805) Pattern 3: a0a = 1f0d2 ##### Building pattern 4 ##### # (F805) Pattern 4: a0a = 0d4d0 ##### Building pattern 5 ##### # (F805) Pattern 5: a0a = 0d0d0 ##### Building pattern 6 ##### # (F805) Pattern 6: a0a = 0d0d0 ##### Building pattern 7 ##### # (F805) Pattern 7: a0a = 0d37c ##### Building pattern 8 ##### # (F805) Pattern 8: a0a = 010d4 ##### Building pattern 9 ##### # (F805) Pattern 9: a0a = 15a7a ##### RESULT ##### All 10 patterns passed! Cycle: 4050 ** Note: ifconfig : C:/Users/Beachomejones/Desktop/Contra/testFixture.vv(92) Time: 091114 on Iteration: 0 Success: /testFixture</pre>		<pre>##### Building pattern 0 ##### # (F805) Pattern 0: a0a = 130d2 ##### Building pattern 1 ##### # (F805) Pattern 1: a0a = 130d4 ##### Building pattern 2 ##### # (F805) Pattern 2: a0a = 0a4d2 ##### Building pattern 3 ##### # (F805) Pattern 3: a0a = 1f0d2 ##### Building pattern 4 ##### # (F805) Pattern 4: a0a = 0d4d0 ##### Building pattern 5 ##### # (F805) Pattern 5: a0a = 0d0d0 ##### Building pattern 6 ##### # (F805) Pattern 6: a0a = 0d0d0 ##### Building pattern 7 ##### # (F805) Pattern 7: a0a = 0d37c ##### Building pattern 8 ##### # (F805) Pattern 8: a0a = 010d4 ##### Building pattern 9 ##### # (F805) Pattern 9: a0a = 15a7a ##### RESULT ##### All 10 patterns passed! Cycle: 4051 ** Note: ifconfig : C:/Users/Beachomejones/Desktop/Contra/testFixture.vv(92) Time: 091204 on Iteration: 0 Success: /testFixture</pre>	
Synthesis Result			
Total logic elements	3,290/55,856 (6%)		
Total memory bits	0/2,396,160 (0%)		
Total registers	497		
Embedded multiplier 9-bit elements	6/308 (2%)		
Clock period (ns)	22		
Total Cycle used	4051		

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Jun 03 04:09:20 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	MCH
Top-level Entity Name	MCH
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	3,290 / 55,856 (6 %)
Total registers	497
Total pins	36 / 325 (11 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	6 / 308 (2 %)
Total PLLs	0 / 4 (0 %)

Description of your design

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graph LR; LOAD --> SORT; SORT --> LOWER; LOWER --> AREA; AREA --> DONE; DONE --> LOAD;
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我是照講義中的演算法來實作。首先，在 **LOAD** 階段會輸入 20 個點的座標，接著從中找出 **Y** 座標最小、**X** 座標最小的那個點作為 **Anchor**。接下來，利用 **Anchor** 當作基準，計算每個點的極角座標，並使用泡排序（**Bubble Sort**）將所有點依照極角大小排列。排序完成後，進入 **LOWER** 階段，也就是 **Graham Scan** 的主體：透過外積（**Cross Product**）來判斷是否是左轉，只有形成左轉的点才會被保留在 **Stack** 中，從而構成一個正確的凸包（**Convex Hull**）。最後，在 **AREA** 階段使用 **Shoelace Formula** 計算多邊形的面積，計算完成後進入 **DONE** 狀態並輸出結果。