2025 Digital IC Design Homework 2

NAME	章元豪
Student ID	N26132314

Functional Simulation Result

Pattern1	Pattern2	Pattern3	Pattern4	Pattern5
Pass	Pass	Pass	Pass	Pass

Pattern 1

```
VSIM 2> run -all
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / 0.0  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/file/testfixture.sv(162)
#    Time: 1345 ns  Iteration: 0  Instance: /testfixture
# 1
# Break in Module testfixture at D:/file/testfixture.sv line 162
```

Pattern 2

```
VSIM 2> run -all
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / 0.0  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/file/testfixture.sv(162)
#    Time: 1405 ns  Iteration: 0  Instance: /testfixture
# 1
# Break in Module testfixture at D:/file/testfixture.sv line 162
```

Pattern 3

```
VSIM 2> run -all
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / 0.0  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/file/testfixture.sv(162)
#    Time: 1485 ns  Iteration: 0  Instance: /testfixture
# 1
# Break in Module testfixture at D:/file/testfixture.sv line 162
```

Pattern 4

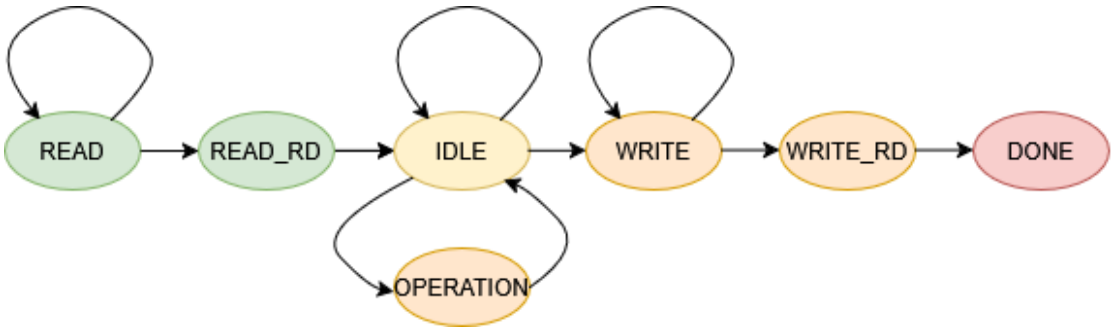
```
VSIM 2> run -all
# All data have been generated successfully!
#
#                    //////////////////////////
#                    /                       /       |__||
#                    /  Congratulations !!   /      / 0.0  |
#                    /                       /    /_____   |
#                    /  Simulation PASS !!   /   /^ ^ ^ \  |
#                    /                       /  |^ ^ ^ ^ |w|
#                    //////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/file/testfixture.sv(162)
#    Time: 1565 ns  Iteration: 0  Instance: /testfixture
# 1
# Break in Module testfixture at D:/file/testfixture.sv line 162

VSIM 3>
```

Pattern 5

```
VSIM 2> run -all
# All data have been generated successfully!
#
#                    //////////////////////////
#                    /                       /       |__||
#                    /  Congratulations !!   /      / 0.0  |
#                    /                       /    /_____   |
#                    /  Simulation PASS !!   /   /^ ^ ^ \  |
#                    /                       /  |^ ^ ^ ^ |w|
#                    //////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/file/testfixture.sv(162)
#    Time: 1605 ns  Iteration: 0  Instance: /testfixture
# 1
# Break in Module testfixture at D:/file/testfixture.sv line 162
```

LCD_CTRL Finite-State Machine Design:



這個狀態機從 READ 狀態開始，會不斷由位址遞增讀取 IROM 直到到達最後一筆；為了確保最尾端的第 64 筆資料也能讀入，特地在讀取結束後多留一個週期進入 READ_RD 狀態，讓最後一筆完成寫入`ImageBuffer。接著進入 IDLE，在這裡可根據使用者指令切換到 OPERATION（進行 Shift/Max/Min/Average 等運算）或進入 WRITE（把結果寫回 IRAM）。同樣地，寫到最後一筆（位址 63）後，會進到 WRITE_RD 狀態，確保最尾端資料也能穩定寫入 IRAM，最後再進入 DONE 表示整個流程結束。