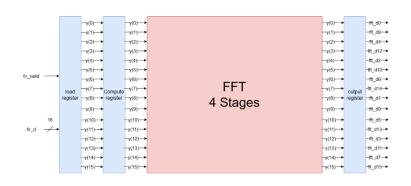
2025 Digital IC Design Homework 3

NAME		章元豪			
Student ID	N261	N26132314			
Simulation Result					
Functional simulation		Pass		Pre-Layout	Pass
				simulation	
				Please specify your clock	
Congratulations! All data have been generated successfully! Congratulations! All data have been generated successfully!				width: 16 (ns) Comparaisation* All data here been persected successfully! Total use 1044 cycles to complete similation. Time: 1612041 ps Totalcastinuture.pr(110) Time: 1612042 ps Totalcastinuture.	
#					
Synthesis Result					
Total logic elements			5588/55856(10%)		
Total memory bits			0/2396160(0%)		
Total registers			1259		
Embedded multiplier 9-bit elements			128/308(42%)		
Flow Status Quartus Prime Version Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total registers Total pins Total virtual pins Total memory bits Embedded Multiplier 9-bit elements Total PLLs	Successful - Sat May 03 02 20.1.1 Build 720 11/11/20 FFT FFT Cyclone IV E EP4CE55F23A7 Final 5,588 / 55,856 (10 %) 1259 277 / 325 (85 %) 0 0 / 2,396,160 (0 %) 128 / 308 (42 %) 0 / 4 (0 %)				
Description of your design					



基本上 butterfly Unit 就是按照助教的電路圖來接就行,然後接之前要睡飽或是喝咖啡,不然很容易接錯。分四個 stage 來計算,因為這裡涉及最多運算單元,所以會大幅度地影響到 clock width 。

在輸入部分,fir_d 會持續地送入資料且不採用 handshake 機制,因此我就不設計額外的狀態機來管理資料流。我採用了類似 pipeline 的方式,讓輸入資料流經 load register 後,直接提供給 compute register 做 FFT 運算。每當累積完 16 筆資料後,即可立即進行 FFT 計算。計算過程與下一批資料的讀入可並行處理,因此只要在下一批 16 筆資料完全接收前完成當前的 FFT 運算,並利用兩個 clock 將計算結果輸出即可。