2025 Digital IC Design Homework 3

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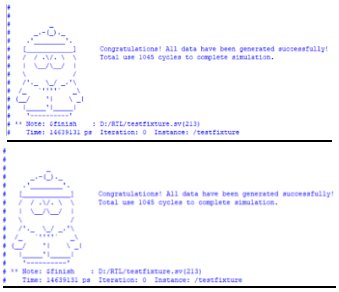
Simulation Result

Functional simulation	Pass	Pre-Layout simulation	Pass

```
#
#
#
#      _.-(_).-_
#    .'_________'.
#   [_____________]      Congratulations! All data have been generated successfully!
#   /  / .\/. \  \       Total use 1043 cycles to complete simulation.
#   |  \__/\__/  |
#   \            /
#   /'._  \_/  _.'\
#  /_    `'''`    _\
# (__/     '|     \_|
#   |_____'|_____|
#    '-----------'
# ** Note: $finish    : D:/file/testfixture.sv(213)
#    Time: 31320 ns  Iteration: 0  Instance: /testfixture
```

Please specify your clock width: 14 (ns)



Synthesis Result

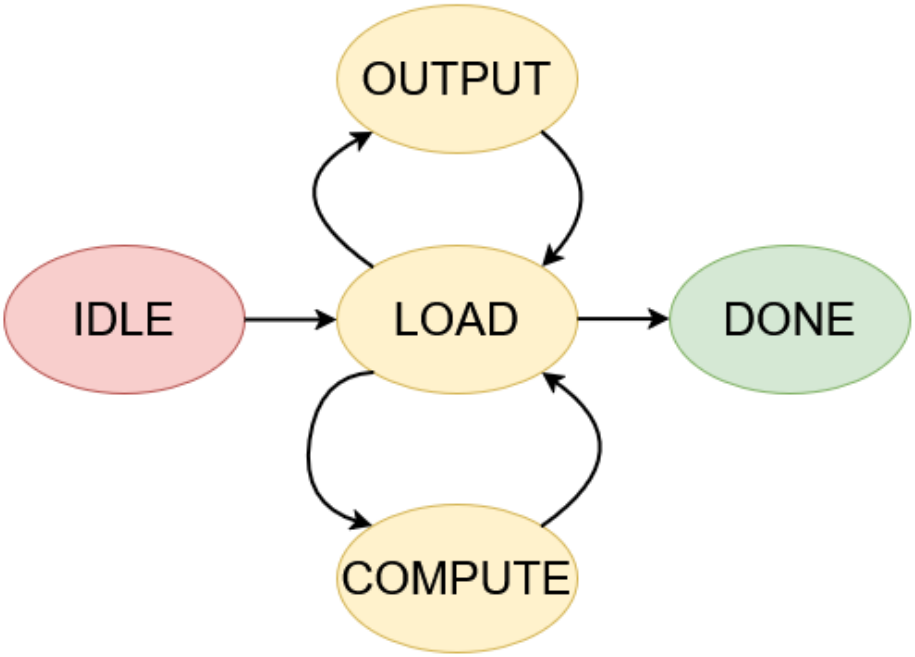
Total logic elements	5,625/55,856(10%)
Total memory bits	0/2,396,160(0%)
Total registers	1266
Embedded multiplier 9-bit elements	128/308(42%)

Flow Summary

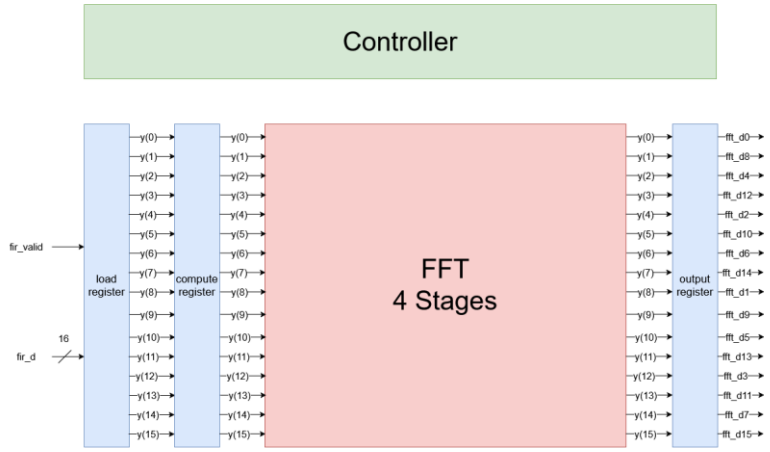
<<Filter>>

Flow Status	Successful - Sun May 04 21:57:55 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	FFT
Top-level Entity Name	FFT
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	5,625 / 55,856 (10 %)
Total registers	1266
Total pins	277 / 325 (85 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	128 / 308 (42 %)
Total PLLs	0 / 4 (0 %)

Description of your design



我分了五個 State ，初始化為 `IDLE` 階段，如果收到 TB 傳來的 fir_valid 就開始進入 `LOAD` 。 接完 16 筆資料就可以進入 `COMPUTE` 把資料丟給 Butterfly_Unit 來運算，算完之後在接下一組的資料期間進到 `OUTPUT` ，把剛剛存在 Output 暫存器的資料輸出給 TB，然後回到 `LOAD` 繼續接資料，最後全部算完就可以進入 `DONE` 。



基本上 Butterfly_Unit 就是按照助教的電路圖來接就行，然後接之前要睡飽或是喝咖啡，不然很容易接錯。分四個 stage 來計算，因為這裡涉及最多運算單元，所以會大幅度地影響到 clock width 。