

2025 Digital IC Design Homework 5

NAME	章元豪																														
Student ID	N26132314																														
Simulation Result																															
Functional simulation	Pass	Pre-Layout simulation	Pass																												
<pre># ===== RESULT ===== # # All 10 patterns passed! # # Cycle: 2608 # # ** Note: \$finish : D:/Convex/testfixture.sv(82) # Time: 54778500 ps Iteration: 0 Instance: /testfixture</pre>		<pre># ===== RESULT ===== # # All 10 patterns passed! # # Cycle: 2609 # # ** Note: \$finish : D:/Convex/testfixture.sv(82) # Time: 54788695 ps Iteration: 0 Instance: /testfixture</pre>																													
Synthesis Result																															
Total logic elements	2,487 / 55,856 (4%)																														
Total memory bits	0 / 2,396,160 (0%)																														
Total registers	514																														
Embedded multiplier 9-bit elements	6/308 (2%)																														
Clock period (ns)	21																														
Total Cycle used	2608																														
Flow Summary																															
<<Filter>>																															
<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Flow Status</td> <td>Successful - Fri Jun 06 06:14:31 2025</td> </tr> <tr> <td>Quartus Prime Version</td> <td>20.1.1 Build 720 11/11/2020 SJ Lite Edition</td> </tr> <tr> <td>Revision Name</td> <td>MCH</td> </tr> <tr> <td>Top-level Entity Name</td> <td>MCH</td> </tr> <tr> <td>Family</td> <td>Cyclone IV E</td> </tr> <tr> <td>Device</td> <td>EP4CE55F23A7</td> </tr> <tr> <td>Timing Models</td> <td>Final</td> </tr> <tr> <td>Total logic elements</td> <td>2,487 / 55,856 (4 %)</td> </tr> <tr> <td>Total registers</td> <td>514</td> </tr> <tr> <td>Total pins</td> <td>36 / 325 (11 %)</td> </tr> <tr> <td>Total virtual pins</td> <td>0</td> </tr> <tr> <td>Total memory bits</td> <td>0 / 2,396,160 (0 %)</td> </tr> <tr> <td>Embedded Multiplier 9-bit elements</td> <td>6 / 308 (2 %)</td> </tr> <tr> <td>Total PLLs</td> <td>0 / 4 (0 %)</td> </tr> </table>				Flow Status	Successful - Fri Jun 06 06:14:31 2025	Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition	Revision Name	MCH	Top-level Entity Name	MCH	Family	Cyclone IV E	Device	EP4CE55F23A7	Timing Models	Final	Total logic elements	2,487 / 55,856 (4 %)	Total registers	514	Total pins	36 / 325 (11 %)	Total virtual pins	0	Total memory bits	0 / 2,396,160 (0 %)	Embedded Multiplier 9-bit elements	6 / 308 (2 %)	Total PLLs	0 / 4 (0 %)
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Description of your design																															



我是照講義中的演算法來實作。首先，在 **LOAD** 階段會輸入 20 個點的座標，接著從中找出 **Y** 座標最小、**X** 座標最小的那個點作為 **Anchor**。接下來，利用 **Anchor** 當作基準，計算每個點的極角座標，並使用 **Insertion Sort** 將所有點依照極角大小排列。排序完成後，進入 **LOWER** 階段，也就是 **Graham Scan** 的主體：透過外積（**Cross Product**）來判斷是否是左轉，只有形成左轉的点才會被保留在 **Stack** 中，從而構成一個正確的凸包（**Convex Hull**）。最後，在 **AREA** 階段使用 **Shoelace Formula** 計算多邊形的面積，計算完成後進入 **DONE** 狀態並輸出結果。