Anirudha Behera

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OBJECTIVE

As a Certified VLSI Physical Design Engineer, I possess extensive expertise in ASIC design, specifically in the RTL to GDSII flow. Throughout my academic journey, I have consistently demonstrated proficiency in utilizing industry-leading EDA tools such as Synopsys, Cadence, Mentor Graphics, and Xilinx, achieving exceptional results. Moreover, I have gained valuable hands-on experience through FPGA projects, effectively utilizing FPGA boards. I am currently seeking an entry-level role where I can apply my skills, contribute to a dynamic team, and continue to learn and grow in my engineering career.

EDUCATION

Master of Science in Electrical and Computer Engineering *CGPA: 3.5/4*
ILLINOIS INSTITUTE OF TECHNOLOGY (IIT), CHICAGO, USA *Jan 2022-Present*
Coursework: Introduction to VLSI, CAD Techniques for VLSI Design, High-Performance VLSI/IC Systems, Digital SoC Design, Computer Organization, and Design, Radio Frequency IC Design, Hybrid Electric Vehicle Drives, Adjustable Speed Drives, Robust Control

Bachelor of Technology in Electrical Engineering *CGPA: 8.1/10*
BIJU PATNAIK UNIVERSITY OF TECHNOLOGY (BPUT), ROURKELA, INDIA *Aug 2014 – July 2018*

TECHNICAL SKILLS

Programming Skills: Proficient in VHDL, Verilog, System Verilog, Basics of TCL/Tk, Python, C
EDA Tools/Debug Tools: Synopsys Design Compiler, Formality, IC Compiler II, Prime Time, Cadence Virtuoso, Encounter, SimVision, Mentor Graphics Calibre, ModelSim, Xilinx Vivado, Hspice, CosmosScope, CACTI, WATCH, Virtual Studio, PyCharm, CodeBlocks
Operating Systems: Linux/Unix, Microsoft Windows, MacOS

TECHNICAL PROJECTS (https://github.com/BeheraAnirudh)

Hierarchical Schematic and Layout Design of 4-bit Carry Look-ahead Adder

- Designed a 4-bit CLA adder schematic, Symbol, Testing Circuit, and Layout using Virtuoso.
- Performed LVS, DRC, and PEX using MG Calibre. Then Formal verification is performed using Formality.
- Measured Power, Delay, and temperature using HSPICE.

Standard Cell-Based ASIC Design for 8-bit Accumulator

- Implemented Verilog code and Testbench for the 8-bit Accumulator, then synthesized the RTL codes.
- Executed Logical Synthesis process using DC tool, and recorded area, power, and timing reports. Performed PnR using Encounter. After PnR buffers are added and then performed Post PnR and recorded optimized area, power, and timing results, and performed Formal verification. Collected GDSII file and plotted the final Layout.

Case Study of the 32-bit Pipelined CPU Design with Modified New ALU Architecture

- Implemented 5 different 32-bit CPU architectures using standard ASIC flow to achieve desired slack time. 4 of them were using CRA, CLA, CSA, and CSeA Adders. The 5th one is with Comparator and CLA adder.
- Performed RTL Synthesis, Logic Synthesis, PnR, and Post PnR, for each design, and initial slack time and final optimized slack time were recorded with power and area reports. Finally, GDSII Layout files were collected.

CAD Tool Design for Static Timing Analysis by using Tcl/Tk and C Programming

- Designed C code to calculate the required time, arrival time, and slack time from the given input matrix file and save the output file separately.
- Designed a Static Timing Analysis CAD tool GUI using TCL/Tk, which can take inputs from the user and optimize the given input matrix using implemented C code and display the output results on the GUI interface.

MMP Configuration for Ultra-low Power Design in Modern VLSI

- **System Level Optimization:** Designed C code for Graph-based slack time analysis method, then reduced the power consumption of the program using Loop unrolling techniques and measured the power using WATCH tool. To minimize further power, catch optimization technique is used and power is measured using the CACTI tool. A total of 85.68% power saving was recorded.
- **RTL Level Optimization:** Implemented ACG, CCG, OCCG, LECG, ECG, and hybrid techniques on a Mobile Multimedia Processor design (MMP) to reduce power consumption by modifying the RTL source code accordingly. Up to 109.75% power saving recorded. Formality and ModelSim were used for equality check and synthesis then Power Compiler is used for power measurement.

PROFESSIONAL EXPERIENCE

- **IC Physical Design Internship, 14nm FinFET PDK library** *Sep 2022-Mar 2023*
  CHIPEDGE TECHNOLOGIES, Chennai, India

Skills: Synthesis, Floorplan, Power Plan, Placement, Clock Tree Synthesis, Routing, Signoff Checks, Static Timing Analysis, Parasitic Extraction, Physical Verification, DFT**,** UVM
EDA Tools: Synopsys IC Compiler II, Prime Time, Mentor Graphics Calibre, Formality, Design Compiler, Linux/Unix

CERTIFICATIONS

- **Essentials of Linux, ChipEdge Technology**
  Linux Commands
- **Google IT Automation with Python Professional Certificate, Coursera**
  Crash Course on Python, Using Python to Interact with Operating System, Introduction to Git and GitHub, Troubleshooting and Debugging Techniques, Configuration Management and the Cloud, Automating Real-World Tasks with Python
- **IBM Data Warehouse Engineer Professional Certificate on Linux commands and Shell Scripting, Coursera**
  Introduction to Linux, Introduction to Linux Commands, Introduction to Shell Scripting, Term Project
- **VHDL for FPGA Engineer with Vivado design suite by Kumar Khandagle, UDEMY**
  VHDL, Xilinx Vivado HL, FPGA Flow, IP Integration
- **Verilog for FPGA Engineer with Vivado design suite by Kumar Khandagle, UDEMY**
  Verilog, Xilinx Vivado HL, FPGA Flow, IP Integration
- **Master C programming, UDEMY**

RESEARCH PAPER

- Design and Performance Evaluation of FPGA-based Audio Systems on ZedBoard-Zynq SoC
- High Performance VLSI PVT-Aware Design for 10T SRAM with Dedicated Noise Trimming Circuit using 15nm FinFET