ANIRUDHA BEHERA
Physical Design Engineer

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Objective

In pursuit of an entry-level Physical Design Engineer role, I offer expertise in RTL2GDSII flow for advanced technology nodes. My skill set encompasses synthesis, place & route, CTS, STA convergence, and signoff DRC/LVS closure, complemented by strong automation proficiency in TCL, Shell, and Python scripting, I bring 1 year of hands-on Physical Design and 2 years of successful business management experience with record of accomplishments. Well-versed in key tools like DC, ICC2/Innovus, StarRC, ICV and Primetime etc.

Experience

Physical Design Engineer   **09/2022 to 10/2023**
ChipEdge Technology   **Bengaluru, India**

- Led end-to-end design phases, encompassing Logic Synthesis, Floorplan, Placement, Clock Tree Synthesis (CTS), Routing and Optimization. Carefully balanced Quality of Results (QOR) against Power, Performance, and Area (PPA).
- Demonstrated expertise in creating efficient power grids (PG grids) and standard cell rails with innovative methods.
- Ensured design integrity during Sign-off by managing parasitic elements and SPEF files and progressively resolving DRC, LVS, ERC, EM/IR, PERC, ANTENNA, and LEC issues.
- Analyzed Timing constraints and resolved STA violations through holistic strategies for designs with up to 5 million standard cell instances and over 80 macros.
- Employed ECO cycles and extensive manual debugging for successful GDSII tape-out.
- Proficient in advanced technology nodes, utilizing advanced Shell and TCL scripting for effective debugging across the entire Physical Design process from RTL to GDSII.

Business Development Associate (BDA)   **01/2021 to 12/2021**
Think & Learn Pvt Ltd (BYJU'S)   **India, Bengaluru**

- Conducted personalized counseling sessions to match clients with suitable product segments and successfully managed to handle every deal from cold calling to product delivery period.
- Earned recognition as the highest-performing Business Development Associate (BDA) with exceptional customer retention due to strong communication, product knowledge, and work ethic.

Asst. MEP Site Engineer   **02/2019 to 02/2020**
Electron Electromechanical LLC   **Doha, Qatar**

- As Asst MEP Site Engineer, successfully managed a team of 20 technicians, 1 supervisor, and 2 foremen, ensuring daily site progress and effective coordination.
- Played a pivotal role in the "Doha Insurance Tower" Project, facilitating the seamless execution of MEP activities and enhancing project planning and resource management by providing on-site technical support and solutions.
- Maintained a strong focus on quality and safety by conducting inspections, enforcing standards, and consistently reporting project updates to senior management, resulting in punctual project completion and successful collaboration with contractors and vendors. My exceptional blend of interpersonal and technical skills was instrumental in the project's success.

Skills

- **Scripting/Programming Skills:** TCL, Shell Scripting, Python, VHDL, Verilog, C/C++, HTML5, CSS3
- **EDA Tools:** Synopsys IC Compiler II, Design Compiler, Prime Time, Star RC, IC Validator, Calibre, Formality, Cadence Virtuoso, Encounter, Model Sim, Hspice, Sim Vision, CACTI, WATCH, Xilinx Vivado
- **Soft Skills:** Leadership, Cross and Bottom-up Communication, Business Management, Customer Centric

Certifications

- Certified **Physical Design Engineer**, **ChipEdge Technology** - 2022
- Certified **Google IT Automation with Python**, **Coursera** - 2023
- Certified **IBM Data Professional Certificate on Linux commands and Shell Scripting** , **Coursera** - 2023
- Certified **VHDL and Verilog for FPGA Engineer with Vivado design suite** , **Udemy** - 2022

Education

Master of Science: **Electrical Engineering**   **Expected in 12/2023**

Illinois Institute of Technology   Chicago, IL

- Relevant Coursework: Introduction to VLSI, CAD Techniques for VLSI Design, High-Performance VLSI/IC Systems, Digital SoC Design, Computer Organization and Design, RF Integrated Circuit Design
- MSc in EE, GPA: 3.6
- Eta Kappa Nu Delta Chapter HKN-IEEE Government, Secretary General, 2023
- Research: **Design and Performance Evaluation of FPGA based Audio Systems on ZedBoard-Zynq SoC**, , Available at : https://www.ijert.org/design-and-performance-evaluation-of-fpgabased-audio-systems-on-zed-board-zynq-soc

B. Tech: **Electrical Engineering**   **07/2018**

Gandhi Institute For Technology   Bhubaneswar, India

- B. Tech in EE, GPA 8.1
- Department Ranked: 1 (5th to 8th Semester)

Academic Projects

Hierarchical Schematic and Layout Design of 4-bit Carry Look-ahead Adder.
- Designed a 4-bit CLA adder schematic, Symbol, Testing Circuit, and Layout using Virtuoso.
- Performed Physical Verifications (LVS, DRC) and Parasitic Extraction using Calibre. Then Formal verification is performed using Formality and measured Power, Delay, and temperature using HSPICE.

Standard Cell-Based RTL to GDSII Design for 8-bit Accumulator
- Developed RTL code and Testbench, synthesized using DC. Optimized Placement and Route with Encounter by adding buffers for area, power, timing then Completed Formal Verification, generated GDSII.

Standard Cell-Based 32-bit Pipelined CPU Design with Modified New ALU Architecture (RTL to GDSII)
- Implemented 5 CPU models with ASIC flow for slack time optimization.
- Executed Synthesis, PNR, and opt then recorded optimized slack time, power, area. Obtained GDSII Layout.
- Utilized CSeA, CLA, CRA and CSA adders and comparator-CLA mix designs and compared their performance.
- I found CSeA has the highest and CRA has lowest performance speed.

CAD Tool Design for Static Timing Analysis by using TCL/Tk and C Programming
- Designed C code to calculate the required time, arrival time, and slack time from the given input vectors and optimized the code to save the output file separately.
- Designed a Static Timing Analysis CAD tool GUI using TCL/Tk, which can take set of inputs from the user and optimize the given input vector using implemented C code and display the output results on the GUI interface.

Multimedia Mobile Processor Configuration for Ultra-low Power Design in Modern VLSI
- System-Level: Coded Graph-based slack analysis in C. Optimized with Loop unrolling and catch technique. WATCH and CACTI tools were used. Achieved 85.68% power reduction.
- RTL-Level: Applied ACG, CCG, OCCG, LECG, ECG, hybrid techniques on MMP. Achieved max 109.75% power reduction. Used Formality, Model Sim, Power Compiler (DC) tools.

Portfolios

- https://anirudhabehera.site/
- https://www.linkedin.com/in/abehera1/
- https://github.com/BeheraAnirudh