ANIRUDHA BEHERA

Physical Design Engineer

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SUMMARY

Dynamic and certified Physical Design Engineer with a robust background in Block-level design, adeptly navigating the Synopsys flow from Synthesis to Tape out while working with nodes as advanced as 14nm. Backed by one year of invaluable hands-on experience, I am now eager to channel my expertise into an entry-level role from December 2023.

EDUCATION

MSc. Electrical Engineering, ***ILLINOIS INSTITUTE OF TECHNOLOGY, Chicago, USA*** **Graduating Dec 2023**

Relevant Coursework: Introduction to VLSI, CAD Techniques for VLSI Design, High-Performance VLSI/IC Systems, Digital SoC Design, Computer Organization and Design, Radio Frequency IC Design

B. Tech in Electrical Engineering, ***GANDHI INSTITUTE FOR TECHNOLOGY, India*** **Aug 2014 – July 2018**

TECHNICAL SKILLS

Scripting/Programming Skills: TCL, Shell, Python, VHDL, Verilog, HTML5, CSS3, C

Physical Design Tools: IC Compiler II, Prime Time, Star RC, IC Validator, Calibre, Formality, Redhawk.

Standard Cell Design Tools: Virtuoso, Design Compiler, Encounter, Calibre, Model Sim, Hspice, Sim Vision, CACTI, WATCH

WORK EXPERIENCE

ChipEdge Technology, Bengaluru, India: Physical Design Engineer **Sep 2022- Present**

- Worked as a Physical Design Engineer Trainee at ChipEdge, where I received comprehensive training in the field.
- Progressed to an intern role, successfully completing two industry-standard projects: CHIPTOP and Falcon.
- Applied Block-Level design methodology and Synopsys tools proficiently throughout project lifecycles.
- Transitioned to an Intern position, contributing to critical real-time projects, namely DTMF and JBI**.**
- Led end-to-end design phases: Floorplan, Power Plan, Placement, CTS, Routing, and Optimization.
- Ensured design integrity by addressing DRC, LVS, EM/IR, and ANTENNA violations, utilizing ECO cycles and manual debugging by successfully taped out GDSII files, achieving impeccable design finalization.
- Demonstrated adeptness across technology nodes, including 14nm, 22nm, 28nm, and 32nm.
- Adept in intricate Floorplan, Placement, CTS, and Routing Designs, coupled with advanced Shell and TCL scripting for efficient debugging across the Physical Design flow.

Technical skills encompass Synthesis, Floorplan, Power Plan, Placement, CTS, Routing, and Sign Off Checks (DRC, LVS, IR/EM, LEC, STA, ANTENNA). Command over EDA Tools: IC Compiler II, Prime Time, Star RC, IC Validator, Formality, Calibre, and Redhawk.

ACADEMIC PROJECTS

Standard Cell-Based RTL to GDSII Design for 8-bit Accumulator

- Developed RTL code and Testbench, synthesized using DC. Optimized Placement and Route with Encounter by adding buffers for area, power, timing then Completed Formal Verification, generated GDSII.

Standard Cell-Based 32-bit Pipelined CPU Design with Modified New ALU Architecture (RTL to GDSII)

- Implemented 5 CPU models with ASIC flow for slack time optimization.
- Executed Synthesis, PNR, and opt then recorded optimized slack time, power, area. Obtained GDSII Layout.
- Utilized different adders and comparator-CLA mix designs and compared their performance.
- I found CSeA has the highest and CRA has lowest performance speed.

CAD Tool Design for Static Timing Analysis by using TCL/Tk and C Programming https://github.com/BeheraAnirudh/

- Designed C code to calculate the required time, arrival time, and slack time from the given input vectors and optimized the code to save the output file separately.
- Designed a Static Timing Analysis CAD tool GUI using TCL/Tk, which can take set of inputs from the user and optimize the given input vector using implemented C code and display the output results on the GUI interface.

Multimedia Mobile Processor Configuration for Ultra-low Power Design in Modern VLSI

- **System-Level:** Coded Graph-based slack analysis in C. Optimized with Loop unrolling and catch technique. WATCH and CACTI tools were used. Achieved 85.68% power reduction.
- **RTL-Level:** Applied ACG, CCG, OCCG, LECG, ECG, hybrid techniques on MMP. Achieved max 109.75% power reduction. Used Formality, Model Sim, Power Compiler (DC) tools.

LEADERSHIP EXPERIENCE

Eta Kappa Nu Delta Chapter IEEE, IIT, Chicago, USA: Secretary General **Mar 2023- Present**

- Technical documentation, managing email formatting, disseminated crucial updates to group, fostered teamwork, collaboration, and hosting technical events.

IEEE Region Zone-4, Chicago, USA: Student Volunteer **Jan 2022- Present**

CERTIFICATIONS

- **Google IT Automation with Python Professional Certificate, Coursera**
  Crash Course on Python**:** Dictionary, List, Tuple, OOPS, Inheritance, Composition, Modules, Automation
- **IBM Data Professional Certificate on Linux commands and Shell Scripting, Coursera**
  Unix/Linux, Linux Commands, Shell Scripting, Pipes, Filters, Loops, Scheduling Jobs using Cron, Automation
- **VHDL and Verilog for FPGA Engineer with Vivado design suite by Kumar Khandagle, Udemy**
  VHDL, Verilog, Xilinx Vivado HL, FPGA Flow, IP Integration