Anirudha Behera

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SUMMARY

I am a **passionate Physical Design Engineer** with **1+ years** of experience in **ASIC design flow**, specializing in **PnR**, **STA**, and **low-power design techniques**. Proficient in **RTL to GDSII implementation** and **optimization** using **Synopsys** and **Cadence tools**. Experienced in resolving design challenges and improving **PPA metrics** across **advanced nodes**.

EDUCATION

Illinois Institute of Technology, Chicago, USA — **01/2022 - 12/2023**

Master of Science in Electrical Engineering — GPA: 3.53/4.0

Relevant Courses: Introduction to VLSI, CAD Techniques for VLSI Design, High-Performance VLSI/IC Systems, Digital SoC Design, Computer Organization and Design, RF Integrated Circuit Design

Gandhi Institute For Technology, Bhubaneswar, India — **08/2014 - 07/2018**

Bachelor of Technology in Electrical Engineering — GPA: 8.1/10

Department Rank 1 (5^{th} - 8^{th} Semester), Recipient of the Best Live Major Project Team Award in 2018

SKILLS

Programming Languages: Perl**,** TCL Methodology, Bash Shell, Basics of Python, Verilog HDL

EDA Tools: Synopsys ICC2, Design Compiler, PrimeTime, Star RC, IC Validator, Cadence Virtuoso, Encounter, Calibre, ModelSim, Innovus, Redhawk

Physical Design Processes: Floorplan, Power Plan, Placement, Routing, CTS, STA, DRC/LVS, ECO, UPF, RC Extraction, DFT, SDC/Timing Constraint

WORK EXPERIENCE

Honorex Technologies, Washington, USA — **05/2024 - Present**

Physical Design Engineer for Marvell Semiconductor

- Contributed to the **Place and Route (PnR)** flow for **AI accelerators** and **high-performance processors** targeting **3nm** node, optimizing for **timing**, **power**, and **area (PPA)** across **multiple process corners (MCMM)**. The designs involved over **5M+ standard cells** and **62 macros**, targeting a frequency of **1.8 GHz**.
- Performed **Static Timing Analysis (STA)** for complex designs, identifying and resolving **timing violations** to ensure that **clock frequencies** met **performance** and **power** requirements for Marvell's **custom processors**.
- Developed and optimized **TCL scripts** to automate key tasks in the **PnR** and **STA** processes, reducing iteration cycles and increasing design efficiency, while maintaining high accuracy in **Design Rule Checks (DRC)** and **Layout Versus Schematic (LVS)**.
- Collaborated with **cross-functional teams** in **design**, **verification**, and **manufacturing** to ensure design integrity and achieve **closure timing**, contributing to the successful **tape-out** of advanced **AI and data center processors**.
- Utilized industry-standard **EDA tools** to address design challenges, including **IR-drop** and **crosstalk** issues, and ensured that the **design integrity** was maintained at sign-off, focusing on **robust performance** across varying operating conditions.

Design Automation LAB, IIT, Chicago, USA — **08/2023 - 12/2023**

Research Assistant

- Dedicated **500+ hours** working with **EDA tools** under Dr. Ken Choi executing the **RTL-to-GDSII flow** for **14nm** and **28nm TSMC nodes** using **Synopsys Design Compiler** and **ICC2**, developing a tailored methodology for efficient **floorplan** and **Power Delivery Network** (**PDN) design**, optimizing **IR-drop resilience** and **power delivery efficiency**.
- Enhanced **QOR** by minimizing **post-Powerplan shorts**, improving **power grid robustness**, and ensuring **design scalability** and **integrity** across **MMMC** and **RC corners** through rigorous **validation**.

ChipEdge Technology, Bengaluru, India — **10/2022 - 07/2023**

Physical Design Apprenticeship

- Managed **physical design** phases including **Logic Synthesis**, **Floorplan**, **Placement**, **CTS**, **Routing**, and **Optimization** to meet **Power**, **Performance**, and **Area (PPA)** targets across **14nm, 22nm, 32nm**, and **45nm nodes** using **TSMC FinFET/CMOS technology**.
- Resolved **STA violations** for designs up to **2M cells** and **80+ macros**, ensuring compliance with **timing** and **power** requirements through thorough **analysis** and **optimization**.
- Achieved successful **GDSII tape-outs** by addressing **DRC**, **LVS**, **ERC**, **IREM**, and **Logic Equivalence (LEC)** issues, leveraging **Shell scripting** and **TCL methodology** for **ECO cycles**, **manual debugging**, and automation.

ACADEMIC PROJECTS

OpenSPARC T1 Block Level design from RTL to GDSII using 14nm and 28nm TSMC nodes | DC | ICC2 — **02/2023**

- 75% core-area utilization and density sweeps were used to understand congestion and routability behavior.
- Optimized design using insertion and size cell techniques to eliminate DRVs like Caps and Trans. [https://github.com]