ANIRUDHA BEHERA

Chicago, IL 60608 | +1 (312) 539-8691 | abehera1@hawk.iit.edu

Objective

I am seeking an entry-level position as a Physical Design Engineer, emphasizing my dynamic skills, Block-level design certification, and over 3 years of diverse hands-on experience. With a robust understanding of the Synopsys flow, I am dedicated to continuous learning and growth, particularly in the field of AI. I am enthusiastic about the opportunity to join a dedicated team and am prepared to begin contributing in January 2024.

Skills

- TCL
- Shell/Bash
- Python
- VHDL
- Verilog
- C/C++
- Synopsys IC Compiler II
- Design Compiler
- Prime Time
- Star RC
- IC Validator
- Formality
- Calibre
- Redhawk.
- Cadence Virtuoso
- Encounter
- Model Sim
- Hspice
- CACTI
- WATCH
- Xilinx Vivado

Experience

Physical Design Engineer Trainee **09/2022 to 10/2023**
Chipedge Technology **Bengaluru, India**

- Received extensive training on the VLSI Physical Design lifecycle and successfully completed two industry-standard projects: CHIPTOP and Falcon.
- Applied Block-Level design methodology and Synopsys EDA tools proficiently throughout 4 projects lifecycle.
- Transitioned to an Intern position, contributing to critical real-time projects, DTMF and OpenSPARC T1 (ORACLE)
- Led end-to-end design phases, encompassing Floorplan, Placement, Clock Tree Synthesis (CTS), and Routing, while meticulously evaluating tradeoffs between Quality of Results (QOR) and Power, Performance, and Area (PPA).
- Ensured design integrity by addressing DRC, LVS, LEC, EM/IR, ANTENNA, and DFM violations.
- Utilized ECO cycles and manual debugging for successful ideal GDSII tape-out.
- Proficient in technology nodes (14nm, 22nm, 28nm, 32nm) and advanced Shell/TCL scripting for efficient debugging in Physical Design.

Business Development Associate (BDA) **01/2021 to 12/2021**
Think & Learn Pvt Ltd (BYJU'S) **India, Bengaluru**

- Conducted Personalized Counseling Sessions: Provided one-on-one counseling sessions to align clients' preferences and knowledge with available product segments.
- Top Revenue-Generating BDA: Achieved recognition as the top-performing Business Development Associate (BDA) with the highest customer retention rate during my tenure.
- Exceptional Skills and Performance: Leveraged excellent communication and pitching skills, coupled with in-depth product knowledge and a strong work ethic, to excel in this role.

COVID-19 Lockdown Break **03/2020 to 01/2021**

Asst. MEP Site Engineer **02/2019 to 02/2020**
Electron Electromechanical LLC **Doha, Qatar**

- Asst MEP Site Engineer: Oversaw daily site progress and led a technician team.
- Key Role in "Doha Insurance Tower" Project: Ensured seamless execution and coordination of MEP activities.
- Technical Problem Solver: Provided on-site technical support and solutions, enhancing project planning and resource management.
- Quality and Safety Oversight: Conducted inspections, maintained quality, and enforced safety standards; reported project updates to senior management.
- Effective Collaboration: Collaborated with contractors and vendors, driving successful project outcomes.
- Punctual Project Completion: Contributed to on-time project completion.
- My exceptional blend of interpersonal and technical skills seamlessly integrated into the project's success.

Education

Master of Science: **Electrical Engineering** **Expected in 12/2023**

Illinois Institute of Technology Chicago, IL

- Relevant Coursework: Introduction to VLSI, CAD Techniques for VLSI Design, High-Performance VLSI/IC Systems, Digital SoC Design, Computer Organization and Design, RF Integrated Circuit Design
- GPA: 3.6
- Member of IEEE Region Zone-4, Chicago, 2022
- Eta Kappa Nu Delta Chapter HKN-IEEE Student Government Secretary General
- Research: **Design and Performance Evaluation of FPGA based Audio Systems on ZedBoard-Zynq SoC**, International Journal of Creative Research Thoughts **(IJCRT)**, ISSN:2320-2882, Volume.11, Issue 8, pp.d778-d786, August 2023, Available at :http://www.ijcrt.org/papers/IJCRT2308403.pdf
- Research: High Performance VLSI PVT-Aware Design for 10T SRAM using 15nm PDK.

B. Tech: **Electrical Engineering** **07/2018**

Gandhi Institute For Technology Bhubaneswar, India, India

- GPA 8.1
- Department Ranked: 1
- Team Leader of Major and Minor Projects

Academic Projects

Hierarchical Schematic and Layout Design of 4-bit Carry Look-ahead Adder.

- Designed a 4-bit CLA adder schematic, Symbol, Testing Circuit, and Layout using Virtuoso.
- Performed Physical Verifications (LVS, DRC) and Parasitic Extraction using Calibre. Then Formal verification is performed using Formality and measured Power, Delay, and temperature using HSPICE.

Standard Cell-Based RTL to GDSII Design for 8-bit Accumulator

- Developed RTL code and Testbench, synthesized using DC. Optimized Placement and Route with Encounter by adding buffers for area, power, timing then Completed Formal Verification, generated GDSII.

Standard Cell-Based 32-bit Pipelined CPU Design with Modified New ALU Architecture (RTL to GDSII)

- Implemented 5 CPU models with ASIC flow for slack time optimization.
- Executed Synthesis, PNR, and opt then recorded optimized slack time, power, area. Obtained GDSII Layout.
- Utilized CSeA, CLA, CRA and CSA adders and comparator-CLA mix designs and compared their performance.
- I found CSeA has the highest and CRA has lowest performance speed.

CAD Tool Design for Static Timing Analysis by using TCL/Tk and C Programming

- Designed C code to calculate the required time, arrival time, and slack time from the given input vectors and optimized the code to save the output file separately.
- Designed a Static Timing Analysis CAD tool GUI using TCL/Tk, which can take set of inputs from the user and optimize the given input vector using implemented C code and display the output results on the GUI interface.

Multimedia Mobile Processor Configuration for Ultra-low Power Design in Modern VLSI

- System-Level: Coded Graph-based slack analysis in C. Optimized with Loop unrolling and catch technique. WATCH and CACTI tools were used. Achieved 85.68% power reduction.
- RTL-Level: Applied ACG, CCG, OCCG, LECG, ECG, hybrid techniques on MMP. Achieved max 109.75% power reduction. Used Formality, Model Sim, Power Compiler (DC) tools.

Certifications

- Certified **Physical Design Engineer**, **Chipedge Technology** - 2022
- Certified **Google IT Automation with Python**, **Coursera** - 2023
- Certified **IBM Data Professional Certificate on Linux commands and Shell Scripting** , **Coursera** - 2023
- Certified **VHDL and Verilog for FPGA Engineer with Vivado design suite** , **Udemy** - 2022

Portfolios

- https://anirudhabehera.site/
- https://www.linkedin.com/in/abehera1/
- https://github.com/BeheraAnirudh