

# ANIRUDHA BEHERA

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## SUMMARY

Passionate **Physical Design Engineer** with over **2 years of experience** in **ASIC design flow**, specializing in **Place and Route (PnR)**, **Static Timing Analysis (STA)**, and **low power design methodologies**. Skilled in **RTL-to-GDSII implementation**, design optimization, and **PPA improvement** across advanced technology nodes. Proficient in industry standard **Synopsys and Cadence** toolchains with strong debugging, floorplanning, and powerplanning expertise.

## SKILLS

**Programming Languages:** Perl, TCL, Bash, Python (basics), Verilog HDL, Makefile

**EDA Tools:** Synopsys Design Compiler, ICC2, StarRC, IC Validator, PrimeTime, Cadence Virtuoso, Encounter, Calibre

**Physical Design Processes:** Logic Synthesis, Floorplan, Powerplanning, Placement, CTS, Routing, Physical Verification (DRC, LVS), UPF (CPF), DFT, RC Extraction, STA, ECO, Timing Constraints (SDC)

## EXPERIENCE

**Honorex Technologies**, Washington, USA

May 2024 – Present

Physical Design Engineer for Marvell Semiconductor

- Executed Place and Route (PnR) for a 7nm AI accelerator block with ~2M standard cells and 32 macros, achieving stringent PPA targets under multi-corner, multi-mode (MCMC) analysis.
- Designed for 2.2 GHz using a multi-VDD architecture; achieved timing closure across SS, TT, and FF corners.
- Contributed to block-level floorplanning, including pin assignment, IP integration, and RDL planning for CPU and AI accelerator designs; coordinated with layout teams for custom layout integration and database delivery.
- Performed Static Timing Analysis (PrimeTime) and parasitic extraction (StarRC) for accurate sign-off; mitigated IR-drop, crosstalk, and reliability issues, supporting successful tape-out of advanced AI and data center processors.
- Optimized Clock Tree Synthesis (CTS) for minimal skew and latency while balancing power and timing margins.
- Implemented ECO flows for late-stage timing fixes, reducing turnaround time and maintaining sign-off quality across modes.

**Design Automation Lab, Illinois Institute of Technology**, Chicago, USA

August 2023 – December 2023

Research Assistant

- Completed 500+ hours of RTL-to-GDSII flow implementation for 14nm and 28nm TSMC nodes under the guidance of Dr. Ken Choi, utilizing the Synopsys tool flow.
- Developed a custom floorplan and PDN methodology that improved IR-drop resilience, minimized post-powerplan shorts, and enhanced design scalability across MMMC/RC corners.
- Designed and validated chip integration workflows for floorplan and power grid planning, ensuring functional and electrical robustness across multiple corners.

**ChipEdge Technology**, Bengaluru, India

October 2022 – July 2023

Physical Design Apprentice

- Executed end-to-end physical design flow: Logic Synthesis, Floorplan, Placement, CTS, Routing, and Optimization for 14nm, and 28nm TSMC nodes.
- Resolved setup/hold violations and achieved timing closure for designs up to ~550K standard cells and 80 macros.
- Delivered clean GDSII by resolving DRC, LVS, ANT, and LEC issues; automated ECO cycles using TCL and Shell scripting.
- Gained hands-on experience in I/O planning, bump assignment, and custom layout for advanced FinFET/CMOS nodes.

## EDUCATION

**Illinois Institute of Technology**, Chicago, USA

January 2022 – December 2023

**Master of Science in Electrical Engineering**

GPA: 3.53/4.0

Relevant Courses: Introduction to VLSI, CAD Techniques for VLSI Design, High-Performance VLSI/IC Systems, Digital SoC Design, Computer Organization and Design, RF Integrated Circuit Design

**Gandhi Institute for Technology**, Bhubaneswar, India

August 2014 – July 2018

**Bachelor of Technology in Electrical Engineering**

GPA: 8.1/10

Department Rank 1 (5th–8th Semester)

## PROJECTS

**OpenSPARC T1 Block Level RTL-to-GDSII Design | ICC2 | DC | ICV | StarRC | PrimeTime** February 2023

- Implemented block-level RTL-to-GDSII design on 14nm and 28nm nodes, achieving 75% core-area utilization, performing density sweeps to analyze congestion and routability, and ensuring power integrity across the design.
- Optimized the design using cell insertion and sizing techniques to eliminate DRVs such as capacitance, transistor violations.