Anirudha Behera

https://anirudhabehera.site/ | abehera1@hawk.iit.edu | +1 (312) 539-8691 | https://www.linkedin.com/in/abehera1/

OBJECTIVE

Experienced Certified Physical Design Engineer with expertise in Synthesis to Tapeout for Block level design using Synopsys flow. Proficient in industry-leading EDA tools from Synopsys, Cadence, Mentor Graphics, and Xilinx. Seeking an entry-level role to contribute to a dynamic team, apply my skills, and foster continuous learning and growth in my engineering career.

EDUCATION

Master of Science in Electrical and Computer Engineering — Chicago, USA

ILLINOIS INSTITUTE OF TECHNOLOGY (IIT) — Jan 2022-Dec 2023

Coursework: Introduction to VLSI, CAD Techniques for VLSI Design, High-Performance VLSI/IC Systems, Digital SoC Design, Computer Organization and Design, Radio Frequency IC Design, Hybrid Electric Vehicle Drives, Adjustable Speed Drives, Robust Control

Bachelor of Technology in Electrical Engineering — Bhubaneswar, India

GANDHI INSTITUTE FOR TECHNOLOGY (GIFT) — Aug 2014 – July 2018

Coursework: BE, BEE, Power Electronics, Advanced Power Electronics, Digital Signal Processing, Microprocessor and Microcontroller, Digital Electronics Circuit, Analog Electronics Circuit, DBMS, Data Structure Using C, OS and EEM.

TECHNICAL SKILLS

Programming Skills: Python, Shell/Bash, VHDL, Verilog, TCL/Tk, HTML5, CSS3, C/C++

EDA Tools/Debug Tools: Synopsys Design Compiler, Formality, IC Compiler II, Prime Time, Star RC, IC Validator, Cadence Virtuoso, Encounter, Mentor Graphics Calibre, Xilinx Vivado, ModelSim, CACTI, WATCH, Virtual Studio, PyCharm, Geany

Operating Systems: Linux/Unix, Microsoft Windows, MacOS

TECHNICAL PROJECTS (https://github.com/BeheraAnirudh)

- **Hierarchical Schematic and Layout Design of 4-bit Carry Look-ahead Adder.**
  - Designed a 4-bit CLA adder schematic, Symbol, Testing Circuit, and Layout using Virtuoso.
  - Performed LVS, DRC, and PEX using MG Calibre. Then Formal verification is performed using Formality.
  - Measured Power, Delay, and temperature using HSPICE.
- **Standard Cell-Based ASIC Design for 8-bit Accumulator**
  - Implemented Verilog code and Testbench for the 8-bit Accumulator, then synthesized the RTL codes.
  - Executed Logical Synthesis process using DC tool, and recorded area, power, and timing reports.
  - Conducted PnR using Encounter with added buffers and achieved optimized area, power, and timing results.
  - Performed Formal verification and obtained GDSII file for the project.
- **Case Study of the 32-bit Pipelined CPU Design with Modified New ALU Architecture**
  - Implemented five different 32-bit CPU architectures using standard ASIC flow to achieve desired slack time.
  - Four of them were using CRA, CLA, CSA, and CSeA Adders and the fifth one was using one Comparator and CLA.
  - Performed RTL Synthesis, Logic Synthesis, PnR, and Post PnR opt, for each design, and initial slack time and final optimized slack time were recorded with power and area reports. Finally, GDSII Layout files were collected.
- **CAD Tool Design for Static Timing Analysis by using TCL/Tk and C Programming**
  - Designed C code to calculate the required time, arrival time, and slack time from the given input vectors and optimized the code to save the output file separately.
  - Designed a Static Timing Analysis CAD tool GUI using TCL/Tk, which can take set of inputs from the user and optimize the given input vector using implemented C code and display the output results on the GUI interface.
- **MMP Configuration for Ultra-low Power Design in Modern VLSI**
  - **System Level Optimization:** Designed C code for Graph-based slack time analysis method, then reduced the power consumption of the program using various Loop unrolling techniques and measured the power using WATCH tool. To minimize further power, catch optimization technique is used and power is measured using the CACTI tool. A total of 85.68% power saving was recorded.
  - **RTL Level Optimization:** Implemented ACG, CCG, OCCG, LECG, ECG, and hybrid techniques on an Industry standard Mobile Multimedia Processor design (MMP) to reduce power consumption. Max 109.75% power saving recorded. Formality and ModelSim were used for LEC check and Synthesis then Power Compiler is used for power measurement.

WORK EXPERIENCE

- **Secretary General** — Chicago, USA
  Eta Kappa Nu Delta Chapter, IIT Chicago — Mar 2023-Present
  - General Secretary of HKN board, IIT Chicago, Computer Engineering department.
  - Attend and document meetings, handle email formatting.
  - Update group members with important information and feeds.
  - Promote collaboration and teamwork within the board.

Skills: Email Writing, Documentation, Critical Thinking, Communication, Collaborative, Event Management.

- **Physical Design Engineer** — Bengaluru, India
  ChipEdge Technology — Sep 2022-Jul 2023
  - Worked as a Physical Design Engineer Trainee at ChipEdge, receiving comprehensive training in the field.
  - Progressed to an intern role, successfully completing four Industry standard projects: CHIPTOP, Falcon, DTMF, and JBI.
  - Diligently employed Block-Level design methodology and utilized various Synopsys tools throughout the projects.
  - Proficient in the entire design flow, from Synthesis to Tape out, and adaptable to different technology nodes.
  - Equipped with expertise and skills to tackle challenges in the semiconductor industry.
  - Eager to contribute to innovative projects and advancements in cutting-edge technologies.

Skills: Synthesis, Floorplan, Power Plan, Placement, CTS, Routing, Sign Off Checks (PV, IR, EM, LEC, STA), ECO cycle, Tape out.
EDA Tools: Design Compiler , IC Compiler II, Prime Time, Star RC, IC Validator, Formality.

- **Business Development Associate (BDA)** — Bhubaneswar, India
  Think & Learn Pvt Ltd (BYJU'S) — Feb 2021-Dec 2021
  - Excelled as a Business Development Associate (BDA), effectively engaging with prospective students and parents.
  - Conducted personalized counseling sessions to align students' educational preferences and knowledge.
  - Advised and recommended appropriate study materials to optimize students' learning outcomes.
  - Recognized and honored as the top revenue-generating BDA during the tenure.

Skills: CRM (LeadSquared), Communication, Pitching, Negotiation, Extensive Travelling, Revenue Generation, Documentation.

- **Asst. MEP Site Engineer** — Doha, Qatar
  Electron Electromechanical LLC — Feb 2020-Jun 2020
  - Asst MEP Site Engineer responsible for monitoring daily site progress and leading a technician team.
  - Involved in the "Doha Insurance Tower" project and ensured smooth execution and coordination of MEP activities.
  - Provided technical support and solutions to on-site challenges by assisting in project planning and resource management.
  - Conducted inspections of quality and safety standards, documented, and reported project updates to senior management.
  - Collaborated with contractors and project stakeholders to achieve project objectives.
  - Contributed to the successful completion of the project on schedule.

Skills: Electrical Wiring, Wire Testing, Screeding, DB wiring, MV room wiring, Appliances Installation, Commissioning, Technical Documentation.

CERTIFICATIONS

- **Physical Design Engineer, ChipEdge Technology**
  Synopsys Tools, Block level Design, Synthesis, Floorplan, Power Plan, Placement, CTS, Sign Off, Tapeout
- **Google IT Automation with Python Professional Certificate, Coursera**
  Crash Course on Python**:** Dictionary, List, Tuple, OOPS, Inheritance, Composition, Modules, Automation
- **IBM Data Professional Certificate on Linux commands and Shell Scripting, Coursera**
  Unix/Linux, Linux Commands, Shell Scripting, Pipes, Filters, Loops, Scheduling Jobs using Cron, Automation
- **VHDL for FPGA Engineer with Vivado design suite by Kumar Khandagle, Udemy**
  VHDL, Xilinx Vivado HL, FPGA Flow, IP Integration
- **Verilog for FPGA Engineer with Vivado design suite by Kumar Khandagle, Udemy**
  Verilog, Xilinx Vivado HL, FPGA Flow, IP Integration

RESEARCH WORK

- Design and Performance Evaluation of FPGA-based Audio Systems on ZedBoard-Zynq SoC
- High Performance VLSI PVT-Aware Design for 10T SRAM with Dedicated Noise Trimming Circuit using 15nm PDK.