Anirudha Behera

Physical Design Engineer

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OBJECTIVE

Diligent and Certified Physical Design Engineer with a strong foundation in Block-level design utilizing the Synopsys flow from Synthesis to Tape out. Seeking an entry-level role to apply my extensive training and hands-on experience, contribute effectively to a dynamic team, and drive continuous growth and innovation in my engineering career.

EDUCATION

MSc. Electrical Engineering, *ILLINOIS INSTITUTE OF TECHNOLOGY, Chicago, USA*-GPA: 3.47/4.0 **Graduating Dec 2023**

Relevant Coursework: Introduction to VLSI, CAD Techniques for VLSI Design, High-Performance VLSI/IC Systems, Digital SoC Design, Computer Organization and Design, Radio Frequency IC Design

B. Tech in Electrical Engineering, *GANDHI INSTITUTE FOR TECHNOLOGY, India*-CGPA: 8.1/10 **Aug 2014 – July 2018**

TECHNICAL SKILLS

Scripting/Programming Skills and OS: TCL/Tk, Shell/Bash, Python, VHDL, Verilog, HTML5, CSS3, Windows, Linux
Physical Design Tools: IC Compiler II, Prime Time, Star RC, IC Validator, Formality, Calibre, Redhawk.
Standard Cell Design Tools: Virtuoso, Design Compiler, Formality, Encounter, Calibre, Model Sim

ACADEMIC PROJECTS

Standard Cell-Based RTL to GDSII Design for 8-bit Accumulator

- Developed RTL code and Testbench, synthesized using DC. Optimized Placement and Route with Encounter by adding buffers for area, power, timing then Completed Formal Verification, generated GDSII.

Standard Cell-Based 32-bit Pipelined CPU Design with Modified New ALU Architecture (RTL to GDSII)

- Implemented 5 CPU models with ASIC flow for slack time optimization.
- Executed Synthesis, PNR, and opt then recorded optimized slack time, power, area. Obtained GDSII Layout.
- Utilized different adders and comparator-CLA mix designs and compared their performance.
- I found CSeA has the highest and CRA has lowest performance speed.

CAD Tool Design for Static Timing Analysis by using TCL/Tk and C Programming (https://github.com/BeheraAnirudh/)

- Designed C code to calculate the required time, arrival time, and slack time from the given input vectors and optimized the code to save the output file separately.
- Designed a Static Timing Analysis CAD tool GUI using TCL/Tk, which can take set of inputs from the user and optimize the given input vector using implemented C code and display the output results on the GUI interface.

Multimedia Mobile Processor Configuration for Ultra-low Power Design in Modern VLSI

- **System-Level:** Coded Graph-based slack analysis in C. Optimized with Loop unrolling and catch technique. WATCH and CACTI tools were used. Achieved 85.68% power reduction.
- **RTL-Level:** Applied ACG, CCG, OCCG, LECG, ECG, hybrid techniques on MMP. Achieved max 109.75% power reduction. Used Formality, Model Sim, Power Compiler (DC) tools.

WORK EXPERIENCE

ChipEdge Technology, Bengaluru, India: Physical Design Engineer **Oct 2022- Dec 2023**

- Worked as a Physical Design Engineer Trainee at ChipEdge, where I received comprehensive training in the field.
- Progressed to an intern role, successfully completing two industry-standard projects: **CHIPTOP** and **Falcon**.
- Diligently applying Block-Level design methodology and utilizing various Synopsys tools throughout the projects.
- Transitioned to Intern position where I got opportunity to work on two real time projects, **DTMF**, and **JBI.**
- Contributed to designing, including Floorplan, Power Plan, Placement, CTS and Optimization, Routing and Optimization and fixing DRC, LVS, EM and IR, ANTENNA violations, ECO Timing fixing and manual debugging and taping out the ideal GDSII file.
- Proficient in the entire design flow, from Synthesis to Tape out, and adaptable to different technology nodes. Experienced with 14nm, 15nm, 22nm, 28nm, and 32nm technology nodes, and able to adapt to new advanced technology nodes.
- Equipped with expertise and skills to work on complex Floorplan, Placement, CTS, and Routing Designs and debugging.
- Possess advanced Shell and TCL scripting skills to debug designs at all levels of the Physical Design flow.

Skills: Synthesis, Floorplan, Power Plan, Placement, CTS, Routing, Sign Off Checks (DRC, LVS, IR and EM, LEC, STA, ANTENNA), ECO cycle, Manual fixing/debugging. | **EDA Tools used:** IC Compiler II, Prime Time, Star RC, IC Validator, Formality, Calibre, Redhawk.

LEADERSHIP EXPERIENCE

Eta Kappa Nu Delta Chapter IEEE, IIT, Chicago, USA: Secretary General **Mar 2023- Present**

- Technical documentation, managing email formatting, disseminated crucial updates to group, fostered teamwork, collaboration, and technical events.

Skills: Email writing, critical thinking, communication, collaboration, event management.

CERTIFICATIONS

- **Google IT Automation with Python Professional Certificate, Coursera**
  Crash Course on Python: Dictionary, List, Tuple, OOPS, Inheritance, Composition, Modules, Automation
- **IBM Data Professional Certificate on Linux commands and Shell Scripting, Coursera**
  Unix/Linux, Linux Commands, Shell Scripting, Pipes, Filters, Loops, Scheduling Jobs using Cron, Automation
- **VHDL and Verilog for FPGA Engineer with Vivado design suite by Kumar Khandagle, Udemy**
  VHDL, Verilog, Xilinx Vivado HL, FPGA Flow, IP Integration