

# Precision Methodology: Transforming VLSI Physical Design with Tailored Floorplan and Power Plan Strategies

ECE597: SPECIAL RESEARCH WORK  
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## ABSTRACT

This project is dedicated to showcasing the effective mitigation of logic (LVS) and design rule (DRC) violations while enhancing Power, Performance, and Area (PPA) metrics through the implementation of tailored design methodologies in the Floorplan and Powerplan stages. A well-optimized Floorplan and Powerplan have the potential to yield significant area savings, up to 80%, and alleviate routing congestions, thereby improving the overall design Quality of Results (QORs). The study employs the Oracle OpenSPARC T1 processor, Synopsys EDA tools, and TSMC libraries for comprehensive research. The demonstrated tactics are illustrated across two technology nodes, 14nm and 28nm, underscoring their applicability across various nodes.

*Er. Anirudha Behera  
Signature*



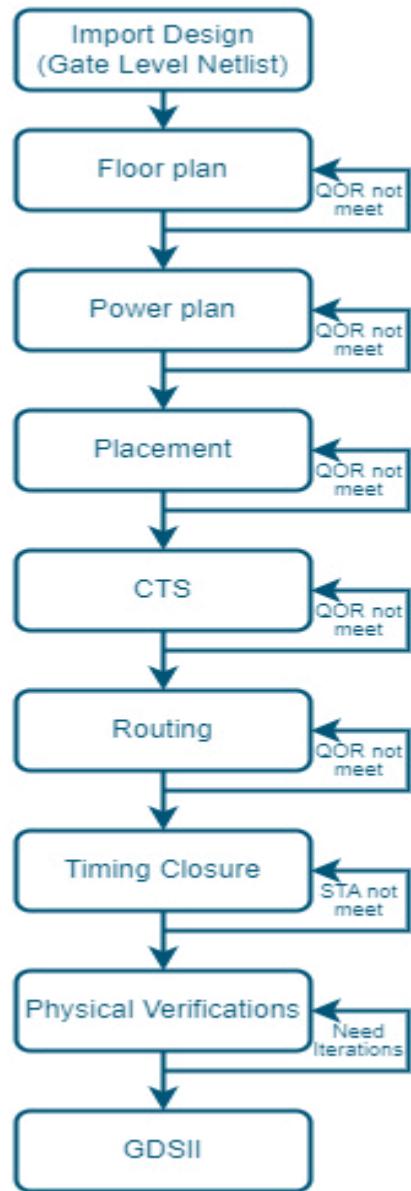
## EDA TOOLS USED

The EDA tools used for this research work are as follows,

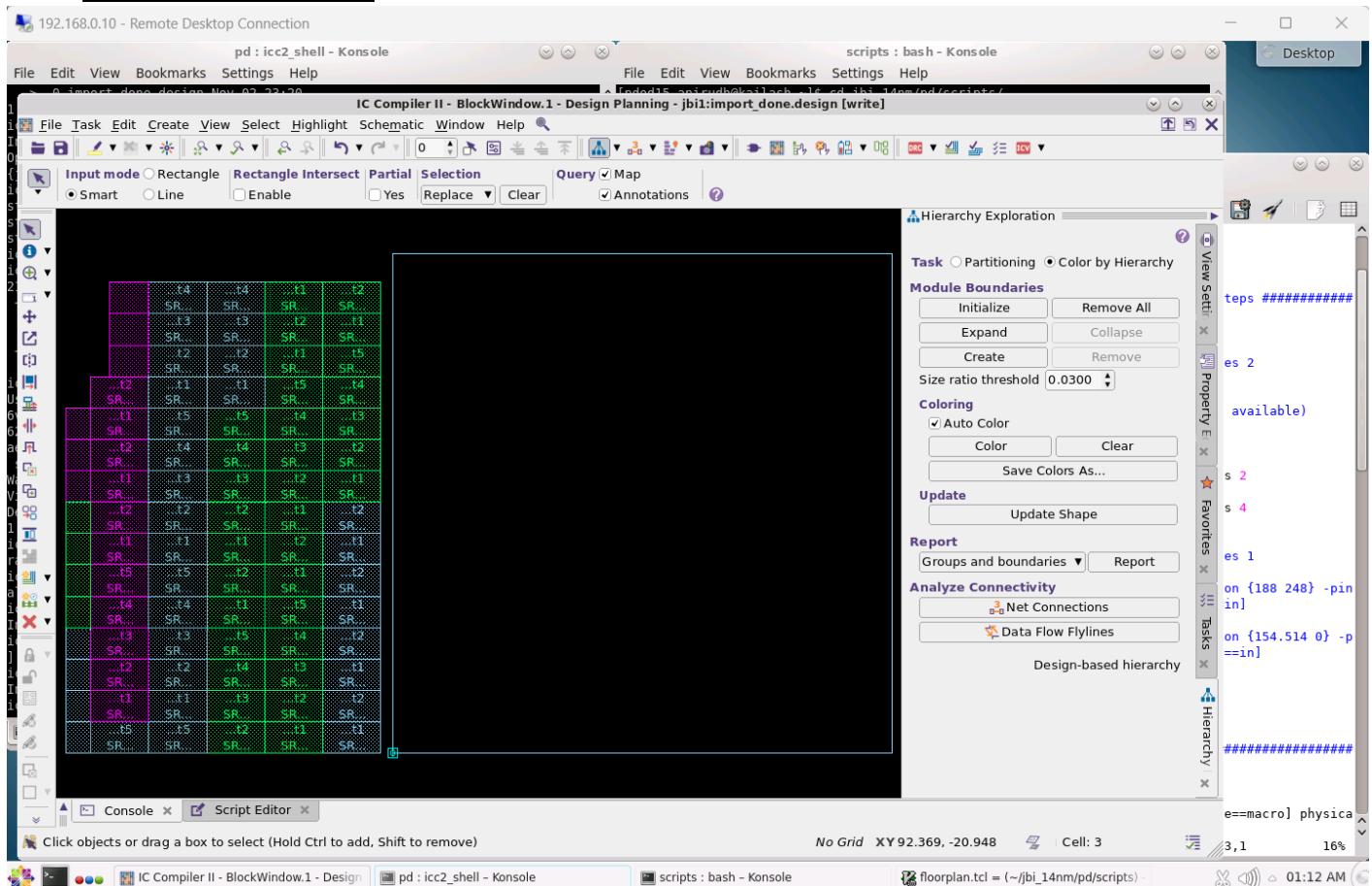
- Logic Synthesis: **Design Compiler**
- PNR: **IC Compiler II**
- Physical Verification: **IC Validator**
- RC Extraction: **StarRC**
- Timing: **Prime Time**



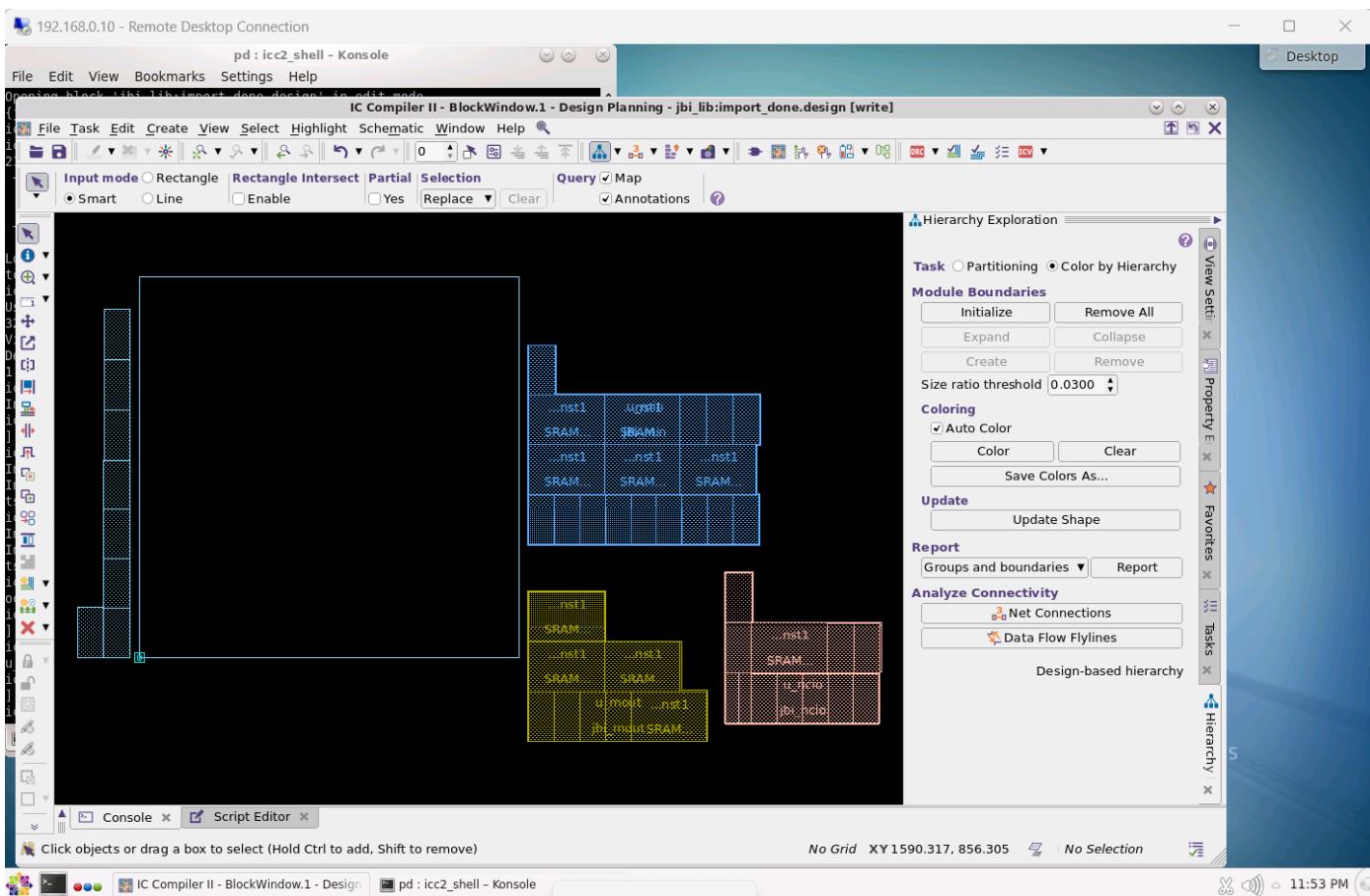
## PHYSICAL DESIGN FLOW



## IMPORT DESIGN

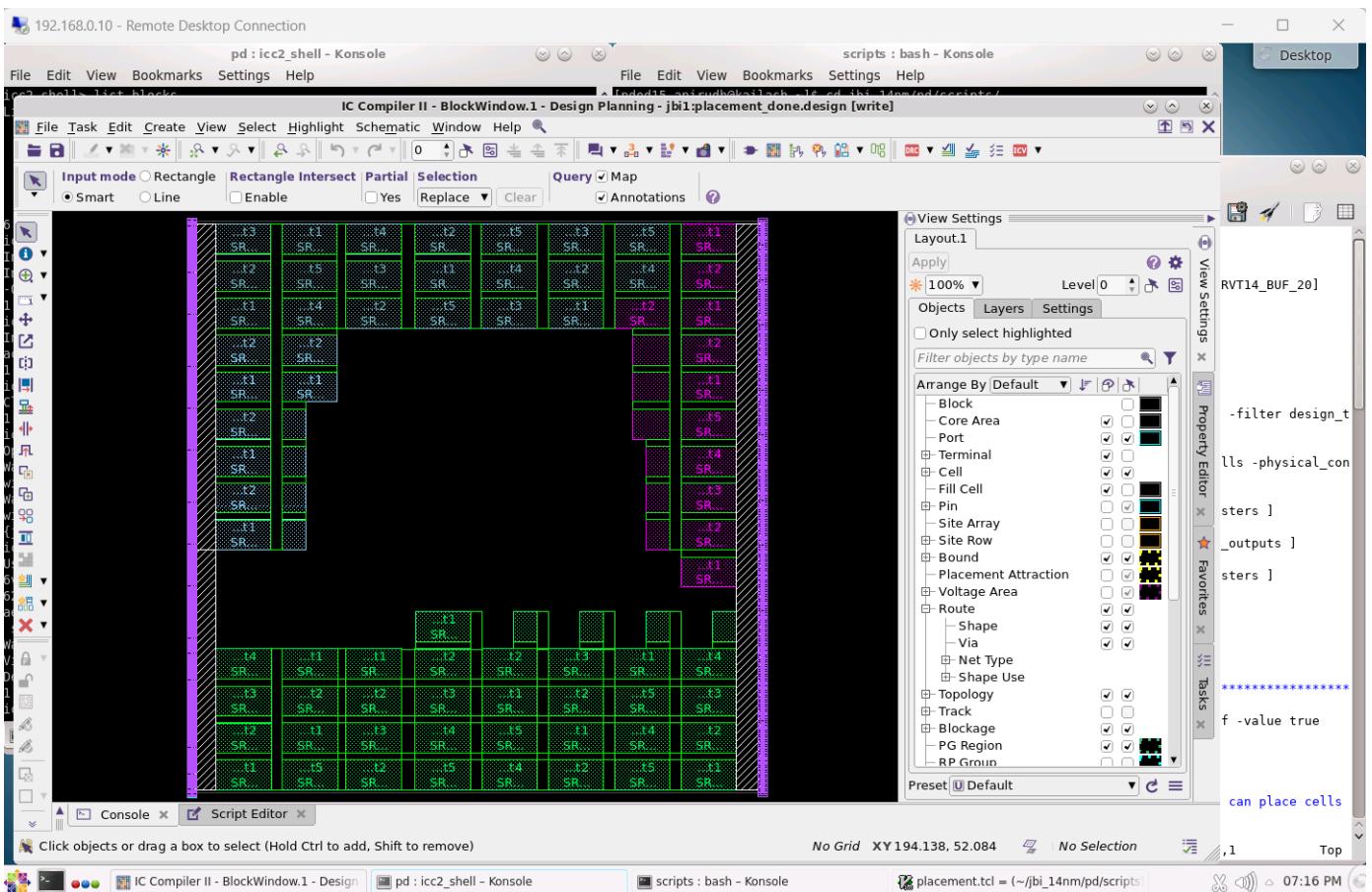


14NM

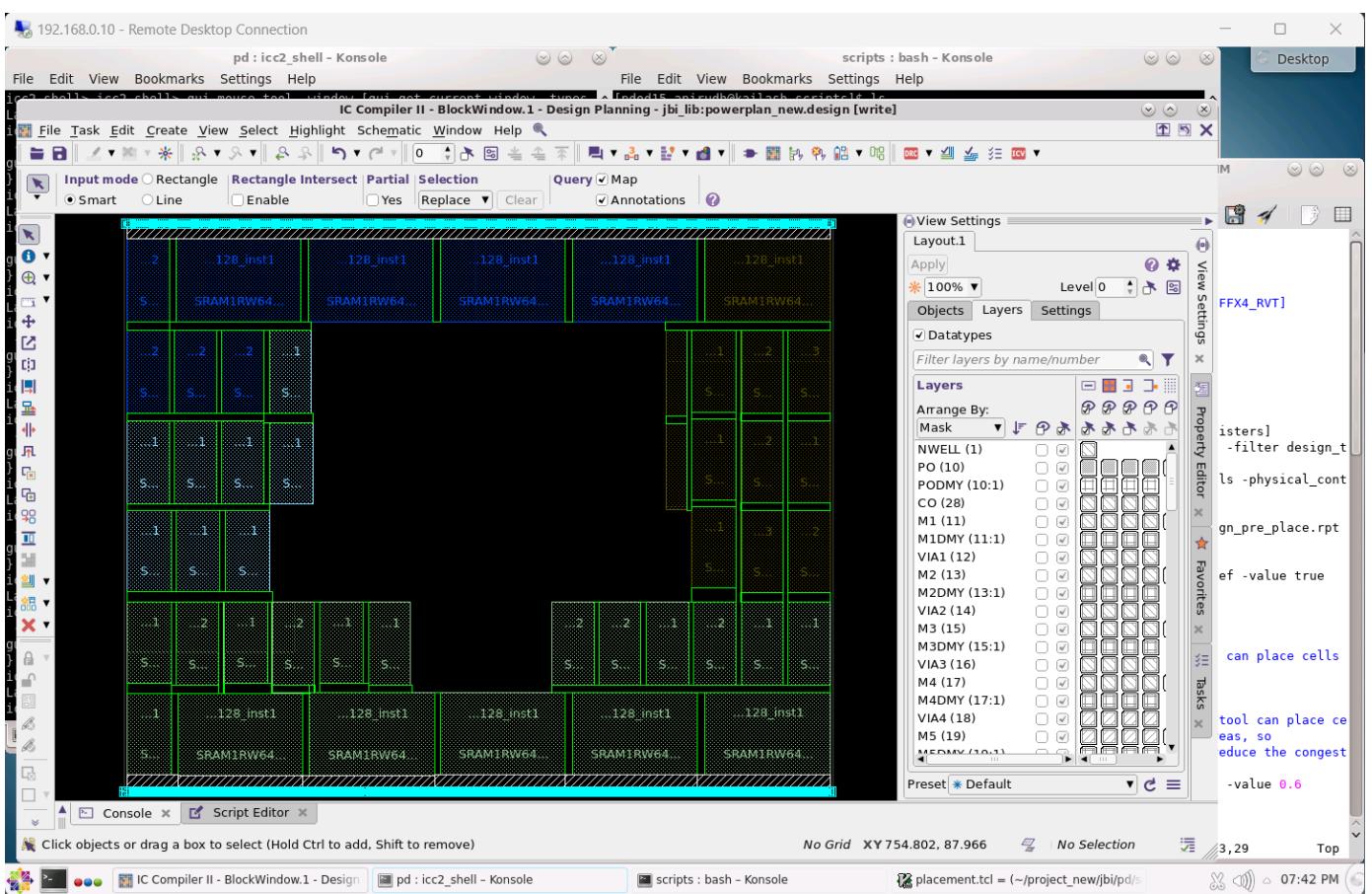


# FLOORPLAN

14NM

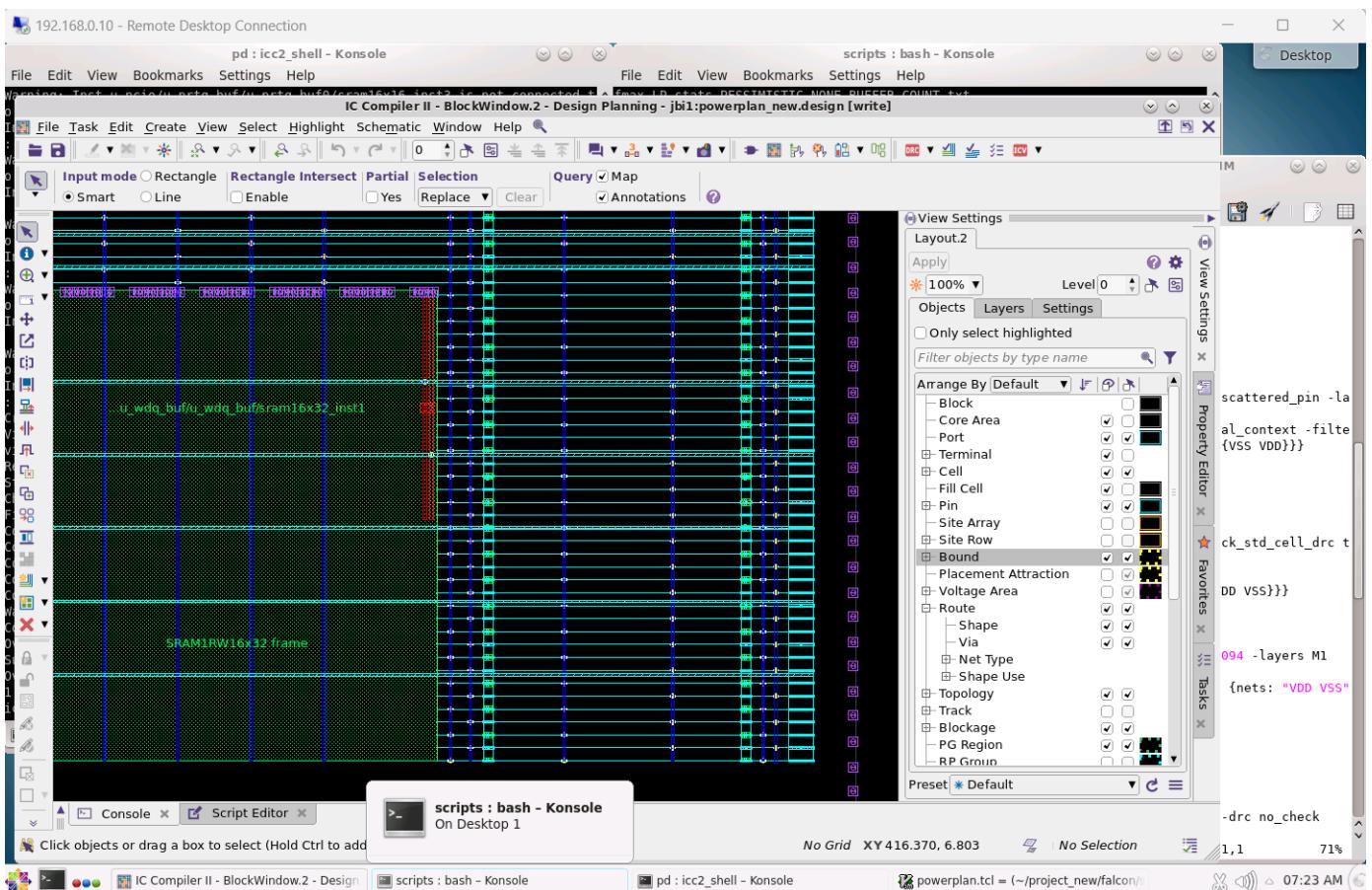


28NM

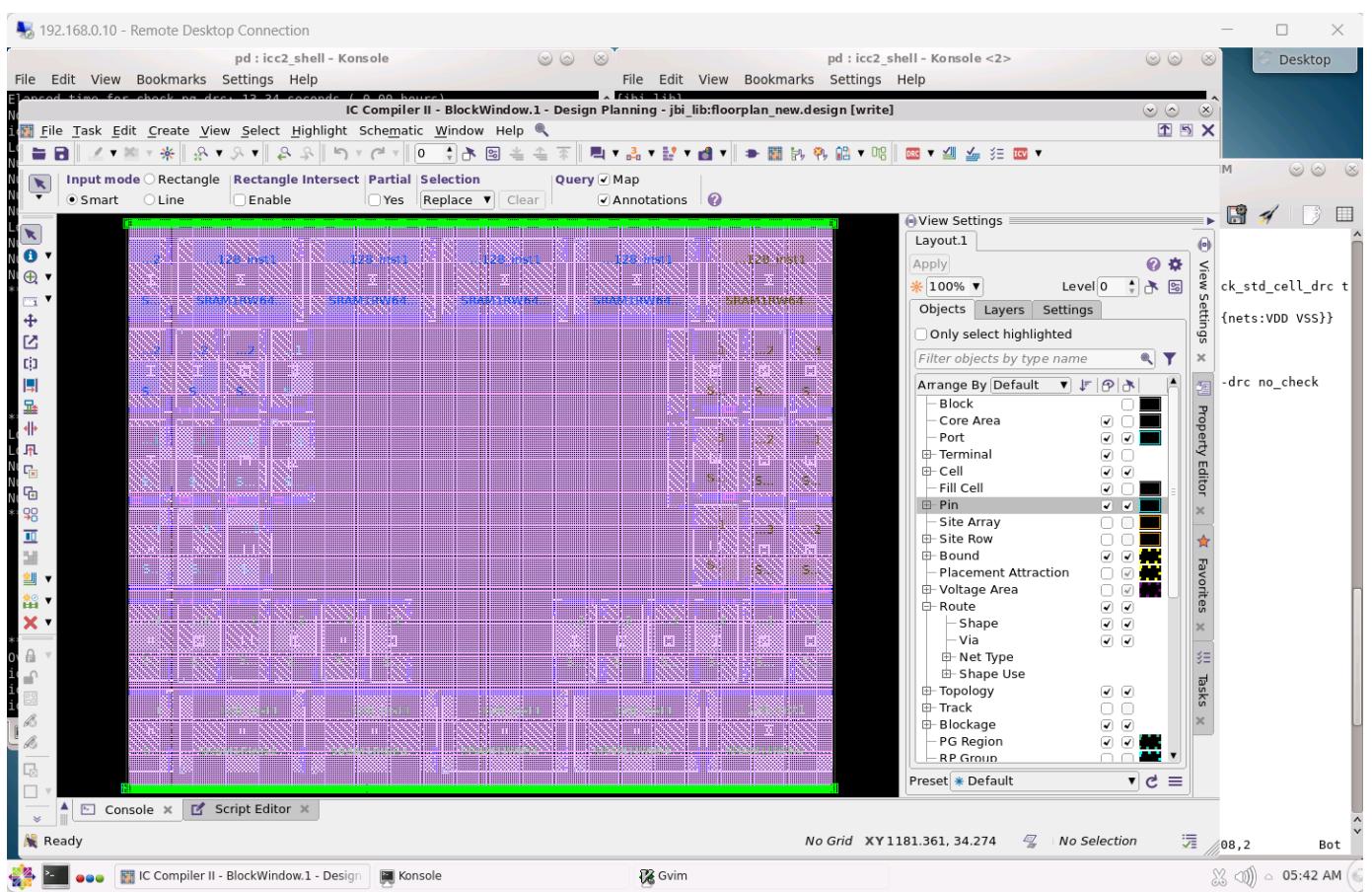


# POWERPLAN

14NM

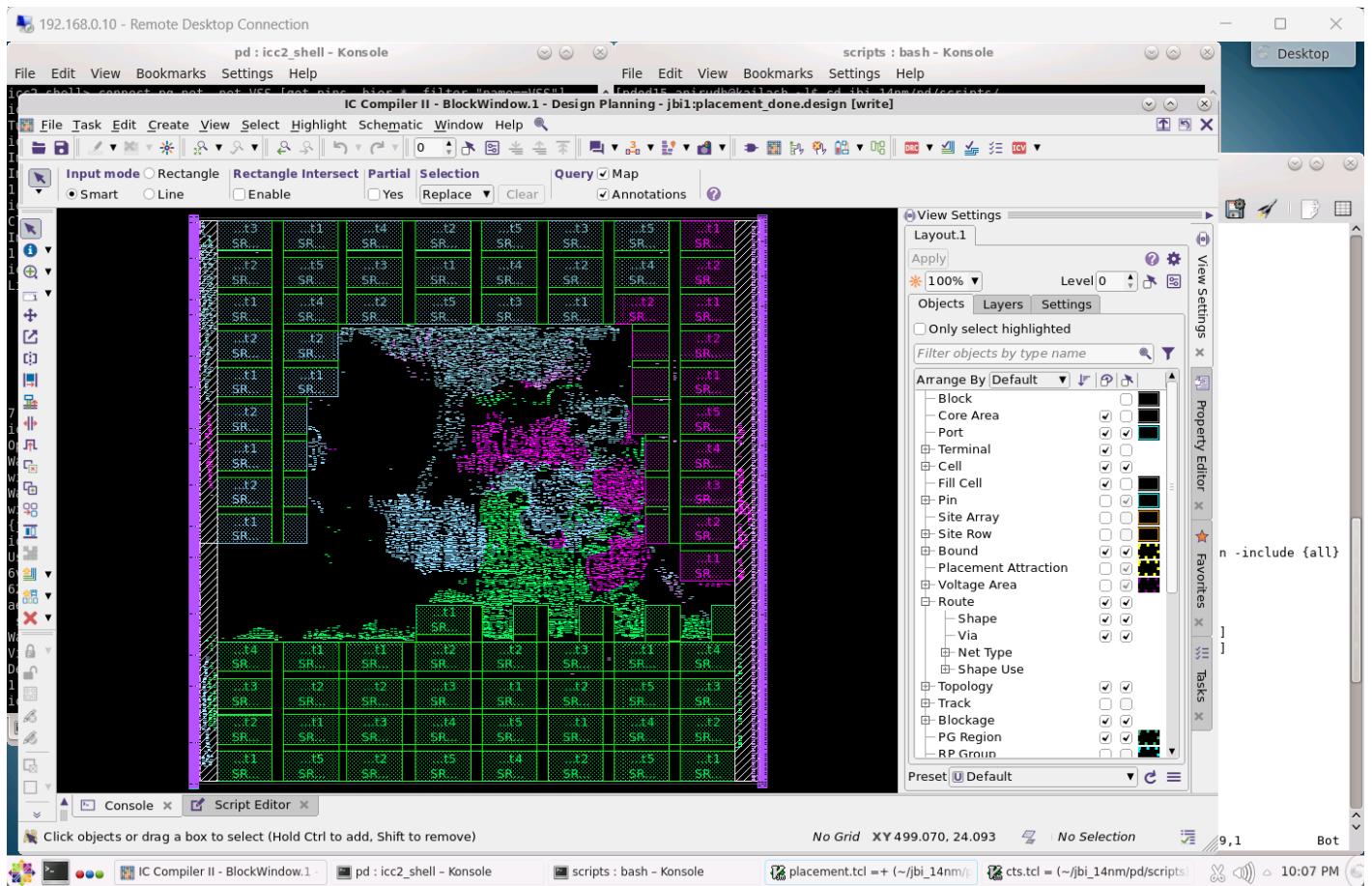


28NM

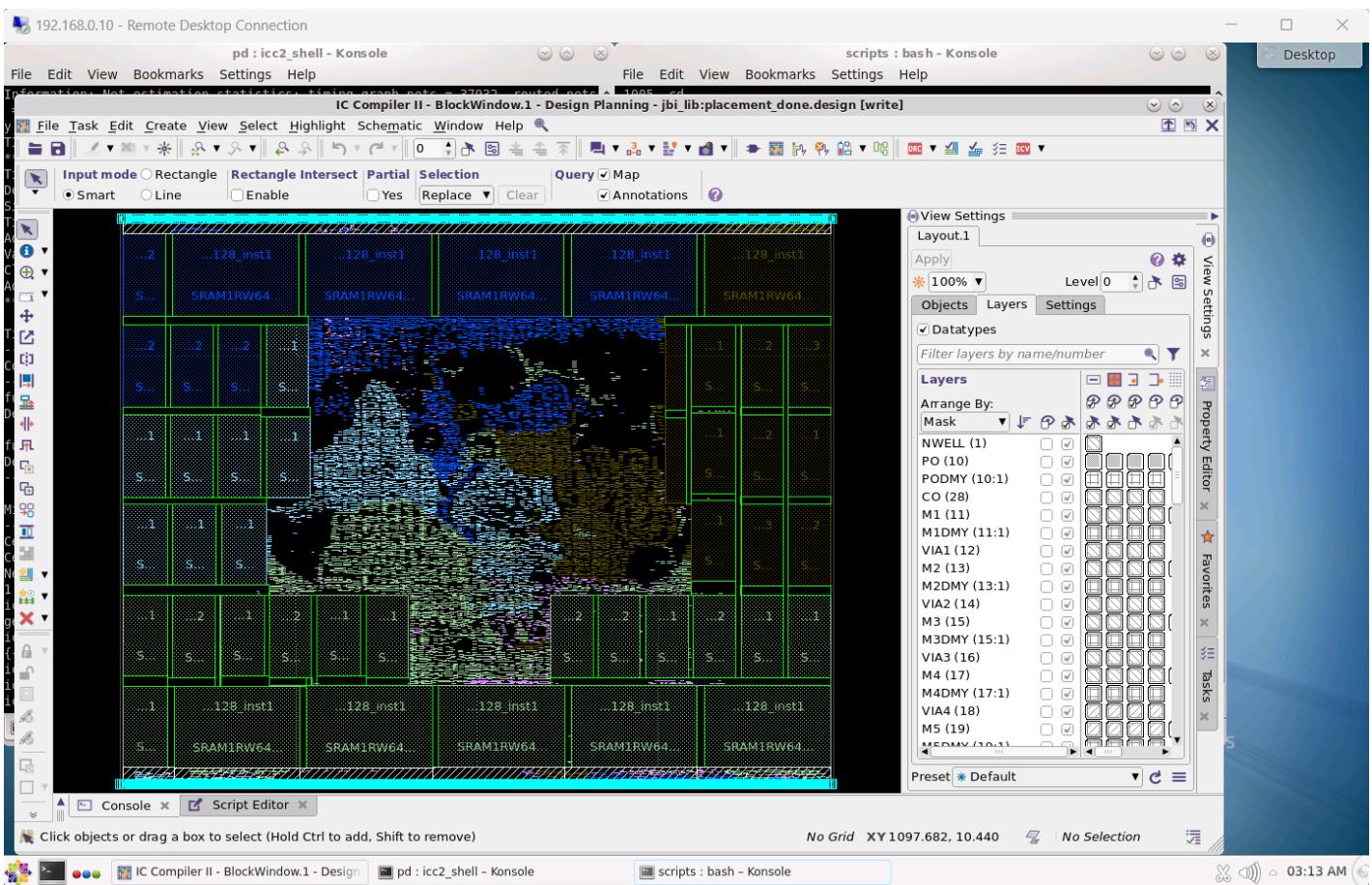


# PLACEMENT

14nm

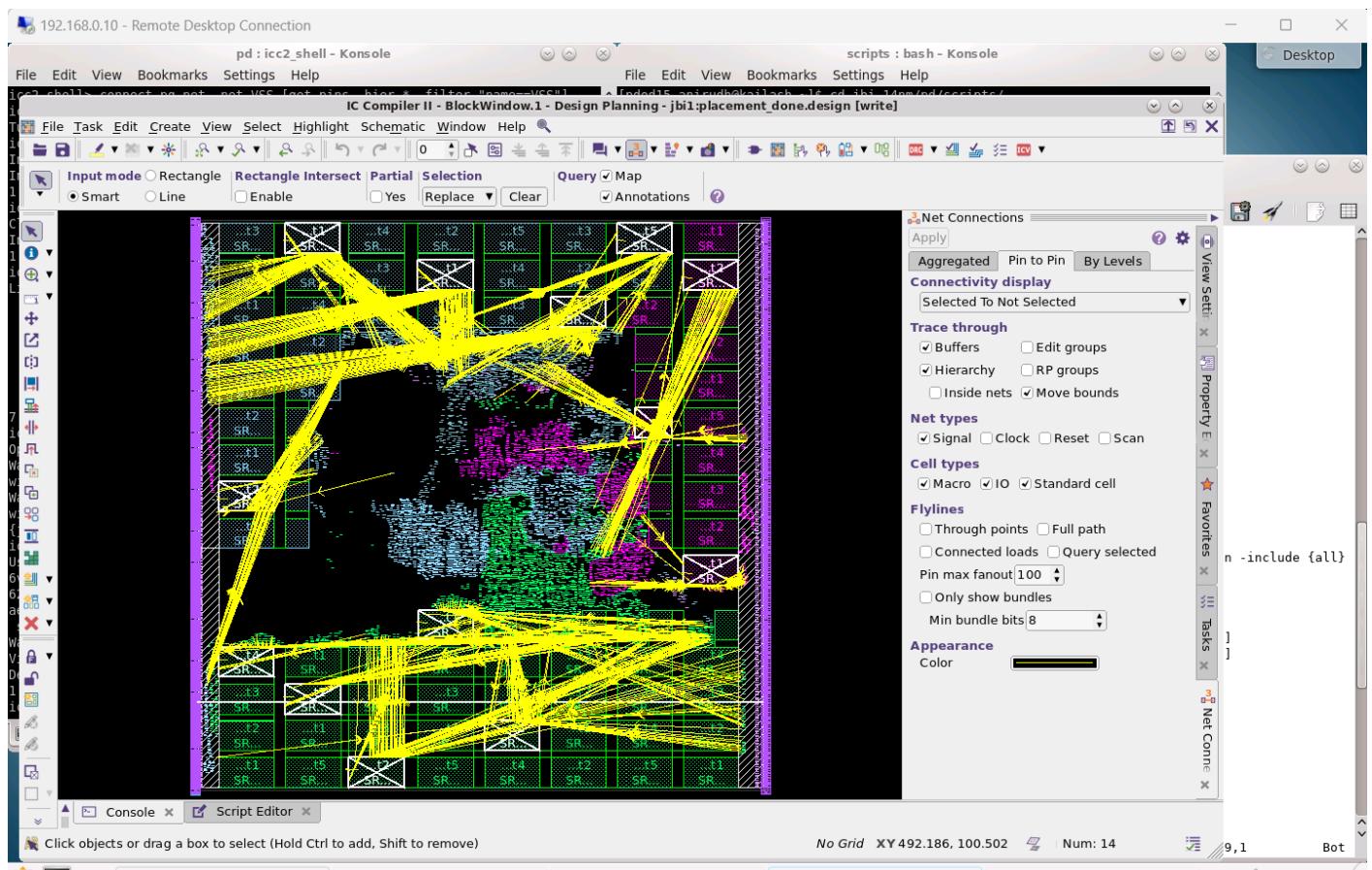


28nm

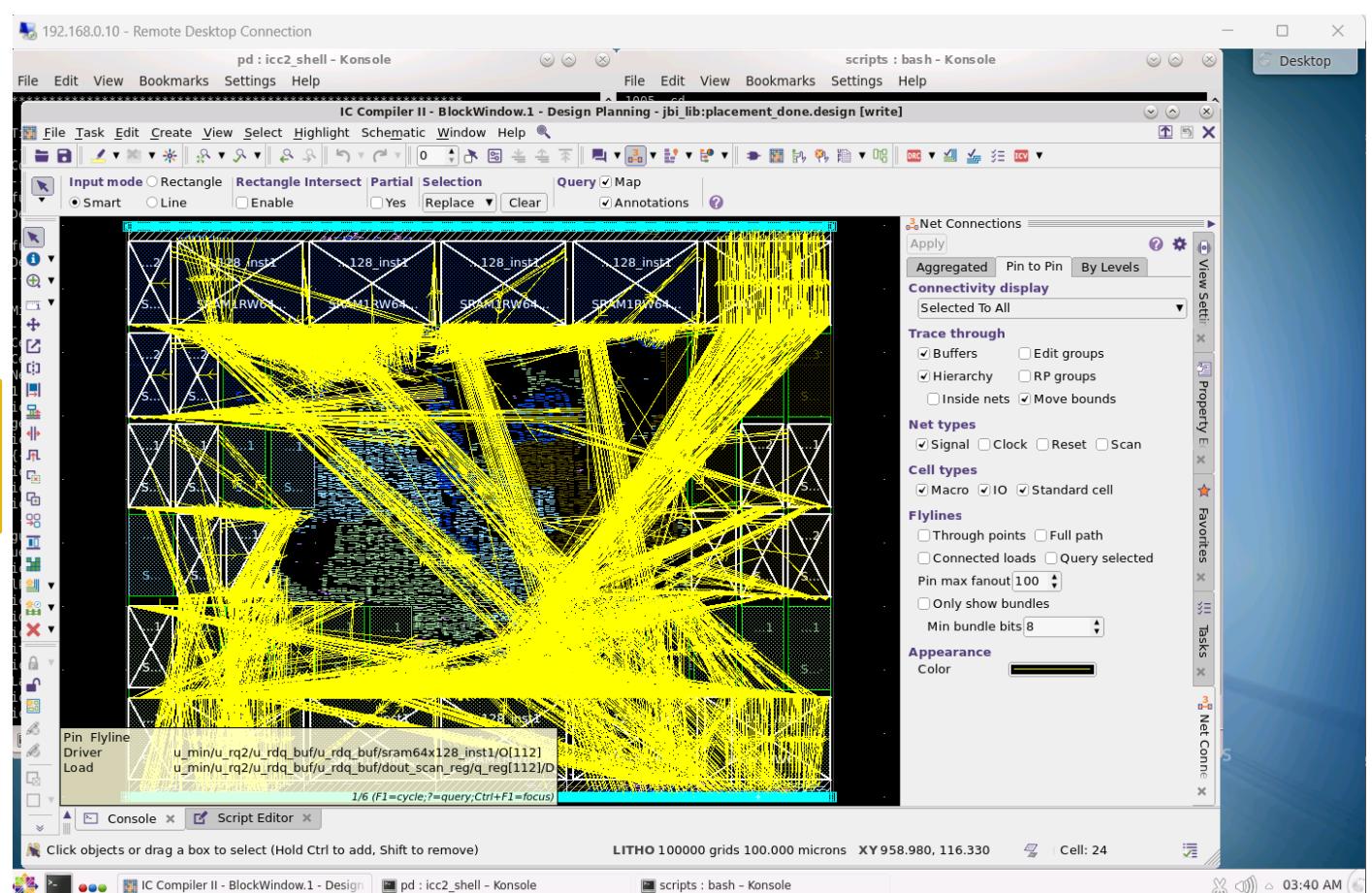


# PLACEMENT- NET CONNECTIONS

14NM

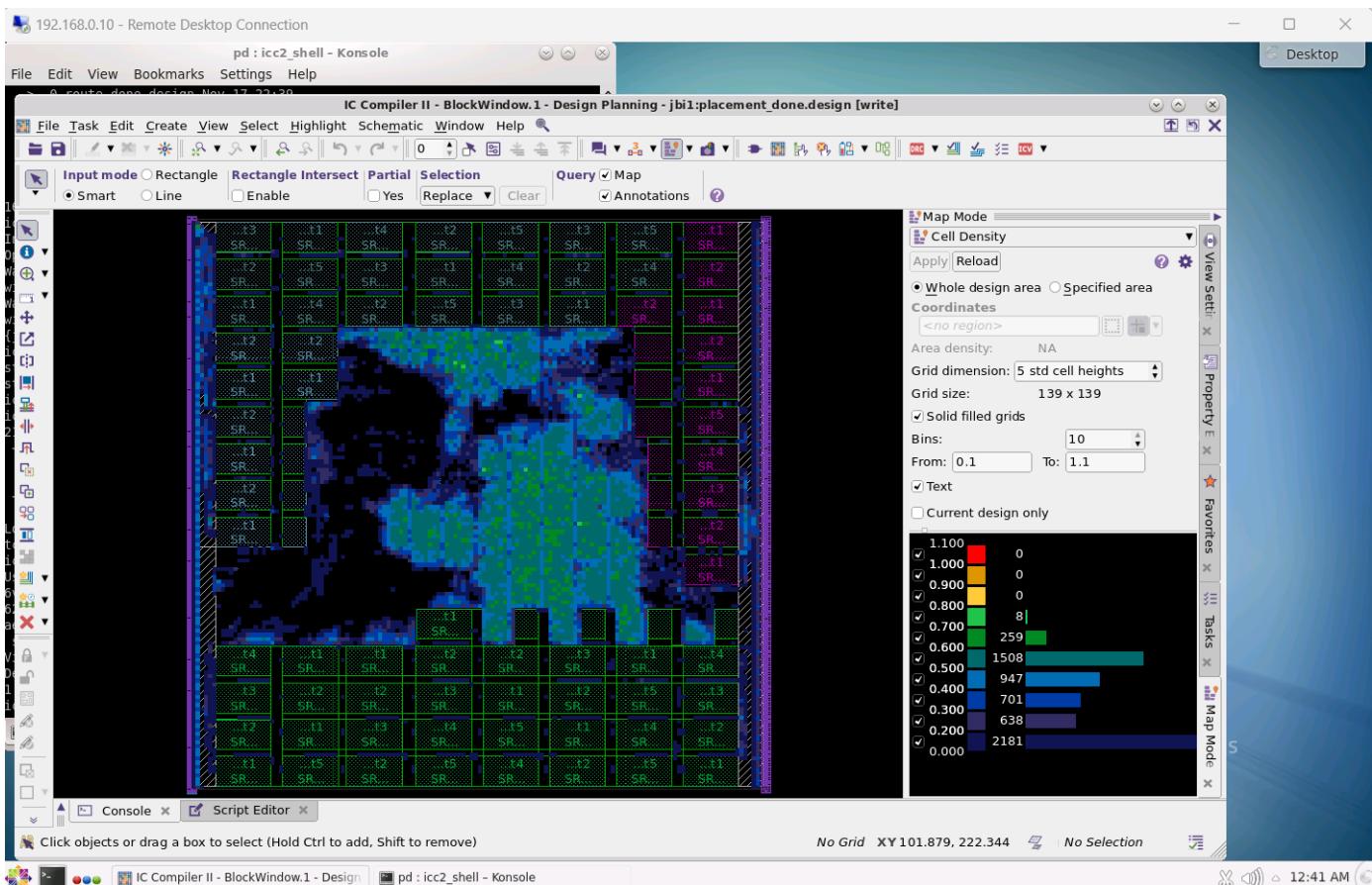


28NM

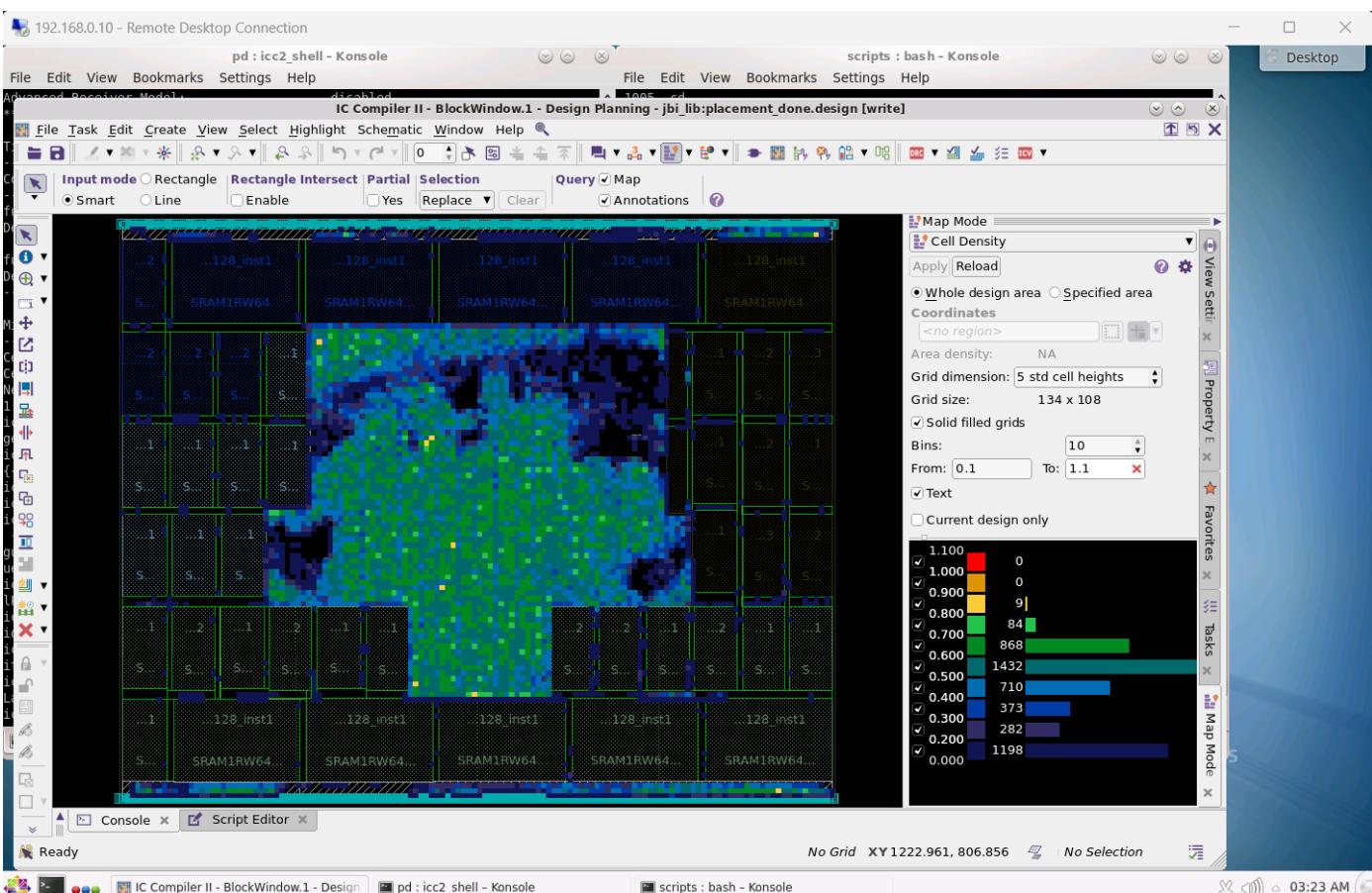


## PLACEMENT CELL DENSITY

14NM

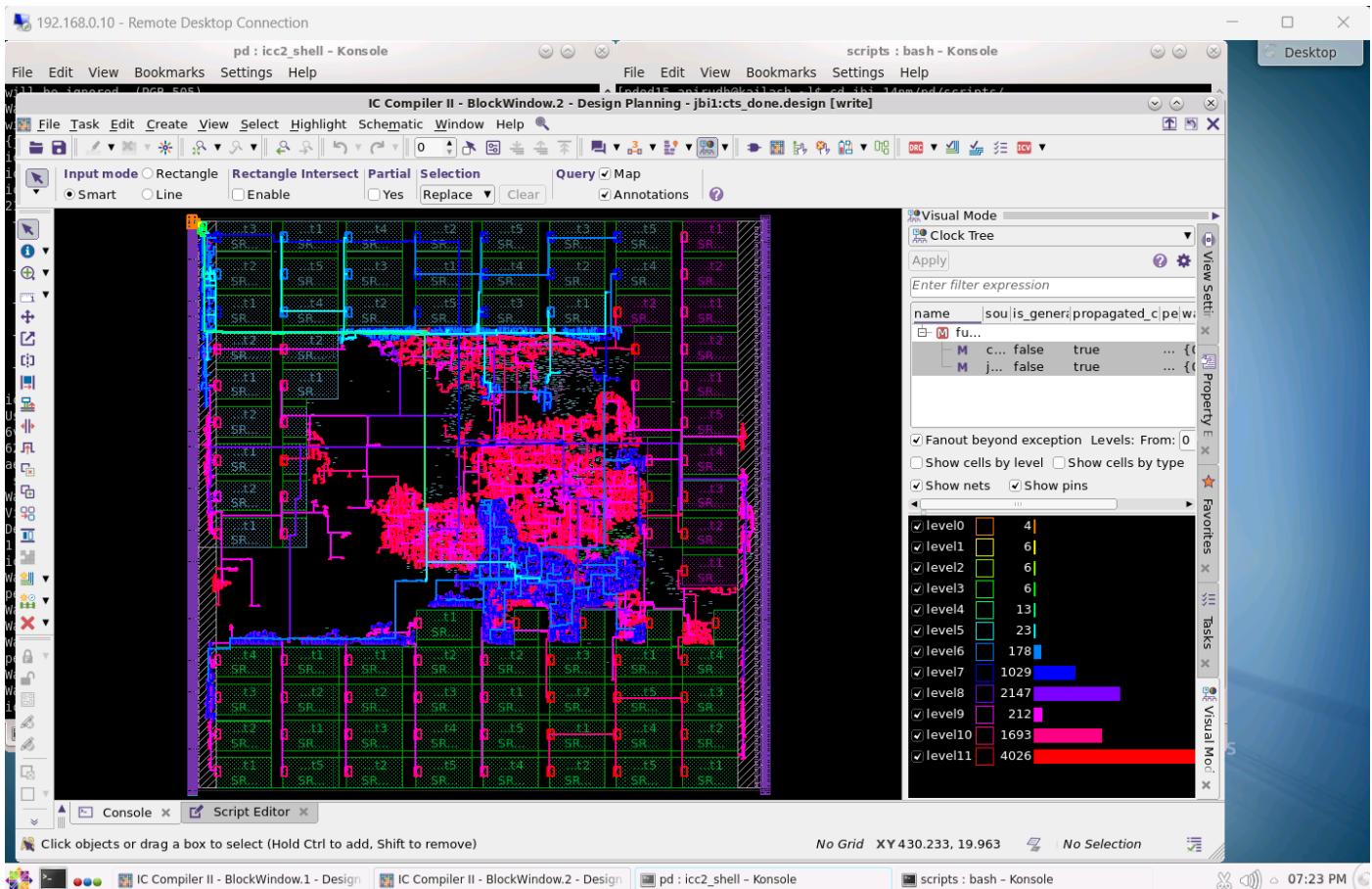


28NM

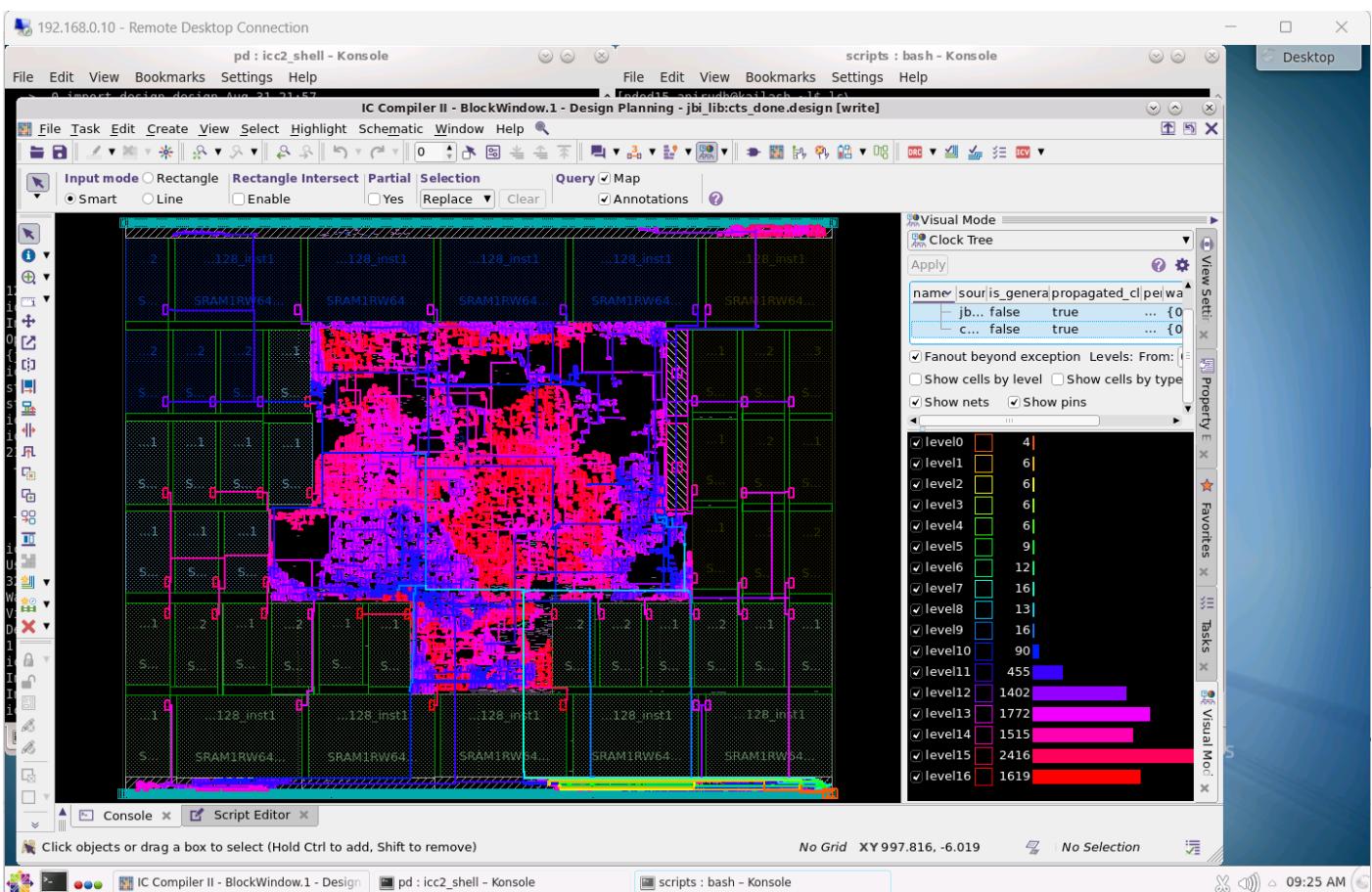


# CLOCK TREE SYNTHESIS (CTS)

14NM

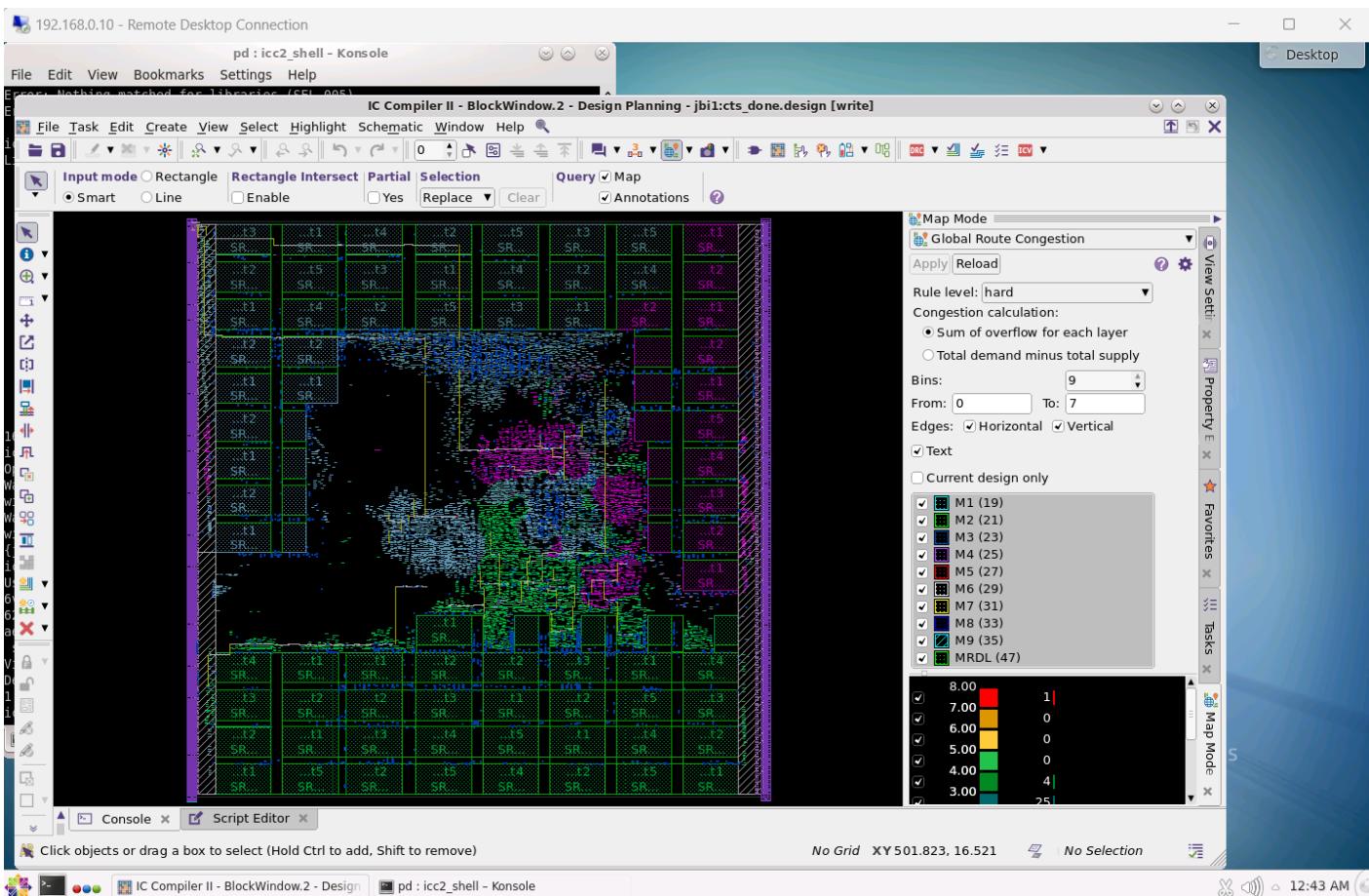


28NM

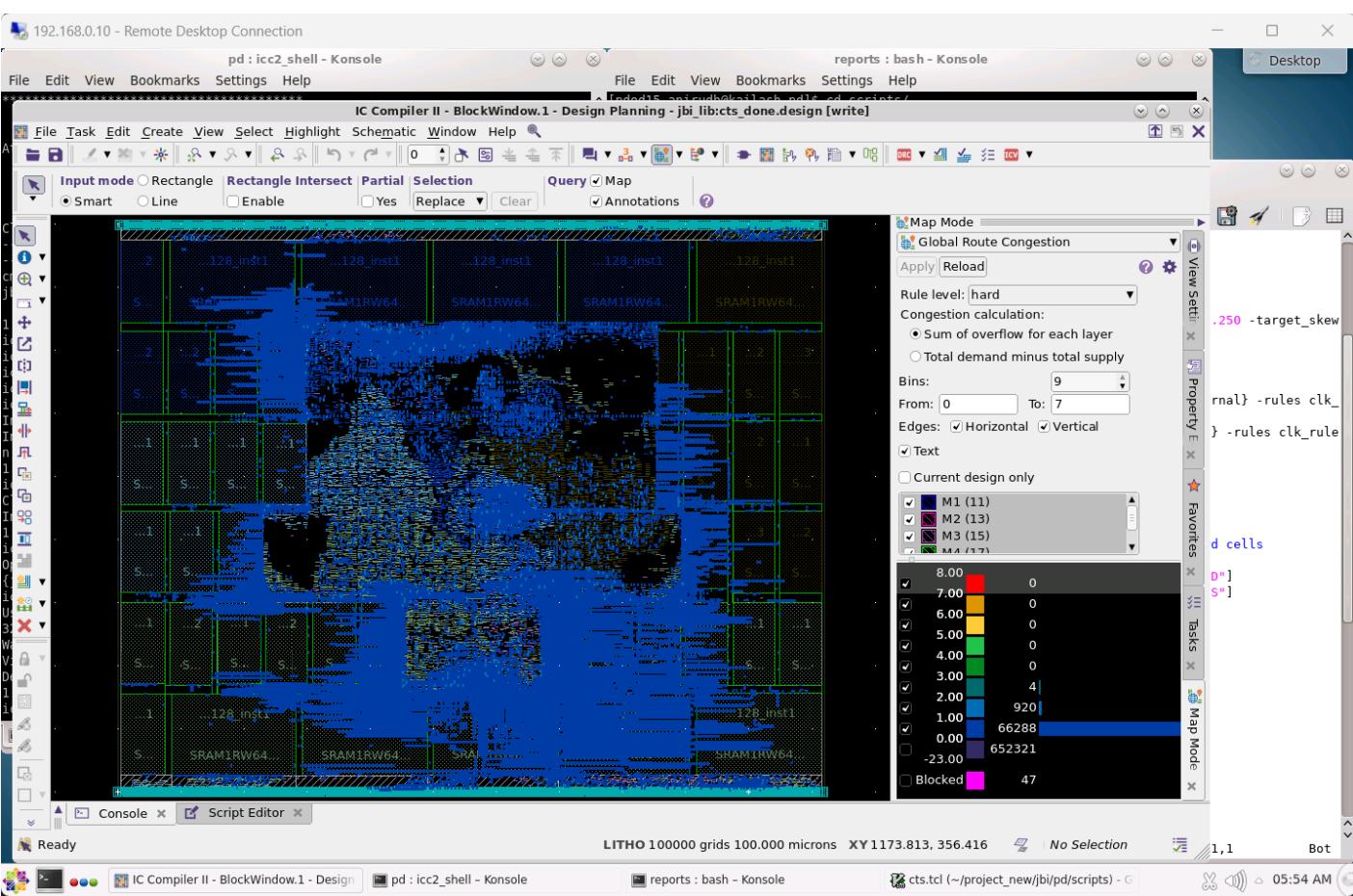


# CTS - GLOBAL ROUTE CONGESTION

14nm

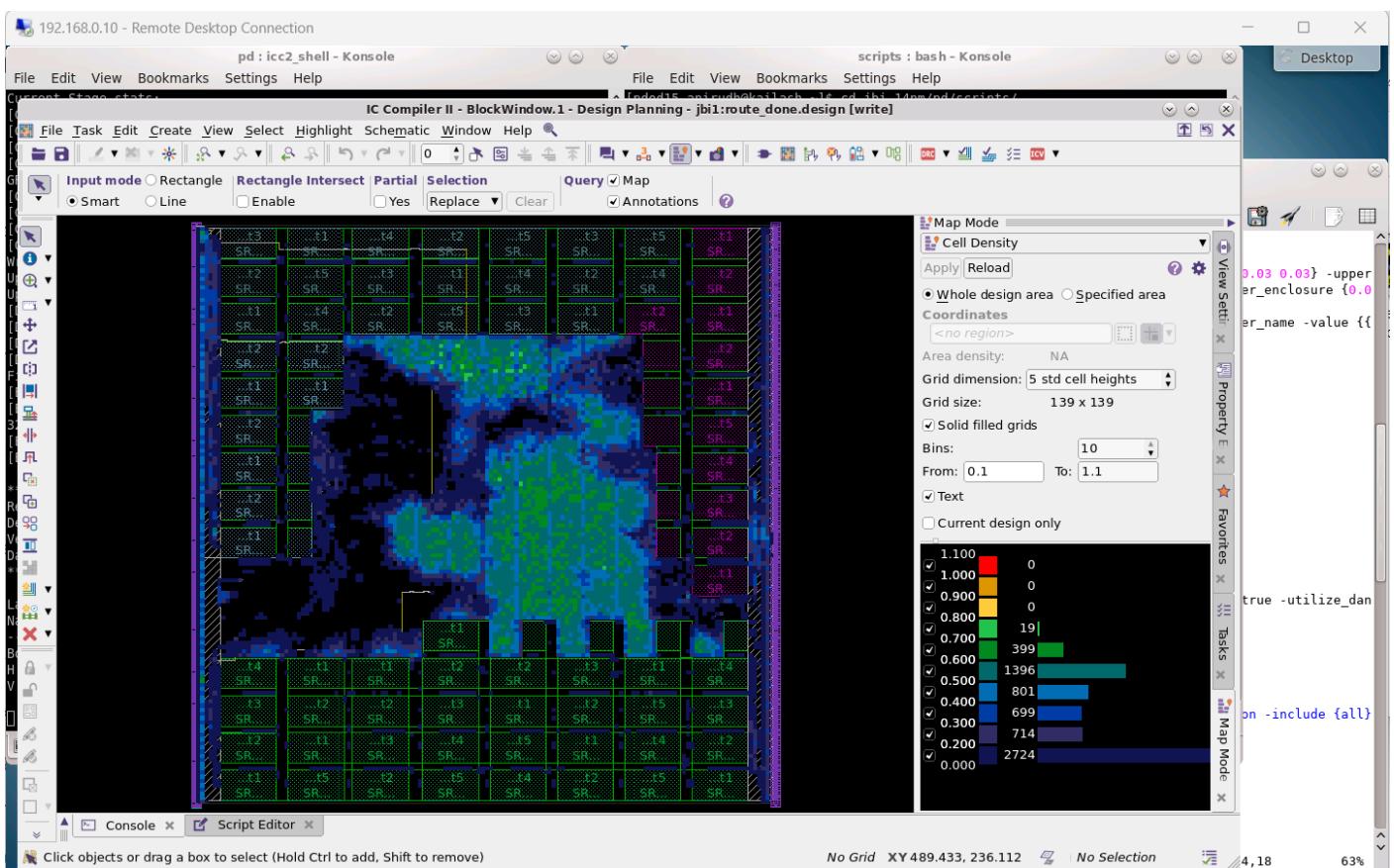


28nm

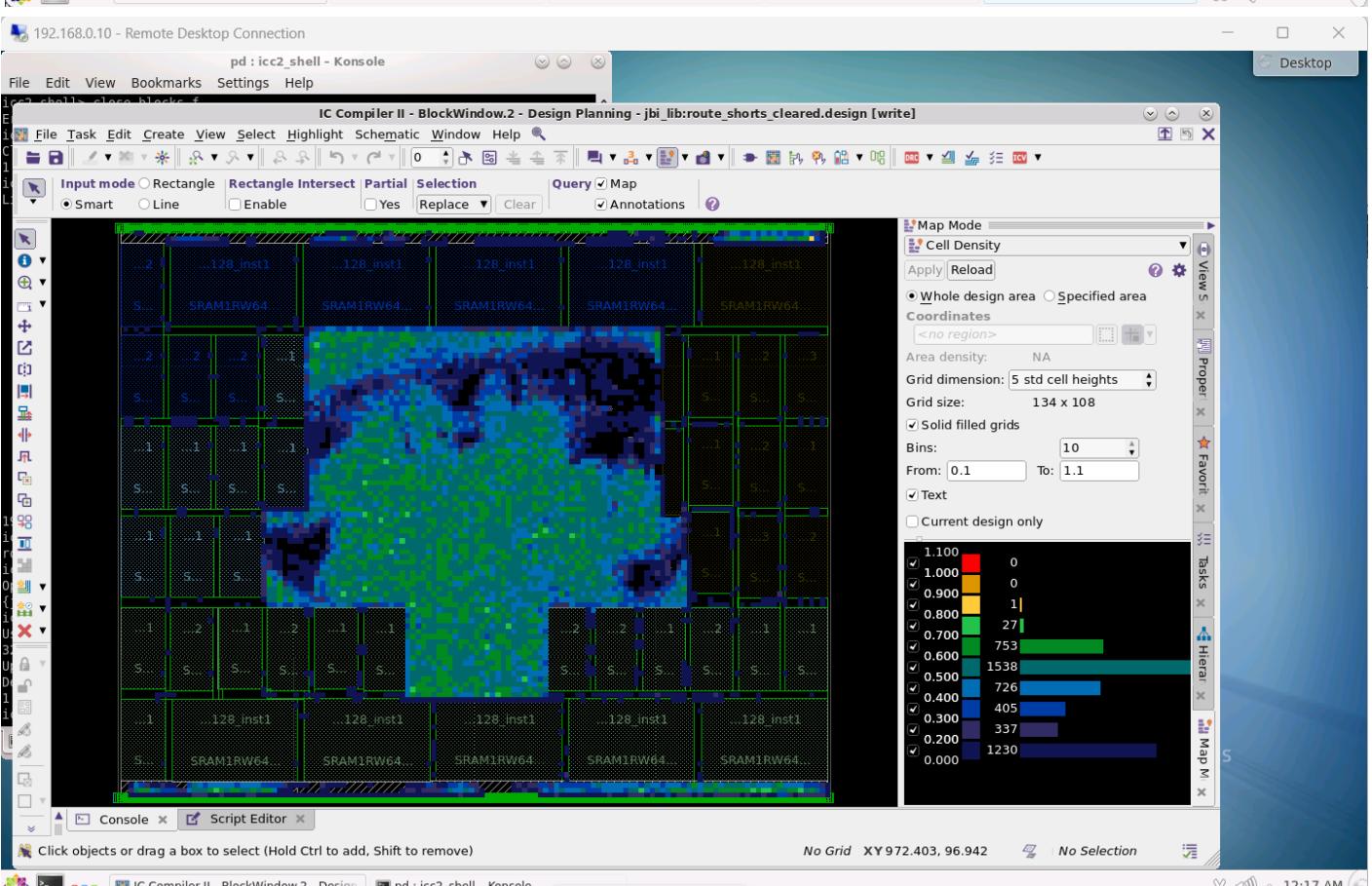


# ROUTING- CELL DENSITY

14nm



28nm



# DRC CLEAN

14NM

```

192.168.0.10 - Remote Desktop Connection
pd : tcsh - Konsole
File Edit View Bookmarks Settings Help
default-20231124 kailash.chipedge.local_19937.svf
default-20231124 kailash.chipedge.local_40704.svf
default-20231126 kailash.chipedge.local_36349.svf
default-20231126 kailash.chipedge.local_41708.svf
default-20231127 kailash.chipedge.local_1381.svf
fmax_LP.stats OPTIMISTIC.txt
fmax_LP.stats PESSIMISTIC HOLD_TNS.txt
fmax_LP.stats PESSIMISTIC NONE_BUFFER_COUNT.txt
fmax_LP.stats PESSIMISTIC NONE_POWER.txt
fmax_LP.stats PESSIMISTIC R2R_TNS.txt
fmax_LP.stats PESSIMISTIC R2R_WNS.txt
icc2_command.log
icc2_output.txt
icvDRC_run
inputs
lib
logs
outputs
PrimeTime
PrimeTime_2
PrimeTime_3
README
report_constraints_all_violator.rpt
report_qor_tapeout.rpt
reports
scripts
signoff_check_drc_live_run
signoff_drc_fix.rpt
signoff_fill_run
signoff_fix_drc_run
Synopsys_stack_trace_25364.txt
Synopsys_stack_trace_31203.txt
work
[pdod15-anirudh@kailash pd]$ gvim si
signoff_check_drc_live_run/ signoff_fix_drc_run/
signoff_drc_fix.rpt           signoff_fix_drc_run/
[pdod15-anirudh@kailash pd]$ gvim signoff_drc_fix.rpt
[pdod15-anirudh@kailash pd]$ gvim signoff_drc_fix.rpt
[pdod15-anirudh@kailash pd]$ 

```

Total number of nets = 39269  
0 open nets, of which 0 are frozen  
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets  
0 ports without pins of 0 cells connected to 0 nets  
0 ports of 0 cover cells connected to 0 non-p  
g nets  
Total number of DRCs = 0  
Total number of antenna violations = antenna checking not active  
Information: Routes in non-preferred voltage areas = 0 (ZRT-559)  
Updating the database ...  
Information: Removed design 'jbill:tape\_out\_ADR.design' from memory and disk. (NDMUI-064)

88572,34 99%

```

192.168.0.10 - Remote Desktop Connection
pd : tcsh - Konsole
File Edit Tools Syntax Buffers Window Help
reports/timing_gqr_placement.rpt
[pdod15-anirudh@kailash ~]$ cd project_new/jbi/pd/report
reports/timing_gqr_placement.rpt
[pdod15-anirudh@kailash ~]$ cd project_new/jbi/pd/reportorts
project_new/jbi/pd/reportorts: No such file or directory.
[pdod15-anirudh@kailash ~]$ cd project_new/jbi/pd/reports
[pdod15-anirudh@kailash reports]$ 
annotated_power.rpt      constraint_violator.rpt
check_design_pre_place.rpt core_utilization.rpt
check_legality_floorplan.txt drc.rpt
check_legality_placement.rpt floorplan_legality.rpt
check_legality.rpt         floorplan_tapcell_legality.rpt
check_pg_connectivity.rpt lvs.rpt
check_pg_drc.rpt          report_gqr.rpt
clock_gating.rpt          report_timing_gqr_placement.rpt
clock_qor.rpt              routes_drc.rpt
clock.rpt                 route_shorts.rpt
clocks.rpt                shorts_clean.rpt
clock_tree_options.rpt    trans_capsViolation.rpt
[pdod15-anirudh@kailash reports]$ ls
annotated_power.rpt      constraint_violator.rpt
check_design_pre_place.rpt core_utilization.rpt
check_legality_floorplan.txt drc.rpt
check_legality_placement.rpt floorplan_legality.rpt
check_legality.rpt         floorplan_tapcell_legality.rpt
check_pg_connectivity.rpt lvs.rpt
check_pg_drc.rpt          report_gqr.rpt
clock_gating.rpt          report_timing_gqr_placement.rpt
clock_qor.rpt              routes_drc.rpt
clock.rpt                 route_shorts.rpt
clocks.rpt                shorts_clean.rpt
clock_tree_options.rpt    trans_capsViolation.rpt
[pdod15-anirudh@kailash reports]$ gvim gvim shorts_clean.rpt
2 files to edit
[pdod15-anirudh@kailash reports]$ gvim rout
routes_drc.rpt route_shorts.rpt
[pdod15-anirudh@kailash reports]$ gvim routes_drc.rpt
[pdod15-anirudh@kailash reports]$ gvim routes_drc.rpt
[pdod15-anirudh@kailash reports]$ 

```

216,44 80t

28NM

## LVS CLEAN

14NM

```
[pdod15-anirudh@kailash reports]$ cd jbi_14nm/pd/reports
[pdod15-anirudh@kailash ~]$ report_constraints_all_violator.rpt
[pdod15-anirudh@kailash ~]$ report_qor_tapeout.rpt
[pdod15-anirudh@kailash ~]$ cd jbi_14nm/pd/report
jbi_14nm/pd/report: No such file or directory.
[pdod15-anirudh@kailash ~]$ cd jbi_14nm/pd/report
report_constraints_all_violator.rpt
report_qor_tapeout.rpt
[pdod15-anirudh@kailash ~]$ cd jbi_14nm/pd/report
report_constraints_all_violator.rpt
report_qor_tapeout.rpt
[pdod15-anirudh@kailash ~]$ cd jbi_14nm/pd/reports
[pdod15-anirudh@kailash reports]$ ls
annotated_power.rpt           report_constraint_all_violators_pt.rpt
check_legality_placement.rpt   report_constraints_all_violation.rpt
check_lvs_clean.rpt            report_qor_placement.rpt
check_lvs_err.rpt              report_qor_pre_placement.rpt
check_pg_connectivity_new_clean.rpt report_qor.rpt
check_pg_connectivity.rpt      report_timing_placement.rpt
check_pg_drc_new_clear.rpt    report_timing_pt.rpt
check_pg_drc_new.rpt          report_utilization.rpt
clock.rpt                      setup_fixed.rpt
hold_fixed.rpt                 trans.rpt
report_clock_qor.rpt
[pdod15-anirudh@kailash reports]$ gvim hold_fixed.rpt
[pdod15-anirudh@kailash reports]$ gvim hold_fixed.rpt
[pdod15-anirudh@kailash reports]$ gvim check_lvs_clean.rpt
check_legality_placement.rpt   check_pg_connectivity.rpt
check_lvs_clean.rpt            check_pg_drc_new_clear.rpt
check_lvs_err.rpt              check_pg_drc_new.rpt
check_pg_connectivity_new_clean.rpt
[pdod15-anirudh@kailash reports]$ gvim check_lvs_err.rpt
check_lvs_clean.rpt            check_lvs_err.rpt
check_lvs_clean.rpt            check_lvs_clean.rpt
[pdod15-anirudh@kailash reports]$ gvim check_lvs_clean.rpt
[pdod15-anirudh@kailash reports]$ 
```

**check\_lvs\_clean.rpt (~/jbi\_14nm/pd/reports) - GVIM**

```
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_22 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_23 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_24 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_25 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_26 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_27 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_28 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_29 has less than 2 valid port. Skip
open checking for this net. (RT-204)
[Check Net] All nets are submitted.
[Check Net] 100% Elapsed = 0:00:26, CPU = 0:00:27
Information: Detected open violation for Net VDD. BBox: (1.9580 1.9060)(412.96
40 412.4940). (RT-585)
Information: Detected open violation for Net VSS. BBox: (1.9580 1.6400)(412.96
40 412.7600). (RT-585)

=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.

=====
Total number of input nets is 39315.
Total number of short violations is 0.
Total number of open nets is 2.
Open nets are VDD VSS
Total number of floating route violations is 0.

Elapsed = 0:00:26, CPU = 0:00:27
1
189,1 Bot
```

28NM

```
[pdod15-anirudh@kailash ~]$ cd project_new/jbi/pd/report
reports                  report_timing_qor_placement.rpt
[pdod15-anirudh@kailash ~]$ cd project_new/jbi/pd/reports
project_new/jbi/pd/reports: No such file or directory.
[pdod15-anirudh@kailash ~]$ cd project_new/jbi/pd/reports
[pdod15-anirudh@kailash reports]$ ls
annotated_power.rpt        constraint_violator.rpt
check_design_pre_place.rpt core_utilization.rpt
check_legality_floorplan.txt drc.rpt
check_legality_placement.rpt floorplan_legality.rpt
check_legality.rpt          floorplan_tapcell_legality.rpt
check_pg_connectivity.rpt   lvs.rpt
check_pg_drc.rpt            report_qor.rpt
clock_gating.rpt           report_timing_qor_placement.rpt
clock_qor.rpt               routes_drc.rpt
clock.rpt                  route_shorts.rpt
clocks.rpt                 shorts_clean.rpt
clock_tree_options.rpt     trans_capsViolation.rpt
[pdod15-anirudh@kailash reports]$ ls
annotated_power.rpt        constraint_violator.rpt
check_design_pre_place.rpt core_utilization.rpt
check_legality_floorplan.txt drc.rpt
check_legality_placement.rpt floorplan_legality.rpt
check_legality.rpt          floorplan_tapcell_legality.rpt
check_pg_connectivity.rpt   lvs.rpt
check_pg_drc.rpt            report_qor.rpt
clock_gating.rpt           report_timing_qor_placement.rpt
clock_qor.rpt               routes_drc.rpt
clock.rpt                  route_shorts.rpt
clocks.rpt                 shorts_clean.rpt
clock_tree_options.rpt     trans_capsViolation.rpt
[pdod15-anirudh@kailash reports]$ gvim gvim shorts_clean.rpt
2 files to edit
[pdod15-anirudh@kailash reports]$ gvim rout
routes_drc.rpt             route_shorts.rpt
[pdod15-anirudh@kailash reports]$ gvim routes_drc.rpt
[pdod15-anirudh@kailash reports]$ gvim routes_drc.rpt
[pdod15-anirudh@kailash reports]$ gvim shorts_clean.rpt
[pdod15-anirudh@kailash reports]$ 
```

**shorts\_clean.rpt (~/project\_new/jbi/pd/reports) - GVIM**

```
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_38 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_39 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_40 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_41 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_42 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_43 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_44 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_45 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_46 has less than 2 valid port. Skip
open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED_47 has less than 2 valid port. Skip
open checking for this net. (RT-204)
[Check Net] All nets are submitted.
[Check Net] 100% Elapsed = 0:00:42, CPU = 0:00:43

=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.

=====
Total number of input nets is 37527.
Total number of short violations is 0.
Total number of open nets is 0.
Total number of floating route violations is 0.

Elapsed = 0:00:42, CPU = 0:00:43
1
227,1 Bot
```

# SETUP TIMING

14NM

192.168.0.10 - Remote Desktop Connection

reports : tcsh - Konsole

```

File Edit View Bookmarks Settings Help
work
[pdod15-anirudh@kailash pd]$ cd re
report_constraints_all_violator.rpt reports/
report_qor_tapeout.rpt
[pdod15-anirudh@kailash pd]$ cd report
report: No such file or directory.
[pdod15-anirudh@kailash pd]$ cd repo
report_constraints_all_violator.rpt reports/
report_qor_tapeout.rpt
[pdod15-anirudh@kailash pd]$ cd report
report_constraints_all_violator.rpt reports/
report_qor_tapeout.rpt
[pdod15-anirudh@kailash pd]$ cd reports/
[pdod15-anirudh@kailash reports]$ ls
annotated_power.rpt           report_constraint_all_violators_pt.rpt
check_legality_placement.rpt   report_constraints_all_violation.rpt
check_lvs_clean.rpt            report_qor_placement.rpt
check_lvs_err.rpt              report_qor_pre_placement.rpt
check_pg_connectivity_new_clean.rpt report_qor.rpt
check_pg_connectivity.rpt      report_timing_placement.rpt
check_pg_drc_new_clear.rpt    report_timing_pt.rpt
check_pg_drc_new.rpt          report_utilization.rpt
clock.rpt                      setup_fixed.rpt
hold_fixed.rpt                 trans.rpt
report_clock_qor.rpt          report_qor_placement.rpt
report_clock_qor.rpt          report_timing_placement.rpt
report_constraint_all_violators_pt.rpt report_constraints_all_violation.rpt
report_qor_placement.rpt       report_qor_pre_placement.rpt
report_qor_pt                  report_timing_pt.rpt
report_utilization.rpt         report_utilization.rpt
[pdod15-anirudh@kailash reports]$ gvim setup_fixed.rpt
[pdod15-anirudh@kailash reports]$ gvim setup_fixed.rpt
[pdod15-anirudh@kailash reports]$ gvim setup_fixed.rpt
[pdod15-anirudh@kailash reports]$ ]

```

reports : tcsh

setup\_fixed.rpt (~/jbi\_14nm/pd/reports) - GVIM

```

File Edit Tools Syntax Buffers Window Help
u_mout/U6684/X (SAEDSLVT14_INV_S_9) 0.00458 1.35532 f
u_mout/U6682/X (SAEDSLVT14_INV_S_20) 0.00509 1.36041 f
u_mout/U627/X (SAEDSLVT14_INV_S_6) 0.01167 1.37208 r
u_mout/U2279/X (SAEDSLVT14_INV_S_16) 0.00664 1.37872 f
u_mout/U3005/X (SAEDSLVT14_NR2_MM_12) 0.00841 1.38713 r
u_mout/U4852/X (SAEDSLVT14_OR3_4) 0.02851 1.41564 r
u_mout/U1955/X (SAEDSLVT14_NR2_MM_4) 0.00816 1.42381 f
u_mout/U335/X (SAEDSLVT14_INV_S_6) 0.00383 1.42764 r
u_mout/U1709/X (SAEDSLVT14_NR2_MM_4) 0.00416 1.43180 f
u_mout/U247/X (SAEDSLVT14_ND2_CDC_4) 0.00532 1.43712 r
u_mout/U228/X (SAEDSLVT14_ND3B_4) 0.01431 1.45143 r
ropt_d_inst_37697/X (SAEDSLVT14_BUF_20) 0.00910 1.46052 r
u_mout/U6947/X (SAEDSLVT14_E04_U_0P5) 0.00721 1.46773 f
u_mout/eco_cell/X (SAEDSLVT14_BUF_6) 0.00965 1.47738 f
u_mout/U6849/X (SAEDSLVT14_E04_1) 0.00300 1.48038 r
mout/ropt_d_inst_37672/X (SAEDSLVT14_BUF_8) 0.00219 1.48257 r
u_mout/U7000/X (SAEDSLVT14_E04_2) 0.00949 1.49206 f
u_mout/ZBUF_162_inst_35891/X (SAEDSLVT14_BUF_20) 0.00205 1.49411 f
u_mout/U6997/X (SAEDSLVT14_BUF_20) 0.00210 1.49621 f
eco_cell_349/X (SAEDSLVT14_BUF_12) 0.00095 1.49716 f
jbi_io_j_adp[1] (out) 0.00008 1.49724 f
data arrival time 1.49724

clock jbus_gclk (rise edge) 1.20000 1.20000
clock network delay (propagated) 0.77122 1.97122
output external delay -0.32000 1.65122
data required time 1.65123

-----
data required time 1.65123
data arrival time -1.49724

-----
slack (MET) 0.15398

```

"setup\_fixed.rpt" 81L, 4752C 81,1 Bot

28NM

192.168.0.10 - Remote Desktop Connection

reports : tcsh - Konsole

```

File Edit View Bookmarks Settings Help
readme_to_run_starrc_prime_time
report_timing_qor_placement.rpt
reports
routes drc.rpt
scripts
setup.rpt
signoff_check_drc_live_run
signoff_fill_run
signoff_fix_drc_run
icc2 shell> exit
Maximum memory usage for this session: 1236.88 MB
Maximum memory usage for this session including child processes: 1236.88 MB
CPU usage for this session: 137 seconds ( 0.04 hours)
Elapsed time for this session: 575 seconds ( 0.16 hours)
Thank you for using IC Compiler II.
[pdod15-anirudh@kailash pd]$ cd repo
reports/           report_timing_qor_placement.rpt
[pdod15-anirudh@kailash pd]$ cd reports/
[pdod15-anirudh@kailash reports]$ ls
annotated_power.rpt           core_utilization.rpt
check_design_pre_place.rpt     drc.rpt
check_legality_floorplan.txt   floorplan_legality.rpt
check_legality_placement.rpt   floorplan_tapcell_legality.rpt
check_legality.rpt             hold.rpt
check_pg_connectivity.rpt      lvs.rpt
check_pg_drc.rpt               report_qor.rpt
clock_gating.rpt               report_timing_qor_placement.rpt
clock_qor.rpt                  routes_drc.rpt
clock.rpt                      route_shorts.rpt
clocks.rpt                     setup.rpt
clock_tree_options.rpt         shorts_clean.rpt
constraint_violator.rpt        trans_capsViolation.rpt
[pdod15-anirudh@kailash reports]$ gvim setup.rpt
[pdod15-anirudh@kailash reports]$ PWD
/tools/synopsys/installers/tetramax/bin/PWD: Permission denied.
[pdod15-anirudh@kailash reports]$ pwd
/home/pdod15-anirudh/project_new/jbi/pd/reports
[pdod15-anirudh@kailash reports]$ gvim setup.rpt
[pdod15-anirudh@kailash reports]$ ]

```

reports : tcsh

setup.rpt (~/project\_new/jbi/pd/reports) - GVIM

```

File Edit Tools Syntax Buffers Window Help
u_mout/pktout_asm/ctmTdsLR_1_7000/Y (NAND2X4_LVT) 0.018234 1.619773 f
u_mout/pktout_asm/ctmTdsLR_1_34568/Y (A0221X1_RVT) 0.041580 1.661353 r
u_mout/pktout_asm/ctmTdsLR_2_32047/Y (A021X1_LVT) 0.041885 1.703238 r
u_mout/pktout_asm/ctmTdsLR_1_32046/Y (OR2X4_LVT) 0.049248 1.752486 r
u_mout/pktout_asm/ctmTdsLR_4_35263/Y (NOR2X1_LVT) 0.042610 1.795096 r
u_mout/pktout_asm/ctmTdsLR_3_35262/Y (INVX1_LVT) 0.041447 1.836543 f
u_mout/pktout_asm/ctmTdsLR_2_35261/Y (MUX2X1_LVT) 0.006962 1.843505 r
u_mout/pktout_asm/ctmTdsLR_1_35260/Y (XNOR3X2_LVT) 0.032196 1.875701 r
u_mout/pktout_asm/ctmTdsLR_1_35260/Y (XNOR3X2_LVT) 0.016932 1.892633 r
u_mout/pktout_asm/U1092/Y (XOR3X2_LVT) 0.025918 1.918551 f
u_mout/pktout_asm/ctmTdsLR_1_9612/Y (XOR3X2_LVT) 0.018629 1.937180 r
gce_d_BUFB_4_inst_45752/Y (NBUFFX16_LVT) 0.025845 1.963025 r
jbi_io_j_adp[2] (out) 0.010275 1.973300 r
data arrival time 1.973300

clock cmp_gclk (rise edge) 1.800000 1.800000
clock network delay (propagated) 0.606017 2.406017
output external delay -0.320000 2.086017
data required time 2.086020

-----
data required time 2.086020
data arrival time -1.973300

-----
slack (MET) 0.112717

```

"setup.rpt" 78L, 4427C 75,3 Bot

setup.rpt (~/project\_new/jbi/pd/reports) - GVIM

```

File Edit Tools Syntax Buffers Window Help
u_mout/pktout_asm/ctmTdsLR_1_7000/Y (NAND2X4_LVT) 0.018234 1.619773 f
u_mout/pktout_asm/ctmTdsLR_1_34568/Y (A0221X1_RVT) 0.041580 1.661353 r
u_mout/pktout_asm/ctmTdsLR_2_32047/Y (A021X1_LVT) 0.041885 1.703238 r
u_mout/pktout_asm/ctmTdsLR_1_32046/Y (OR2X4_LVT) 0.049248 1.752486 r
u_mout/pktout_asm/ctmTdsLR_4_35263/Y (NOR2X1_LVT) 0.042610 1.795096 r
u_mout/pktout_asm/ctmTdsLR_3_35262/Y (INVX1_LVT) 0.041447 1.836543 f
u_mout/pktout_asm/ctmTdsLR_2_35261/Y (MUX2X1_LVT) 0.006962 1.843505 r
u_mout/pktout_asm/ctmTdsLR_1_35260/Y (XNOR3X2_LVT) 0.032196 1.875701 r
u_mout/pktout_asm/ctmTdsLR_1_35260/Y (XNOR3X2_LVT) 0.016932 1.892633 r
u_mout/pktout_asm/U1092/Y (XOR3X2_LVT) 0.025918 1.918551 f
u_mout/pktout_asm/ctmTdsLR_1_9612/Y (XOR3X2_LVT) 0.018629 1.937180 r
gce_d_BUFB_4_inst_45752/Y (NBUFFX16_LVT) 0.025845 1.963025 r
jbi_io_j_adp[2] (out) 0.010275 1.973300 r
data arrival time 1.973300

clock cmp_gclk (rise edge) 1.800000 1.800000
clock network delay (propagated) 0.606017 2.406017
output external delay -0.320000 2.086017
data required time 2.086020

-----
data required time 2.086020
data arrival time -1.973300

-----
slack (MET) 0.112717

```

setup.rpt (~/project\_new/jbi/pd/reports) - GVIM

# HOLD TIMING

14NM

192.168.0.10 - Remote Desktop Connection

reports : tcsh - Konsole

```
[pdod15-anirudh@kailash reports]$ gvim setup.rpt
[pdod15-anirudh@kailash reports]$ pwd
/tools/synopsys/installers/tetramax/bin/PWD: Permission denied.
[pdod15-anirudh@kailash reports]$ pwd
/home/pdod15-anirudh/project_new/jbi/pd/reports
[pdod15-anirudh@kailash reports]$ gvim setup.rpt
[pdod15-anirudh@kailash reports]$ gvim hold.rpt
[pdod15-anirudh@kailash reports]$ gvim hold.rpt
[pdod15-anirudh@kailash reports]$ gvim hold.rpt
[pdod15-anirudh@kailash reports]$ cd
CD: Command not found.
[pdod15-anirudh@kailash reports]$ cd
[pdod15-anirudh@kailash ~]$ cd jbi_14nm/pd/reports
report_constraints_all_violator.rpt reports/
report_qor_tapeout.rpt
[pdod15-anirudh@kailash ~]$ cd jbi_14nm/pd/report
jbi_14nm/pd/report: No such file or directory.
[pdod15-anirudh@kailash ~]$ cd jbi_14nm/pd/report
report_constraints_all_violator.rpt reports/
report_qor_tapeout.rpt
[pdod15-anirudh@kailash ~]$ cd jbi_14nm/pd/reports
[pdod15-anirudh@kailash reports]$ ls
annotated_power.rpt          report_constraint_all_violators_pt.rpt
check_legality_placement.rpt   report_constraints_allViolation.rpt
check_lvs_clean.rpt           report_qor_placement.rpt
check_lvs_err.rpt              report_qor_pre_placement.rpt
check_pg_connectivity_new_clean.rpt report_qor.rpt
check_pg_connectivity.rpt      report_timing_placement.rpt
check_pg_drc_new_clear.rpt    report_timing_pt.rpt
check_pg_drc_new.rpt          report_utilization.rpt
clock.rpt                     setup_fixed.rpt
hold_fixed.rpt                trans.rpt
report_clock_qor.rpt
[pdod15-anirudh@kailash reports]$ gvim hold_fixed.rpt
[pdod15-anirudh@kailash reports]$ gvim hold_fixed.rpt
[pdod15-anirudh@kailash reports]$ 
```

hold\_fixed.rpt (~/jbi\_14nm/pd/reports) - GVIM

Path Type: min

Point	Incr	Path
clock jbus_gclk (rise edge)	0.00000	0.00000
clock network delay (propagated)	0.49492	0.49492
u_ncio/u_ncio_ucbp/ucb_bus_in/indata_buf_ff/q_reg[108]/CK (SAEDHVT14_FDP_V2L_P_1)	0.00000	0.49492 r
u_ncio/u_ncio_ucbp/ucb_bus_in/indata_buf_ff/q_reg[108]/Q (SAEDHVT14_FDP_V2LP_1)	0.04603	0.54095 f
u_ncio/U880/X (SAEDHVT14_INV_S_1)	0.03670	0.57765 r
u_ncio/U882/X (SAEDHVT14_OAI22_0P5)	0.05181	0.62946 f
u_ncio/u_ncio_ucbp/ucb_bus_in/indata_buf_ff/q_reg[44]/D (SAEDHVT14_FDP_V2LP_1)	-0.00277	0.62669 f
data arrival time	0.62669	
clock jbus_gclk (rise edge)	0.00000	0.00000
clock network delay (propagated)	0.59637	0.59637
u_ncio/u_ncio_ucbp/ucb_bus_in/indata_buf_ff/q_reg[44]/CK (SAEDHVT14_FDP_V2LP_1)	0.00000	0.59637 r
library hold time	0.02211	0.61849
data required time	0.61849	
data required time	0.61849	
data arrival time	-0.62669	
slack (MET)	0.00082	

"hold\_fixed.rpt" 49L, 2506C 49,1 Bot

192.168.0.10 - Remote Desktop Connection

reports : tcsh - Konsole

hold\_fixed.rpt (~/jbi\_14nm/pd/reports)

28NM

192.168.0.10 - Remote Desktop Connection

reports : tcsh - Konsole

```
routes drc.rpt
scripts
setup.rpt
signoff check_drc_live_run
signoff fill run
signoff fix drc run
icc2_shell> exit
Maximum memory usage for this session: 1236.88 MB
Maximum memory usage for this session including child processes: 1236.88 MB
CPU usage for this session: 137 seconds ( 0.4 hours)
Elapsed time for this session: 575 seconds ( 0.16 hours)
Thank you for using IC Compiler II.
[pdod15-anirudh@kailash pd]$ cd repo
reports/          report_timing_qor_placement.rpt
[pdod15-anirudh@kailash pd]$ cd reports/
[pdod15-anirudh@kailash reports]$ ls
annotated_power.rpt core_utilization.rpt
check_design_pre_place.rpt drc.rpt
check_legality_floorplan.txt floorplan_legality.rpt
check_legality_placement.rpt floorplan_tapcell_legality.rpt
check_legality.rpt hold.rpt
check_pg_connectivity.rpt lvs.rpt
check_pg_drc.rpt report_qor.rpt
clock_gating.rpt report_timing_qor_placement.rpt
clock_qor.rpt routes_drc.rpt
clock_rpt route_shorts.rpt
clocks.rpt setup.rpt
clock_tree_options.rpt shorts_clean.rpt
constraint_violator.rpt trans_capsViolation.rpt
[pdod15-anirudh@kailash reports]$ gvim setup.rpt
[pdod15-anirudh@kailash reports]$ PWD
/tools/synopsys/installers/tetramax/bin/PWD: Permission denied.
[pdod15-anirudh@kailash reports]$ pwd
/home/pdod15-anirudh/project_new/jbi/pd/reports
[pdod15-anirudh@kailash reports]$ gvim setup.rpt
[pdod15-anirudh@kailash reports]$ gvim hold.rpt
[pdod15-anirudh@kailash reports]$ gvim hold.rpt
[pdod15-anirudh@kailash reports]$ gvim hold.rpt
[pdod15-anirudh@kailash reports]$ 
```

hold.rpt (~/project\_new/jbi/pd/reports) - GVIM

Endpoint: u\_ncio/u\_mrqq\_buf/u\_mrqq\_buf/dout\_scan\_reg/q\_reg[54] (rising edge-triggered flip-flop clocked by jbus\_gclk)

Mode: func  
Corner: fast  
Scenario: func\_fast  
Path Group: MACRO2REG  
Path Type: min

Point	Incr	Path
clock jbus_gclk (rise edge)	0.000000	0.000000
clock network delay (propagated)	0.457993	0.457993
u_ncio/u_mrqq_buf/u_mrqq_buf/sram64x128_inst1/CE (SRAM1RW64x128)	0.000000	0.457993 r
u_ncio/u_mrqq_buf/u_mrqq_buf/sram64x128_inst1/[54] (SRAM1RW64x128)	0.088406	0.538398 r
u_ncio/u_mrqq_buf/u_mrqq_buf/dout_scan_reg/q_reg[54]/D (SDFFARX1_HVT)	-0.006131	0.532268 r
data arrival time	0.532268	
clock jbus_gclk (rise edge)	0.000000	0.000000
clock network delay (propagated)	0.545044	0.545044
u_ncio/u_mrqq_buf/u_mrqq_buf/dout_scan_reg/q_reg[54]/CLK (SDFFARX1_HVT)	0.000000	0.545044 r
library hold time	-0.018421	0.526623
data required time	0.526623	
data required time	0.526623	
data arrival time	-0.532268	
slack (MET)	0.005645	

"hold.rpt" 48L, 2426C 48,1 Bot

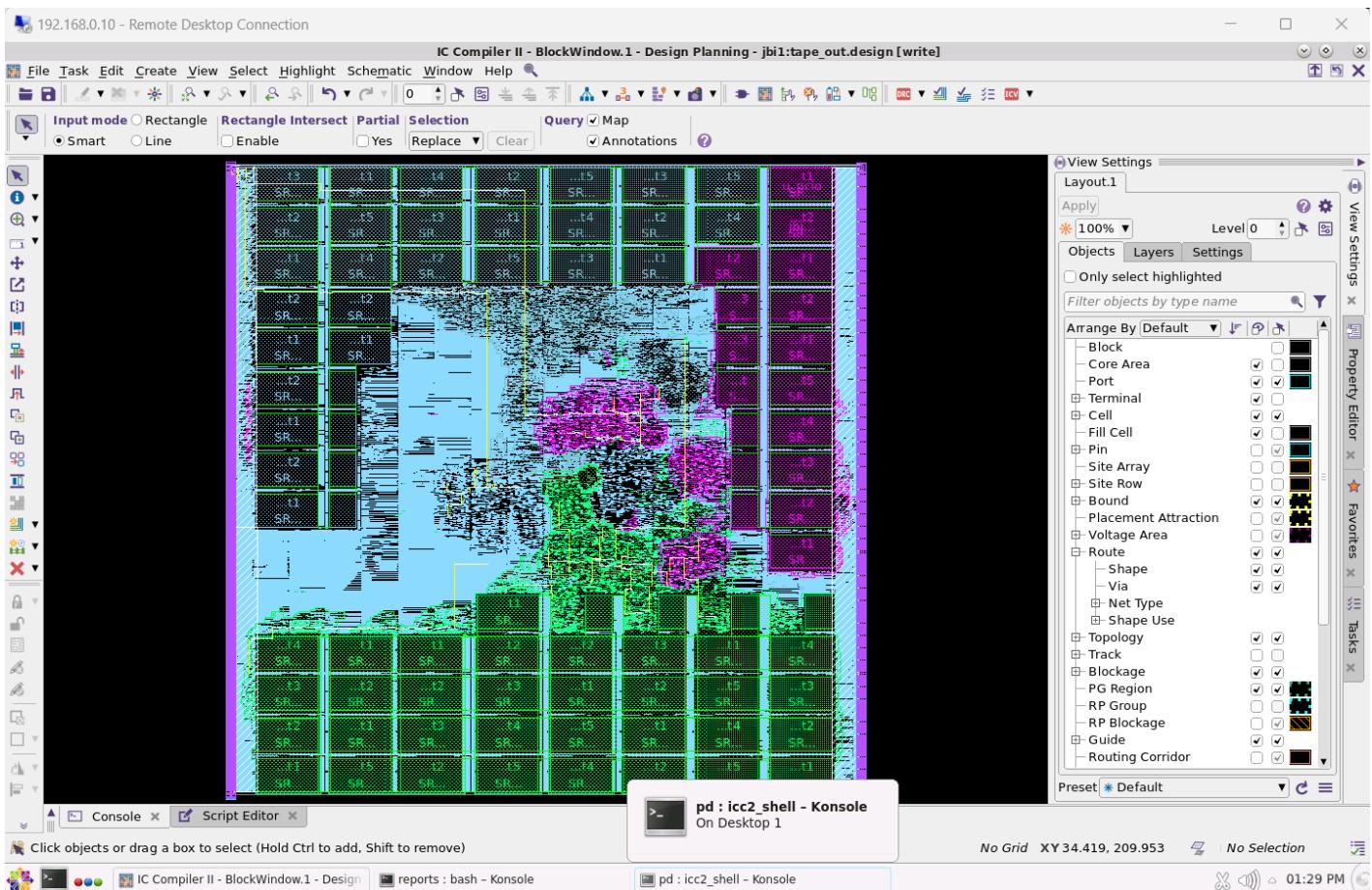
192.168.0.10 - Remote Desktop Connection

reports : tcsh - Konsole

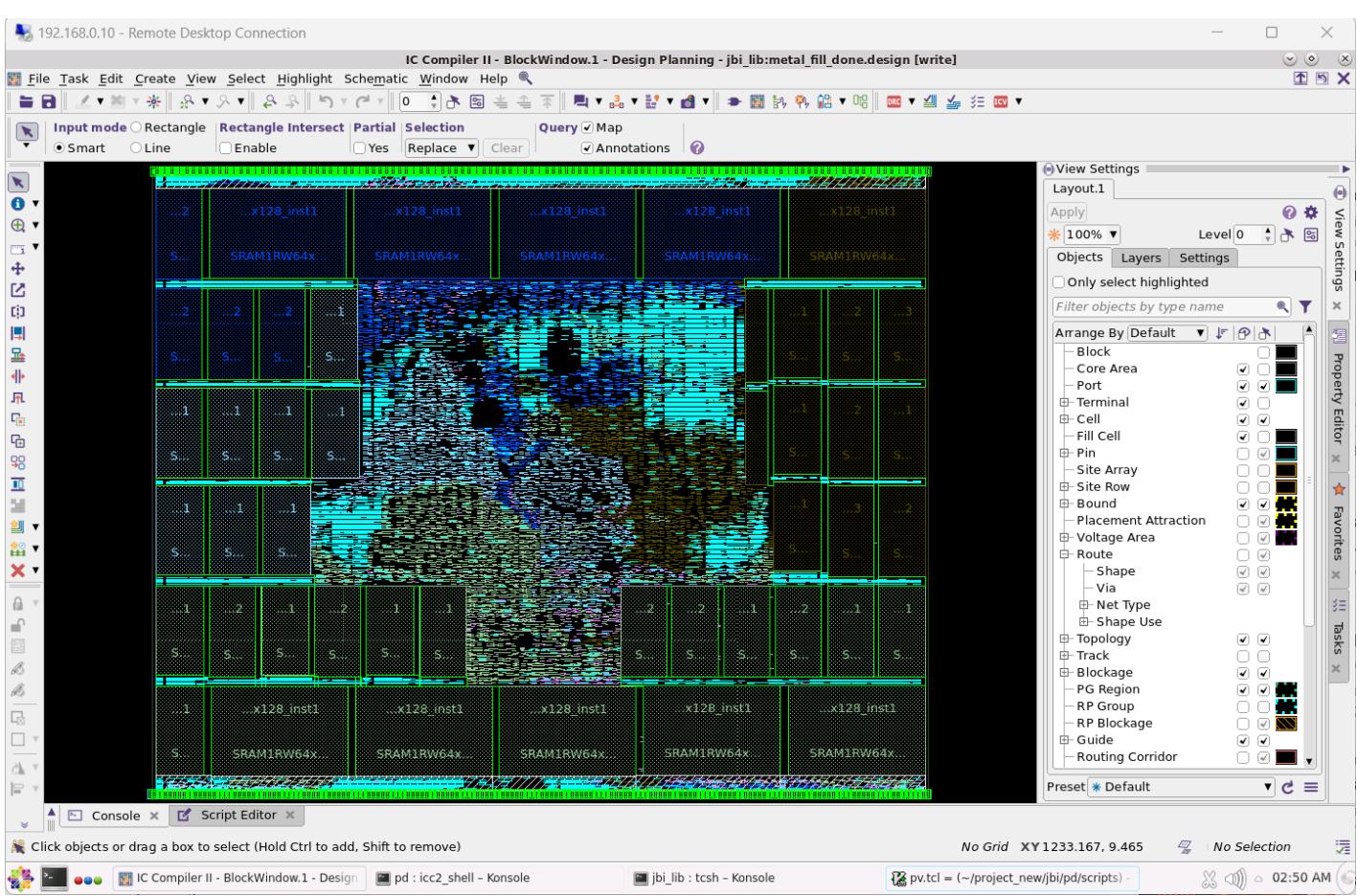
hold.rpt (~/project\_new/jbi/pd/reports)

# CLEAN GDS II

14NM



28NM



## CONCLUSION

In conclusion, the implementation of my tailored floorplanning and power planning methodology, applied across both the 14nm and 28nm nodes using Synopsys EDA tools, has demonstrated superior efficiency and error-free results in the physical design flow. This approach not only significantly accelerates the design process, saving valuable time for designers, but also enhances the Quality of Results (QOR) of the final design. The observed improvements underscore the effectiveness and reliability of the tailored methodology in optimizing the floorplan and power plan during the physical design phase.

## ACKNOWLEDGEMENT

Dear Dr. Choi,

I extend my sincere thanks for granting me the opportunity to conduct this research under your expert guidance. I have attached the research paper formatted according to the IEEE Conference guidelines and am eager to move forward with the publication process at your earliest convenience.

I remain open to any edits or modifications deemed necessary for the journal submission.

Thank you once again.

Best regards,

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PH: 3125398691  
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