ECE597: SPECIAL PROBLEM

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SUMMARY REPORT

Title: Precision Methodology: Enhancing VLSI Physical Design through Tailored Floorplan and Power Plan Strategies

Abstract:

This summary presents a research report comparing industry-standard Floorplan and Powerplan methodologies with an innovative approach. The proposed methodologies were validated through practical implementation on two real-time Block Level designs, utilizing 14nm and 28nm technology nodes for the OpenSPARC T1 processor.

Introduction:

This research provides a comparative analysis between conventional industry methods and a novel approach in Floorplan and Powerplan design. The effectiveness of the proposed methodology was validated through rigorous testing on two distinct technology nodes (14nm and 28nm) using the OpenSPARC T1 processor as the benchmark.

Comparison:

The paper meticulously contrasts the industry-standard methodology with the proposed approach, emphasizing the significance of error-free, efficient Floorplan and Powerplan design. The validation process involved the implementation of the methodologies on two OpenSPARC T1 processors designed in different technology nodes, showcasing the versatility and applicability of the proposed methodology across various technology nodes.

Key Points:

1. **Innovation in Methodology:** The research introduces a novel approach to Floorplan and Powerplan design, offering a promising alternative to existing industry standards.

2. **Practical Validation:** The proposed methodology was applied to two Block Level designs, each using different technology nodes (14nm and 28nm), ensuring practical applicability and adaptability.

3. **Technology Node Versatility:** The OpenSPARC T1 processor serves as a consistent benchmark, demonstrating the methodology's effectiveness across diverse technology nodes.

4. **Optimal Quality of Results (QOR):** The proposed methodology not only ensures error-free designs but also aims for optimum Quality of Results, contributing to enhanced overall chip performance.

5. **Efficient and Quick Implementation:** Emphasis is placed on the efficiency and speed of the proposed methodology, addressing the industry's demand for timely and accurate Floorplan and Powerplan strategies.

This research contributes valuable insights into advancing VLSI Physical Design methodologies, showcasing the adaptability and performance gains achieved through precision Floorplan and Powerplan strategies.

Industry used/Traditional technique:

Floorplan Methodology:

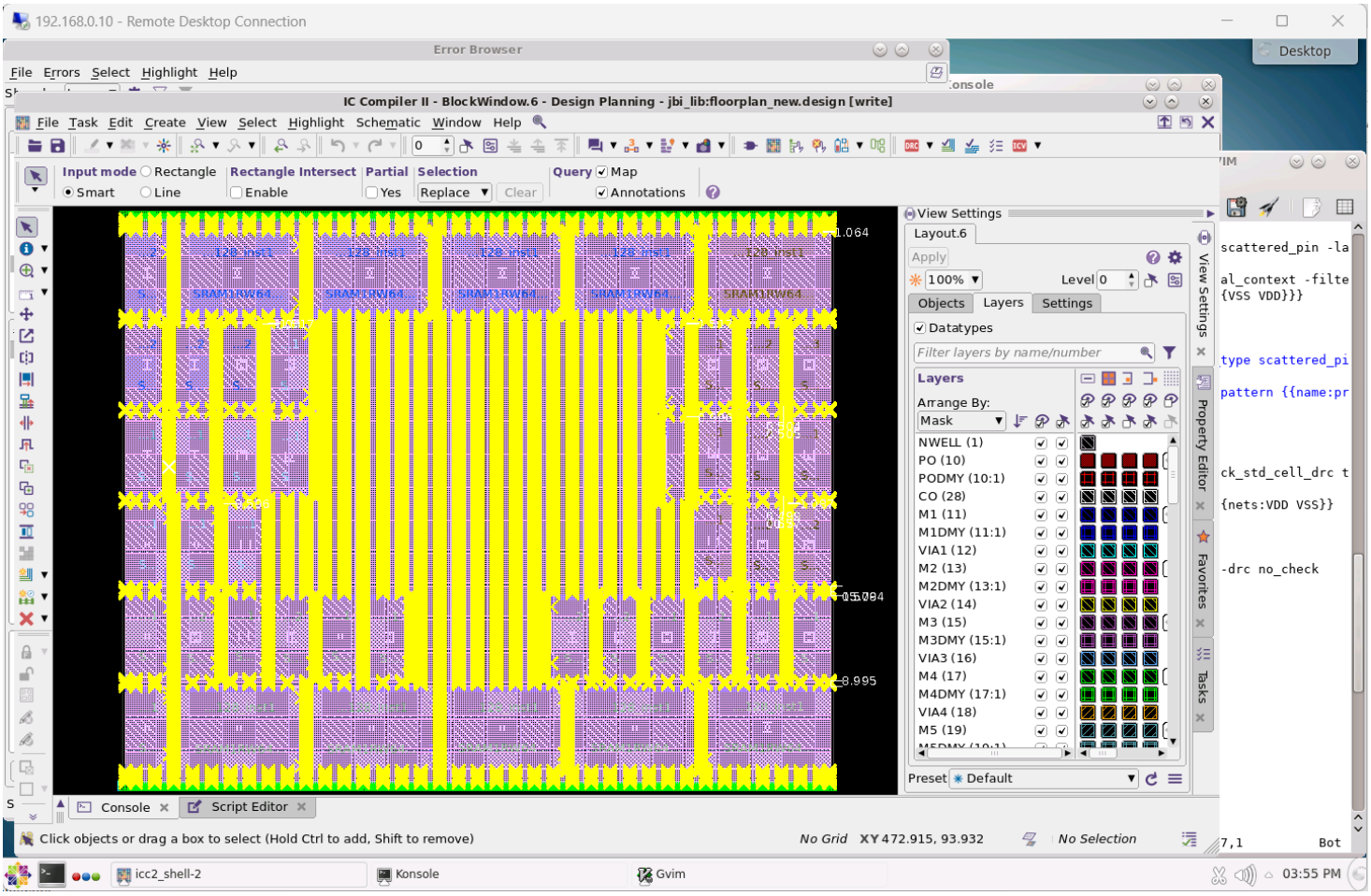
1) Sanity Check
   - check_netlist()
   - check_timing()
   - report_design_mismatch()
2) Initialize Floorplan
   - initialize_floorplan()
3) Set Block Pin Constraints for I/O Ports
   - set_block_pin_constraints()
4) Fix Physical Status of I/O Pins
   - fix_physical_status_io_pins()
5) Place and Fix Physical Status of Macros
   - fix_physical_status_macros()
6) Create Keepout margin for macros
   - create_keepout_margin()
7) Set and Compile Boundary Cell
   - set_and_compile_boundary_cell()
8) Create Tap Cells
   - create_tap_cells()

Powerplan Methodology:

1) Create the PG Net
   • create_nets()
2) Making Logical Connection
   • connect_pg_nets()
3) Setting Attributes for TIE Cells
   • set_attribute()
4) Creating PG Rails
   • create_pg_pattern()
   • set_pg_strategy()
   • compile_pg()
5) Create Macro Pin Connection
   • create_pg_macro_conn_pattern()
   • create_pg_strategy()
   • compile_pg()
6) Create Standard Cell Pin Connection
   • create_pg_std_cell_conn_pattern()
   • create_pg_strategy()
   • compile_pg()
7) Creation of Vias between Rails and PG Straps
   • create_pg_vias()

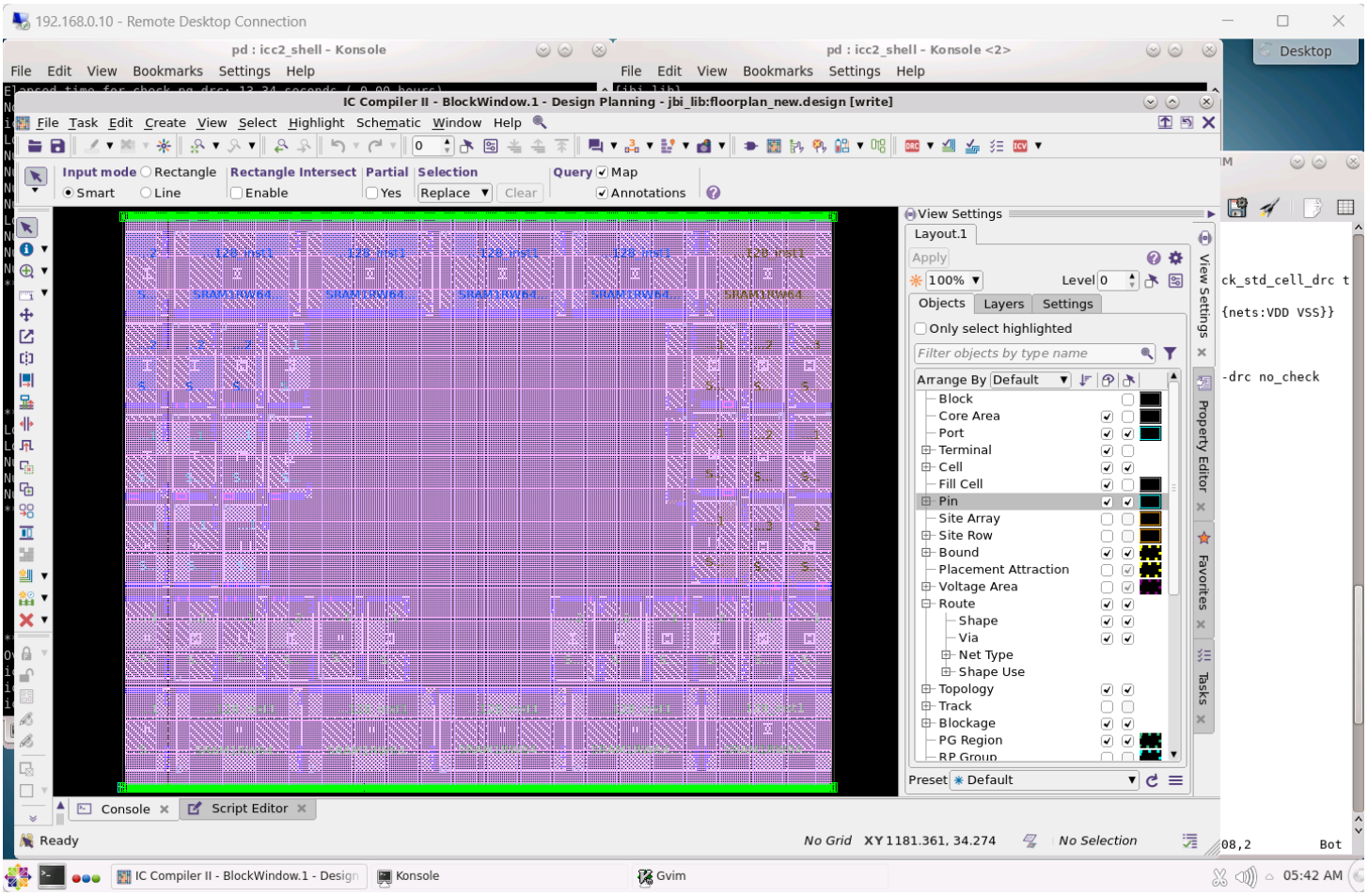
These two above methodologies demonstrate vital steps of both Floorplan and Powerplan methodology. Industry follows them separately, Powerplan after Floorplan. Which are generally prone to show DRCs and Shorts (LVS).

Like below example: OpenSPARC T1 (28nm)



In the above design we can see thousands of errors after doing Floorplan and applying Powerplan to the design using typical methodology.

Below one is My new methodology applied design:



We can see zero errors due to the precise use of new Tailored methodology for Floorplan and Powerplan integrated.

This is proposed methodology:

1) Sanity Check
   - check_netlist()
   - check_timing()
   - report_design_mismatch()
2) Initialize Floorplan
   - initialize_floorplan()
3) Set Block Pin Constraints for I/O Ports
   - set_block_pin_constraints()
4) Fix Physical Status of I/O Pins
   - fix_physical_status_io_pins()
5) 5) Place Macros
   - place_macros()
6) Create the PG Net
   - create_net()
7) Making Logical Connection
   - connect_pg_net()
8) Setting Attributes for TIE Cells
   - set_attribute()
9) Creating PG Grids
   - create_pg_pattern()
   - set_pg_strategy()
   - compile_pg()
10) Set and Compile Boundary Cell
   - set_and_compile_boundary_cell()
11) Create Tap Cells
   - create_tap_cells()
12) Create Standard Cell Rails
   - create_pg_std_cell_conn_pattern()
   - create_pg_strategy()
   - compile_pg()
13) Creation of Vias between Rails and PG Straps
   - create_pg_vias()
14) Create Macro Pin Connection
   - create_pg_macro_conn_pattern()
   - create_pg_strategy()
   - compile_pg()
15) Create Keepout margin for macros
   - create_keepout_margin()
16) Fix Physical Status of Macros
   - fix_physical_status_macros()

Node	Shape	Core Area Utilization	Offset
14nm	Rect	58%	4
28nm	Rect	72%	4

TABLE I
INITIALIZE FLOORPLAN

This core area utilization table is not for comparison basis but only to support the experiment related results and parameters used from both 14nmand 28nm nodes.

Node	Power	Performance	Area
14nm	5.25 pW	250 MHz	168642
28nm	7.01 pW	250 MHz	985543

TABLE II
PPA METRICS OF FINAL GDSII

Same, this PPA table shows used Frequency for both designs and Power and Area results after successful GDSII tape out.

LVS, DRC, Setup time and Hold time clearance reports were attached in Experiment Results PDF file.

Conclusion:

In conclusion, this research advocates an integrated methodology-based scripting approach for designing clean Floorplan and Powerplan efficiently. By excluding traditional PPA or Area Utilization comparisons, the emphasis is placed on the methodology's effectiveness, demonstrated through practical validation on distinct technology nodes. The proposed analytical methodologies further contribute to advancing VLSI Physical Design practices.

This is a methodology-based Scripting comparison and research, to design and implement Clean Floorplan and Powerplan quickly by following few direct steps and considering some proposed Analytical methodology in between the steps (Explained in detail in IEEE format Conference Paper).