Design of Four Quadrant Analog Multiplier with High Robustness against PVT Variations using Genetic Algorithm

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Abstract: *In this paper, a new current mode four-quadrant analog multiplier circuit is proposed. The circuit structure is based on dual trans-linear loops. The new structure used in the circuit shows more promising features for the purposes of lower power consumption, wider bandwidth (BW), and lower Total Harmonic Distortion (THD). The structure of the circuit is such that it is almost independent of process, temperature, and supply-voltage, PVT, variations. In addition, the circuit was optimized using Multi-Objective Genetic Algorithm (MOGA) and the results demonstrate the power of this tool in the optimization of electronic circuits. The designed circuit with 1.8 V supply voltage and 53 μW power consumption, results in 1.503 GHz BW, 0.53% THD (in 1 MHz frequency) and also 0.84% maximum nonlinearity error.*

Keywords: *Current Mode Analog Multiplier, Translinear Loops, Evolutionary Algorithms, Multi-Objective Optimization.*

1. Introduction

The real-time analog multiplication of two signals is one of the most important operations in analog signal processing [1]. Analog multiplier is used not only in computational building blocks, but also useful in modulators, mixers, filters, and neural networks [1] [2] [3]. Current mode circuits have some benefits like wider bandwidth (BW), lower power consumption, higher linearity, wider dynamic range, and simpler circuitry [4].

Up to now, few studies have been done in current mode analog multipliers; however, each of them faced with specific limitations. Proposed circuit in [5] though has differential output, but holds high power consumption and very small BW. Circuit complexity is also remarkable. Proposed circuit in [6] has used geometric mean blocks and squarer/divider blocks to the design of multiplier. Despite having low voltage supply and power consumption and also relatively low THD, the circuit has not a satisfactory BW. Differential squarer has been used in [7]. Though this circuit has a good BW, but holds high nonlinearity error and has used two supply voltages. Reference [8], like [7], has used two supply voltages and has a high nonlinearity error; in addition [8] has high power consumption and used BJT transistor in its structure. Including four squarer blocks

and ACM model of MOS transistor, [9] keeps high supply voltage and low BW. The designed multiplier in this paper includes two squarer blocks and in addition to its simple structure, preserves high BW and very low sensitivity to PVT variations.

Due to the complexity of circuit relations, optimal design faces with great challenges. Without considering circuit complexity and its scopes, Evolutionary Algorithms (EAs) seeks to exploring solution space in the way of evolutionary and finding its optimized points, thus in the last two decades it had significant role in optimization of electronic circuits [10].

CMOS technology presents a highly reliable, well-established, cost-effective platform for integration, so the applied technology in this work is TSMC CMOS 0.18μm. This paper organized as follows. In Section 2, circuit structure of multiplier will be investigated. Some analysis is performed in Section 3 to predict circuit performance theoretically. Circuit optimization using MOGA is accompanied in Section 4. Simulation results of the circuit and comparison with previously reported papers will be investigated in Section 5 and finally Section 6 will be devoted to the conclusions.

2. Current Mode Multiplier

Fig. 1 shows the squarer circuit proposed in [11]. Excessive use of PMOS transistors causes the low speed of this circuit. Fig. 2 shows the new squarer proposed to overcome the difficulties imposed by the squarer of [11]. Based on MOS trans-linear law in saturation region, for M1 to M4 transistors we have ($K_{NMOS} = K_{PMOS}$, $V_{TH,N} = V_{TH,P}$):

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4} \tag{1}$$

Where I_1-I_4 are drain currents of M1-M4. The drain current of transistors M1 and M2 are the same and equal to constant current, I_B. then:

$$2\sqrt{I_B} = \sqrt{I_3} + \sqrt{I_4} \qquad (2)$$
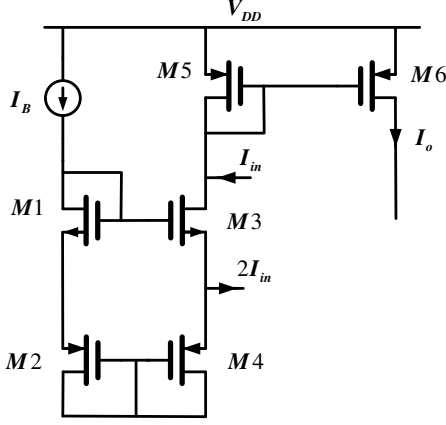
On the other hand, for transistors M3 and M4 we have:

Fig. 1: Proposed squarer in [11].

$$I_3 = I_o + I_{in} \quad , \quad I_4 = I_o - I_{in} \qquad (3)$$

Where I_o and I_{in} are the output and input currents of the squarer. Substituting Eq. (3) in Eq. (2) and performing some mathematical operations we have:

$$I_o = \frac{I_{in}^2}{4I_B} + I_B \qquad (4)$$

Using the new two quadrant squarer and applying signals I_x+I_y and I_x-I_y to the specified nodes of the circuit shown in Fig. 3 and based on Eq. (4), the multiplication of I_x and I_y will be resulted in the output branch:

$$I_{out} = \left(\frac{(I_x + I_y)^2}{4I_B} + I_B \right) - \left(\frac{(I_x - I_y)^2}{4I_B} + I_B \right) = \frac{I_x I_y}{I_B} \qquad (5)$$
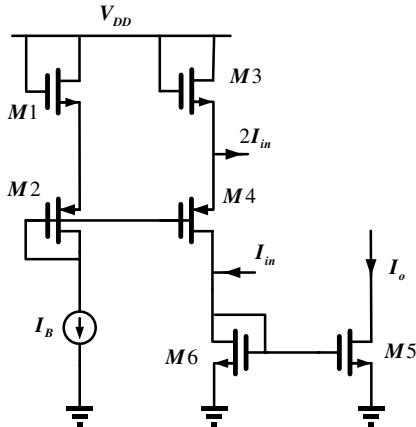

Fig. 2: New two quadrant squarer.

To improve the performance of the circuit for power, area, linearity, and frequency response, the followings are suggested:

Using I_B and two diode connected transistors (M1 and M2) for both squarers. By applying this change in the circuit, the power and area consumption will be reduced.

Eliminating I_x's at the drain of transitors M4 and M8. This is because these two signals will be cancelled at the output branch. This modification reduces the voltage swing at the input node of the current mirror and as a result, improves the linearity and frequency response of the circuit.

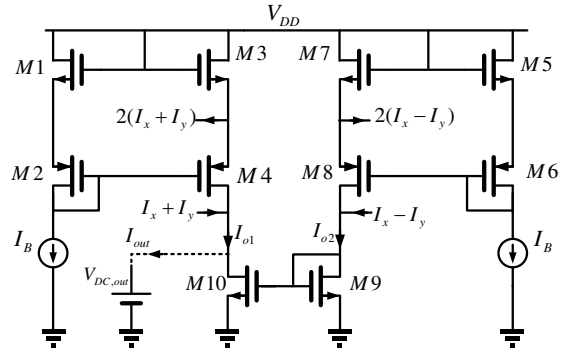Fig. 4 shows the final modified version of the proposed circuit of Fig. 3.

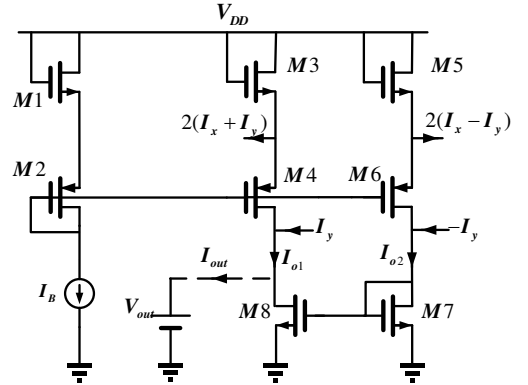Fig. 3 Schematic of the new four quadrant multiplier circuit.

Fig. 4: The final modified version of the proposed circuit of Fig.3.

Supposing the supply voltage V_{DD} of 1.8 V and the bias current I_B of 10 µA and starting from output node, transistors dimensions will be obtained as Table I. The output current enters to a supply voltage of 0.6 V. In practice, each load which satisfies the above condition ($V_{DC,out}=V_{DD}/3$) may be placed at the output node. Fig. 5 shows a current load that is true in the above qualifications. We have used simple current mirrors for implementing current sources (I_B) and input current signals (I_x, I_y). The simulation results of the manually designed circuit will be investigated in Section 4.

Table I: Transistors' dimensions obtained by manual designing
(All values are in µm)

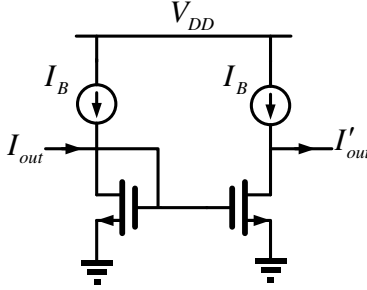| $(W/L)_{6,7}$	$(W/L)_{2,4,6}$	$(W/L)_{1,3,5}$
5.4/0.9	4/0.81	0.72/0.81

Fig. 5: Simple current load used at the output of the proposed circuit.

2. Performance Analysis

2.1. Operating Range

From saturation condition, we can conclude that:

$$| I_x + I_y | \leq 2I_B \ , | I_x - I_y | \leq 2I_B \qquad (6)$$

Equation (6) results in:

$$| I_x | = | I_y | \leq I_B \qquad (7)$$

The last expression shows the operating range of the input signals. This means that the circuit is a four quadrant analog multiplier.

2.1. V_{TH} Mismatch Effect

The threshold voltage of a MOS transistor is affected by the body-source voltage V_{SB} by Eq. (8):

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\phi_b + V_{SB}} - \sqrt{2\phi_b} \right) \qquad (8)$$

Fig. 6 shows the DC transfer characteristics in the presence of the body effect. From this figure, the maximum nonlinearity error is 3.5%. Our further simulations show that the output error can be reduced if we don't have body effect.

In recent technologies like twin-well and triple-well, the effect of source-body voltage on V_{TH} can be easily canceled by connecting the source contact to body contact. However, if threshold voltages are not equal, according to Fig. 2, we can rewrite trans-linear principle as follows:

$$\sqrt{\frac{I_1}{K}} + V_{TH1} + \sqrt{\frac{I_2}{K}} + |V_{TH2}| = \sqrt{\frac{I_3}{K}} + V_{TH3} + \sqrt{\frac{I_4}{K}} + |V_{TH4}| \ (9)$$
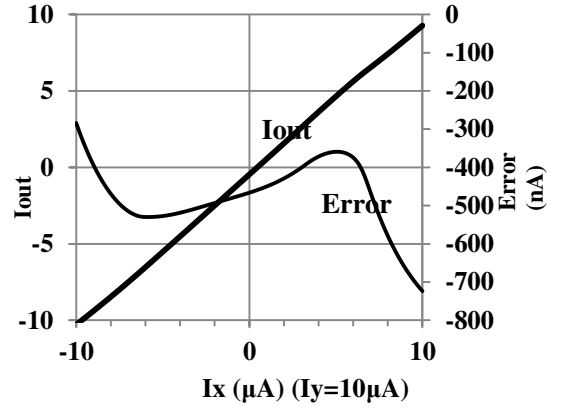
Results in:

Fig. 6: output error when bodies of transistors are tied to the highest (PMOSs) and lowest (NMOSs) voltages in the circuit.

$$\sqrt{\frac{I_{o1} + I_{in}}{K}} + \sqrt{\frac{I_{o1} - I_{in}}{K}} = \sqrt{\frac{I_B}{K}} + \sqrt{\frac{I_B}{K}} + $$
$$V_{TH3} + |V_{TH4}| - (V_{TH1} + |V_{TH2}|) \qquad (10)$$

Assume $V_{TH3} + |V_{TH4}| - (V_{TH1} + |V_{TH2}|) = \Delta V$, then we have:

$$\sqrt{I_{o1} + I_{in}} + \sqrt{I_{o1} - I_{in}} = 2\sqrt{I_B} + \sqrt{K}\Delta V \qquad (11)$$

Performing some mathematical operations and neglecting expressions including ΔV^2, we have:

$$I_o = \frac{I_{in}^2}{4I_B \left(1 + \sqrt{\frac{K}{I_B}}\Delta V \right)} + $$
$$\frac{I_B}{1 + \sqrt{\frac{K}{I_B}}\Delta V} + \frac{2\sqrt{KI_B}\Delta V}{1 + \sqrt{\frac{K}{I_B}}\Delta V} \qquad (12)$$

Considering the mentioned second order deviation in the multiplier circuit of Fig. 4 results in:

$$I_o = \frac{I_x I_y}{I_B \left(1 + \sqrt{\frac{K}{I_B}}\Delta V \right)} \approx \frac{I_x I_y}{I_B} \left(1 - \sqrt{\frac{K}{I_B}}\Delta V \right) \qquad (13)$$

Equation (13) shows that the error due to V_{TH} mismatch will decrease with increasing I_B and decreasing K.

2.2. K Mismatch Effect

Suppose that $K_{NMOS} \neq K_{PMOS}$, we have the following mismatch expression for the proposed multiplier circuit:

$$K_{PMOS} = K(1 + \delta/2), \quad K_{NMOS} = K(1 - \delta/2), \quad \delta \ll 1 \quad (14)$$

Rewriting trans-linear law for the squarer circuit shown in Fig. 2, and supposing the last mismatch effect in Eq. 14, we have:

$$\sqrt{\frac{I_B}{K(1 - \delta/2)}} + \sqrt{\frac{I_B}{K(1 + \delta/2)}} = $$
$$\sqrt{\frac{I_o + I_{in}}{K(1 - \delta/2)}} + \sqrt{\frac{I_o - I_{in}}{K(1 + \delta/2)}} \quad (15)$$

By performing some mathematical operations and neglecting expressions including δ^2, it can be deduced:

$$I_o = \frac{I_{in}^2}{4I_B} + I_B + \frac{\delta I_{in}^3}{16 I_B^2} + \frac{\delta I_{in}}{4} \quad (16)$$

The final expression can be derived by applying Eq. (16) to the multiplier circuit of Fig. 4:

$$I_o = \frac{I_x I_y}{I_B} - \frac{\delta}{2} I_y + \frac{\delta}{16 I_B^2}\left(6 I_x^2 I_y + I_y^3\right) \quad (17)$$

There are three types of input signals: 1) I_x be a sinusoidal with the angular frequency ω_1 and I_y a DC signal, 2) vice versa, and 3) both of them be sinusoidal signals with angular frequencies of ω_1 and ω_2, respectively. Table II shows the harmonics appeared in the output signal for the mentioned types of the input signals.

2.3. Channel Length Modulation Effect

In the proceeding, we have derived an expression which addresses the channel length issue in the output current of the presented four quadrant analog multiplier. For this purpose, we rewrite the trans-linear loop (TL) equations in the presence of channel length modulation effect. For the loop including transistors M1, M2, M3, and M4, the TL are as follows:

$$\sqrt{\frac{I_1}{1 + \lambda_1(V_{DG,1} - V_{TH})}} + \sqrt{\frac{I_2}{1 + \lambda_2(V_{GD,2} - |V_{TH}|)}} = $$
$$\sqrt{\frac{I_3}{1 + \lambda_3(V_{DG,3} - V_{TH})}} + \sqrt{\frac{I_4}{1 + \lambda_4(V_{GD,4} - |V_{TH}|)}} \quad (18)$$

where $\lambda_1 = \lambda_2 = \lambda_3 = \lambda_4 = \lambda$ and $V_{TH,1} = |V_{TH,2}| = V_{TH,3} = |V_{TH,4}| = V_{TH}$. According to Fig. 4, we have:

$$I_1 = I_2 = I_B \quad , \quad I_4 = I_{o1} - I_y \quad ,$$
$$I_3 = I_{o1} + 2I_x + I_y \quad (19)$$

Substituting Eq. (19) in Eq. (18) and considering $V_{DG,1} = V_{GD,2} = V_{DG,3} = 0$ results in:

Table II: Output signals for different input signals in presence of K mismatch

inputs	Output signal	harmonics
$I_y = I_B \cos(\omega_2 t)$ and $I_x = I_B$	$I_B \cos(\omega_2 t) - \frac{5}{64}\delta I_B \cos(\omega_2 t) + \frac{1}{64}\delta I_B \cos(3\omega_2 t)$	HD3= $0.0156\,\delta$
$I_x = I_B \cos(\omega_1 t)$ and $I_y = I_B$	$I_B \cos(\omega_1 t) - \frac{1}{4}\delta I_B + \frac{3}{16}\delta I_B \cos(2\omega_1 t)$	HD2= $0.1875\,\delta$
$I_x = I_B \cos(\omega_1 t)$ and $I_y = I_B \cos(\omega_2 t)$	$\frac{I_B}{2}\cos((\omega_1 + \omega_2)t) + \frac{I_B}{2}\cos((\omega_1 - \omega_2)t) - \frac{17}{64}\delta I_B \cos(\omega_2 t) + \frac{6}{64}\delta I_B \cos((2\omega_1 + \omega_2)t) + \frac{6}{64}\delta I_B \cos((2\omega_1 - \omega_2)t) + \frac{1}{64}\delta I_B \cos(3\omega_2 t)$	IM3= 0.09375δ

$$2\sqrt{\frac{I_B}{1 - \lambda V_{TH}}} = \sqrt{\frac{I_{o1} + 2I_x + I_y}{1 - \lambda V_{TH}}} + \sqrt{\frac{I_{o1} - I_y}{1 + \lambda(V_{GD,4} - V_{TH})}} \quad (20)$$

For simplification, we multiply both sides of Eq. (20) by $\sqrt{1 - \lambda V_{TH}}$:

$$2\sqrt{I_B} = \sqrt{I_{o1} + 2I_x + I_y} + \sqrt{\frac{1 - \lambda V_{TH}}{1 + \lambda(V_{GD,4} - |V_{TH}|)}}\sqrt{I_{o1} - I_y} \quad (21)$$

According to:

$$\frac{1 - \lambda V_{TH}}{1 + \lambda(V_{GD,4} - |V_{TH}|)} \approx $$
$$(1 - \lambda V_{TH})(1 - \lambda(V_{GD,4} - |V_{TH}|)) = \quad (22)$$
$$1 - \lambda V_{GD,4} - \lambda V_{TH}^2 + \lambda^2 V_{GD,4} V_{TH} \approx 1 - \lambda V_{GD,4}$$

if $\sigma_1 = \lambda V_{GD,4}$, then we can rewrite Eq. (22) as:

$$2\sqrt{I_B} = \sqrt{I_{o1} + 2I_x + I_y} + \sqrt{1 - \sigma_1}\sqrt{I_{o1} - I_y} \quad (23)$$

By expanding Eq.(23), eliminating expressions including σ_1^2, and using approximation ($x \ll 1$ then $\frac{1}{1-x} \approx 1 + x$), the following equation will be obtained:

$$I_{o1} = I_B + \frac{(I_x + I_y)^2}{4I_B} - I_x + \frac{\sigma_1}{2}I_B - \frac{\sigma_1}{4}(I_x + I_y)$$
$$- \frac{\sigma_1 I_x I_y}{4I_B} - \frac{\sigma_1}{8I_B}(I_x^2 + I_y^2) + \frac{\sigma_1}{16I_B^2}(I_x + I_y)^3 \qquad (24)$$

To investigate the second TL including M1, M2, M5, and M6, we apply the above operations, which yield to:

$$I_{o2} = I_B + \frac{(I_x - I_y)^2}{4I_B} - I_x + \frac{\sigma_2}{2}I_B - \frac{\sigma_2}{4}(I_x - I_y)$$
$$+ \frac{\sigma_2 I_x I_y}{4I_B} - \frac{\sigma_2}{8I_B}(I_x^2 + I_y^2) + \frac{\sigma_2}{16I_B^2}(I_x - I_y)^3 \qquad (25)$$

where $\sigma_2 = \lambda V_{GD,6}$.

Without considering the channel length effect of the current mirror transistors (note that current mirrors are not part of the circuit), the output current of the multiplier considering the channel length modulation of the transistor loops, can be written as:

$$I_o = I_{o1} - I_{o2} = \frac{I_x I_y}{I_B} + \frac{I_B}{2}(\sigma_1 - \sigma_2) + \frac{I_x}{4}(\sigma_2 - \sigma_1)$$
$$- \frac{I_y}{4}(\sigma_1 + \sigma_2) - \frac{I_x I_y}{4I_B}(\sigma_1 + \sigma_2) +$$
$$\frac{(I_x^2 + I_y^2)}{8I_B}(\sigma_2 - \sigma_1) + \frac{I_x^3}{16I_B^2}(\sigma_2 - \sigma_1) + \qquad (26)$$
$$\frac{3I_x^2 I_y}{16I_B^2}(\sigma_1 + \sigma_2) + \frac{3I_x I_y^2}{16I_B^2}(\sigma_1 - \sigma_2) + \frac{I_y^3}{16I_B^2}(\sigma_1 + \sigma_2)$$

If we suppose $\sigma_1 = \sigma_2 = \sigma$ then the above equation can be rewritten as:

$$I_o = \frac{I_x I_y}{I_B} - \frac{I_y}{2}\sigma - \frac{I_x I_y}{2I_B}\sigma + \frac{3I_x^2 I_y}{8I_B^2}\sigma + \frac{I_y^3}{8I_B^2}\sigma \qquad (27)$$

Equation (27) illustrates short channel modulation effect in the term of $V_{DS,4,6}$ and input signals (I_x and I_y).

2.4. Input Currents Mismatch Effect

In this section we have derived an expression to model the effect of mismatch between input currents. Suppose we have an error to produce $2(I_x + I_y)$ and $2(I_x - I_y)$ from input currents I_x and I_y. Each input current in relation to possible mismatches can be defined as follows:

$$2(I_x + I_y)' = 2(I_x + I_y) + \delta i_1 \quad ,$$
$$2(I_x - I_y)' = 2(I_x - I_y) + \delta i_2 \qquad (28)$$

Where $2(I_x + I_y)'$ and $2(I_x - I_y)'$ are the input currents to the source of M3-M4 and M5-M6 respectively. δi_1 and δi_2 are deviations of applied currents from their real amount. Applying equation (28) to the fig. 4, performing mathematical operations, using approximation ($x \ll 1$ then $\frac{1}{1-x} \approx 1 + x$) and neglecting δi_1^2 and δi_2^2 we have:

$$I_{o1} = \frac{(I_x + I_y)^2}{4I_B} + I_B - I_x + \frac{\delta i_1(I_x - I_y)}{4I_B} - \delta i_1 \qquad (29)$$

$$I_{o2} = \frac{(I_x - I_y)^2}{4I_B} + I_B - I_x + \frac{\delta i_2(I_x + I_y)}{4I_B} - \delta i_2 \qquad (30)$$

And finally for the output current we have:

$$I_o = \frac{I_x I_y}{I_B} + \frac{\delta i_1(I_x - I_y) - \delta i_2(I_x + I_y)}{4I_B} + \delta i_2 - \delta i_1 \qquad (31)$$

3. Circuit Optimization

Multi-objective EAs were known as powerful methods to optimize electronic circuits in the last two decades [12]. These algorithms emulate nature's evolution procedure, which includes several operands as follows: obtaining an initial set, fitness assignment to each set member, selection of the proper members based on their fitness, crossover of the selected members, mutation of each newly produced member, and finally reproduction of a new set for the process of the next generation. Multi-objective optimization or minimizing of vector function $F(x)$ defines as follows [12]:

Minimize: $F(x) = [f_1(x), f_2(x), ..., f_m(x)]$
with $x = [W_1, L_1, ..., W_i, L_i]$ (32)

Subject to constraints: $\begin{cases} g_j(x) \le 0 \;\; ; \; j = 1,2,...,J \\ h_k(x) = 0 \; ; \; k = 1,2,...,K \end{cases}$

in which W_i and L_i are the length and width of the ith transistor and f_m is mth target (i.e. THD, BW, error or power consumption). In order to prevent numerical problems, in Eq. (32), the normalized form of f_m is used as follows:

$$f_m = w_m \frac{T_m - O_m}{T_m - B_m} \qquad (33)$$

Which w_m is the fitness function weight, O_m is the amount of each output function, T_m is the target value, and B_m is the quantity of the mth target at the worst case. Each individual x, is a vector of variants and variants are the length and width of the transistors in our case. First, some initial members, x's, are produced within the boundary region imposed by constraint functions (circuit limitations here), and their fitness are assigned by fitness assignment operator. Those individuals that are more competent are selected as parents and new individuals will be produced from these parents. Crossover and mutation operators are applied to these parents and

produce new individuals. Crossover operator will combine one individual by another. Mutation operator tries to make some changes by altering one or several bits of those that are produced by crossover operator [12]. To transfer members of present population to the next one, the variants of each individual will be replaced by their same kind of variants from other one; this event called reproduction. These later three functions are used to expand the research space of the solutions. Fitness assignment operator determines the goodness of the new produced members (individuals). Those that are more competent will be selected as the next set. Since the selection performs before exploring the solution space, therefore this algorithm will be classified as *a priori* algorithm. While performing the evolutionary process, few subpopulations will be made from individuals. After several periods, best individuals of the subpopulations will be replaced the worst ones in another subpopulations. This process will continue until no changes seen in the set of solutions. By this way, we will say that algorithm is in steady state.

According to the fitness of the members, the best ones will be selected in Pareto front. The closer is individual to the origin, i.e. the goal; the greater is fitness value. Fig. 7 indicates the meaning of Pareto front in the case of our circuit. This figure demonstrates the trade-off between two outputs, which are in conflict, i.e. THD increases by error reduction. Our interest is those points which have been made bigger.

Fig. 8 shows the block diagram of the circuit optimization main loop. The characteristics of MOGA are as follows: Initial population: 103 members; selection type: competitive; amount of reproduction: 0.8; mutation: 0.2; crossover type: scattered; migration type: forwarding and equals to 0.2; and stopping criteria: function tolerance lower than 10^{-4}. Table III shows the dimensions of transistors after optimization. Multiplier performance improvements are shown in Table IV, which are from 1.3% (power) to 252% (BW).
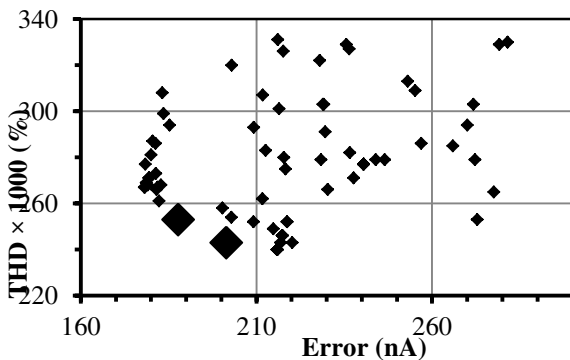

Fig. 7: Pareto front of THD versus output current error.

Table III: Transistors' dimensions obtained from optimization (All values are in µm)

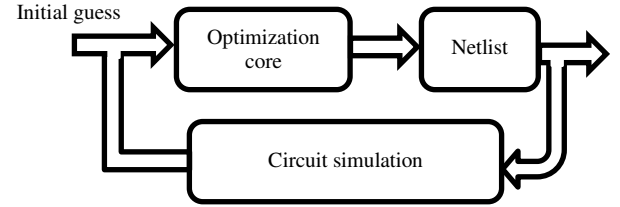| $(W/L)_{6,7}$	$(W/L)_{2,4,6}$	$(W/L)_{1,3,5}$
0.63/1.26	1.17/0.36	1.26/0.45

Fig. 8: Main loop of circuit optimization.

Table IV: Comparison between optimization and manual designing results

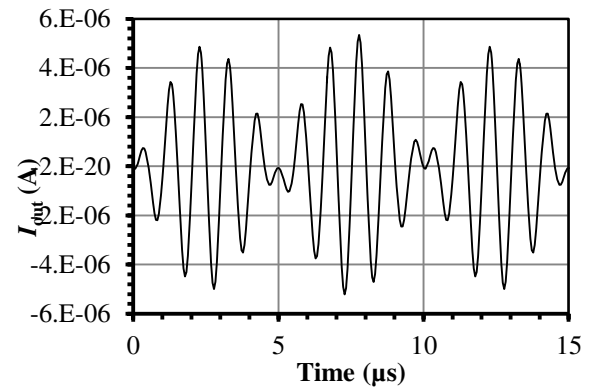| Characteristic	Before Opt.(manual)	After Opt.	Improvement (%)
Power consumption (µW)	53.64	52.93	1.3
Voltage Supply (V)	1.8	1.8	--
THD (%)	0.73	0.53	27.4
Bandwidth (MHz)	427	1503	252
Non-linearity error (%)	1.43	0.84	41.2

[*]@1MHz, 10µA amplitude

Fig. 9: Output current of the circuit with I_x= 10 sin($2\pi \times$1e6 t) (µA) and I_y= 5 sin($2\pi \times$1e5 t) (µA).

4. Simulation Results

In this section we have investigated results in time and frequency domain and Monte Carlo analysis will be performed in terms of PVTs. Layout and comparison table will finalize this section.
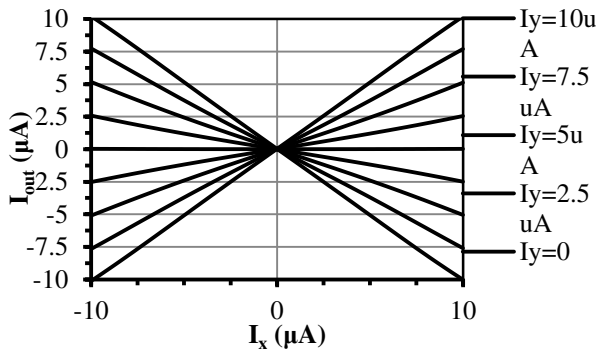
Fig. 10: DC transfer function.

4.1. Time Domain Results

Fig. 9 illustrates typical circuit output current in time domain. Input I_x is a sinusoidal signal with 1 MHz frequency and the amplitude of 10 µA. I_y is a sinusoidal signal with 100 KHz frequency and amplitude of 5µA.

Fig. 10 illustrates the DC transfer characteristic of the output current according to the input currents. Crossing from center and monotone gradient curves justify high linearity of the circuit in the whole operating range.

To calculate nonlinearity error, a low frequency triangle wave with the amplitude of 10 μA is given to the input I_x and the circuit output difference from ideal state, where $I_{y,DC}$=10 μA, is obtained. Maximum nonlinearity error is equals to 0.84%.

Fig. 11 shows total harmonic distortion in the four input frequency of 1, 5, 10, and 20 MHz versus input signal I_x. In this case, results are more favorable than [13].
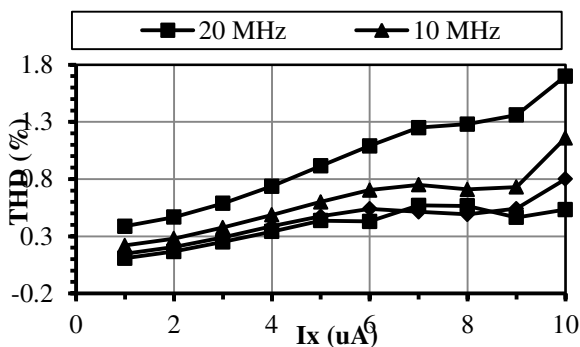
Fig. 11: Total harmonic distortion versus input current ($I_{y,DC}$=10 µA).

4.2. Frequency Domain Results

Fig. 12 shows the frequency response of the circuit, in which input I_x is a small signal and input I_y is a DC signal. BW is 1503 MHz, which is higher than other reported papers. Fig. 13 shows the small signal gain of the output to the power supply variations when the input

signals were equal to zero. Very low sensitivity to power supply variations obviously can be deduced from this figure.

To verify the frequency response of the circuit, we derive a hand calculated expression to estimate the BW. Fig. 14 shows the small-signal model of the four quadrant multiplier in Fig. 4. To determine this model we have made the following considerations:

1. All nodes of the circuit are low-impedance. Thus the drain-source resistance is not considered in the small-signal model.

2. Capacitances smaller than the gate-source capacitances are not embedded in this model.

3. M1 and M2 transistors have a constant current of I_B and all of their nodes have constant voltages plus a low percentage of small-signal. Since these two transistors are used for biasing other transistors, thus the equivalent model of these two transistors is not embedded and the gate of transistor M2 is grounded.

As illustrated in Fig. 14, one of the inputs is applied to the node N3 and the other to the node N5. The circuit has a unique response for each of these two inputs. So, based on the superposition theorem, we calculate the overall AC response of the circuit for $I_{in1}=I_{in2}=i_x$ as follows:

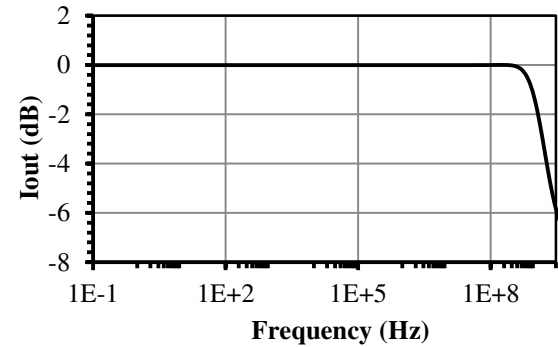$$i_{out} = A_1 i_{in1} + A_2 i_{in2}; \quad \text{Hint: } i_{in1} = i_{in2} = i_x \quad (34)$$

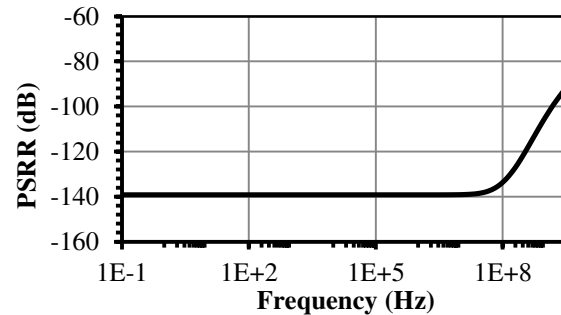Fig. 12: AC response of the multiplier.
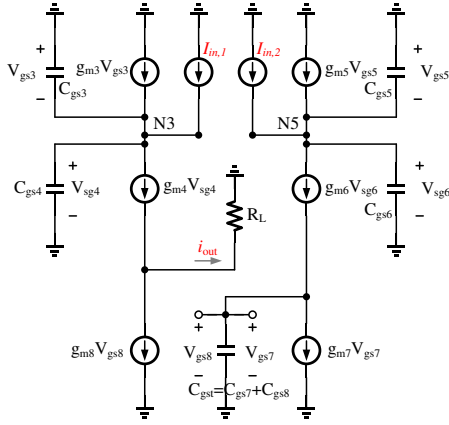

Fig. 13: PSRR versus frequency.

Fig. 14: The small-signal model of the circuit of Fig. 4.

In which,

$$A_1 = \frac{N_1(s)}{D(s)}; \quad A_2 = \frac{N_2(s)}{D(s)} \tag{35}$$

$$N_1(s) = (\ gm7 \ gm5 \ gm4 + gm7 \ gm6 \ gm4) + \\ (\ gm7 \ gm4 \ Cgs5 + gm7 \ gm4 \ Cgs6 + \\ gm5 \ gm4 \ Cgst + gm6 \ gm4 \ Cgst) \ s + \\ (\ gm4 \ Cgst \ Cgs5 + gm4 \ Cgst \ Cgs6) \ s^2 \tag{36}$$

$$N_2(s) = (\ -gm8 \ gm6 \ gm3 - gm8 \ gm6 \ gm4) + \\ (\ -gm8 \ gm6 \ Cgs3 - gm8 \ gm6 \ Cgs4) \ s \tag{37}$$

$$D(s) = (\ gm7 \ gm5 \ gm3 + gm7 \ gm6 \ gm3 + \\ gm7 \ gm5 \ gm4 + gm7 \ gm6 \ gm4) + \\ (\ gm7 \ gm5 \ Cgs3 + gm7 \ gm6 \ Cgs3 + \\ gm7 \ gm5 \ Cgs4 + gm7 \ gm6 \ Cgs4 + \\ gm7 \ gm3 \ Cgs5 + gm7 \ gm4 \ Cgs5 + \\ gm7 \ gm3 \ Cgs6 + gm7 \ gm4 \ Cgs6 + \\ gm5 \ gm3 \ Cgst + gm6 \ gm3 \ Cgst + \\ gm5 \ gm4 \ Cgst + gm6 \ gm4 \ Cgst) \ s + \\ (\ gm7 \ Cgs5 \ Cgs3 + gm7 \ Cgs6 \ Cgs3 + \\ gm5 \ Cgst \ Cgs3 + gm6 \ Cgst \ Cgs3 + \\ gm7 \ Cgs5 \ Cgs4 + gm7 \ Cgs6 \ Cgs4 + \\ gm5 \ Cgst \ Cgs4 + gm6 \ Cgst \ Cgs4 + \\ gm3 \ Cgst \ Cgs5 + gm4 \ Cgst \ Cgs5 + \\ gm3 \ Cgst \ Cgs6 + gm4 \ Cgst \ Cgs6) \ s^2 + \\ (\ Cgst \ Cgs5 \ Cgs3 + Cgst \ Cgs6 \ Cgs3 + \\ Cgst \ Cgs5 \ Cgs4 + Cgst \ Cgs6 \ Cgs4) \ s^3 \tag{38}$$

The applied values of the circuit's parameters are (these values are extracted from the circuit netlist which is derived by HSPICE simulator, also $I_y=10u$):
Cgs3=4.5 (fF); Cgs4=2.5 (fF); Cgs5=4.1 (fF); Cgs6=2.6 (fF); Cgst=6.6 (fF); gm3=73 (µS); gm4=23 (µS);

gm5=23.7 (µS); gm6=70 (µS); gm7=126 (µS); gm8=126 (µS); RL=1 KΩ.

Fig. 15 shows the frequency response of Eq. 34 in the range of 0 Hz to 3 GHz. As illustrated in this figure, the BW of the circuit is about 1.75 GHz.
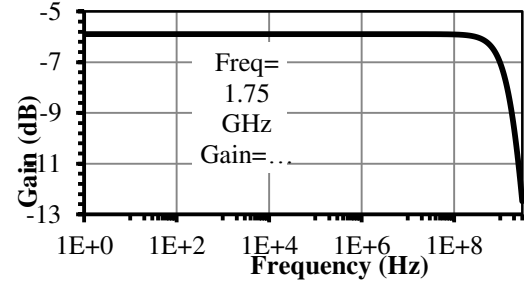

Fig. 15: Hand-calculated frequency response of the presented multiplier.

4.3. Monte Carlo

Monte Carlo simulation is a statistical analysis that shows effects of process variation on circuit performance. In this work, we have changed width (W), length (L), threshold voltage (V_{TH}), and oxide thickness (t_{ox}) of the transistors according to Gaussian distribution with 3% random variations and a standard deviation of 3. Simulations repeated 50 times. As is shown in Fig. 16, Monte Carlo simulation results demonstrate very low variations on the DC response of the proposed current mode multiplier.
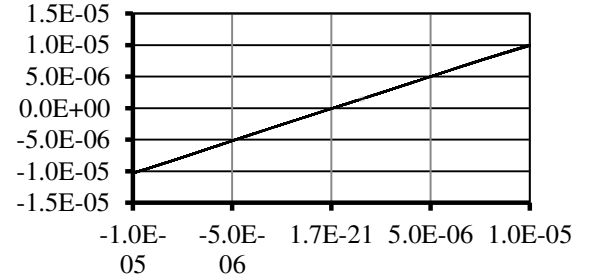

Fig. 16: Monte Carlo simulation of DC characteristic.

4.4. Sensitivity to Temperature

Sensitivity to temperature is another analysis that has been performed for the circuit. Very low sensitivity to temperature is a feature of the circuit that is proven by Fig. 17. Accordingly, the variation of the output signal is very low through 100°C temperature variations. Our simulations show that optimization has improved circuit sensitivity to PVT.
The layout of the proposed circuit is shown in Fig. 18. The size of the circuit is 14.8µm×13.2µm or 193.4 µm².

Table V shows a comparison between this work and the other reported current mode analog multipliers. For a

better comparison, we introduce two figures of merit, *FOM*, as follows:

$$FOM\,1 = \frac{BW\,[MHz]\,.NumQuad\,.}{P_{diss}\,[\mu W\,]\,THD[\%]} \tag{39}$$

$$FOM\,2 = \frac{NumQuad\,.}{P_{diss}\,[\mu W\,]\,.NE[\%]} \tag{40}$$

Fig. 18: The layout of the proposed circuit
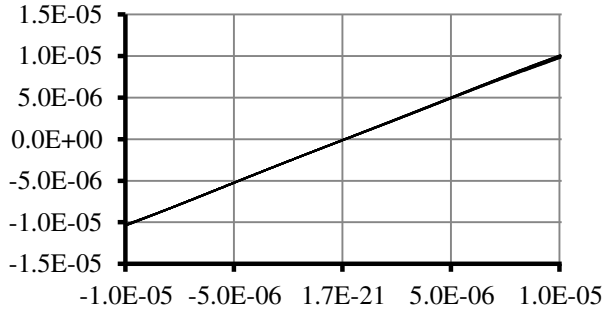
Fig. 17: DC response for temperature variations from -25°C to +75°C.
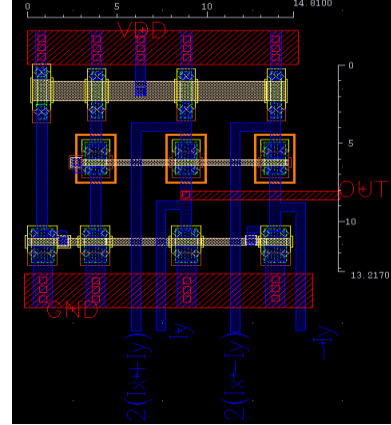
Table V: Comparison between this work and other reported papers

Reference	*This work*	[5]	[6]	[7]	[11]	[8]	[9]	[14]	[15]	[13]
Year		2011	2010	2009	2009	2009	2008	2007	2006	2005
F.S.† (µm)	*0.18*	0.5	0.5	0.35	0.35	--	0.35	0.35	0.25	0.35
V_{DD} (V)	*1.8*	3.3	1.5	3.3	3.3	±1.5	3	3	1.5	2
I_B (µA)	*10*	--	--	10	10	--	10	--	80	0.25
P_{diss} (µW)	*52.93*	2000	120	240	340	1830	3000>	538	--	5.5
THD (%)[1]	*0.53[8]*	0.2[1]	0.63[2]	0.76	0.97	1.39[3]	1[4,5]	0.144[5]	0.25[7]	0.9[6]
BW (MHz)	*1503*	3	18	44.9	41.8	53.1	1	44	154	0.2
N. E.‡ (%)	*0.84*	--	--	1.15	1.1	--	--	--	0.8	5
Number of quadrants	*4*	2	2	4	4	4	4	1	4	4
FOM1	*214.3*	0.014	0.94	0.97	0.51	0.083	4<	0.57	20.52<	0.17
FOM2	*0.090*	0.004<	0.026<	0.005	0.010	--	0.001	0.037<	0.040<	0.143
Meas/ Sim	*Sim*	Meas	Meas	Sim	Sim	Sim	Meas	Meas	Sim	Sim

[1]f=10KHz; [2]I_x=50µA; [3]f=100KHz; [4]I_x=5µA; [5]f=1KHz; [6]for I_x=112nA in I_y=210nA-DC (f=2KHz); [7]f=1MHz; [8]@ 1MHz, 10µA; †Feature Size; ‡Non-linearity Error

The two latest row of Table V shows the *FOM1* and *FOM2* of the compared works. Obviously, the proposed circuit in this work pertians the largest value in both *FOM*s except for the *FOM2* in compare to reference [13].

5. Conclusion

The designed current mode four-quadrant analog multiplier has remarkable advantages towards other reported ones thanks to the new squarer proposed here. Lower harmonic distortion, lower power consumption - although our used technology is relatively new-, and higher BW are some of these advantages. Very low sensitivity to process variations, voltage supply and temperature (PVT) are the other important features of the circuit. It was shown that using MOGA helps designer to optimize circuit as well as possible and increases circuit robustness versus main circuit parameter deviations from theirs optimum solutions.

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