

wiggleport

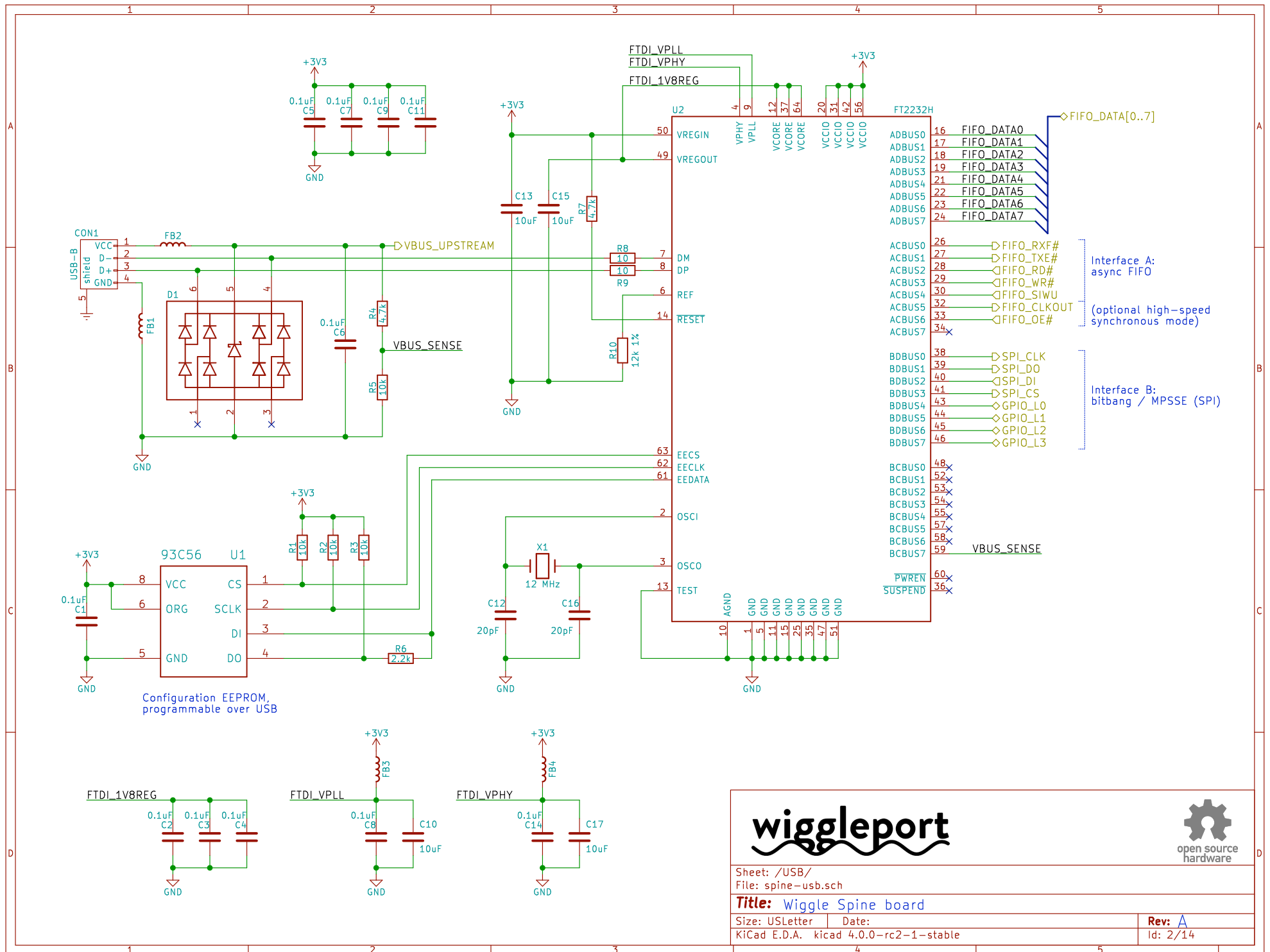


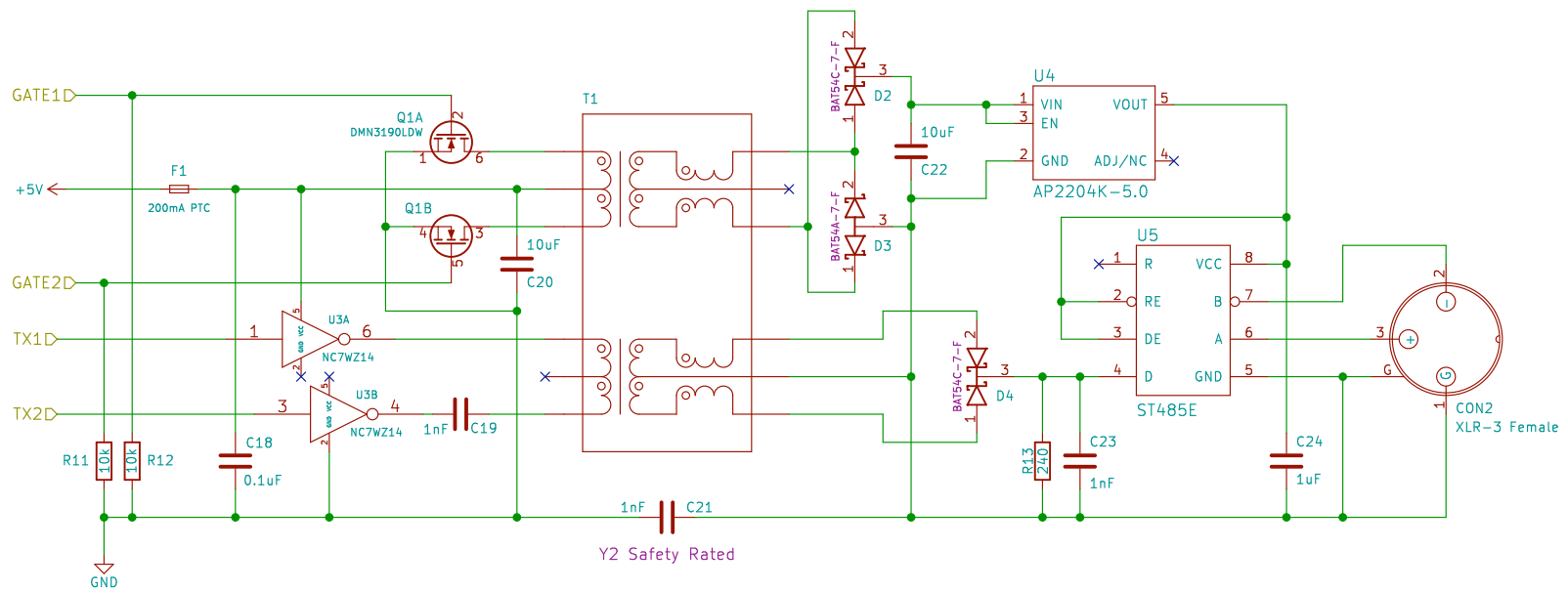
Sheet: /
File: wiggle-spine.sch

Title: Wiggle Spine board

Size: USLetter Date:
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Sheet: /DMX512/
File: spine-dmx512.sch

Title: Wiggle Spine board

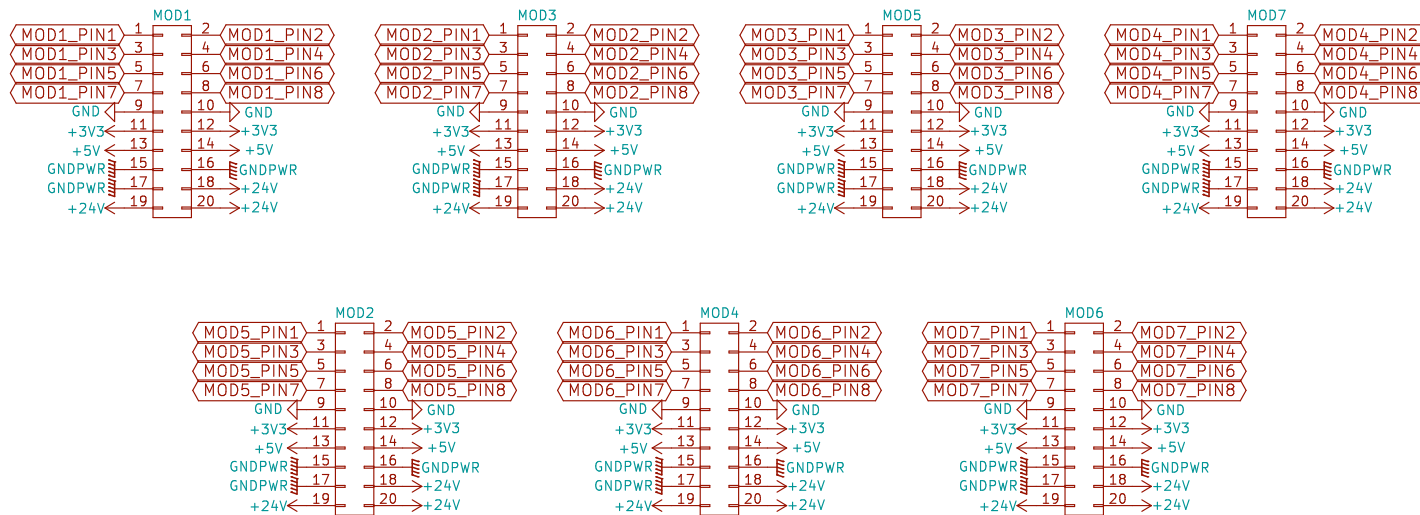
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8x GPIOs per module (3.3V ONLY)
Limited ESD protection (2kV HBM) on each I/O.

3.3v and 5v supplied by system DC/DC converters.
At least 100mA available per module.

24v rail is actually 5–24v, up to 4A per module.



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Sheet: /Modules/
File: spine-modules.sch

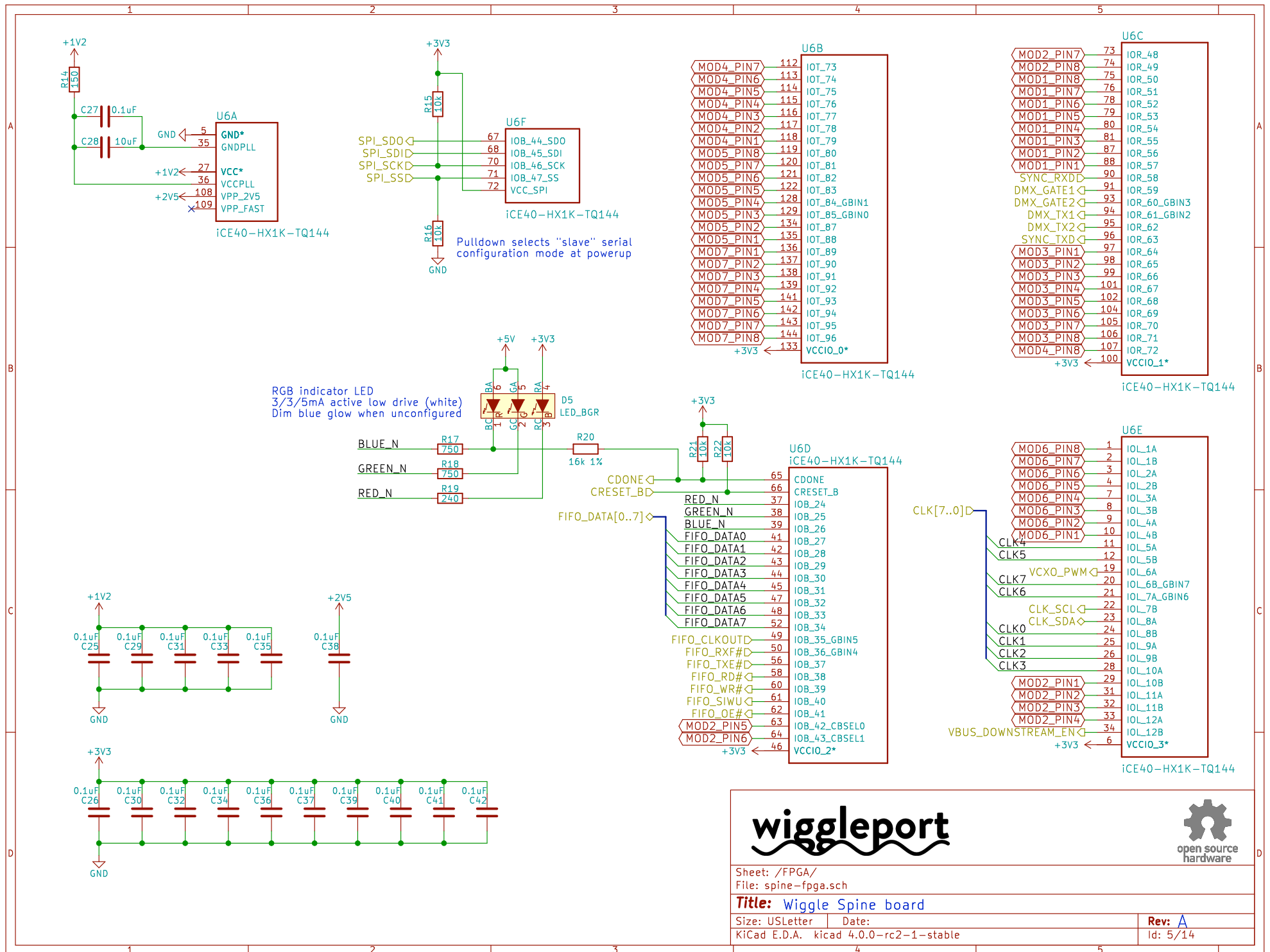
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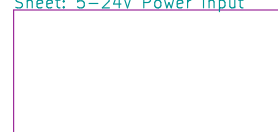
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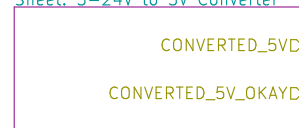
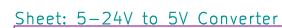
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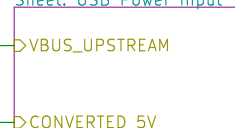




File: power-24v.sch



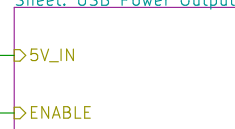
File: power-5v.sch



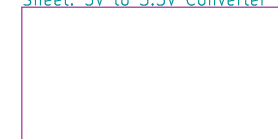
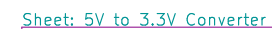
→ CONVERTED_5V

→ CONVERTED_5V_OKAY

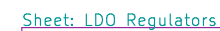
File: power-usb-in.sch



File: power-usb-out.sch



File: power-3v3.sch



File: power-ldo.sch

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Sheet: /Power/

File: spine-power.sch

Title: Wiggle Spine board

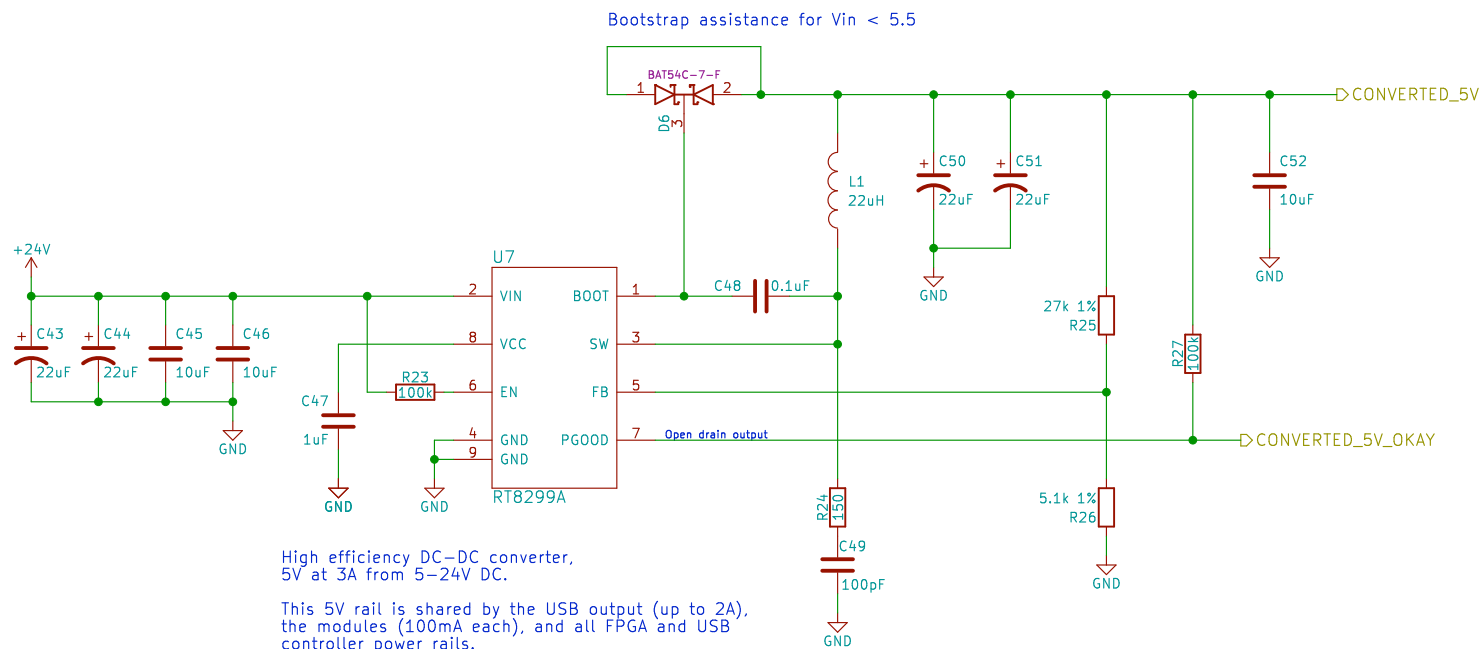
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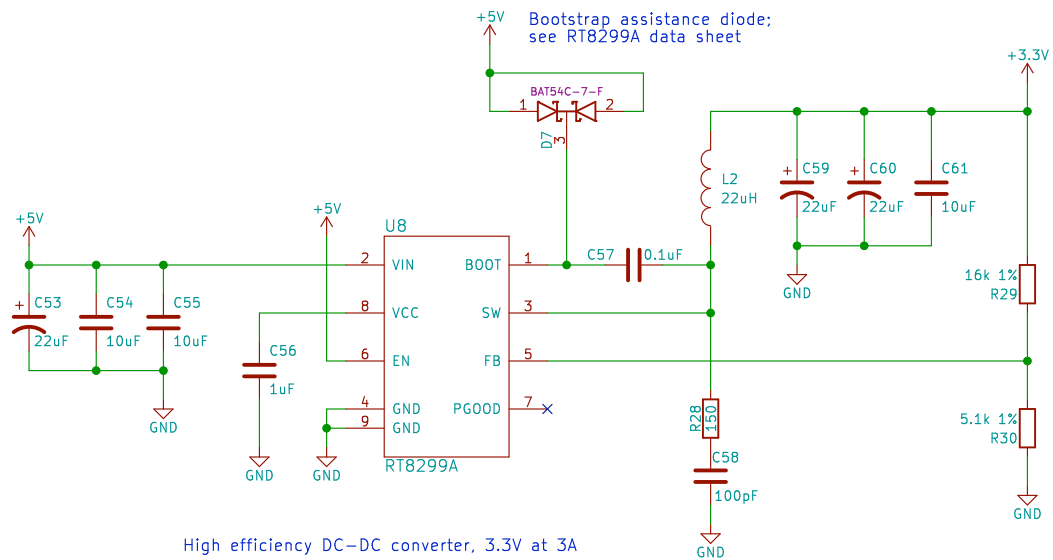
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File: power-5v.sch

Title: Wiggle Spine board

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Sheet: /Power/5V to 3.3V Converter/
File: power-3v3.sch

Title: Wiggle Spine board

Size: USLetter

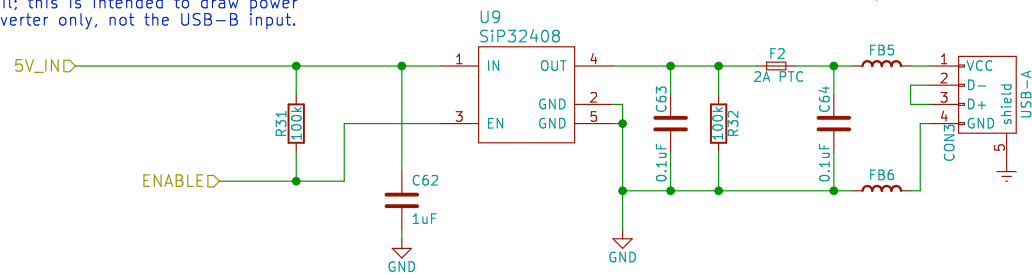
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Not the main +5V rail; this is intended to draw power from the DC-DC converter only, not the USB-B input.



USB power output, 5V 2A.

Intended to power a small computer, like the Raspberry Pi 2.

Optional hardware watchdog timer, implemented in the FPGA.

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Sheet: /Power/USB Power Output/
File: power-usb-out.sch

Title: Wiggle Spine board

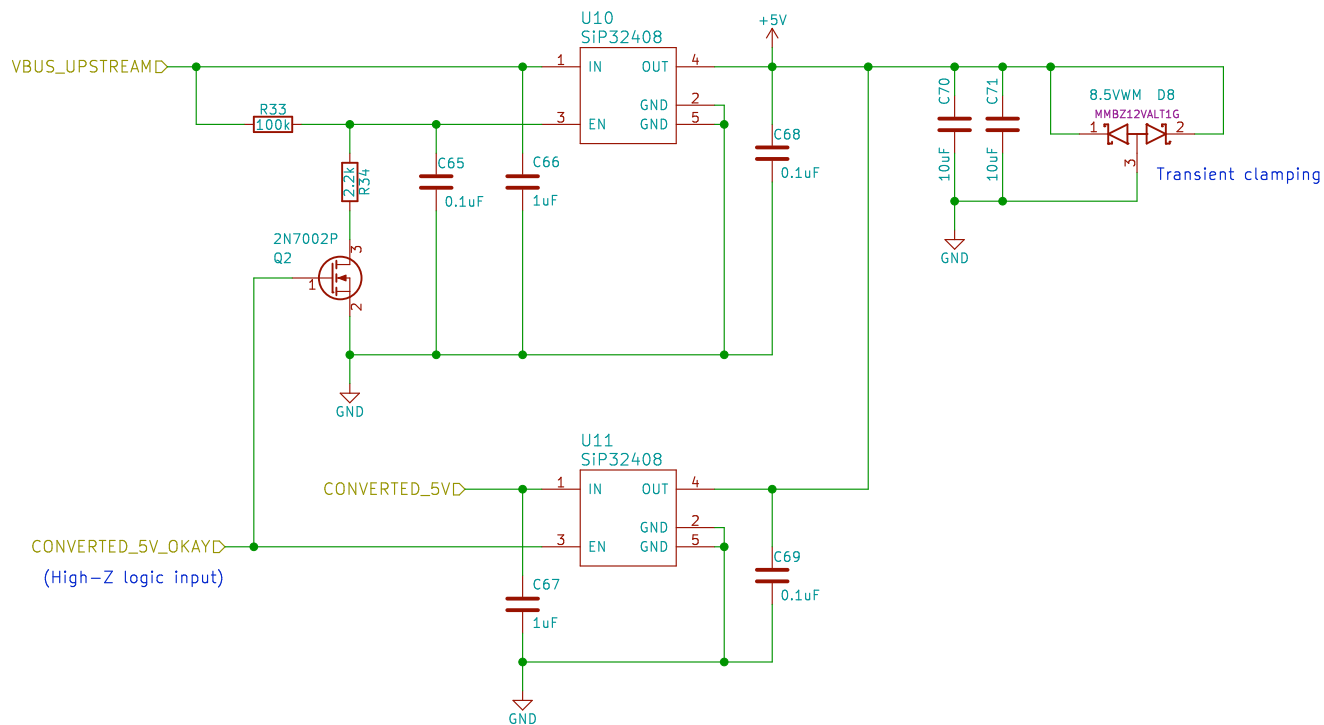
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When USB power is available, route it to the +5V rail
(with reverse current protection)

When/if external 5V becomes available, switch to it
softly, then draw no power from upstream USB.



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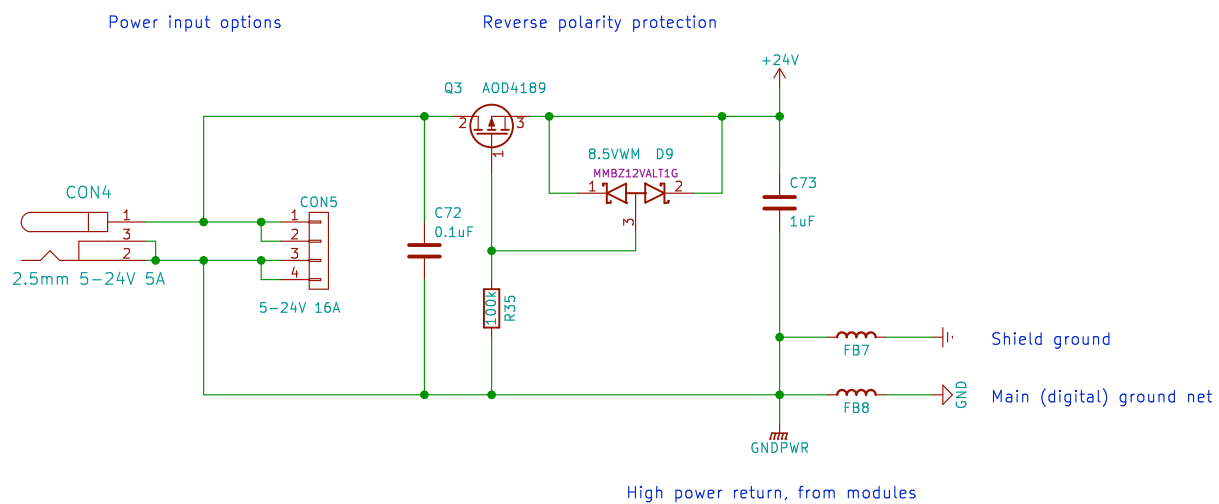
Sheet: /Power/USB Power Input/
File: power-usb-in.sch

Title: Wiggle Spine board

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Sheet: /Power/5-24V Power Input/
File: power-24v.sch

Title: Wiggle Spine board

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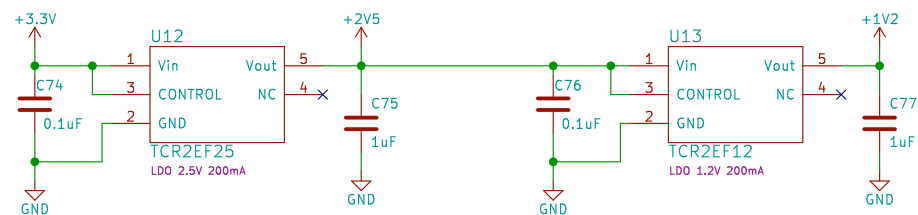
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Low voltage / low current
LDO regulators for FPGA

2.5v = FPGA NVCM programming voltage

(Some circuits approximate this with a diode
drop from 3.3v, but that's pretty dirty and
these LDOs are about as cheap as a diode.)

1.2v = FPGA core voltage



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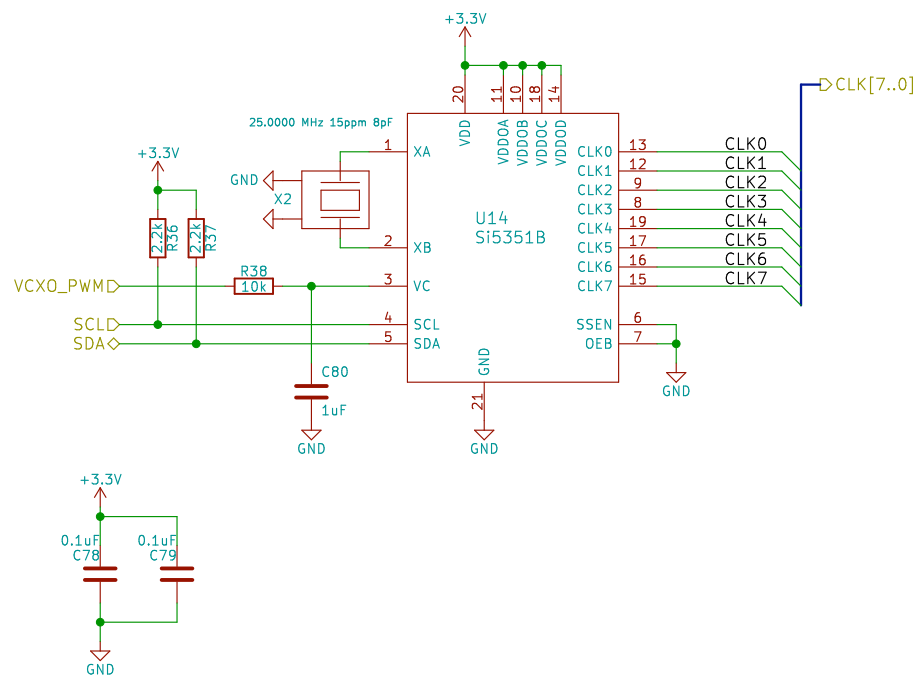
Sheet: /Power/LDO Regulators/
File: power-ldo.sch

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Includes analog VCXO, used to synthesize stable local clocks that match the rate of another Spine unit.



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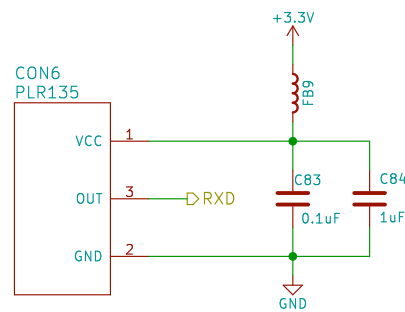
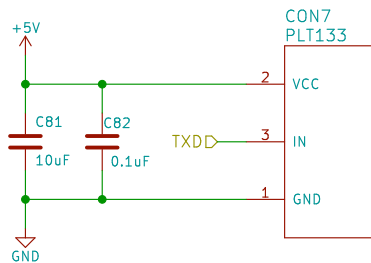


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Sync IN / OUT

Using "TOSLINK" style modules for low jitter, low cost, and galvanic isolation.



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