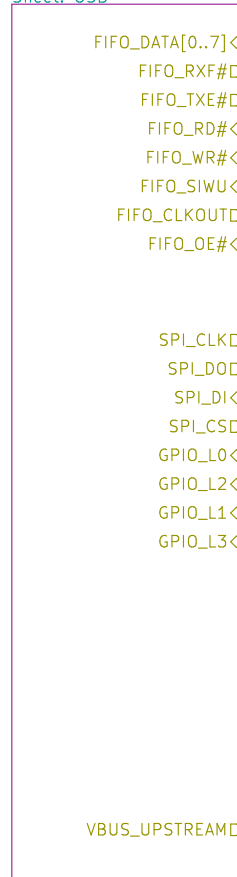
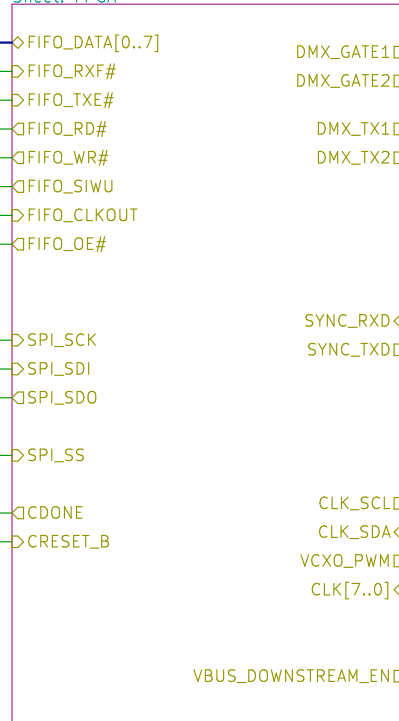


## Sheet: USB



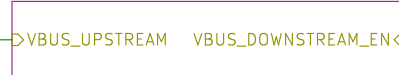
File: spine-usb.sch

## Sheet: FPGA



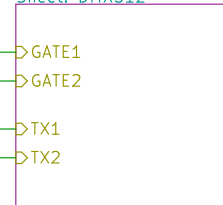
File: spine-fpga.sch

## Sheet: Power



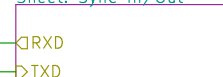
File: spine-power.sch

## Sheet: DMX512



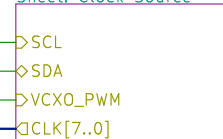
File: spine-dmx512.sch

## Sheet: Sync In/Out



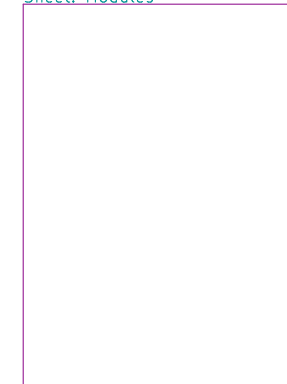
File: spine-sync.sch

## Sheet: Clock Source



File: spine-clock.sch

## Sheet: Modules



File: spine-modules.sch

# wiggleport

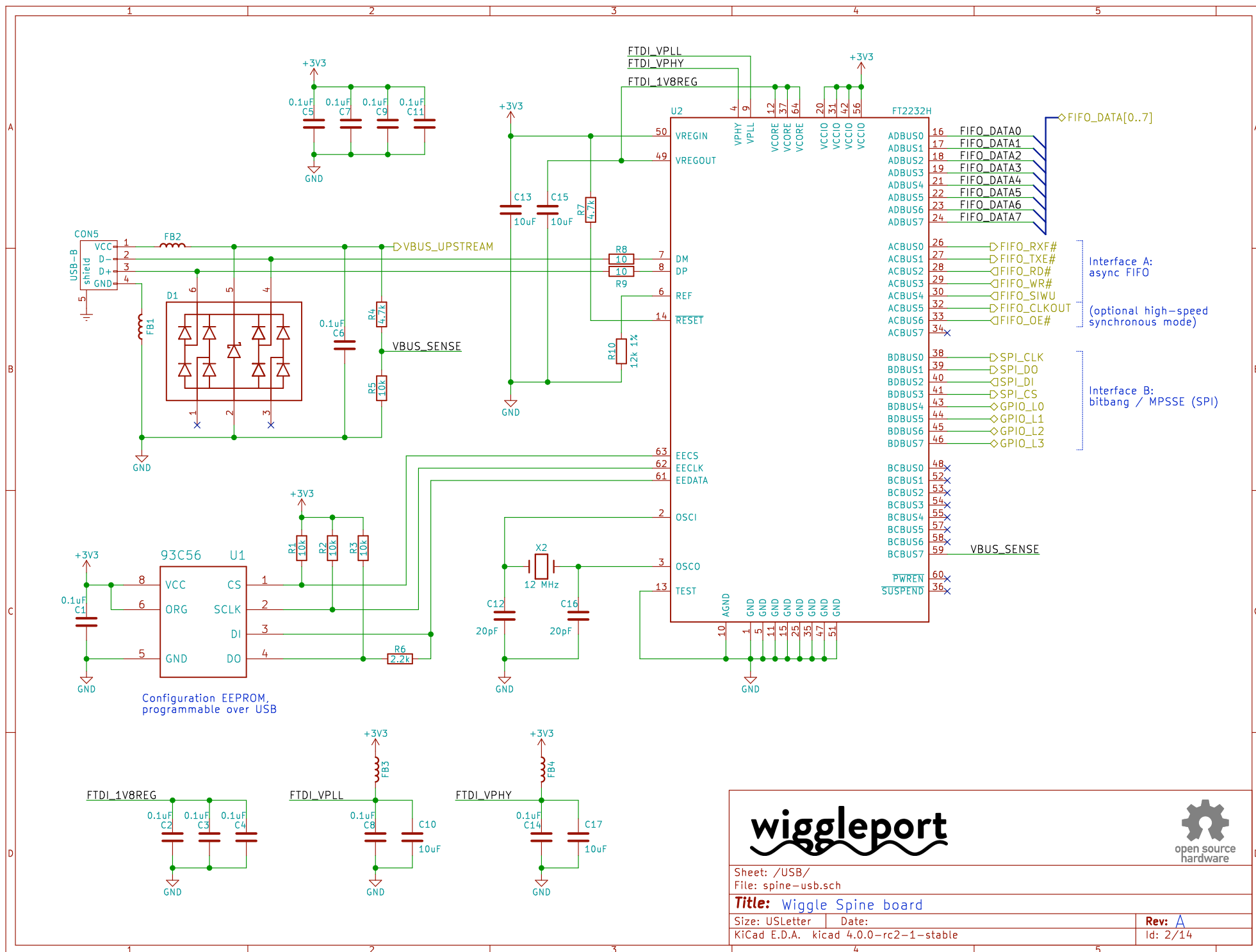


Sheet: /  
File: wiggle-spine.sch

**Title:** Wiggle Spine board

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**Rev:** A  
Id: 1/14



wiggleport

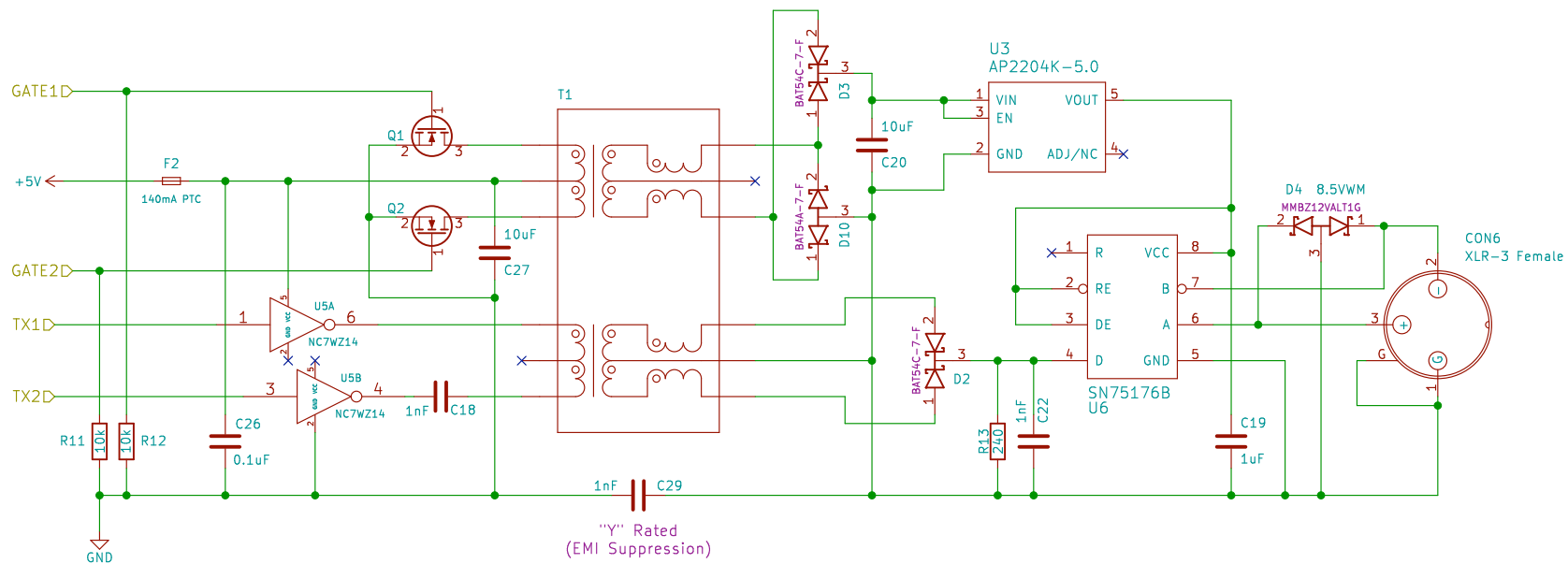


Sheet: /USB/  
File: spine-usb.sch

Title: Wiggle Spine board

Size: USLetter Date:  
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Id: 2/14



wiggleport



Sheet: /DMX512/  
File: spine-dmx512.sch

**Title:** Wiggle Spine board

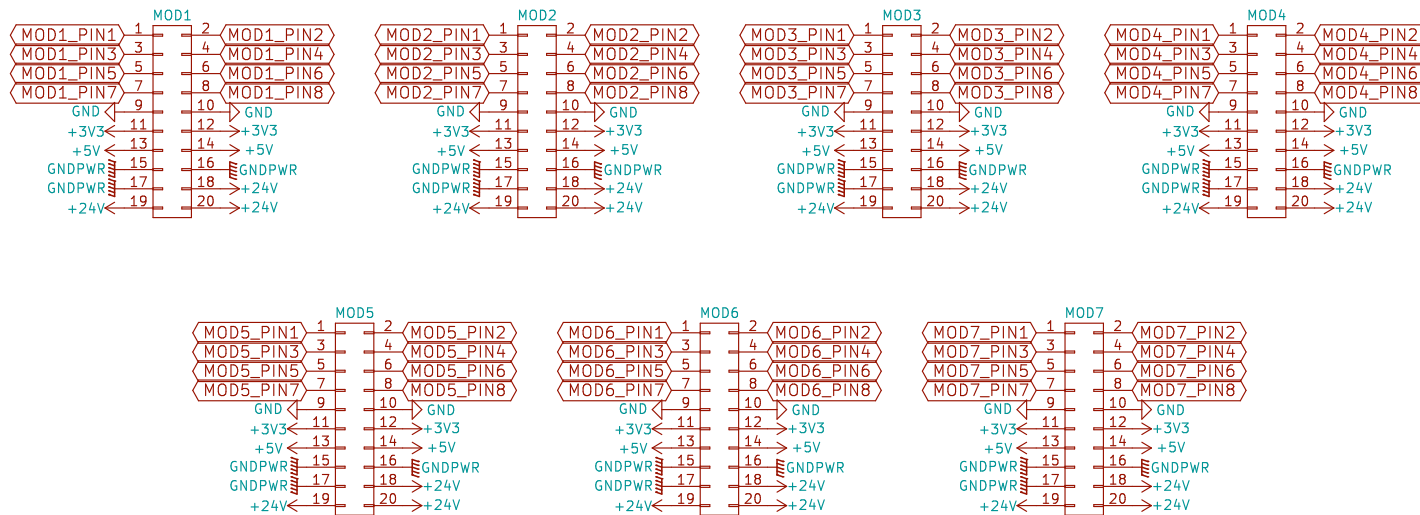
Size: USLetter Date:  
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Rev: A  
Id: 3/14

8x GPIOs per module (3.3V ONLY)  
Limited ESD protection (2kV HBM) on each I/O.

3.3v and 5v supplied by system DC/DC converters.  
At least 100mA available per module.

24v rail is actually 5–24v, up to 4A per module.



wiggleport



Sheet: /Modules/  
File: spine-modules.sch

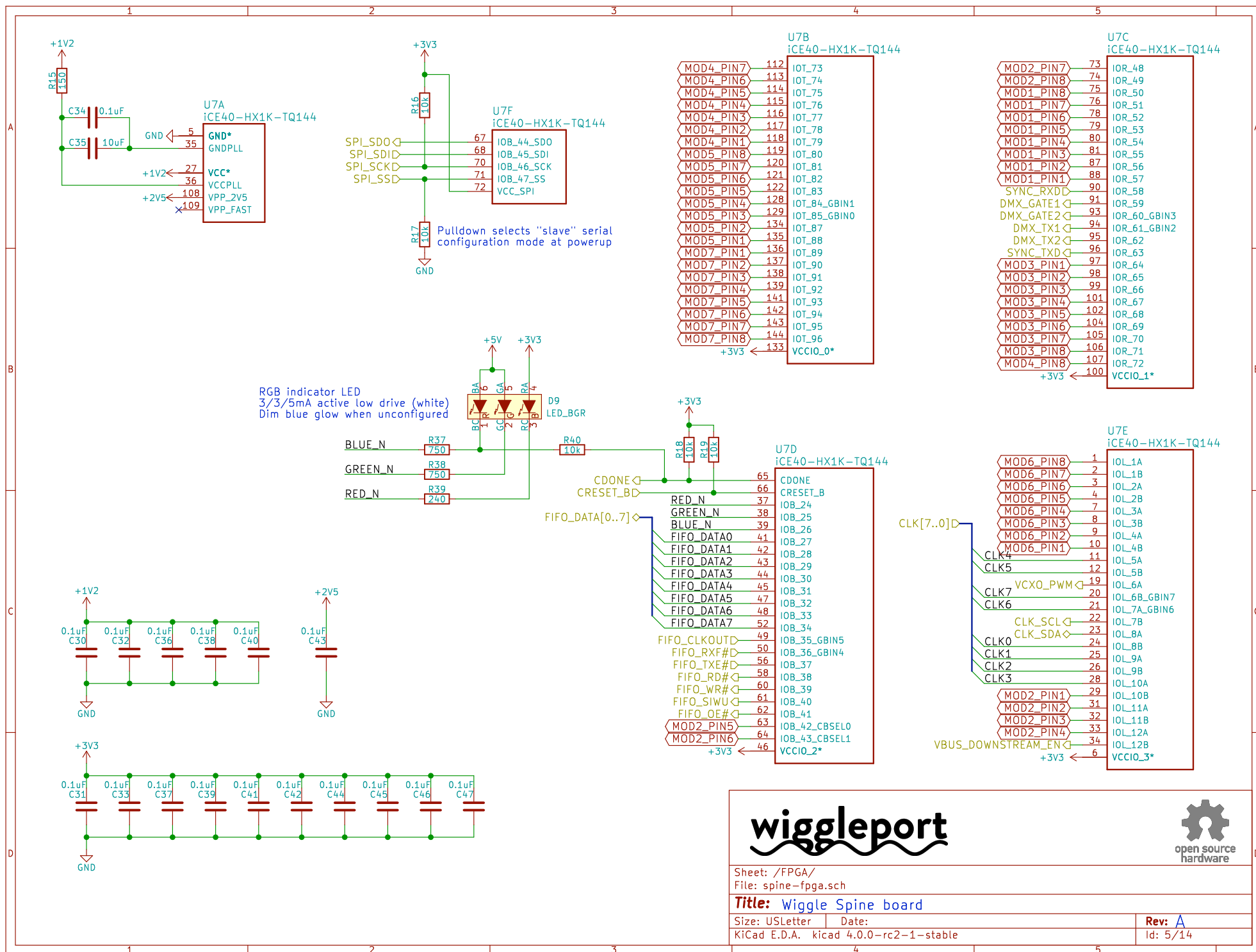
**Title:** Wiggle Spine board

Size: USLetter Date:

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Rev: A

Id: 4/14



wiggleport

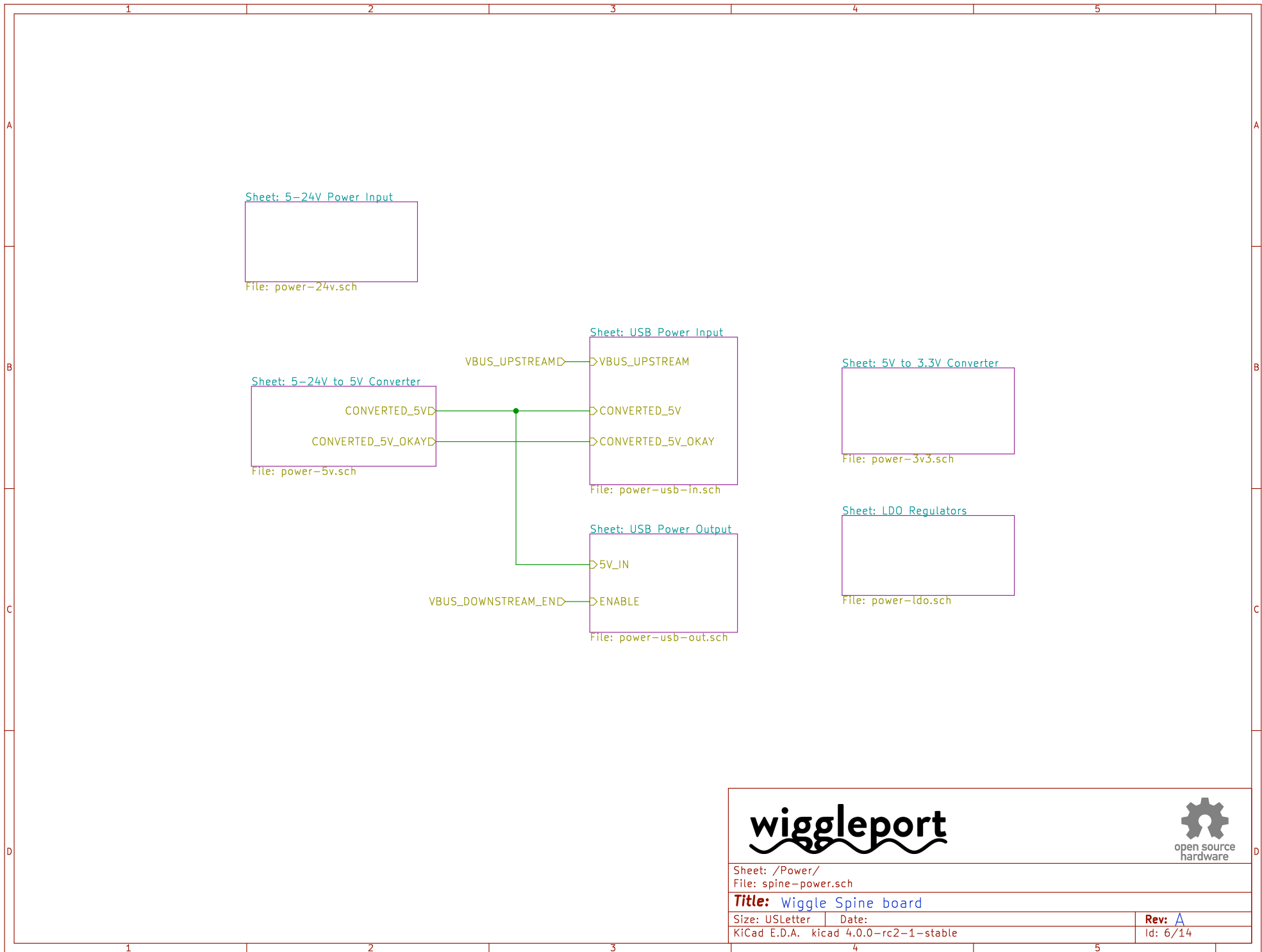


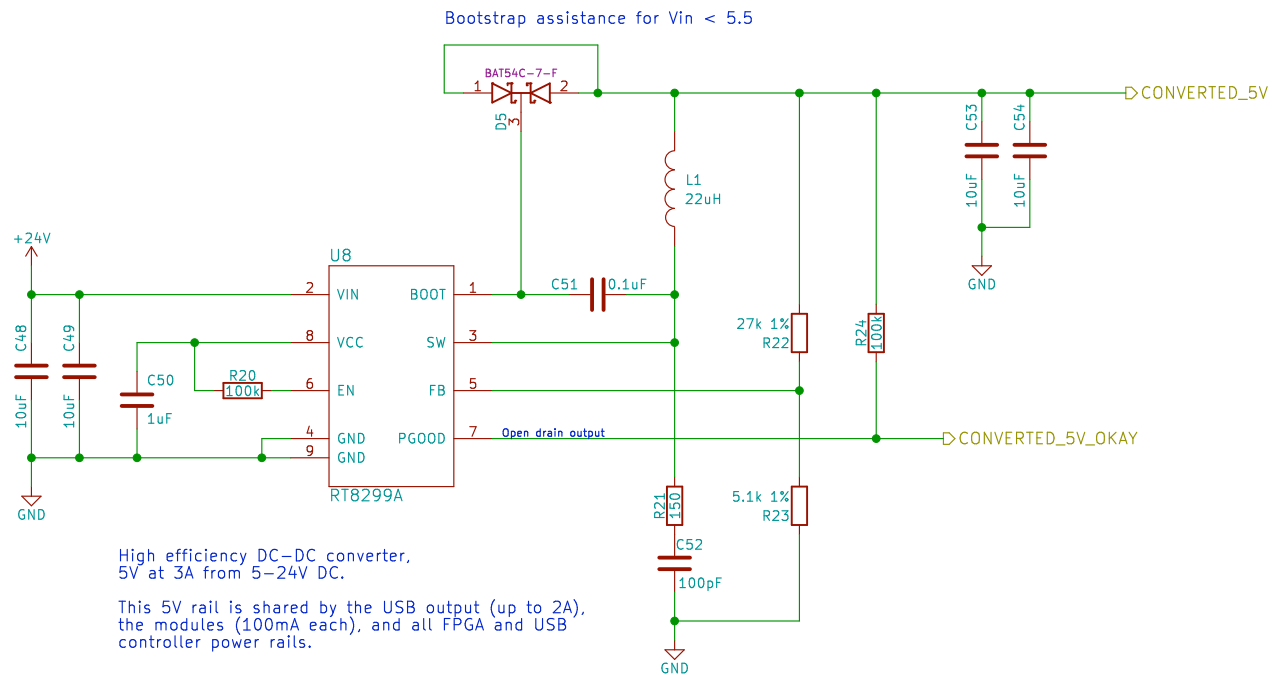
Sheet: /FPGA/  
File: spine-fpga.sch

**Title:** Wiggle Spine board

Size: USLetter Date:  
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Rev: A  
Id: 5/14





wiggleport



Sheet: /Power/5-24V to 5V Converter/  
File: power-5v.sch

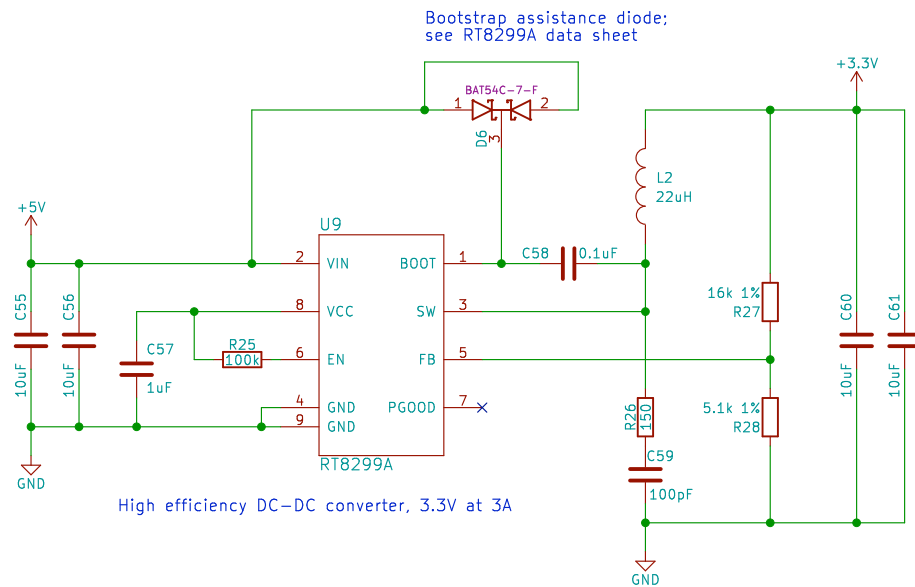
**Title:** Wiggle Spine board

Size: USLetter Date:

KiCad E.D.A. kicad 4.0.0-rc2-1-stable

**Rev:** A

Id: 7/14



wiggleport



Sheet: /Power/5V to 3.3V Converter/  
File: power-3v3.sch

**Title:** Wiggle Spine board

Size: USLetter Date:

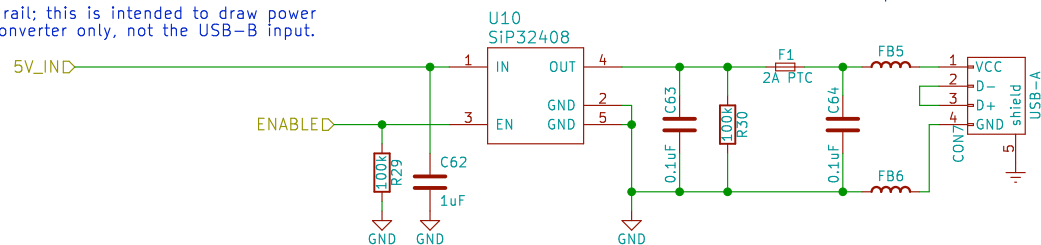
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**Rev:** A

Id: 8/14



Not the main +5V rail; this is intended to draw power from the DC-DC converter only, not the USB-B input.



USB power output, 5V 2A.

Intended to power a small computer, like the Raspberry Pi 2.

Optional hardware watchdog timer, implemented in the FPGA.

wiggleport



Sheet: /Power/USB Power Output/  
File: power-usb-out.sch

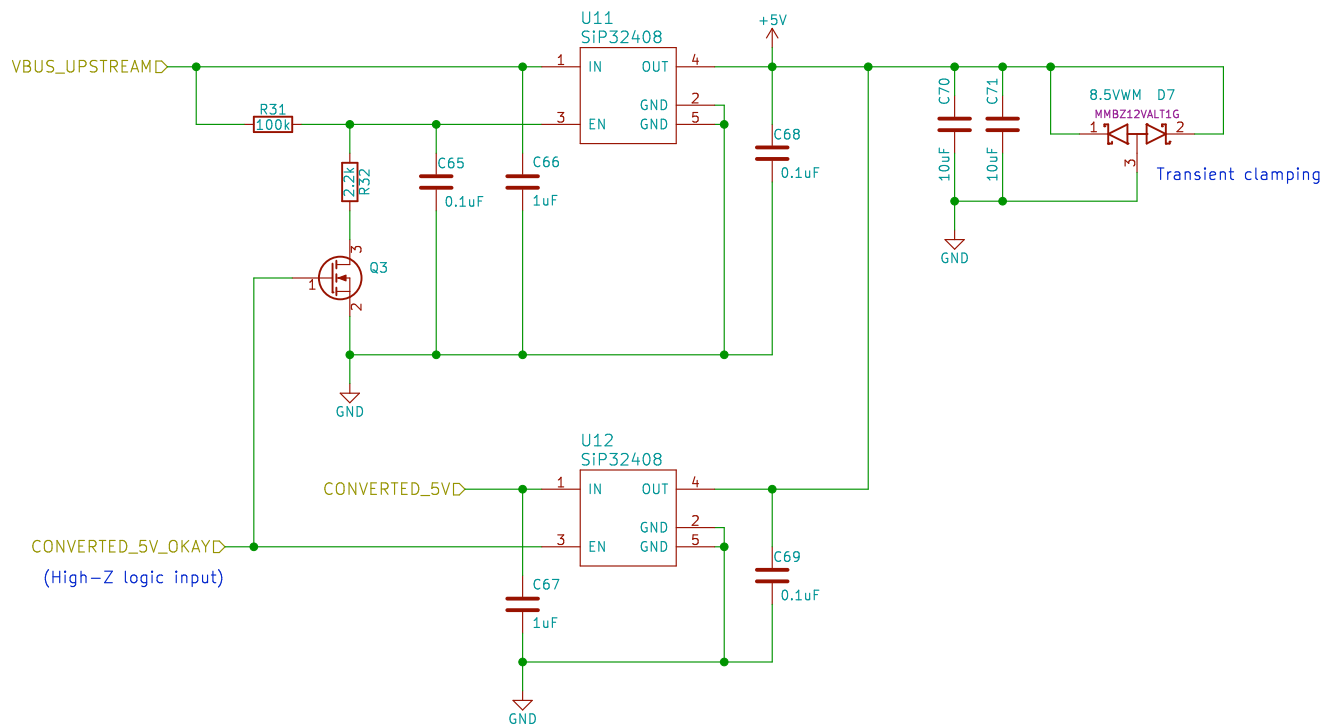
**Title:** Wiggle Spine board

Size: USLetter Date:

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**Rev:** A  
Id: 9/14

When/if external 5V becomes available, switch to it softly, then draw no power from upstream USB.

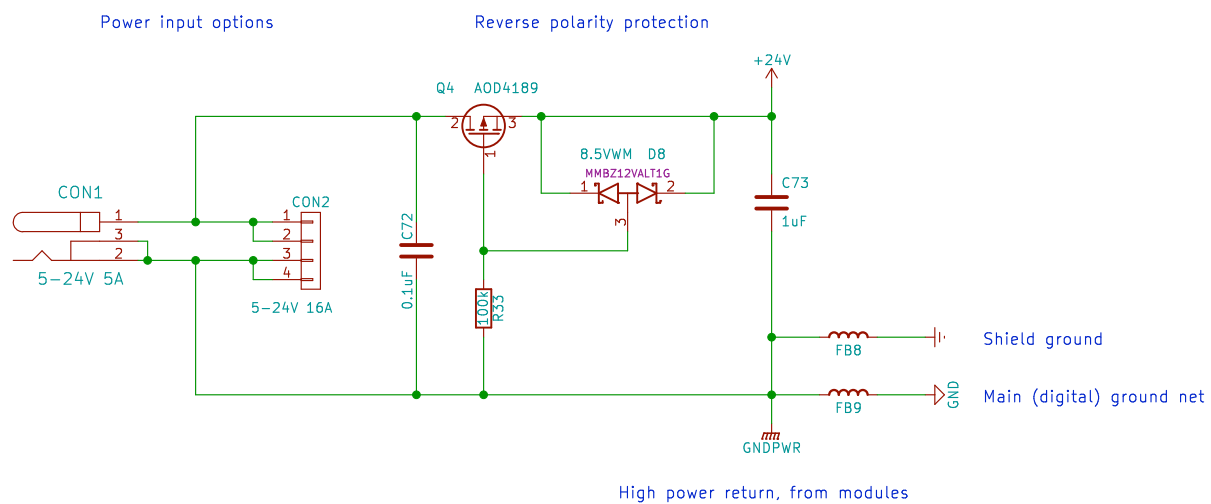
The logo for wigggleport, featuring the word "wigggleport" in a lowercase, rounded, sans-serif font. Below the text is a stylized wavy line representing water.

**Title:** Wiggle Spine board

**Title:** Wiggle Spine board

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Id: 10/14



wiggleport



Sheet: /Power/5-24V Power Input/  
File: power-24v.sch

**Title:** Wiggle Spine board

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Rev: A

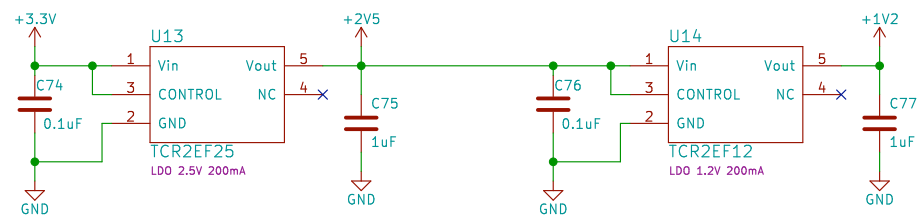
Id: 11/14

Low voltage / low current  
LDO regulators for FPGA

2.5v = FPGA NVCM programming voltage

(Some circuits approximate this with a diode  
drop from 3.3v, but that's pretty dirty and  
these LDOs are about as cheap as a diode.)

1.2v = FPGA core voltage



wiggleport



Sheet: /Power/LDO Regulators/  
File: power-ldo.sch

**Title:** Wiggle Spine board

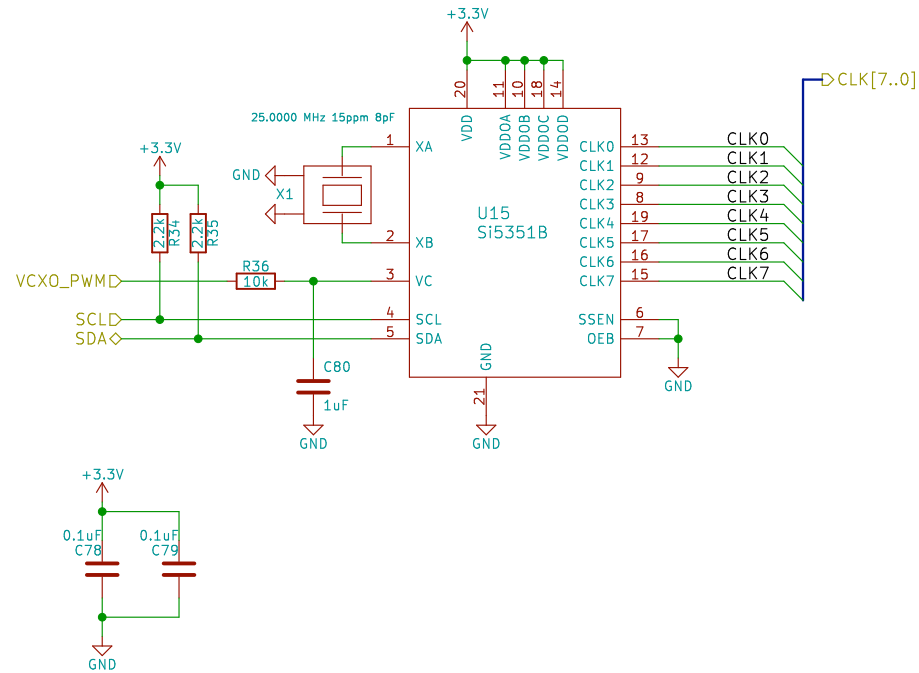
Size: USLetter Date:

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Rev: A  
Id: 12/14

# Programmable clock synthesizer

Includes analog VCXO, used to synthesize stable local clocks that match the rate of another Spine unit.



wiggleport



Sheet: /Clock Source/  
File: spine-clock.sch

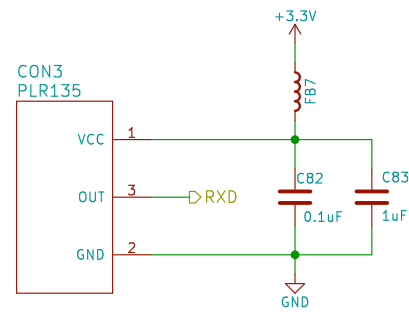
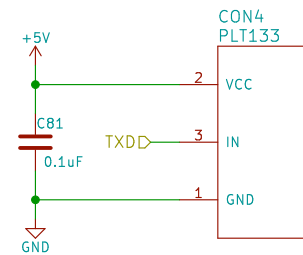
Title: Wiggle Spine board

Size: USLetter Date:  
KiCad E.D.A. kicad 4.0.0-rc2-1-stable

Rev: A  
Id: 13/14

### Sync IN / OUT

Using "TOSLINK" style modules for low jitter, low cost, and galvanic isolation.



wiggleport



Sheet: /Sync In/Out/  
File: spine-sync.sch

**Title:** Wiggle Spine board

Size: USLetter Date:

KiCad E.D.A. kicad 4.0.0-rc2-1-stable

**Rev:** A  
Id: 14/14