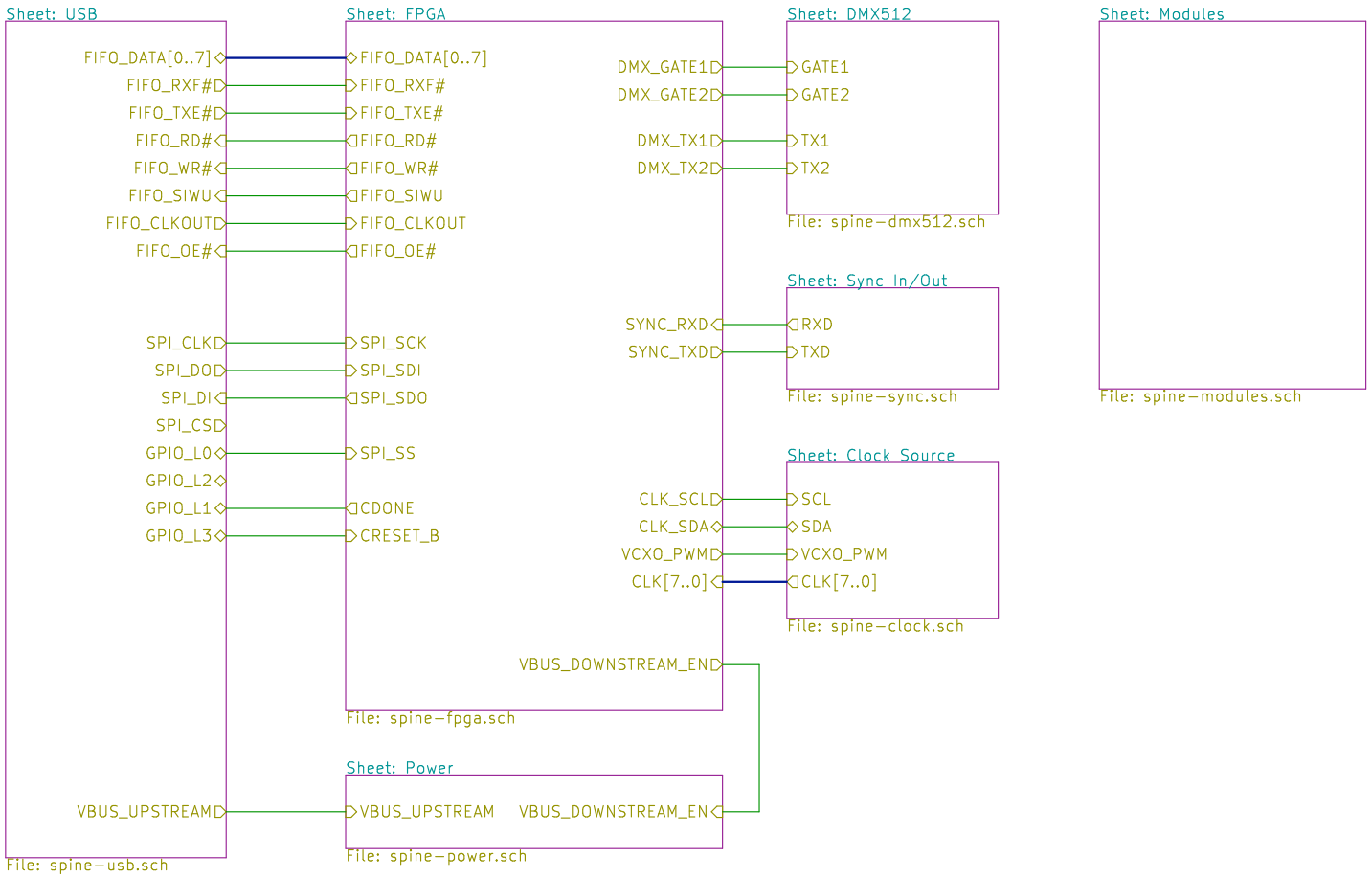


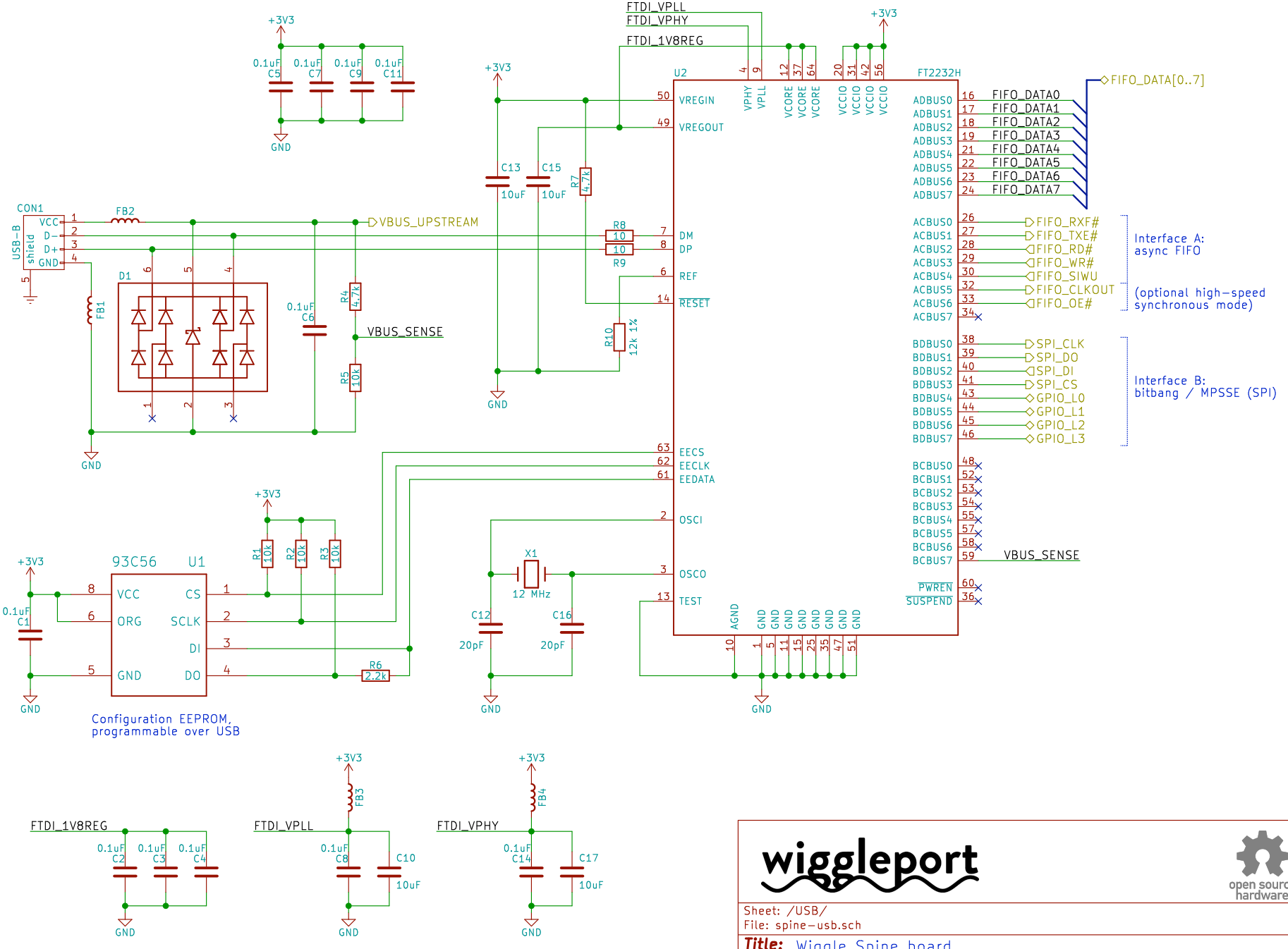
wiggleport

open source hardware

Sheet: /
File: wiggle-spine.sch

Title: Wiggle Spine board

Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable		Id: 1/14



wiggleport

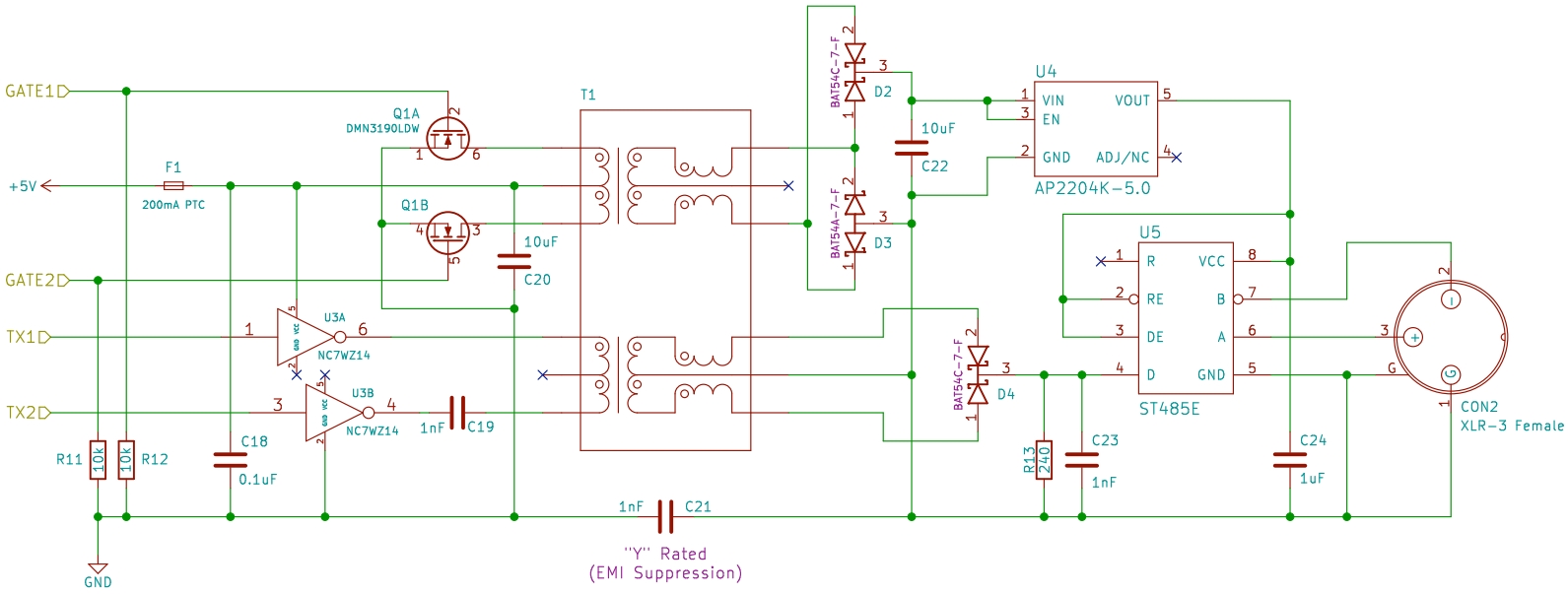
open source hardware

Sheet: /USB/
File: spine-usb.sch

Title: Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 2/14



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Sheet: /DMX512/
File: spine-dmx512.sch

Title: Wiggle Spine board

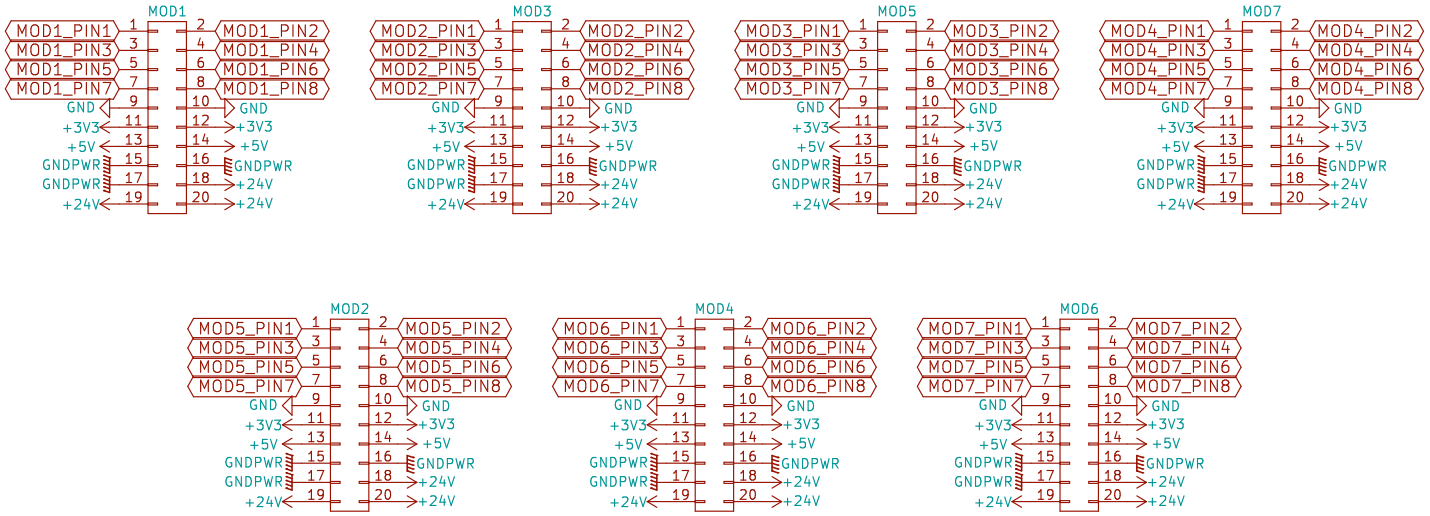
Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 3/14

8x GPIOs per module (3.3V ONLY)
Limited ESD protection (2kV HBM) on each I/O.

3.3v and 5v supplied by system DC/DC converters.
At least 100mA available per module.

24v rail is actually 5–24v, up to 4A per module.



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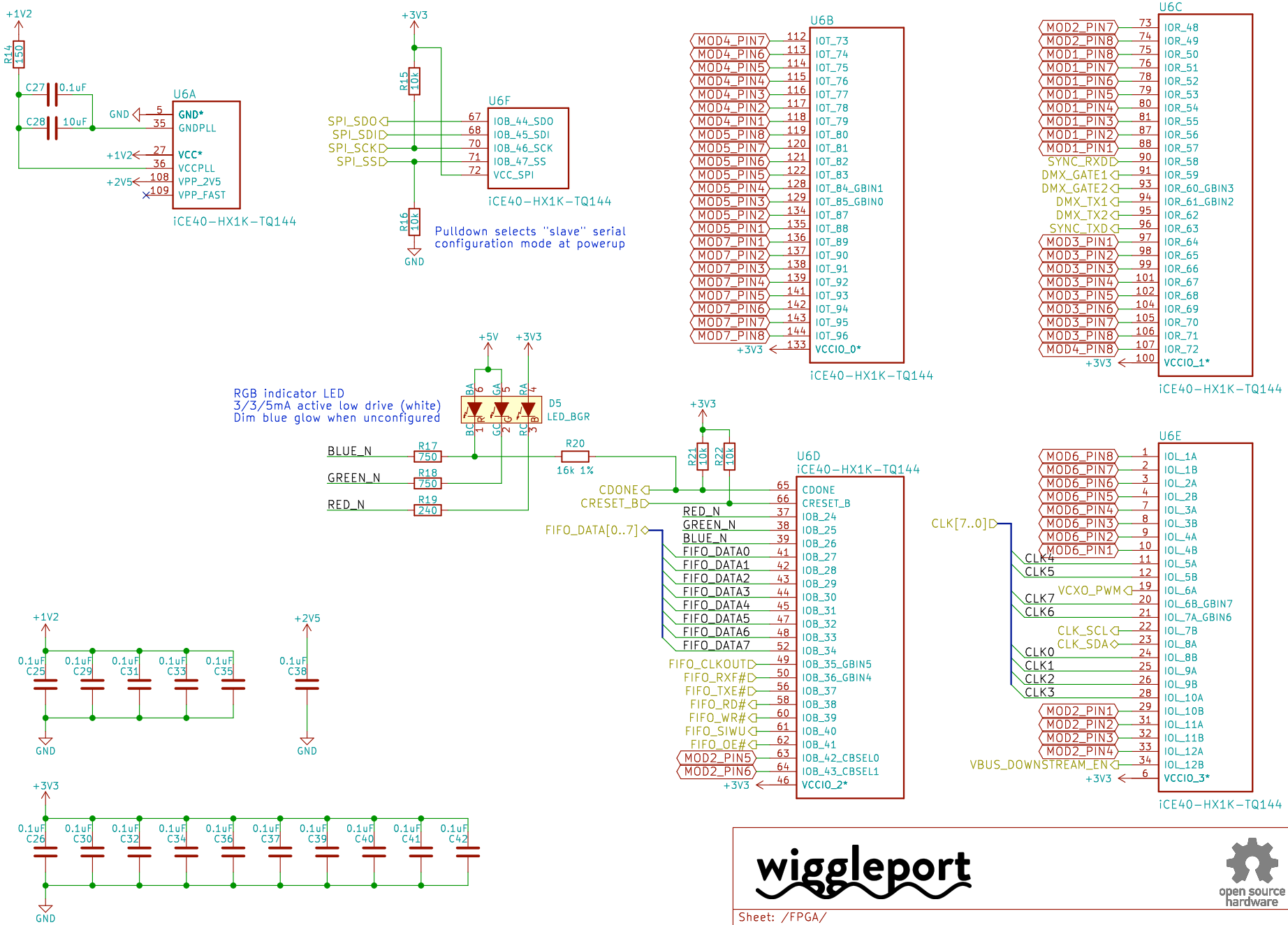
Sheet: /Modules/
File: spine-modules.sch

Title: Wiggle Spine board

Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable		Id: 4/14


+1V2
R14 150
C27 0.1uF
C28 10uF
GND
U6A
GND*
GNDPLL
VCC*
VCCPLL
VPP_2V5
VPP_FAST
iCE40-HX1K-TQ144
+3V3
R15 10k
R16 10k
SPI_SDO
SPI_SDI
SPI_SCK
SPI_SS
U6F
IOB_44_SDO
IOB_45_SDI
IOB_46_SCK
IOB_47_SS
VCC_SPI
iCE40-HX1K-TQ144
Pulldown selects "slave" serial configuration mode at powerup
U6B
iCE40-HX1K-TQ144
U6C
iCE40-HX1K-TQ144
+5V
RGB indicator LED
3/3/5mA active low drive (white)
Dim blue glow when unconfigured
D5
LED_BGR
BLUE_N
GREEN_N
RED_N
R17 750
R18 750
R19 240
R20 16k 1%
R21 10k
R22 10k
U6D
iCE40-HX1K-TQ144
CDONE
CRESET_B
FIFO_DATA[0..7]
FIFO_CLKOUT
FIFO_RXF#
FIFO_TXE#
FIFO_RD#
FIFO_WR#
FIFO_SIWU
FIFO_OE#
MOD2_PIN5
MOD2_PIN6
U6E
iCE40-HX1K-TQ144
CLK[7..0]
VCXO_PWM
CLK_SCL
CLK_SDA
VBUS_DOWNSTREAM_EN
+2V5
0.1uF C25
0.1uF C29
0.1uF C31
0.1uF C33
0.1uF C35
0.1uF C38
0.1uF C26
0.1uF C30
0.1uF C32
0.1uF C34
0.1uF C36
0.1uF C37
0.1uF C39
0.1uF C40
0.1uF C41
0.1uF C42
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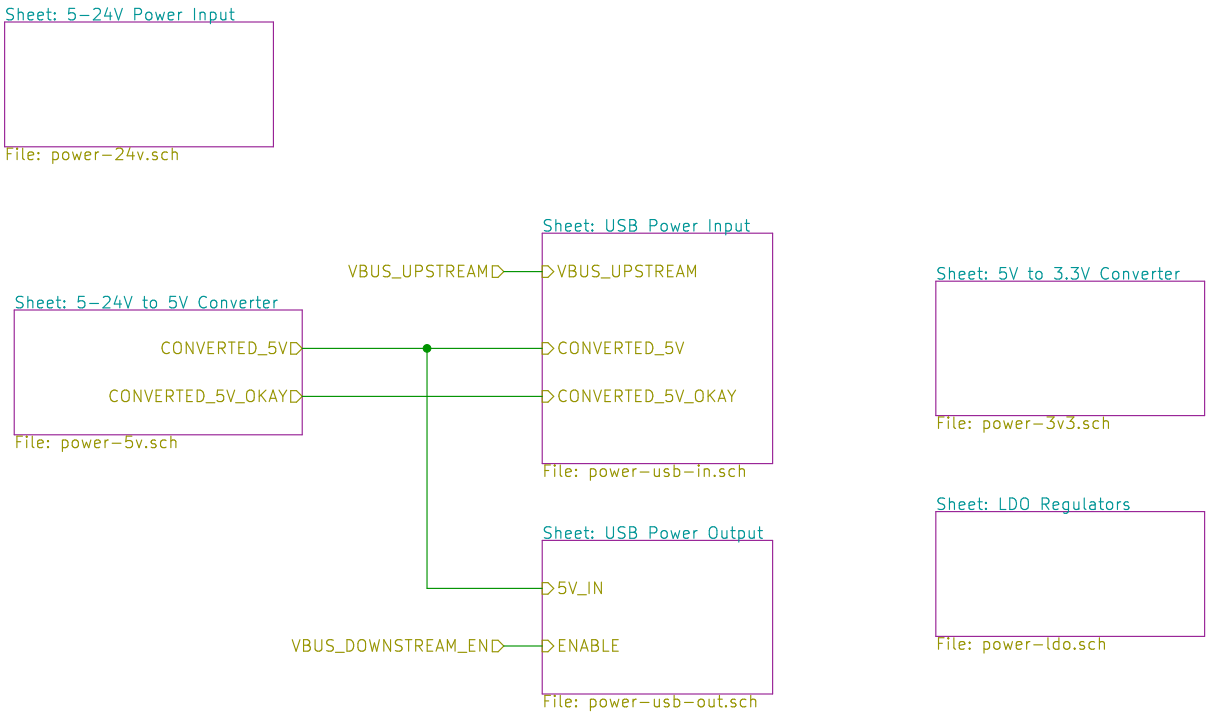
Sheet: /FPGA/
File: spine-fpga.sch
Title: Wiggle Spine board
Size: USLetter
Date:
Rev: A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable
Id: 5/14



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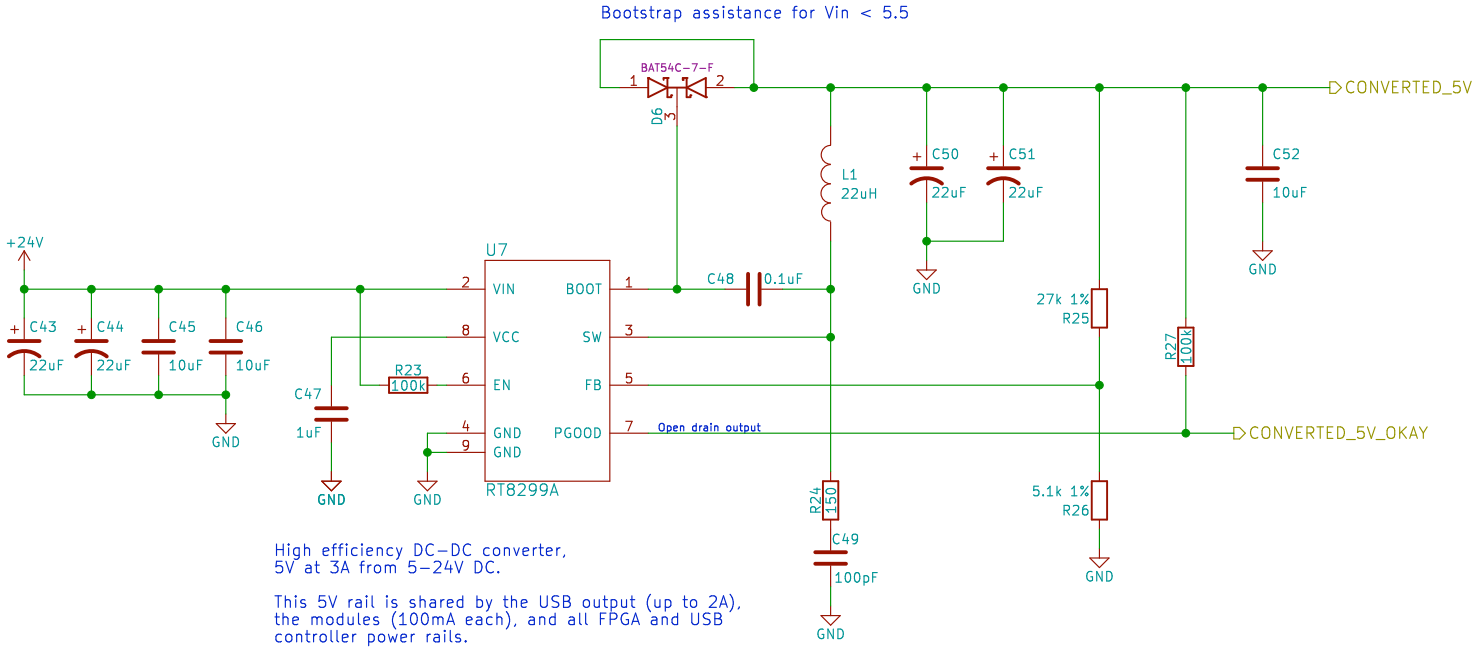
Sheet: /Power/
File: spine–power.sch

Title: Wiggle Spine board

Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0–rc2–1–stable		Id: 6/14



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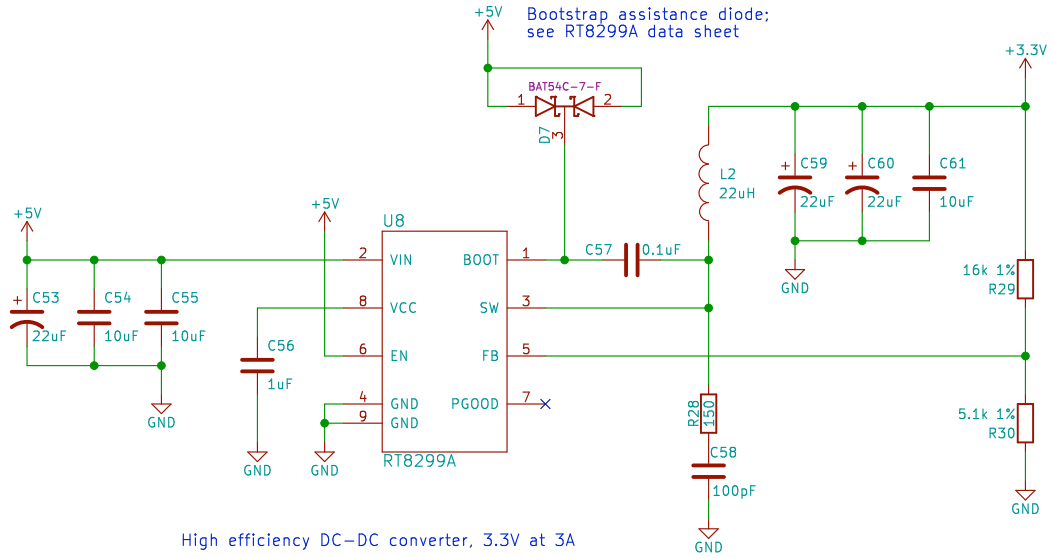
Sheet: /Power/5-24V to 5V Converter/
File: power-5v.sch

Title: Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 7/14



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open source hardware

Sheet: /Power/5V to 3.3V Converter/
File: power-3v3.sch

Title: Wiggle Spine board

Size: USLetter | Date:

Rev: A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable

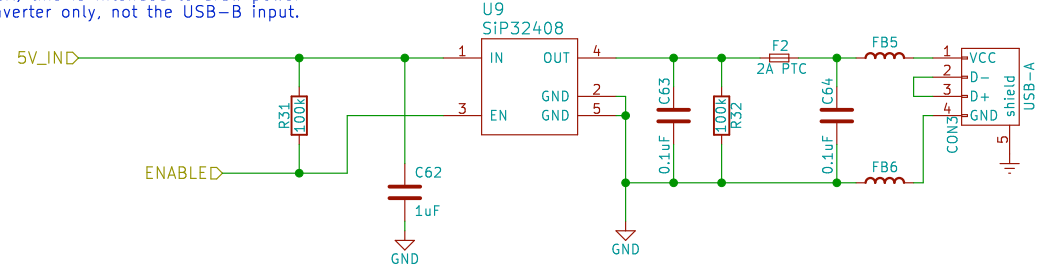
Id: 8/14

USB power output, 5V 2A.

Intended to power a small computer, like the Raspberry Pi 2.

Optional hardware watchdog timer, implemented in the FPGA.

Not the main +5V rail; this is intended to draw power from the DC-DC converter only, not the USB-B input.



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Sheet: /Power/USB Power Output/
File: power-usb-out.sch

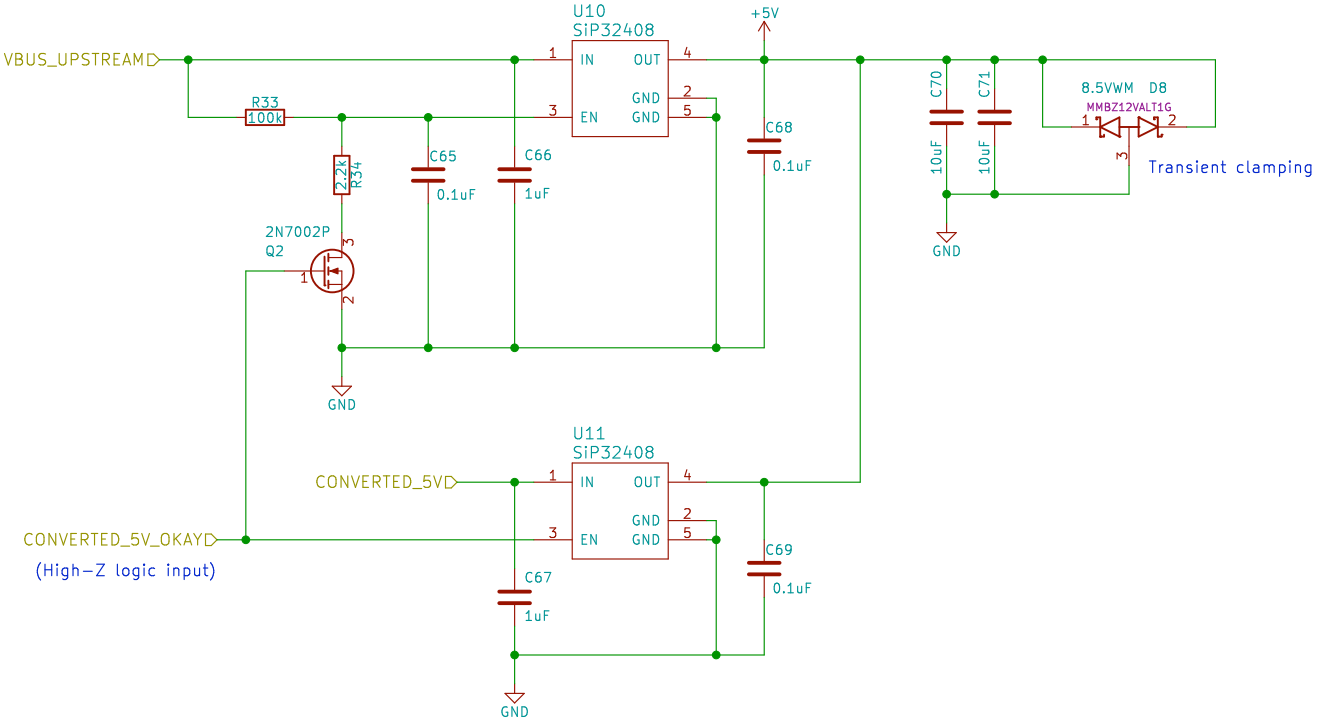
Title: Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 9/14

When USB power is available, route it to the +5V rail
(with reverse current protection)

When/if external 5V becomes available, switch to it
softly, then draw no power from upstream USB.



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Sheet: /Power/USB Power Input/
File: power-usb-in.sch

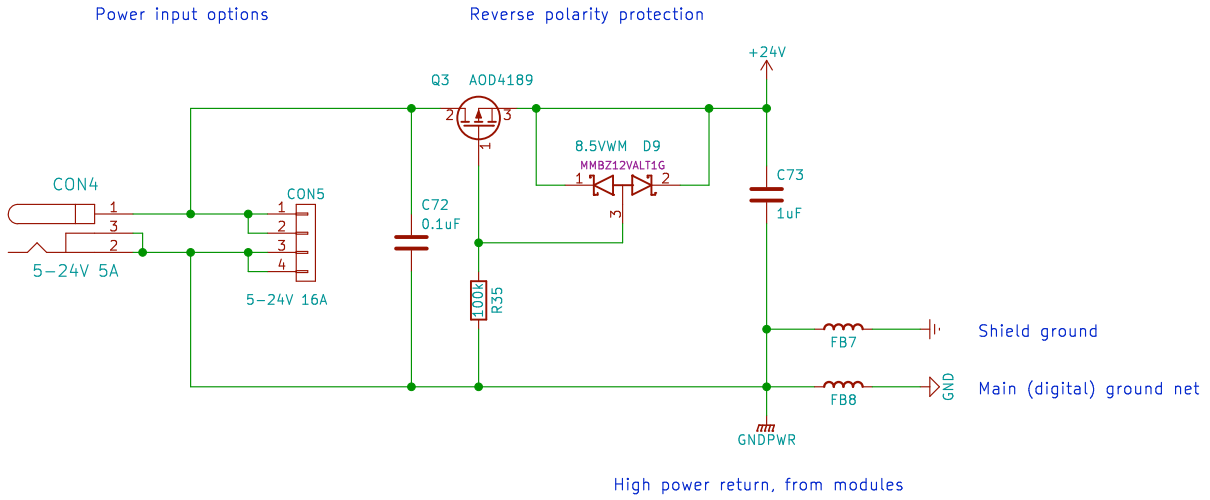
Title: Wiggle Spine board

Size: USLetter | Date:

Rev: A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable

Id: 10/14



wiggleport

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Sheet: /Power/5-24V Power Input/
File: power-24v.sch

Title: Wiggle Spine board

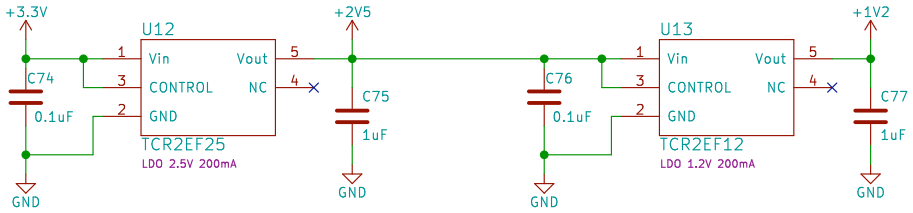
Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable		Id: 11/14

Low voltage / low current
LDO regulators for FPGA

2.5v = FPGA NVCM programming voltage

(Some circuits approximate this with a diode drop from 3.3v, but that's pretty dirty and these LDOs are about as cheap as a diode.)

1.2v = FPGA core voltage



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open source hardware

Sheet: /Power/LDO Regulators/
File: power-ldo.sch

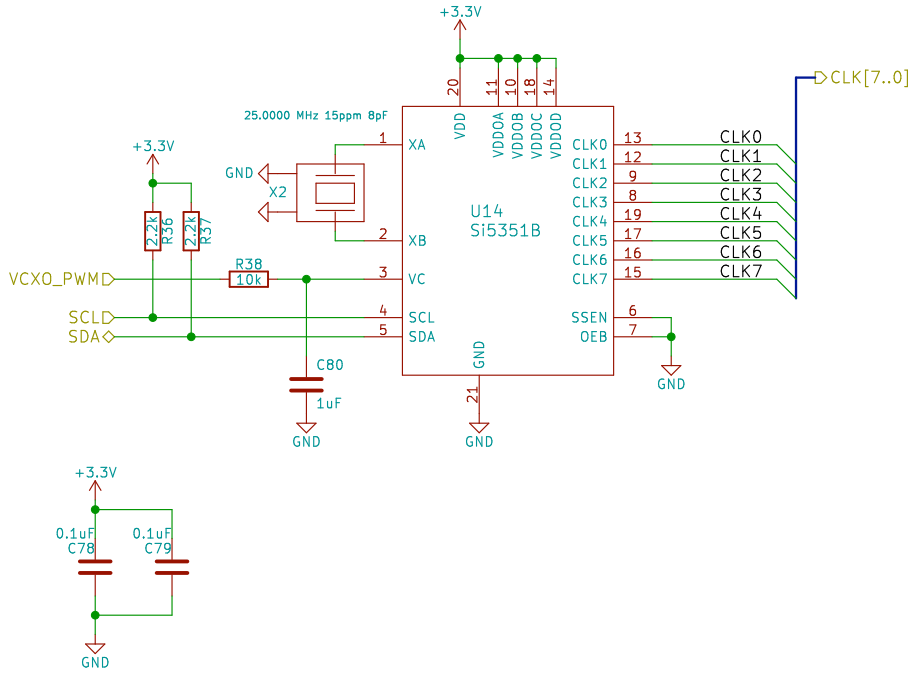
Title: Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 12/14

Programmable clock synthesizer

Includes analog VCXO, used to synthesize stable local clocks that match the rate of another Spine unit.



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Sheet: /Clock Source/
File: spine-clock.sch

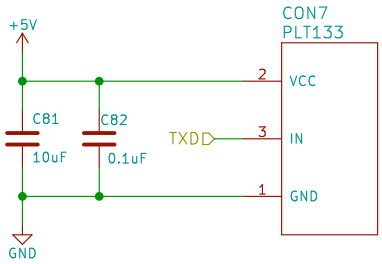
Title: Wiggle Spine board

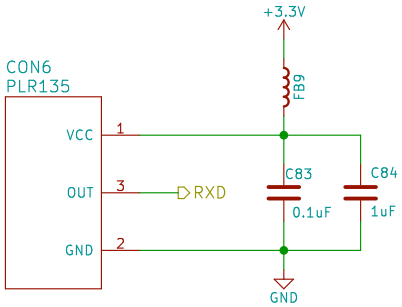
Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 13/14

Sync IN / OUT

Using "TOSLINK" style modules for low jitter, low cost, and galvanic isolation.





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open source hardware

Sheet: /Sync In/Out/
File: spine-sync.sch

Title: Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 14/14