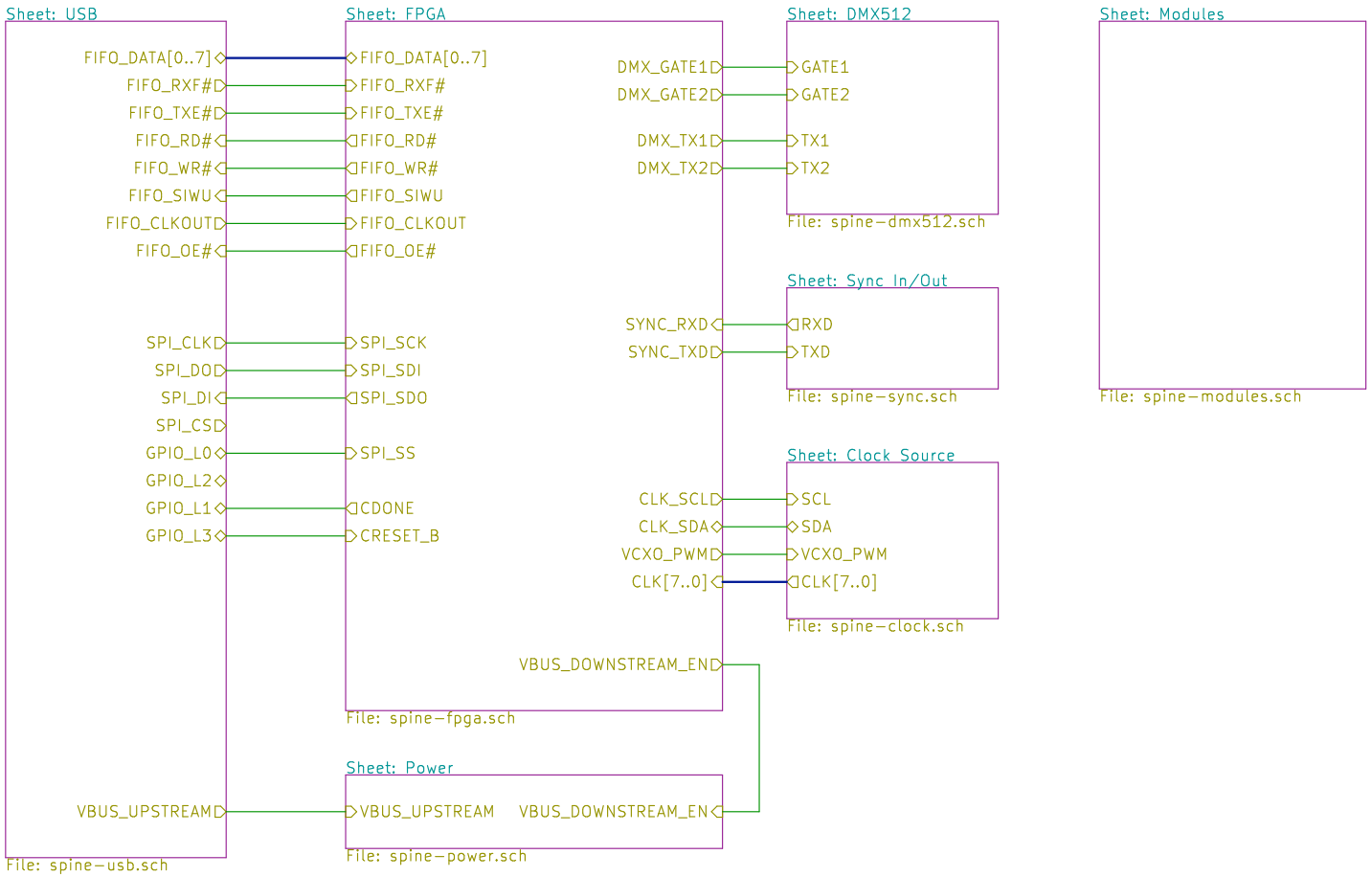


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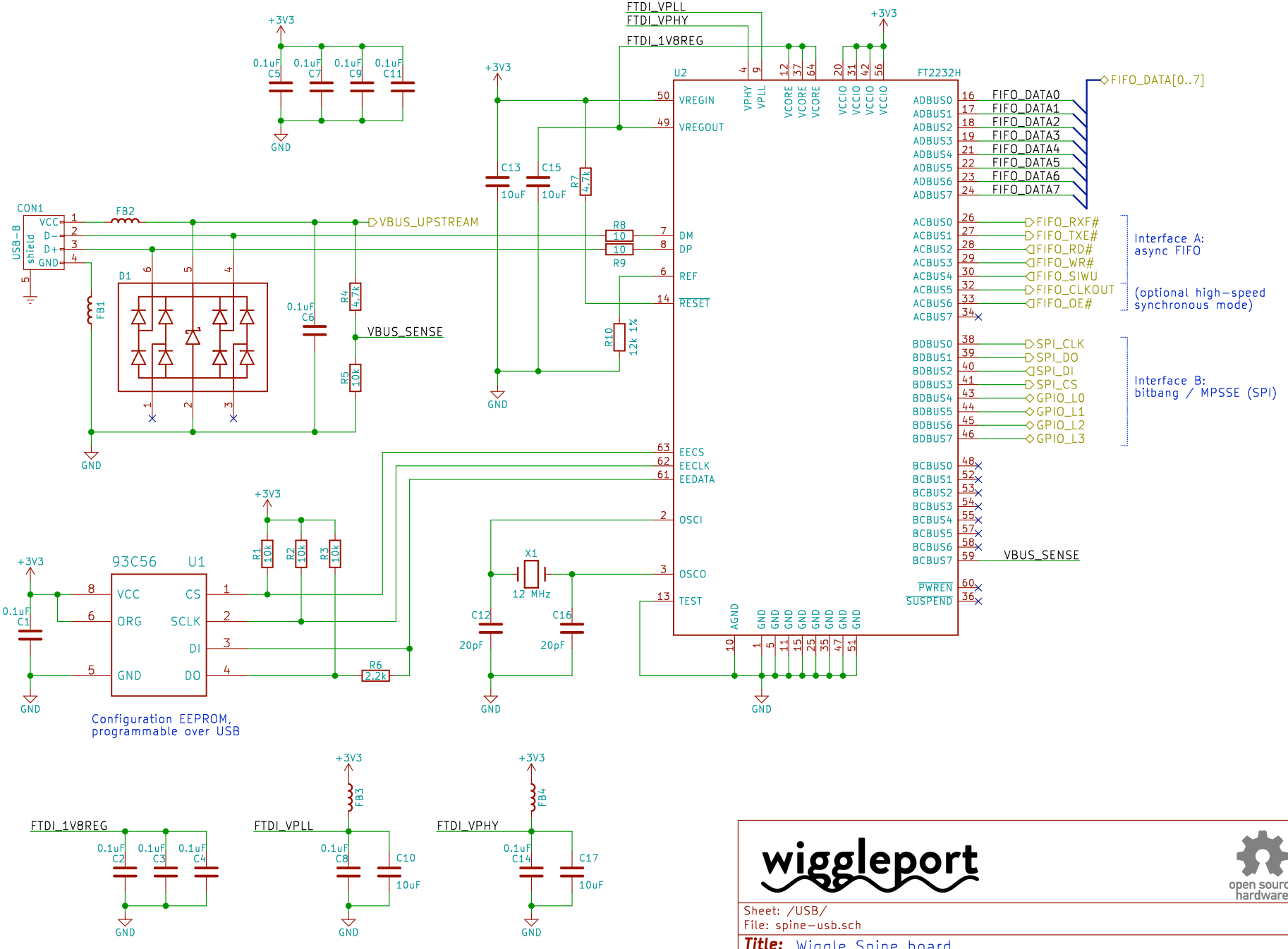
Sheet: /
File: wiggle-spine.sch

**Title:** Wiggle Spine board

| Size: USLetter | Date: | **Rev:** A |
|---|---|---|
| KiCad E.D.A. kicad 4.0.0-rc2-1-stable | | Id: 1/14 |

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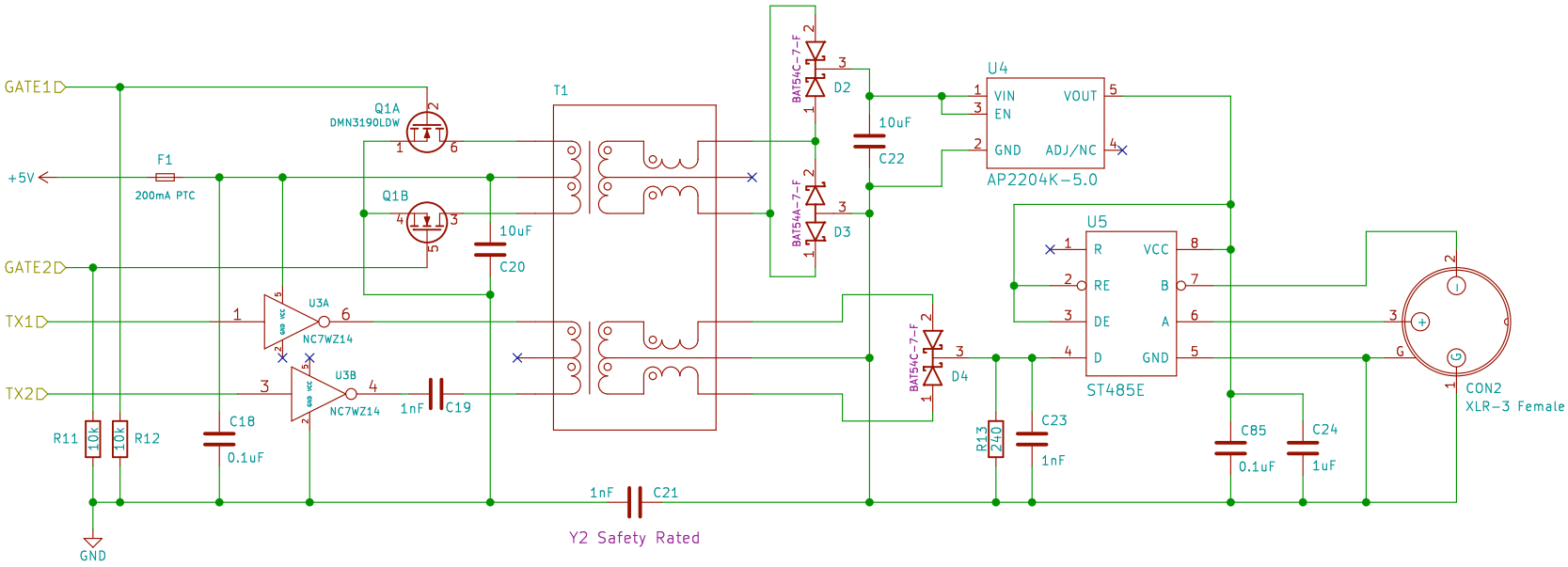
| | |
|---|---|
| Sheet: /USB/ | |
| File: spine-usb.sch | |
| **Title:** Wiggle Spine board | |
| Size: USLetter \| Date: | **Rev:** A |
| KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 2/14 |

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Sheet: /DMX512/
File: spine-dmx512.sch

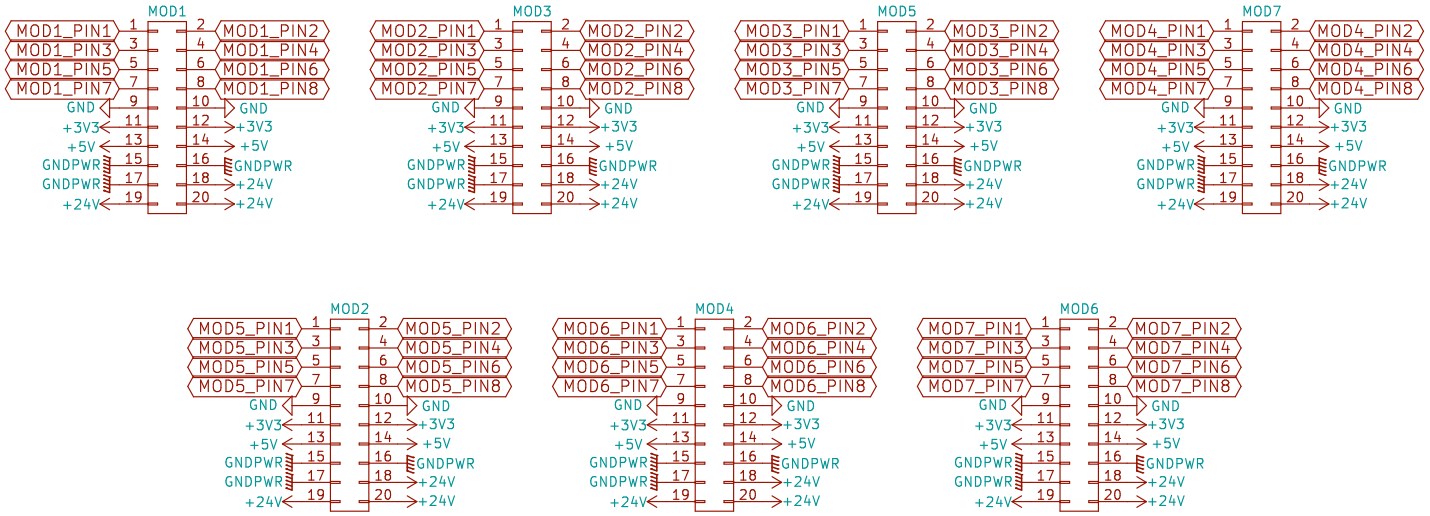
**Title:** Wiggle Spine board

| Size: USLetter | Date: | **Rev:** A |
|---|---|---|
| KiCad E.D.A. kicad 4.0.0-rc2-1-stable | | Id: 3/14 |

8x GPIOs per module (3.3V ONLY)
Limited ESD protection (2kV HBM) on each I/O.

3.3v and 5v supplied by system DC/DC converters.
At least 100mA available per module.

24v rail is actually 5–24v, up to 4A per module.

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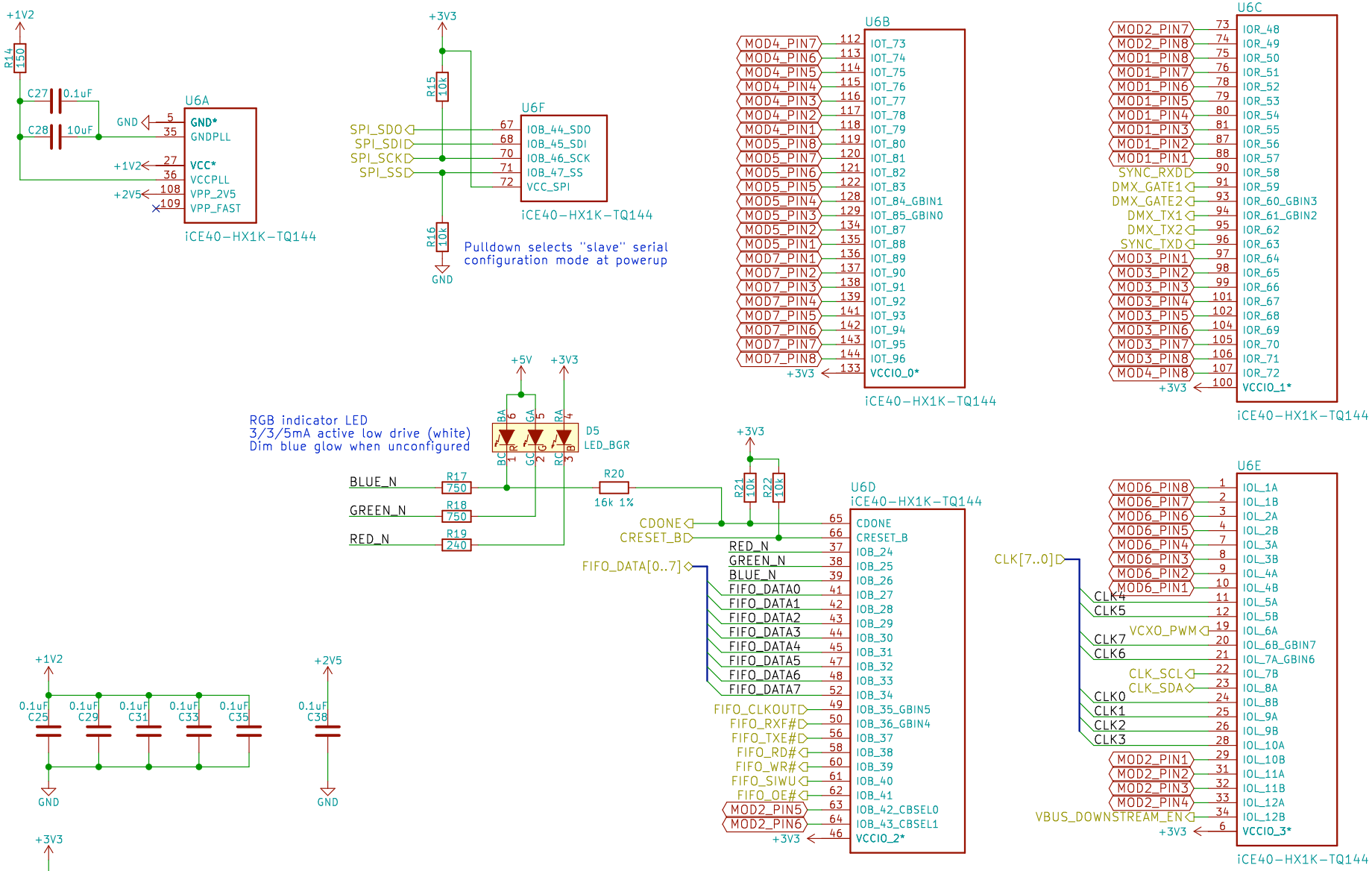
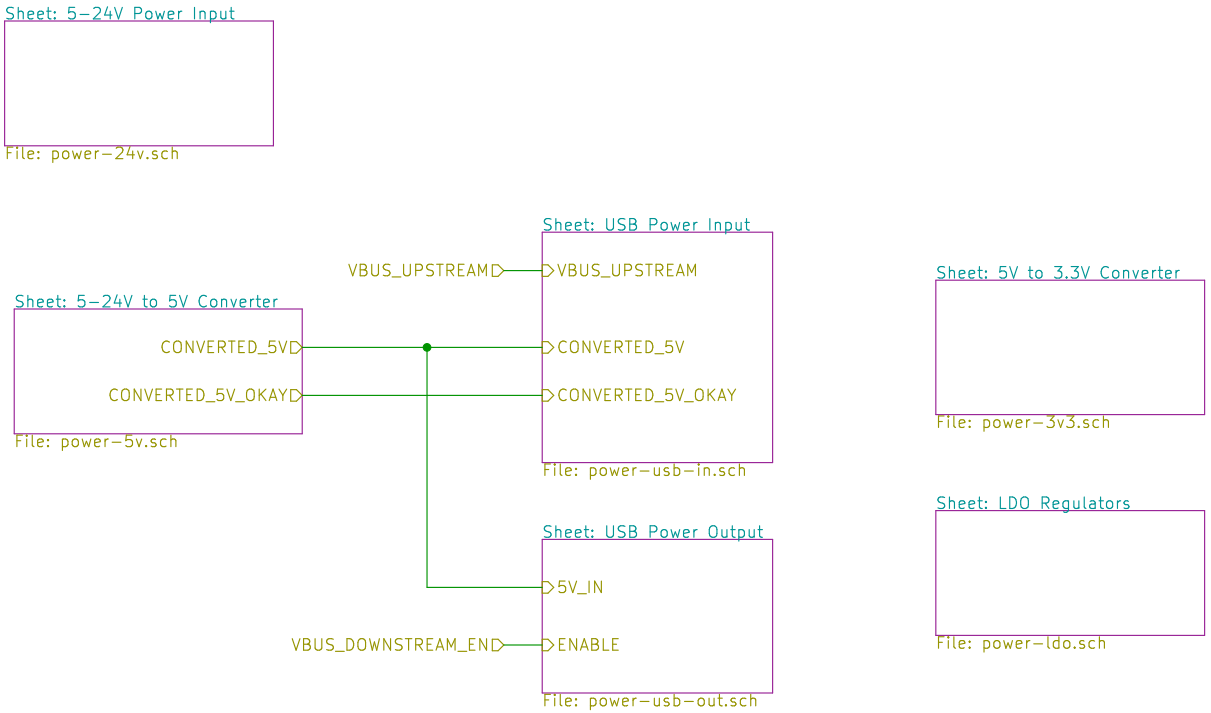
Sheet: /Modules/
File: spine-modules.sch

**Title:** Wiggle Spine board

| Size: USLetter | Date: | **Rev:** A |
|---|---|---|
| KiCad E.D.A. kicad 4.0.0-rc2-1-stable | | Id: 4/14 |


+1V2
R14 150
C27 0.1uF
C28 10uF
GND
U6A
GND*
GNDPLL
VCC*
VCCPLL
VPP_2V5
VPP_FAST
iCE40-HX1K-TQ144
+3V3
R15 10k
R16 10k
SPI_SDO
SPI_SDI
SPI_SCK
SPI_SS
U6F
IOB_44_SDO
IOB_45_SDI
IOB_46_SCK
IOB_47_SS
VCC_SPI
iCE40-HX1K-TQ144
Pulldown selects "slave" serial configuration mode at powerup
U6B
MOD4_PIN7
MOD4_PIN6
MOD4_PIN5
MOD4_PIN4
MOD4_PIN3
MOD4_PIN2
MOD4_PIN1
MOD5_PIN8
MOD5_PIN7
MOD5_PIN6
MOD5_PIN5
MOD5_PIN4
MOD5_PIN3
MOD5_PIN2
MOD5_PIN1
MOD7_PIN1
MOD7_PIN2
MOD7_PIN3
MOD7_PIN4
MOD7_PIN5
MOD7_PIN6
MOD7_PIN7
MOD7_PIN8
IOT_73
IOT_74
IOT_75
IOT_76
IOT_77
IOT_78
IOT_79
IOT_80
IOT_81
IOT_82
IOT_83
IOT_84_GBIN1
IOT_85_GBIN0
IOT_87
IOT_88
IOT_89
IOT_90
IOT_91
IOT_92
IOT_93
IOT_94
IOT_95
IOT_96
VCCIO_0*
iCE40-HX1K-TQ144
U6C
MOD2_PIN7
MOD2_PIN8
MOD1_PIN8
MOD1_PIN7
MOD1_PIN6
MOD1_PIN5
MOD1_PIN4
MOD1_PIN3
MOD1_PIN2
MOD1_PIN1
SYNC_RXD
DMX_GATE1
DMX_GATE2
DMX_TX1
DMX_TX2
SYNC_TXD
MOD3_PIN1
MOD3_PIN2
MOD3_PIN3
MOD3_PIN4
MOD3_PIN5
MOD3_PIN6
MOD3_PIN7
MOD3_PIN8
MOD4_PIN8
IOR_48
IOR_49
IOR_50
IOR_51
IOR_52
IOR_53
IOR_54
IOR_55
IOR_56
IOR_57
IOR_58
IOR_59
IOR_60_GBIN3
IOR_61_GBIN2
IOR_62
IOR_63
IOR_64
IOR_65
IOR_66
IOR_67
IOR_68
IOR_69
IOR_70
IOR_71
IOR_72
VCCIO_1*
iCE40-HX1K-TQ144
+5V
+3V3
RGB indicator LED
3/3/5mA active low drive (white)
Dim blue glow when unconfigured
D5
LED_BGR
BLUE_N
GREEN_N
RED_N
R17 750
R18 750
R19 240
R20 16k 1%
R21 10k
R22 10k
U6D
iCE40-HX1K-TQ144
CDONE
CRESET_B
FIFO_DATA[0..7]
FIFO_DATA0
FIFO_DATA1
FIFO_DATA2
FIFO_DATA3
FIFO_DATA4
FIFO_DATA5
FIFO_DATA6
FIFO_DATA7
FIFO_CLKOUT
FIFO_RXF#
FIFO_TXE#
FIFO_RD#
FIFO_WR#
FIFO_SIWU
FIFO_OE#
MOD2_PIN5
MOD2_PIN6
IOB_24
IOB_25
IOB_26
IOB_27
IOB_28
IOB_29
IOB_30
IOB_31
IOB_32
IOB_33
IOB_34
IOB_35_GBIN5
IOB_36_GBIN4
IOB_37
IOB_38
IOB_39
IOB_40
IOB_41
IOB_42_CBSEL0
IOB_43_CBSEL1
VCCIO_2*
U6E
CLK[7..0]
MOD6_PIN8
MOD6_PIN7
MOD6_PIN6
MOD6_PIN5
MOD6_PIN4
MOD6_PIN3
MOD6_PIN2
MOD6_PIN1
CLK4
CLK5
VCXO_PWM
CLK7
CLK6
CLK_SCL
CLK_SDA
CLK0
CLK1
CLK2
CLK3
MOD2_PIN1
MOD2_PIN2
MOD2_PIN3
MOD2_PIN4
VBUS_DOWNSTREAM_EN
IOL_1A
IOL_1B
IOL_2A
IOL_2B
IOL_3A
IOL_3B
IOL_4A
IOL_4B
IOL_5A
IOL_5B
IOL_6A
IOL_6B_GBIN7
IOL_7A_GBIN6
IOL_7B
IOL_8A
IOL_8B
IOL_9A
IOL_9B
IOL_10A
IOL_10B
IOL_11A
IOL_11B
IOL_12A
IOL_12B
VCCIO_3*
iCE40-HX1K-TQ144
+1V2
+2V5
+3V3
C25 0.1uF
C29 0.1uF
C31 0.1uF
C33 0.1uF
C35 0.1uF
C38 0.1uF
C26 0.1uF
C30 0.1uF
C32 0.1uF
C34 0.1uF
C36 0.1uF
C37 0.1uF
C39 0.1uF
C40 0.1uF
C41 0.1uF
C42 0.1uF
GND
wiggleport
open source hardware
Sheet: /FPGA/
File: spine-fpga.sch
Title: Wiggle Spine board
Size: USLetter
Date:
Rev: A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable
Id: 5/14

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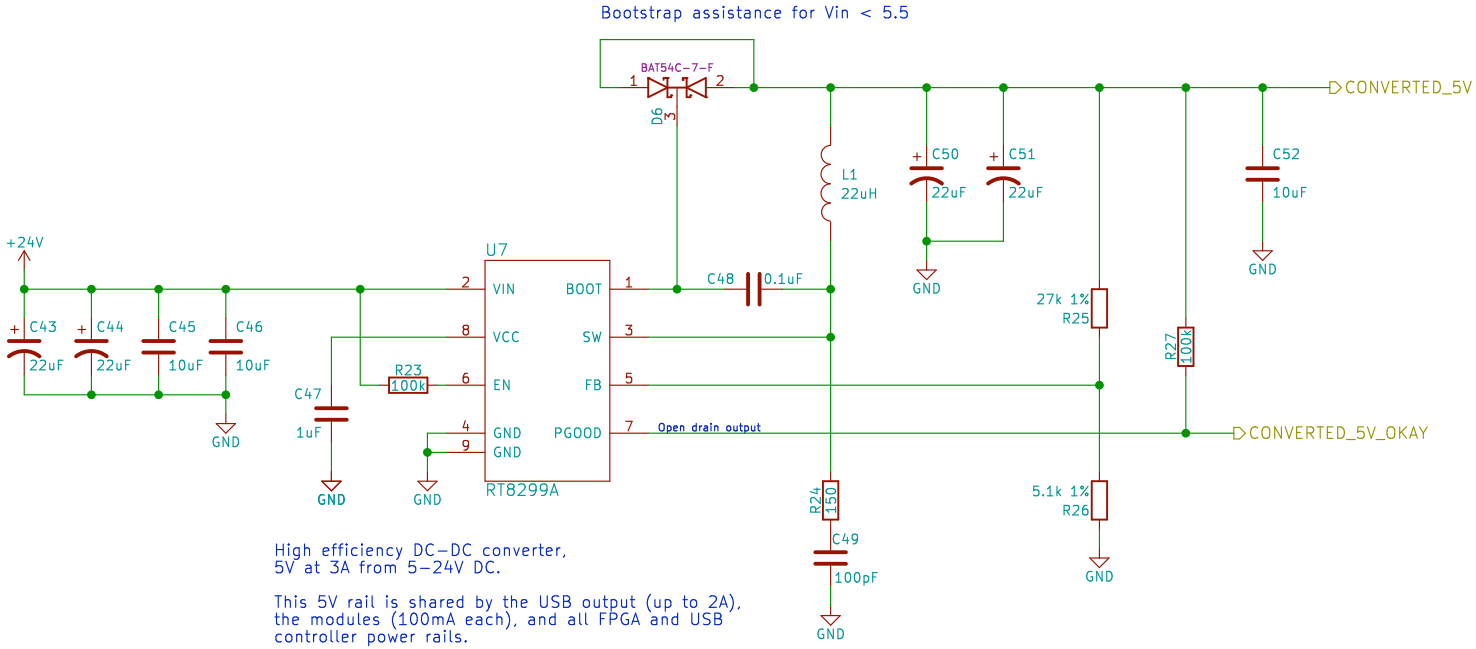
open source hardware

Sheet: /Power/
File: spine–power.sch

**Title:** Wiggle Spine board

| Size: USLetter | Date: | **Rev:** A |
|---|---|---|
| KiCad E.D.A. kicad 4.0.0–rc2–1–stable | | Id: 6/14 |

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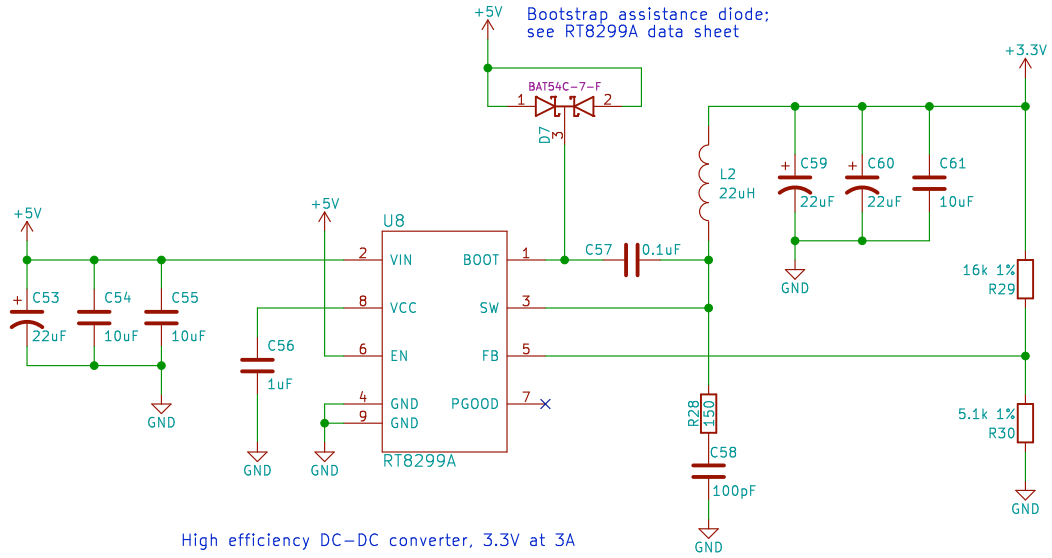
open source hardware

Sheet: /Power/5-24V to 5V Converter/
File: power-5v.sch

**Title:** Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 7/14

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Sheet: /Power/5V to 3.3V Converter/
File: power-3v3.sch

**Title:** Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

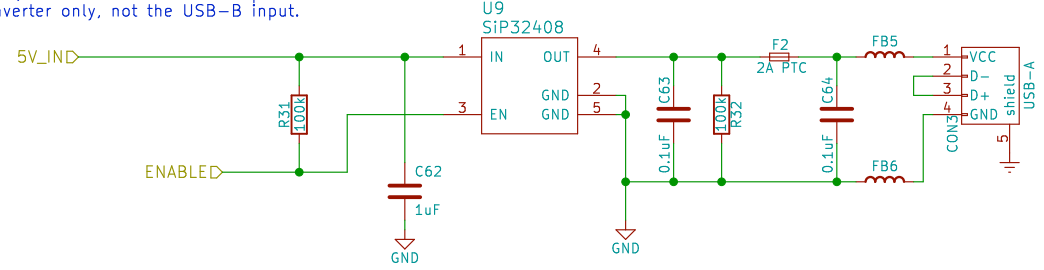
KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 8/14

USB power output, 5V 2A.

Intended to power a small computer,
like the Raspberry Pi 2.

Optional hardware watchdog timer,
implemented in the FPGA.

Not the main +5V rail; this is intended to draw power
from the DC-DC converter only, not the USB-B input.

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Sheet: /Power/USB Power Output/
File: power-usb-out.sch

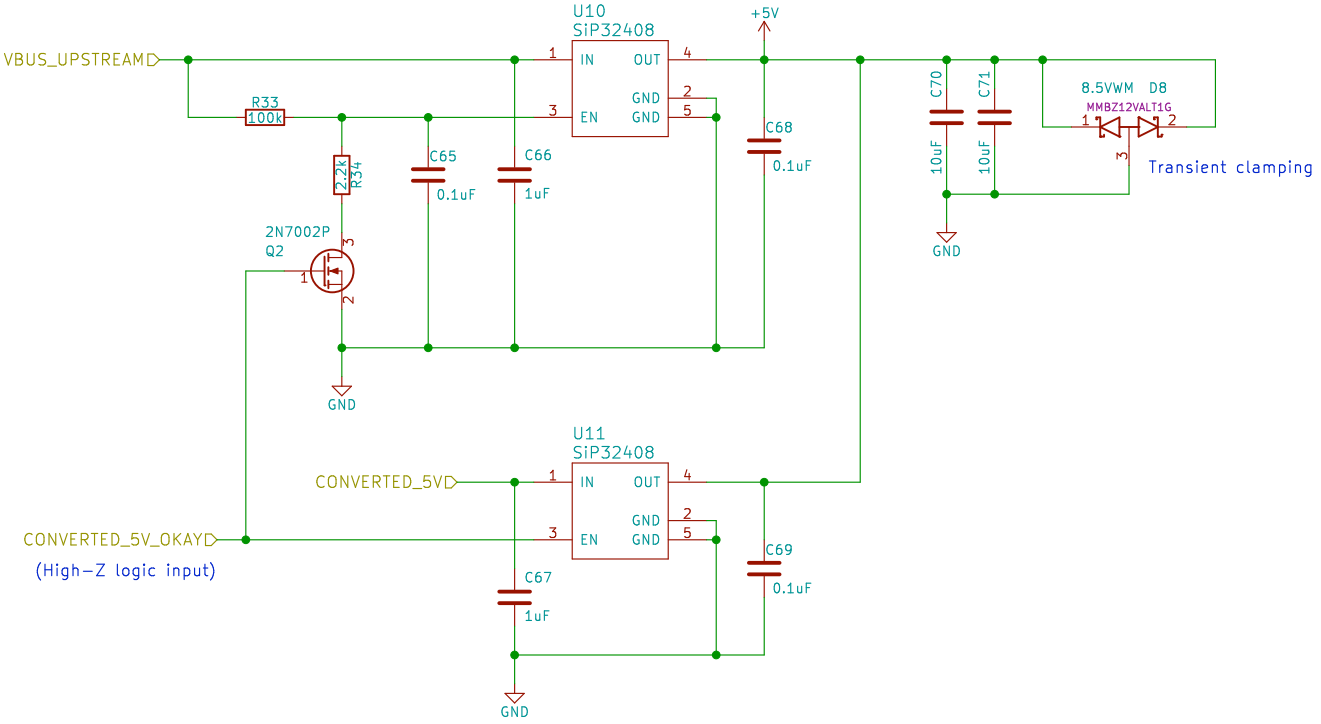
**Title:** Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 9/14

When USB power is available, route it to the +5V rail
(with reverse current protection)

When/if external 5V becomes available, switch to it
softly, then draw no power from upstream USB.

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Sheet: /Power/USB Power Input/
File: power-usb-in.sch

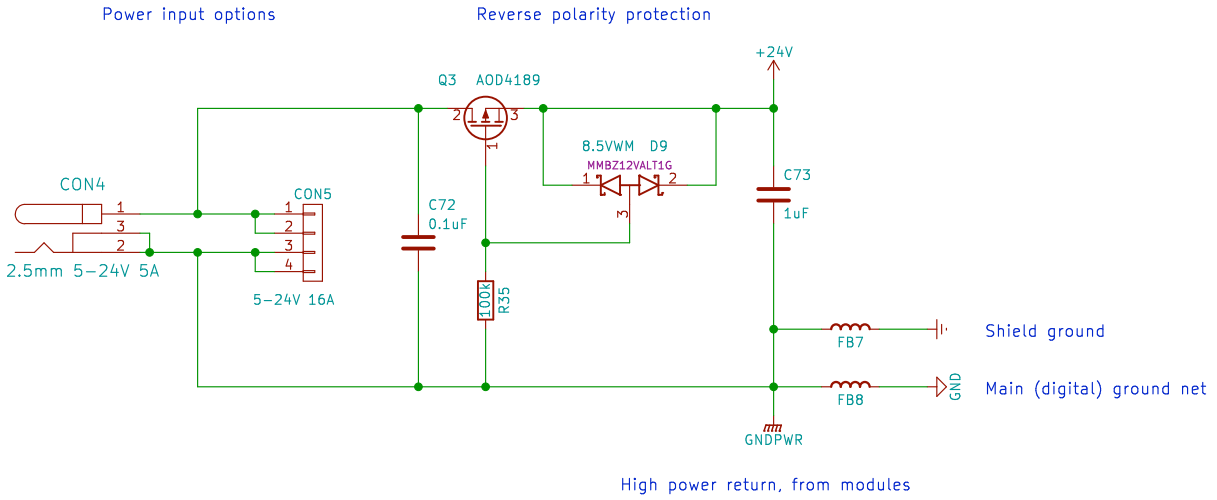
**Title:** Wiggle Spine board

Size: USLetter | Date:

**Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable

Id: 10/14

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Sheet: /Power/5-24V Power Input/
File: power-24v.sch

**Title:** Wiggle Spine board

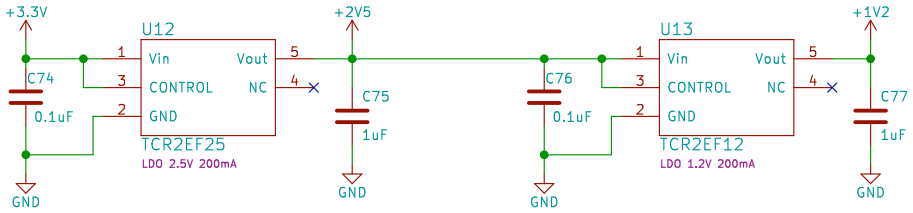
| Size: USLetter | Date: | **Rev:** A |
|---|---|---|
| KiCad E.D.A. kicad 4.0.0-rc2-1-stable | | Id: 11/14 |

Low voltage / low current
LDO regulators for FPGA

2.5v = FPGA NVCM programming voltage

(Some circuits approximate this with a diode drop from 3.3v, but that's pretty dirty and these LDOs are about as cheap as a diode.)

1.2v = FPGA core voltage

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Sheet: /Power/LDO Regulators/
File: power-ldo.sch

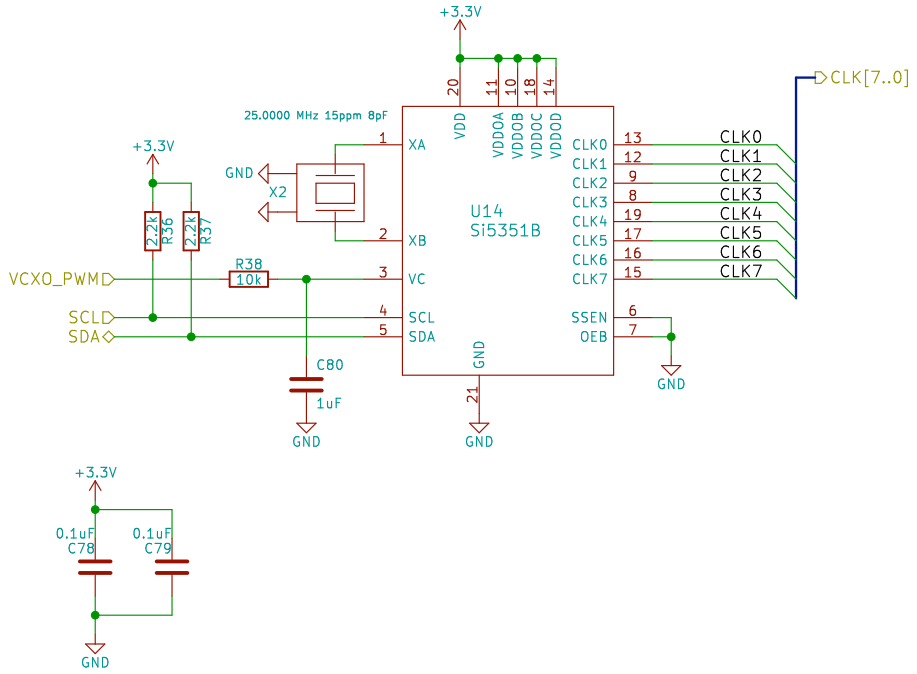
**Title:** Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 12/14

Programmable clock synthesizer

Includes analog VCXO, used to synthesize stable local clocks that match the rate of another Spine unit.

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Sheet: /Clock Source/
File: spine-clock.sch

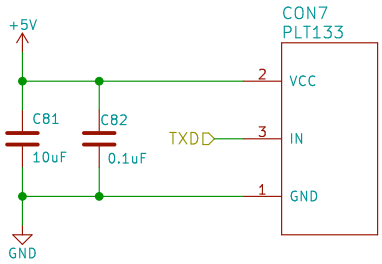
**Title:** Wiggle Spine board

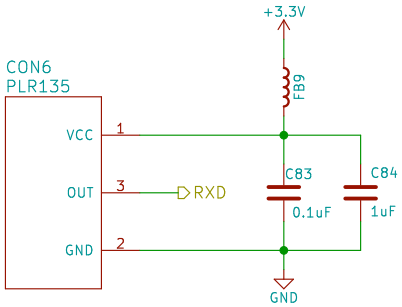
Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 13/14

Sync IN / OUT

Using "TOSLINK" style modules for low jitter, low cost, and galvanic isolation.

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open source hardware

Sheet: /Sync In/Out/
File: spine-sync.sch

**Title:** Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 14/14