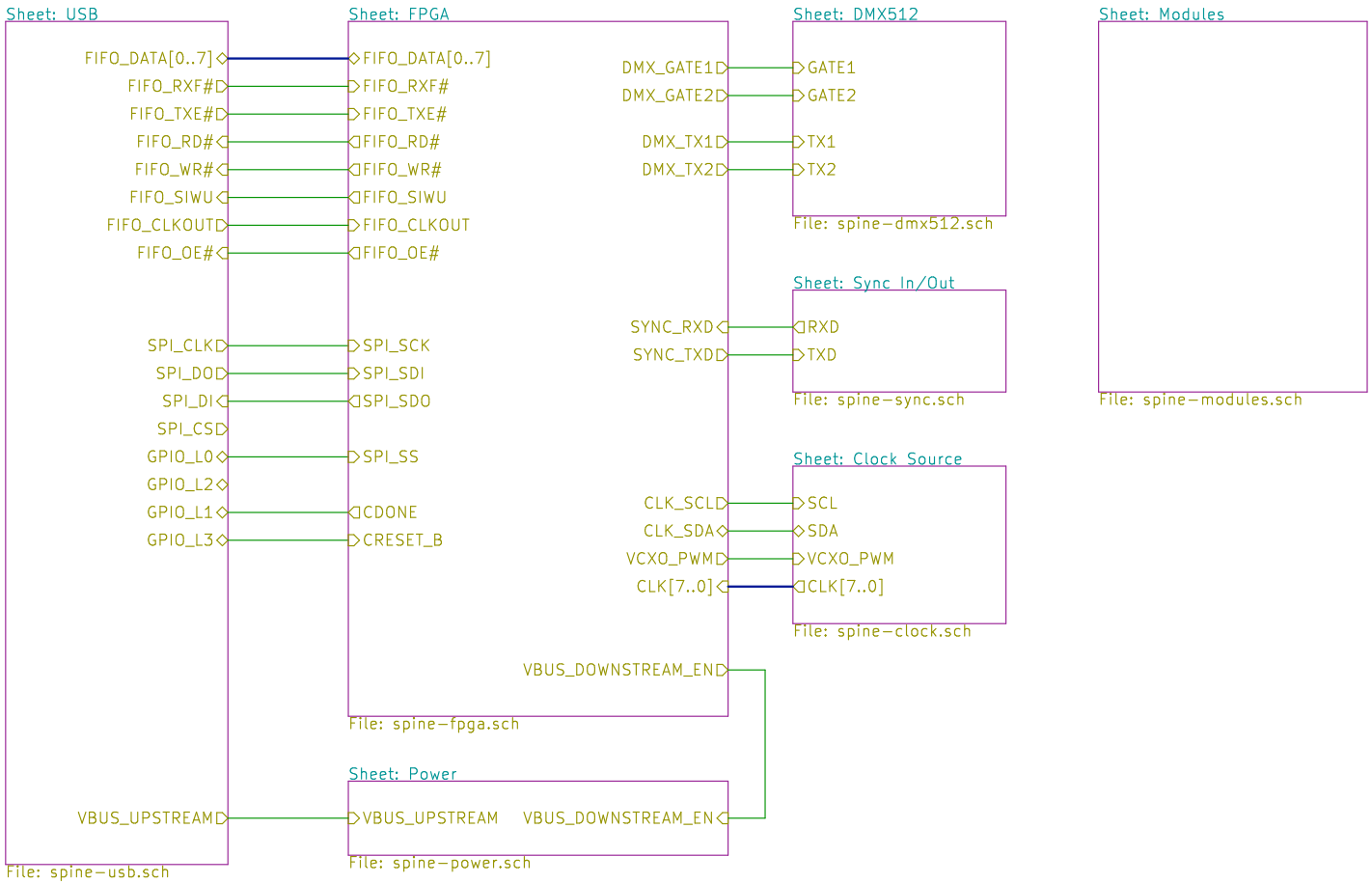


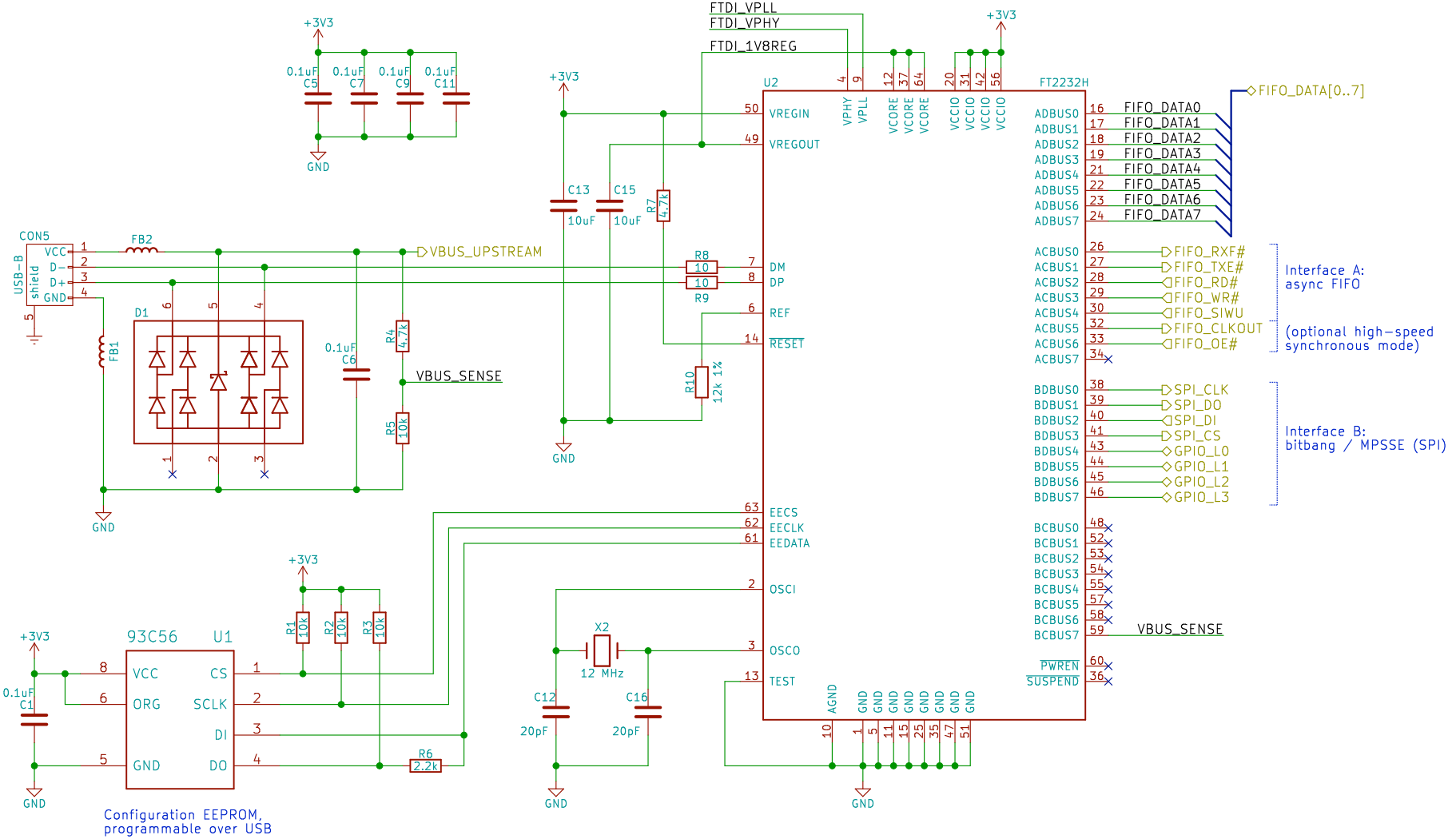
wiggleport

open source hardware

Sheet: /
File: wiggle-spine.sch

Title: Wiggle Spine board

Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable		Id: 1/14



wiggleport

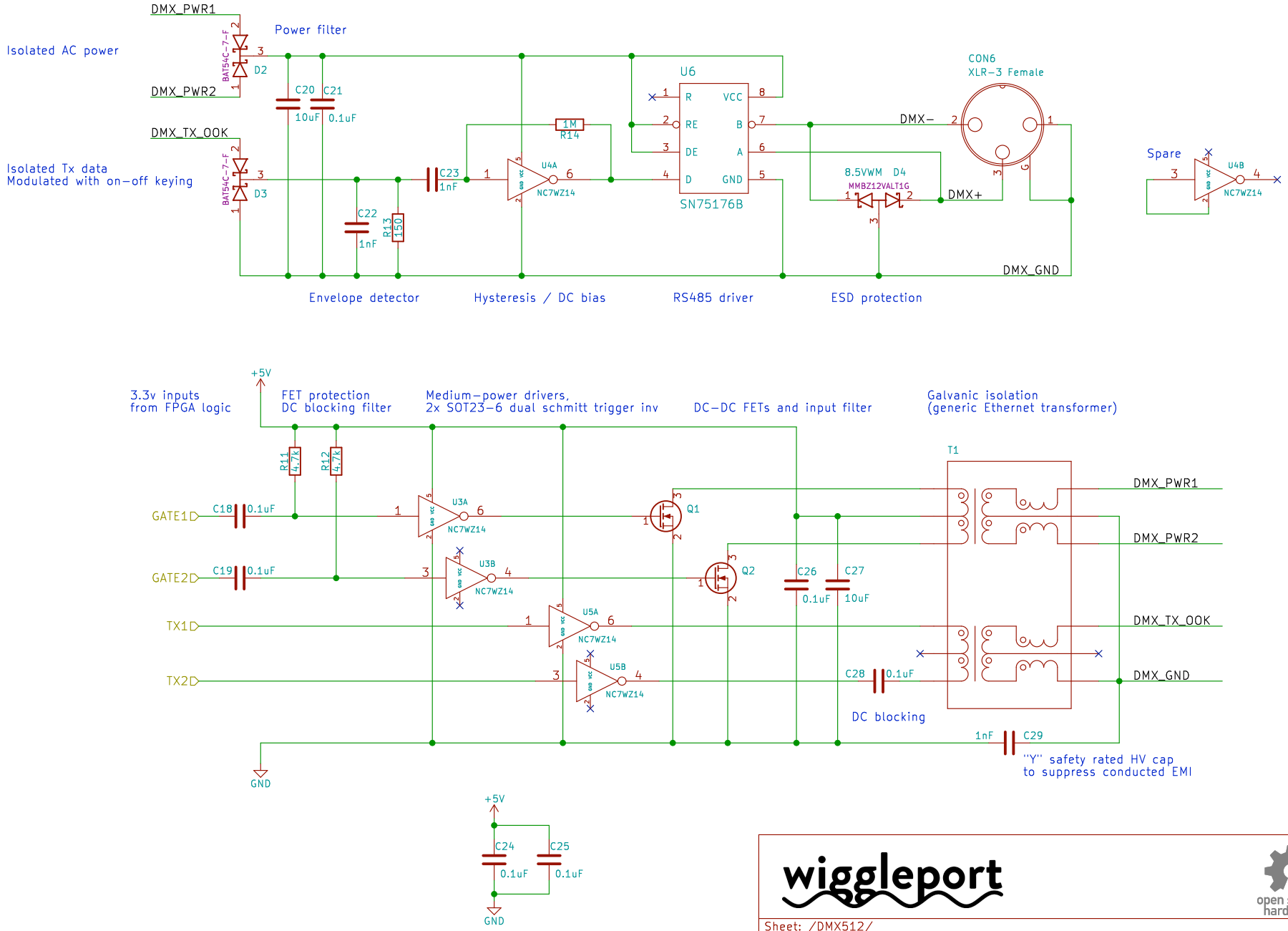
open source hardware

Sheet: /USB/
File: spine-usb.sch

Title: Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 2/14



wiggleport

open source hardware

Sheet: /DMX512/
File: spine-dmx512.sch

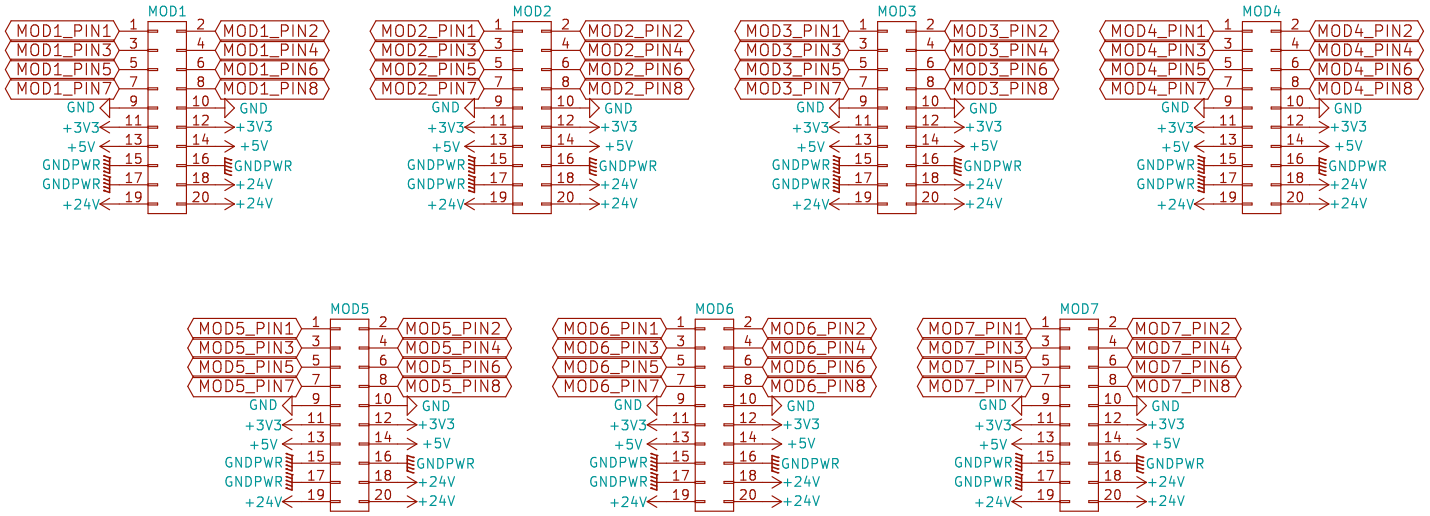
Title: Wiggle Spine board

Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable		Id: 3/14

8x GPIOs per module (3.3V ONLY)
Limited ESD protection (2kV HBM) on each I/O.

3.3v and 5v supplied by system DC/DC converters.
At least 100mA available per module.

24v rail is actually 5–24v, up to 4A per module.



wiggleport

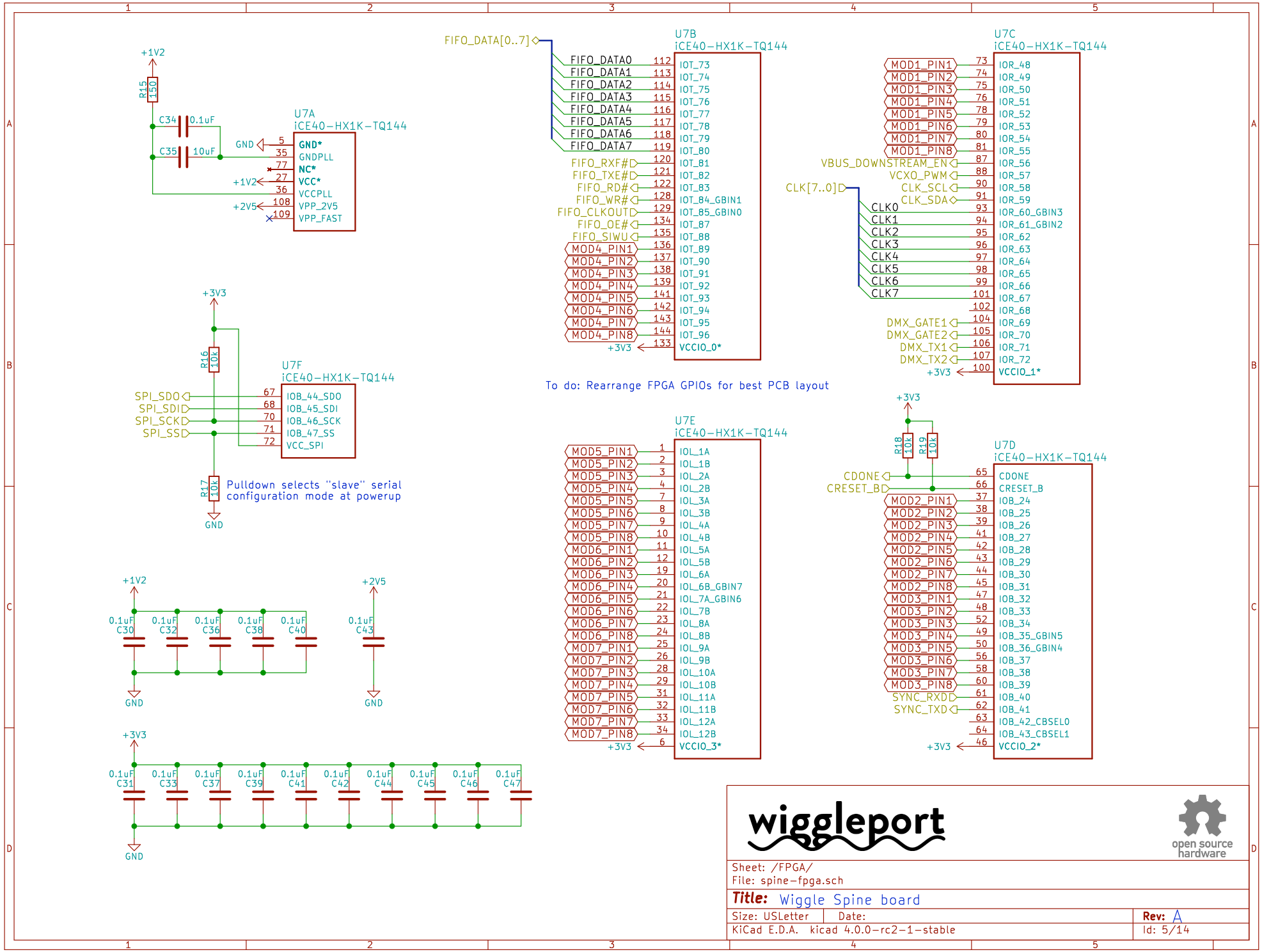
open source hardware

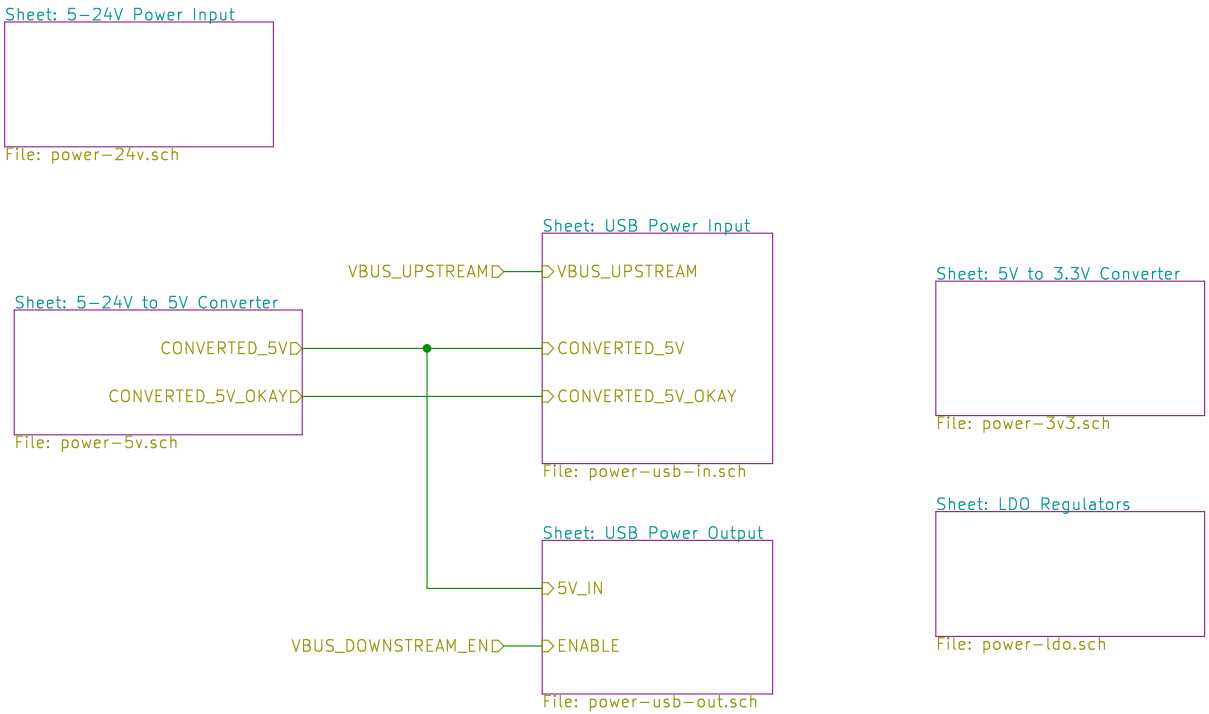
Sheet: /Modules/
File: spine-modules.sch

Title: Wiggle Spine board

Size: USLetter | Date: | **Rev:** A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable | Id: 4/14


+1V2
R15
150
C34
0.1uF
C35
10uF
GND
U7A
iCE40-HX1K-TQ144
5 GND*
35 GNDPLL
77 NC*
27 VCC*
36 VCCPLL
108 VPP_2V5
109 VPP_FAST
+2V5
+3V3
R16
10k
SPI_SDO
SPI_SDI
SPI_SCK
SPI_SS
U7F
iCE40-HX1K-TQ144
67 IOB_44_SDO
68 IOB_45_SDI
70 IOB_46_SCK
71 IOB_47_SS
72 VCC_SPI
R17
10k
Pulldown selects "slave" serial configuration mode at powerup
GND
+1V2
0.1uF C30
0.1uF C32
0.1uF C36
0.1uF C38
0.1uF C40
GND
+2V5
0.1uF C43
GND
+3V3
0.1uF C31
0.1uF C33
0.1uF C37
0.1uF C39
0.1uF C41
0.1uF C42
0.1uF C44
0.1uF C45
0.1uF C46
0.1uF C47
GND
FIFO_DATA[0..7]
U7B
iCE40-HX1K-TQ144
FIFO_DATA0 112 IOT_73
FIFO_DATA1 113 IOT_74
FIFO_DATA2 114 IOT_75
FIFO_DATA3 115 IOT_76
FIFO_DATA4 116 IOT_77
FIFO_DATA5 117 IOT_78
FIFO_DATA6 118 IOT_79
FIFO_DATA7 119 IOT_80
FIFO_RXF# 120 IOT_81
FIFO_TXE# 121 IOT_82
FIFO_RD# 122 IOT_83
FIFO_WR# 128 IOT_84_GBIN1
FIFO_CLKOUT 129 IOT_85_GBIN0
FIFO_OE# 134 IOT_87
FIFO_SIWU 135 IOT_88
MOD4_PIN1 136 IOT_89
MOD4_PIN2 137 IOT_90
MOD4_PIN3 138 IOT_91
MOD4_PIN4 139 IOT_92
MOD4_PIN5 141 IOT_93
MOD4_PIN6 142 IOT_94
MOD4_PIN7 143 IOT_95
MOD4_PIN8 144 IOT_96
+3V3 133 VCCIO_0*
U7C
iCE40-HX1K-TQ144
MOD1_PIN1 73 IOR_48
MOD1_PIN2 74 IOR_49
MOD1_PIN3 75 IOR_50
MOD1_PIN4 76 IOR_51
MOD1_PIN5 78 IOR_52
MOD1_PIN6 79 IOR_53
MOD1_PIN7 80 IOR_54
MOD1_PIN8 81 IOR_55
VBUS_DOWNSTREAM_EN 87 IOR_56
VCXO_PWM 88 IOR_57
CLK_SCL 90 IOR_58
CLK_SDA 91 IOR_59
CLK[7..0]
CLK0 93 IOR_60_GBIN3
CLK1 94 IOR_61_GBIN2
CLK2 95 IOR_62
CLK3 96 IOR_63
CLK4 97 IOR_64
CLK5 98 IOR_65
CLK6 99 IOR_66
CLK7 101 IOR_67
102 IOR_68
DMX_GATE1 104 IOR_69
DMX_GATE2 105 IOR_70
DMX_TX1 106 IOR_71
DMX_TX2 107 IOR_72
+3V3 100 VCCIO_1*
To do: Rearrange FPGA GPIOs for best PCB layout
U7E
iCE40-HX1K-TQ144
MOD5_PIN1 1 IOL_1A
MOD5_PIN2 2 IOL_1B
MOD5_PIN3 3 IOL_2A
MOD5_PIN4 4 IOL_2B
MOD5_PIN5 7 IOL_3A
MOD5_PIN6 8 IOL_3B
MOD5_PIN7 9 IOL_4A
MOD5_PIN8 10 IOL_4B
MOD6_PIN1 11 IOL_5A
MOD6_PIN2 12 IOL_5B
MOD6_PIN3 19 IOL_6A
MOD6_PIN4 20 IOL_6B_GBIN7
MOD6_PIN5 21 IOL_7A_GBIN6
MOD6_PIN6 22 IOL_7B
MOD6_PIN7 23 IOL_8A
MOD6_PIN8 24 IOL_8B
MOD7_PIN1 25 IOL_9A
MOD7_PIN2 26 IOL_9B
MOD7_PIN3 28 IOL_10A
MOD7_PIN4 29 IOL_10B
MOD7_PIN5 31 IOL_11A
MOD7_PIN6 32 IOL_11B
MOD7_PIN7 33 IOL_12A
MOD7_PIN8 34 IOL_12B
+3V3 6 VCCIO_3*
+3V3
R18
10k
R19
10k
CDONE
CRESET_B
U7D
iCE40-HX1K-TQ144
65 CDONE
66 CRESET_B
MOD2_PIN1 37 IOB_24
MOD2_PIN2 38 IOB_25
MOD2_PIN3 39 IOB_26
MOD2_PIN4 41 IOB_27
MOD2_PIN5 42 IOB_28
MOD2_PIN6 43 IOB_29
MOD2_PIN7 44 IOB_30
MOD2_PIN8 45 IOB_31
MOD3_PIN1 47 IOB_32
MOD3_PIN2 48 IOB_33
MOD3_PIN3 52 IOB_34
MOD3_PIN4 49 IOB_35_GBIN5
MOD3_PIN5 50 IOB_36_GBIN4
MOD3_PIN6 56 IOB_37
MOD3_PIN7 58 IOB_38
MOD3_PIN8 60 IOB_39
SYNC_RXD 61 IOB_40
SYNC_TXD 62 IOB_41
63 IOB_42_CBSEL0
64 IOB_43_CBSEL1
+3V3 46 VCCIO_2*
wiggleport
open source hardware
Sheet: /FPGA/
File: spine-fpga.sch
Title: Wiggle Spine board
Size: USLetter
Date:
Rev: A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable
Id: 5/14



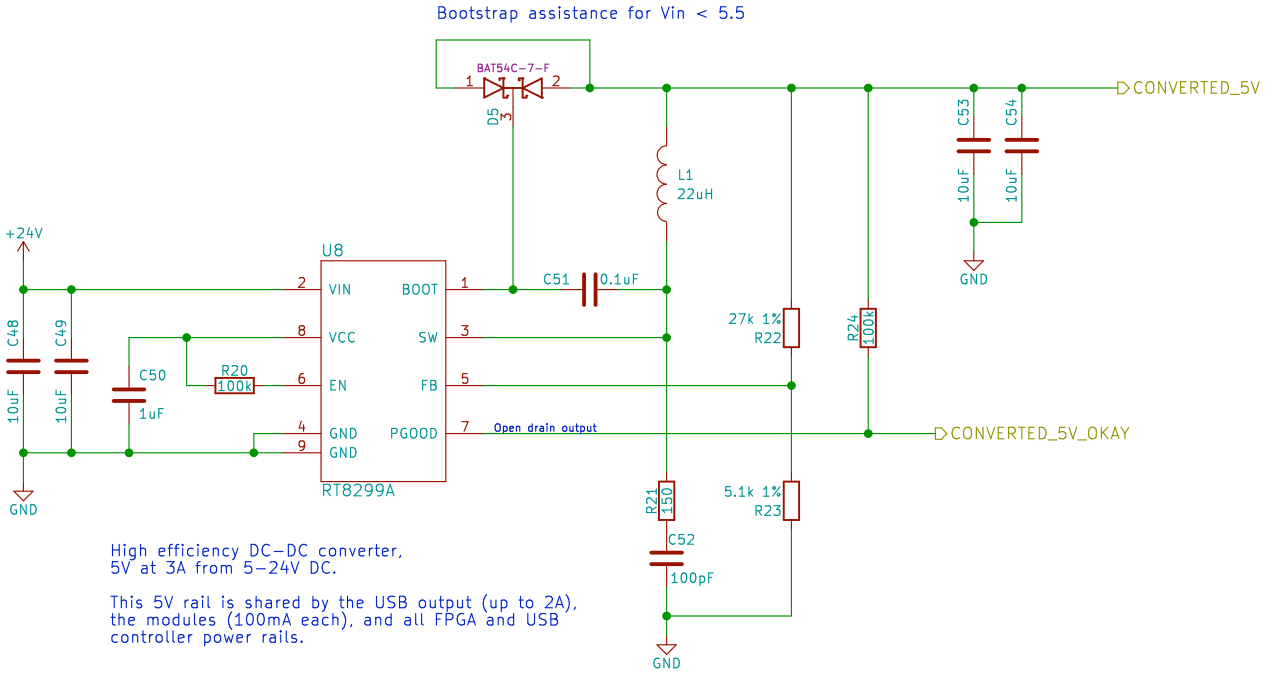
wiggleport

open source hardware

Sheet: /Power/
File: spine–power.sch

Title: Wiggle Spine board

Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0–rc2–1–stable		Id: 6/14



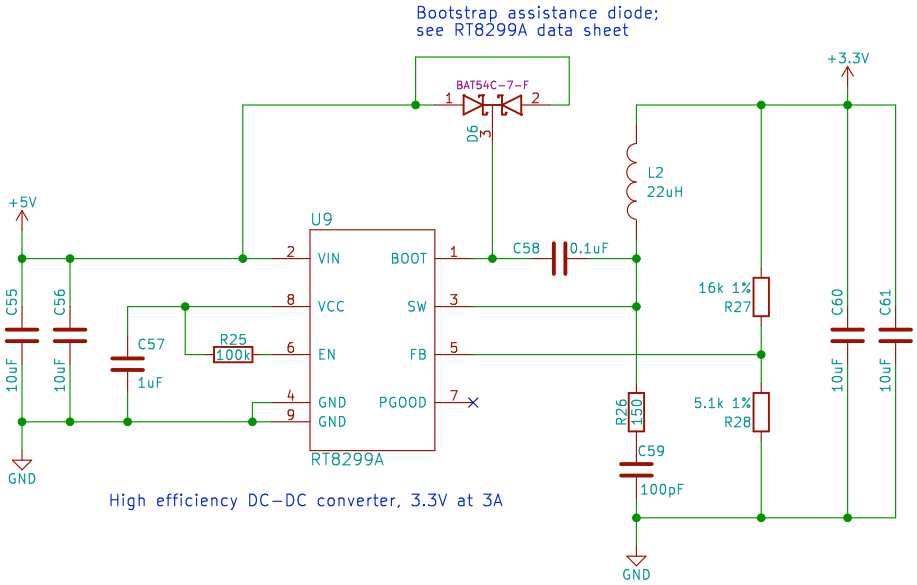
wiggleport

open source hardware

Sheet: /Power/5-24V to 5V Converter/
File: power-5v.sch

Title: Wiggle Spine board

Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable		Id: 7/14



wiggleport

open source hardware

Sheet: /Power/5V to 3.3V Converter/
File: power-3v3.sch

Title: Wiggle Spine board

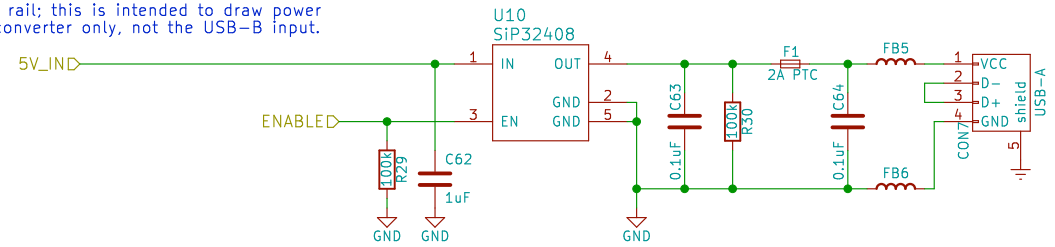
Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable		Id: 8/14

USB power output, 5V 2A.

Intended to power a small computer,
like the Raspberry Pi 2.

Optional hardware watchdog timer,
implemented in the FPGA.

Not the main +5V rail; this is intended to draw power
from the DC-DC converter only, not the USB-B input.



wiggleport

open source hardware

Sheet: /Power/USB Power Output/
File: power-usb-out.sch

Title: Wiggle Spine board

Size: USLetter | Date:

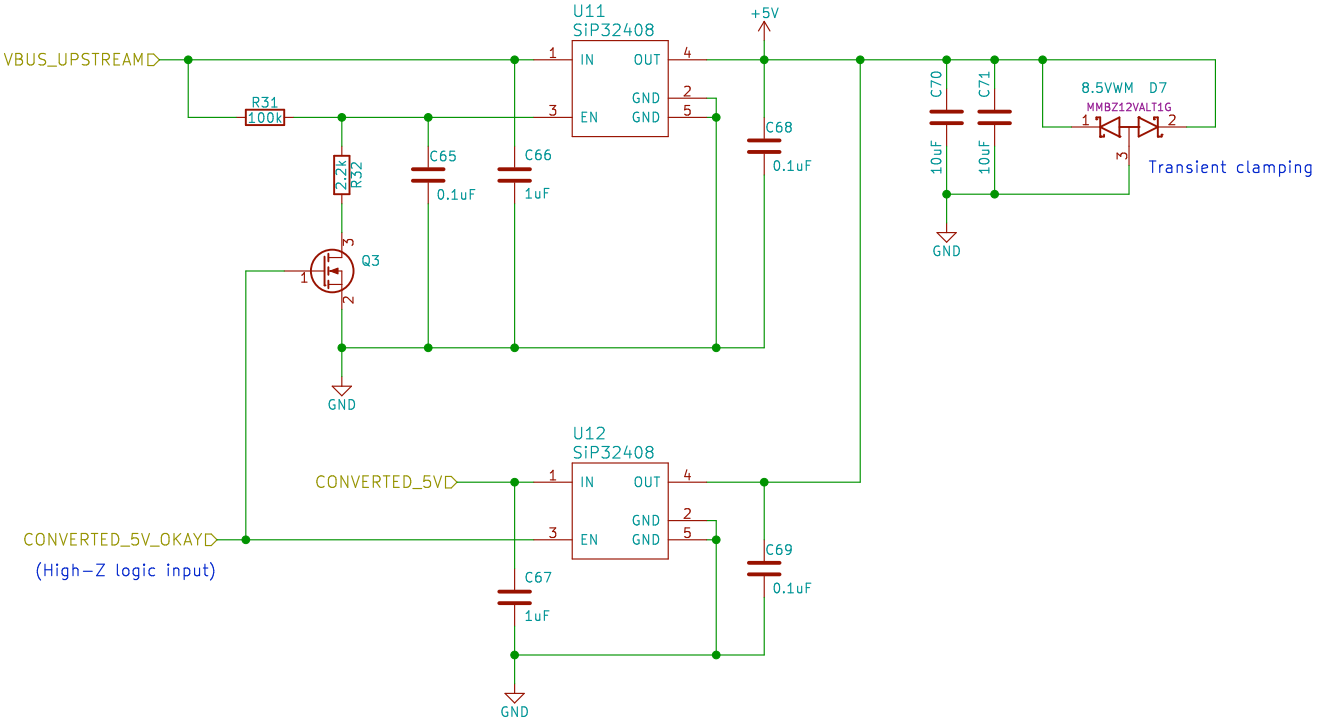
Rev: A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable

Id: 9/14

When USB power is available, route it to the +5V rail
(with reverse current protection)

When/if external 5V becomes available, switch to it
softly, then draw no power from upstream USB.



wiggleport

open source hardware

Sheet: /Power/USB Power Input/
File: power-usb-in.sch

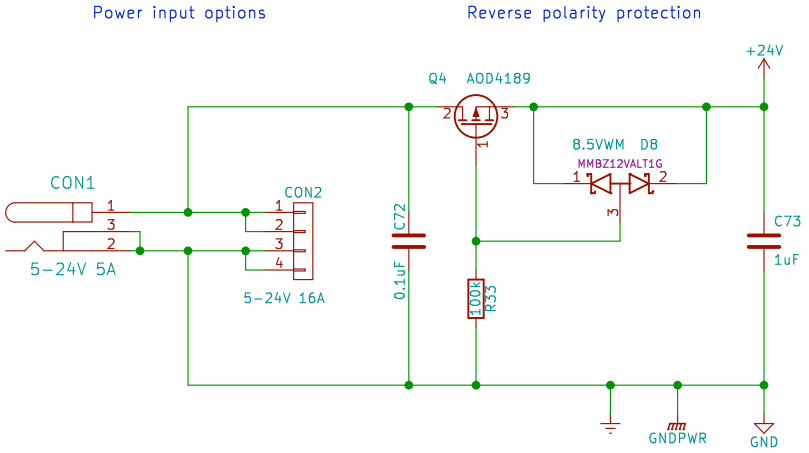
Title: Wiggle Spine board

Size: USLetter | Date:

Rev: A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable

Id: 10/14



wiggleport

open source hardware

Sheet: /Power/5-24V Power Input/
File: power-24v.sch

Title: Wiggle Spine board

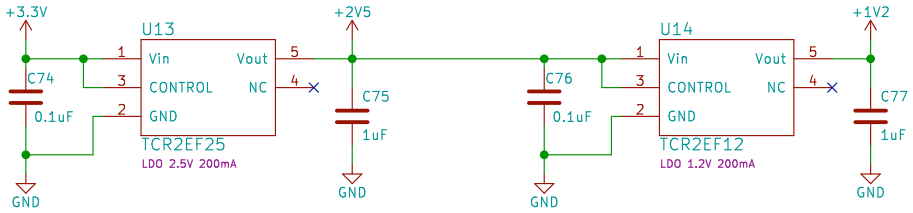
Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable		Id: 11/14

Low voltage / low current
LDO regulators for FPGA

2.5v = FPGA NVCM programming voltage

(Some circuits approximate this with a diode drop from 3.3v, but that's pretty dirty and these LDOs are about as cheap as a diode.)

1.2v = FPGA core voltage



wiggleport

open source hardware

Sheet: /Power/LDO Regulators/
File: power-ldo.sch

Title: Wiggle Spine board

Size: USLetter | Date:

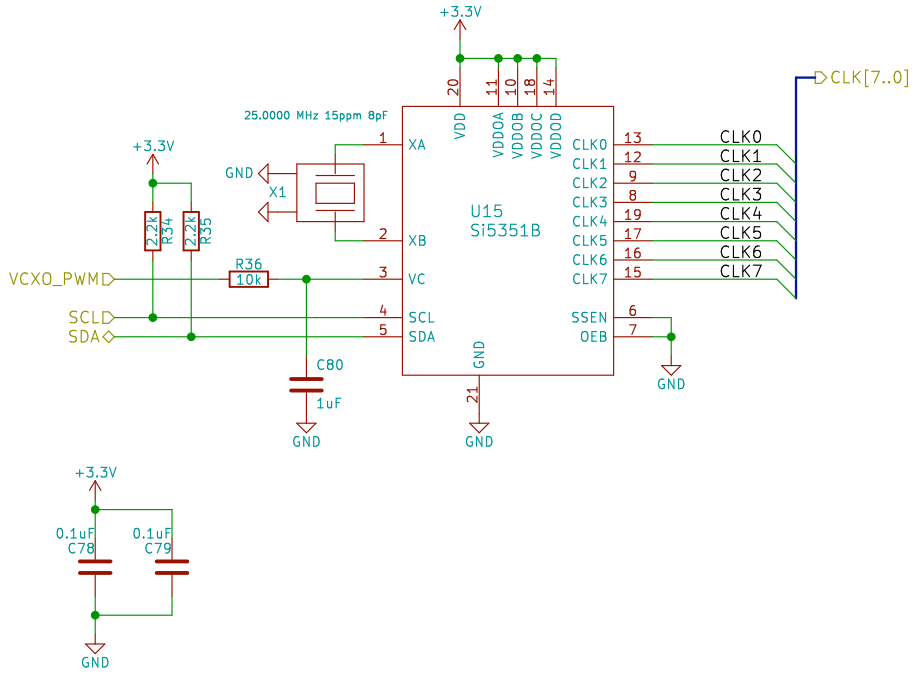
Rev: A

KiCad E.D.A. kicad 4.0.0-rc2-1-stable

Id: 12/14

Programmable clock synthesizer

Includes analog VCXO, used to synthesize stable local clocks that match the rate of another Spine unit.



wiggleport

open source hardware

Sheet: /Clock Source/
File: spine-clock.sch

Title: Wiggle Spine board

Size: USLetter | Date:

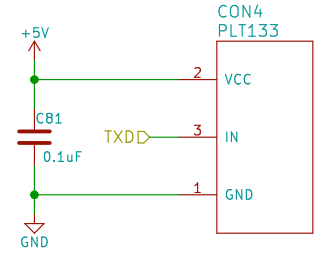
Rev: A

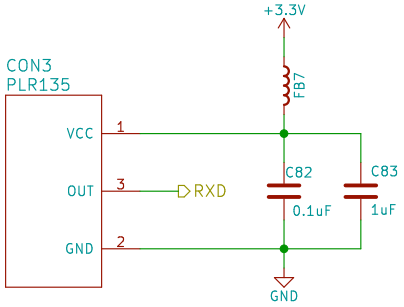
KiCad E.D.A. kicad 4.0.0-rc2-1-stable

Id: 13/14

Sync IN / OUT

Using "TOSLINK" style modules for low jitter, low cost, and galvanic isolation.





wiggleport

open source hardware

Sheet: /Sync In/Out/
File: spine-sync.sch

Title: Wiggle Spine board

Size: USLetter	Date:	**Rev:** A
KiCad E.D.A. kicad 4.0.0-rc2-1-stable		Id: 14/14