浙江大学实验报告

课程名称：计算机体系结构　　实验类型：综合

实验项目名称：Topic 4. Pipelined CPU with Cache

指导教师：何水兵　　完成时间：2023.9.16

姓名	詹含蓓	**学号**	3210106333
同组学生姓名	居圣桐	**学号**	3210105812
分工信息	共同完成		

一、　实验目的和要求

- Understand the principle of Cache Management Unit (CMU) and State Machine of CMU
- Master the design methods of CMU and Integrate it to the CPU.
- Master verification methods of CMU and compare the performance of CPU when it has cache or not.

要求

- Design of Cache Management Unit and integrate it to CPU.
- Observe and Analyze the Waveform of Simulation.
- Compare the performance of CPU when it has cache or not.

二、　实验内容和原理

1. 基于 lab3，可以知道本次实验的地址寻址方式如下：

```
| ----------- address 32 ----------- |
| 31   9 | 8     4 | 3    2 | 1    0 |
| tag 23 | index 5 | word 2 | byte 2 |
```

根据地址，可以计算出某个指令访问的 cache 中的 line 和 set，并且通过判断 tag 来判断是否 hit。

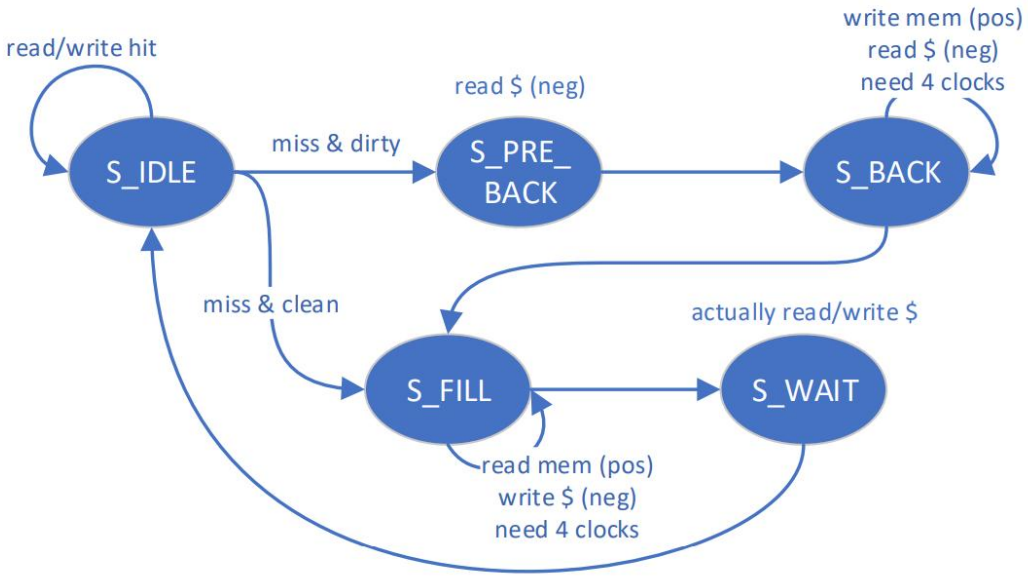
2. Lab4 实验实现了 cache 处理的状态机，状态机如下：

(1) 当 read/write hit 的时候，状态机处于 idle 状态，每次执行一条指令花费一个周期

(2) 当 read/write miss，并且 block 是 dirty 的时候，block 需要写回 memory 当中，此时首先在下降沿进入 pre_back 阶段，之后在进入 back 状态，该状态当中为了模拟读取内存花费的时间，每次读取一个 word 需要花费 4 个 clock，读取四个 word 需要花费 16 个周期。随后进入 fill 状态，即和 clean 相同状态

(3) 当 read/write miss，并且 block 是 clean 的时候，状态机进入 fill 状态。该状态当中为了模拟读取内存花费的时间，每次读取一个 word 需要花费 4 个 clock，读取四个 word 需要花费 16 个周期

(4) 执行完 fill 状态之后进入 wait 状态，进行实际的读写操作，该状态持续一个周期。



三、 实验过程和数据记录及结果分析

（一）实验过程

1. S_IDLE 状态

(1) 判断是否是进行读写操作，并且判断 cache 是否 hit

(2) 如果 hit 则继续 idle 状态，如果 block 有效并且又脏页，则进入 S_PRE_BACK 状态

(3) 如果都不满足则进入 fill 状态填装 cache

```
case (state)
    S_IDLE: begin
        if (en_r || en_w) begin
            if (cache_hit)
                next_state = S_IDLE;
            else if (cache_valid && cache_dirty)
                next_state = S_PRE_BACK;
            else
                next_state = S_FILL;
        end
        next_word_count = 2'b00;
    end
```

2. S_PRE_BACK 状态

(1) 做 S_BACK 状态的准备，并且把 next_word_count 值设置为 0

```
S_PRE_BACK: begin
    next_state = S_BACK;
    next_word_count = 2'b00;
end
```

3. S_BACK 状态

(1) 这里为了模拟 memory 访问速度比访问 cache 更慢，设置了计时器，当经过了四个始终，即 word_count = 2'b11 的时候进入下一状态

```
S_BACK: begin
    if (mem_ack_i && word_count == {ELEMENT_WORDS_WIDTH{1'b1}})    // 2'b11 in default case
        next_state = S_FILL;
    else
        next_state = S_BACK;

    if (mem_ack_i)
        next_word_count = word_count + 1;
    else
        next_word_count = word_count;
end
```

4. S_FILL 状态

(1) 和 S_BACK 状态相同，使用了 word_count 来使得状态机在经过四个周期之后再进入下一个状态，来模拟 memory 访问的延迟

```
S_FILL: begin
    if (mem_ack_i && word_count == {ELEMENT_WORDS_WIDTH{1'b1}})
        next_state = S_WAIT;
    else
        next_state = S_FILL;

    if (mem_ack_i)
        next_word_count = word_count + 1;
    else
        next_word_count = word_count;
end
```

5. S_WAIT 状态

(1) 等待状态，并且将 word_count 清零

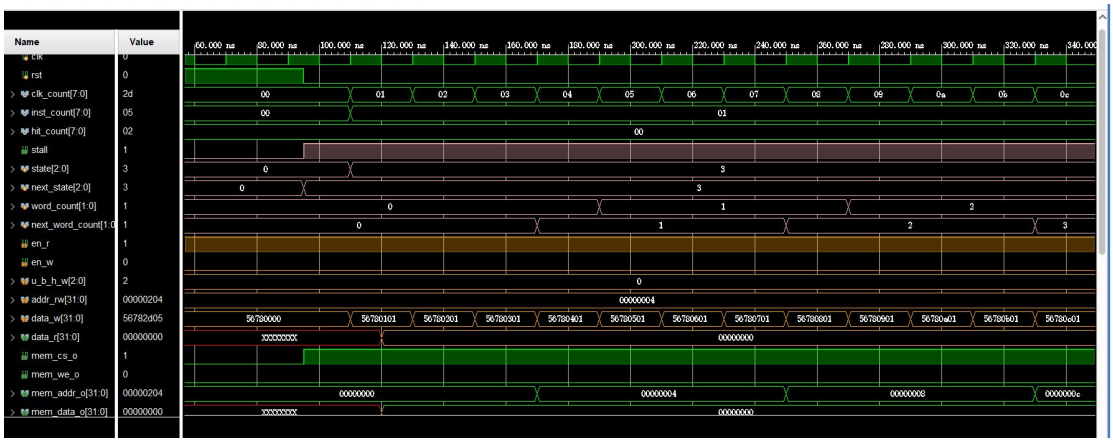
```
    S_WAIT: begin
        next_state = S_IDLE;
        next_word_count = 2'b00;
    end
endcase
```

6. Stall 信号处理

```
assign stall = (next_state != S_IDLE);
```

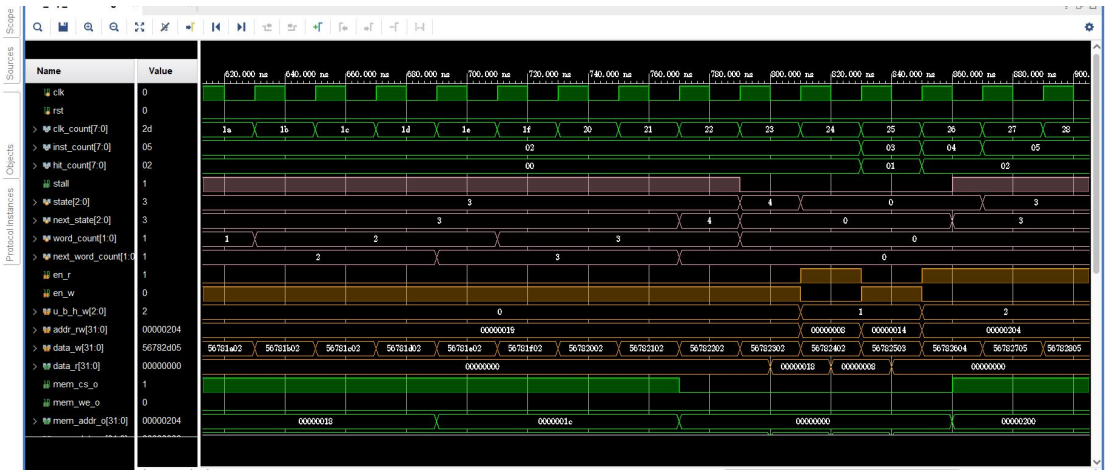
（二）结果分析

1. 在第一条指令发生 read miss 的情况，此时 cache 为空，此时花费周期为 idle 1 + fill 16 + wait 1 = 18 个周期。

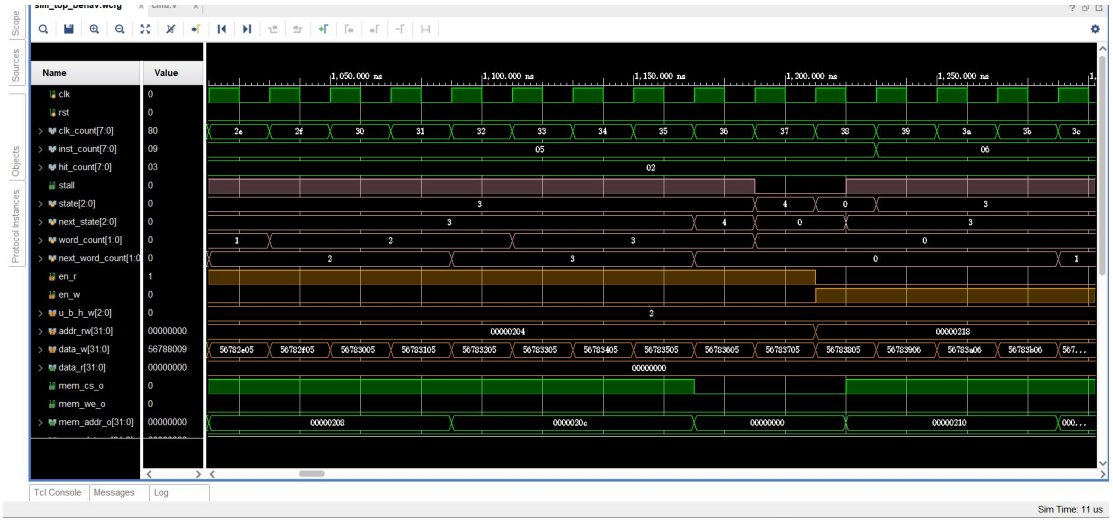


2. 第二条指令发生 write miss，情况和第一条指令相同，需要 18 个周期。

3. 第三，四条指令分别是 read hit 和 write hit，都只需要执行一个周期。

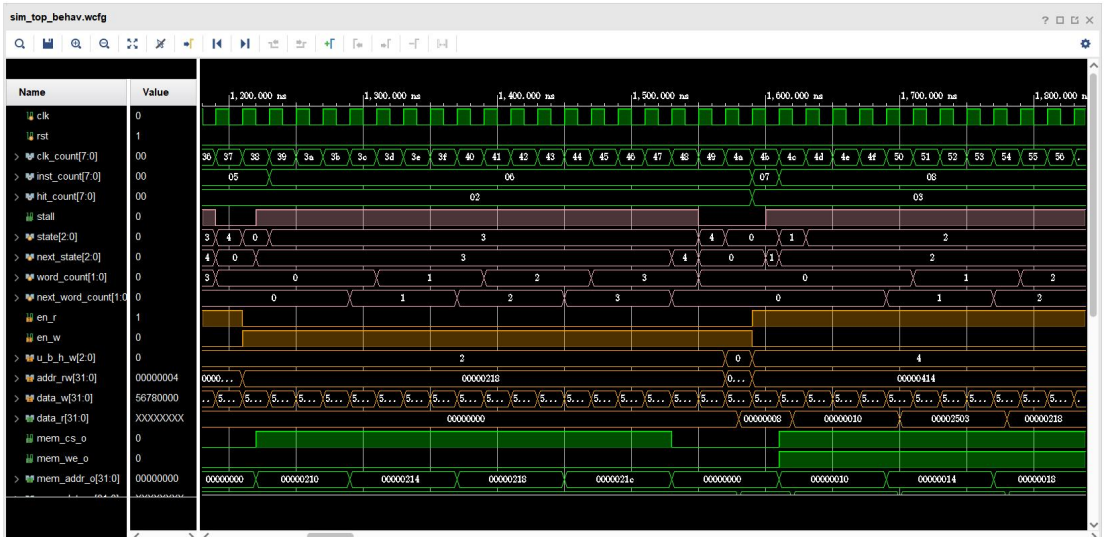


4. 第五条指令发生 read miss，花费周期为 idle 1 + fill 16 + wait 1 = 18 个周期。



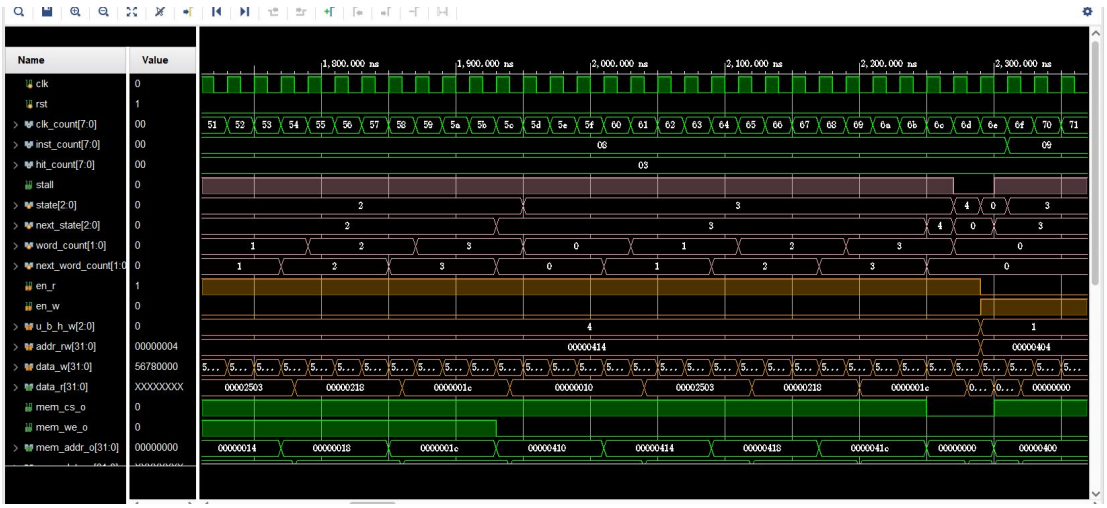
5. 第六条指令发生 write miss，花费周期为 idle 1 + fill 16 + wait 1 = 18 个周期。

6. 第七条指令 write hit，花费一个周期。

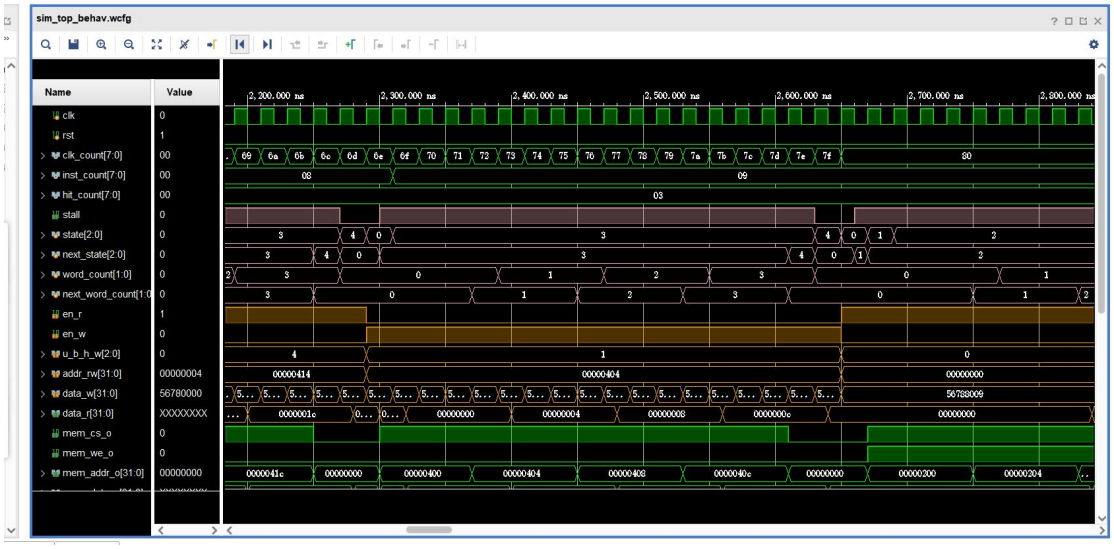


7. 第八条指令发生 read miss，同时需要将脏页面写回，此时花费的周期为 idle 1

+ pre_back 1 + back 16 + fill 16 + wait 1 = 35 个周期。



8. 第六条指令发生 write miss，但是 block 此时为 clean，花费周期为 idle 1 + fill 16 + wait 1 = 18 个周期。



9. 一共花费 128 个周期

（三）实验板验证

在仿真当中以及对代码和相应的周期数进行了很详尽的分析，因此实验板的照片就不做详细分析，主要为证明实验上板成功。


Zhejiang University Computer Organization Experimental
SOC Test Environment (With RISC-V)
x0:zero 00000000 x01: ra ABCDE71C x02: sp 0000001C x03: gp 0000001C
x04: tp 0000001C x05: t0 0000001C x06: t1 00000000 x07: t2 00000000
x8:fps0 00000000 x09: s1 00000000 x10: a0 00000000 x11: a1 00000000
x12: a2 00000000 x13: a3 00000000 x14: a4 00000000 x15: a5 00000000
x16: a6 000000ED x17: a7 00000000 x18: s2 00000000 x19: s3 00000000
x20: s4 00000000 x21: s5 00000000 x22: s6 00000000 x23: s7 00000000
x24: s8 00000000 x25: s9 00000000 x26:s10 00000000 x27:s11 00000000
x28: t3 00000000 x29: t4 00000000 x30: t5 00000000 x31: t6 00000000
PC---IF 00000010 INST-IF 01C04203 rs1Data 00000000 rs2Data 00000000
PC---ID 0000000C INST-ID 01C02183 rs1Addr 00000000 rs2Addr 0000001C
PC---EXE 00000008 INST-EX 01C01103 CMU-RAM 00030003 PCJumpA 0000002B
PC---MEM 00000004 INST-M 01C00083 B/PCE-S 00000000 D/C-Hzd 00000000
PC---WB 00000000 INST-WB 00000013 I/ABSel 00010001 PCIFMxt 00000014
ALU-Ain 00000000 ALU-Bin 0000001C CPUAddr 00000000 ALUCtrl 00000001
ALU-Bin 0000001C WB-Data 00000000 CPU-DAi 00000000 WR--MIO 00000001
Imm32ID 0000001C WB-Addr 00000000 CPU-DAo 00000000 RegW/DR 00010000
CODE-00 00000013 CODE-01 01C00083 CODE-02 01C01103 CODE-03 01C02183
CODE-04 01C04203 CODE-05 01C05283 CODE-06 21002003 CODE-07 ABCDE0B7
CODE-08 71C00893 CODE-09 00100023 CODE-0A 00101223 CODE-0B 00102423
CODE-0C 20002303 CODE-0D 40002383 CODE-0E 41002403 CODE-0F 0ED06813
CODE-10 FFDFF06F CODE-11 00000000 CODE-12 00000000 CODE-13 00000000
CODE-14 00000000 CODE-15 00000000 CODE-16 00000000 CODE-17 00000000
CODE-18 00000000 CODE-19 00000000 CODE-1A 00000000 CODE-1B 00000000
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POWER VOL- VOL+ MENU CH- CH+ MODE


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x16: a6 000000ED x17: a7 00000000 x18: s2 00000000 x19: s3 00000000
x20: s4 00000000 x21: s5 00000000 x22: s6 00000000 x23: s7 00000000
x24: s8 00000000 x25: s9 00000000 x26:s10 00000000 x27:s11 00000000
x28: t3 00000000 x29: t4 00000000 x30: t5 00000000 x31: t6 00000000
PC---IF 00000010 INST-IF 01C04203 rs1Data 00000000 rs2Data 00000000
PC---ID 0000000C INST-ID 01C02183 rs1Addr 00000000 rs2Addr 0000001C
PC---EXE 00000008 INST-EX 01C01103 CMU-RAM 00040000 PCJumpA 0000002B
PC---MEM 00000004 INST-M 01C00083 B/PCE-S 00000100 D/C-Hzd 00000000
PC---WB 00000000 INST-WB 00000013 I/ABSel 00010001 PCIFMxt 00000014
ALU-Ain 00000000 ALU-Bin 0000001C CPUAddr 00000000 ALUCtrl 00000001
ALU-Bin 0000001C WB-Data 00000000 CPU-DAi 0000001C WR--MIO 00000001
Imm32ID 0000001C WB-Addr 00000000 CPU-DAo 00000000 RegW/DR 00010000
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x28: t3 00000000 x29: t4 00000000 x30: t5 00000000 x31: t6 00000000
PC---IF 00000020 INST-IF 71C00893 rs1Data 00000000 rs2Data 00000000
PC---ID 0000001C INST-ID ABCDE0B7 rs1Addr 0000001D rs2Addr 0000001C
PC---EXE 00000018 INST-EX 21002003 CMU-RAM 00000000 PCJumpA ABCDE01C
PC---MEM 00000014 INST-M 01C05283 B/PCE-S 00000100 D/C-Hzd 00000000
PC---WB 00000010 INST-WB 01C04203 I/ABSel 00054001 PCIFMxt 00000024
ALU-Ain 00000000 ALU-Bin 0000001C CPUAddr 00000000 ALUCtrl 0000000C
ALU-Bin 00000210 WB-Data 0000001C CPU-DAi 0000001C WR--MIO 00000001
Imm32ID ABCDE000 WB-Addr 00000004 CPU-DAo 00000000 RegW/DR 00010001
CODE-00 00000013 CODE-01 01C00083 CODE-02 01C01103 CODE-03 01C02183
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POWER VOL- VOL+ MENU CH- CH+ MODE


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x28: t3 00000000 x29: t4 00000000 x30: t5 00000000 x31: t6 00000000
PC---IF 00000024 INST-IF 00100023 rs1Data 0000001C rs2Data 00000000
PC---ID 00000020 INST-ID 71C00093 rs1Addr 00000001 rs2Addr 0000001C
PC--EXE 0000001C INST-EX ABCDE0B7 CMU-RAM 00030001 PCJumpA 0000073C
PC--MEM 00000018 INST-M 21002003 B/PCE-S 00000000 D/C-Hzd 00000000
PC---WB 00000014 INST-WB 01C05283 I/nBSel 00010001 PC1FMxt 0000002B
ALU-Ain 00000000 ALU-Bin 00000210 CPUAddr 00000000 ALUCtrl 00000001
ALU-Bin ABCDE000 WB-Data 01C00083 CPU-DAi 00000000 WR--MIO 00000001
Imm32ID 0000071C WB-Addr 00000005 CPU-DAo 000000ED RegW/DR 00010001
CODE-00 00000013 CODE-01 01C00083 CODE-02 01C01103 CODE-03 01C02183
CODE-04 01C04203 CODE-05 01C05283 CODE-06 21002003 CODE-07 ABCDE0B7
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x24: s8 00000000 x25: s9 00000000 x26:s10 00000000 x27:s11 00000000
x28: t3 00000000 x29: t4 00000000 x30: t5 00000000 x31: t6 00000000
PC---IF 00000024 INST-IF 00100023 rs1Data 0000001C rs2Data 00000000
PC---ID 00000020 INST-ID 71C00093 rs1Addr 00000001 rs2Addr 0000001C
PC--EXE 0000001C INST-EX ABCDE0B7 CMU-RAM 00030001 PCJumpA 0000073C
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ALU-Ain 00000000 ALU-Bin 00000210 CPUAddr 00000000 ALUCtrl 00000001
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PC---IF 00000020 INST-IF 00101223 rs1Data 00000000 rs2Data 0000001C
PC---ID 00000024 INST-ID 00100023 rs1Addr 00000000 rs2Addr 00000001
PC--EXE 00000020 INST-EX 00102423 CMU-RAM 00000000 PCJumpA 00000024
PC--MEM 0000001C INST-M ABCDE0B7 B/PCE-S 00000100 D/C-Hzd 00000000
PC---WB 00000018 INST-WB 21002003 I/nBSel 00010001 PC1FMxt 0000002C
ALU-Ain ABCDE000 ALU-Bin 00000210 CPUAddr 00000000 ALUCtrl 00000001
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POWER VOL- VOL+ MENU CH- CH+ MODE

四、　讨论与心得

本次实验基于 lab3 进行实现，代码量并不大，主要需要我们根据状态图进行理解。在上实验板的过程中发现 rom 的代码和仿真当中的不一样，但是好在程序也正确地处理了各种指令。

通过此次实验和 lab2，我加深了对通过状态机处理体系结构问题的理解，对于未来的学习十分有帮助。