UVM-Simulationsmodell eines JTAG-Interfaces

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Abstract

[1]

[1]Keywords: Universal Verification Methodology, JTAG, verification component, TAP controller, boundary scan

Contents

1 Abbreviations used

- UVM - Universal Verification Methodology
- OVM - Open Verification Methodology
- DUT - Device Under Test
- BSDL - Boundary Scan Description Language
- DR - Data Register
- IR - Instruction Register
- TAP - Test Access Port
- TCK - Test ClocK input
- TDI - Test Data Input
- TDO - Test Data Output
- TMS - Test Mode Select
- TRST - Test ReSeT input
- VC - Verification Component
- IP - Intellectual Property
- PCB - Printed Circuit Board
- IC - Integrated Circuit
- FSM - Finite State Machine
- BSR - Boundary Scan Register
- RTL - Register Transfer Level
- DUT - Device Under Test
- IDE - Integrated Development Environment

2 Introduction

2.1 Introduction to Boundary Scan and JTAG

Boundary Scan is a method of testing interconnects on PCBs and internal IC sub-blocks. This standard is defined in IEEE 1149.1 For boundary scan tests, additional logic is added to the device. The boundary scan cells are placed between the core logic and the ports.

JTAG is an established technology(and industry standard) with a potential that is only now becoming fully realised. Connection testing and In System Programming(ISP) are the two applications most often associated with JTAG, but it has far more to offer.

2.1.1 Background

JTAG was initially conceived to address difficulties in testing circuits using the traditional 'bed-of-nails' approach. Modern packaging technologies like BGA and Chip Scale Packaging limit and in some cases eliminate physical access to pins. JTAG overcomes this problem, by placing cells between the external connections and the internal logic of the device. With the cells configured as a shift register, JTAG can be used to set and retrieve the values of pins(and nets connected to them) without physical access.

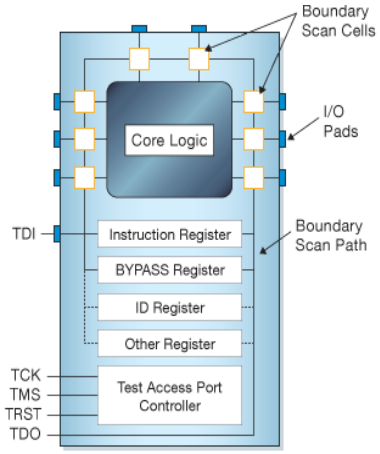


Figure 1: JTAG Block Diagram

There is also an option to sample the data values as they pass between the core logic and the pins during the normal operation of the device.

The JTAG interface adds four extra pins to each device:

- TDI to input data to the device
- TDO to output data from the device
- TMS to control what should be done with the data
- TCK clock signal to synchronize everything

If a circuit contains more than one JTAG-compliant device, these can be linked together to form a JTAG chain. In a JTAG chain the data output from the first device becomes the data input to the second device; the control and the clock signals are common to all the devices in the chain. Fig. provides a representation of a simple JTAG chain containing three devices.

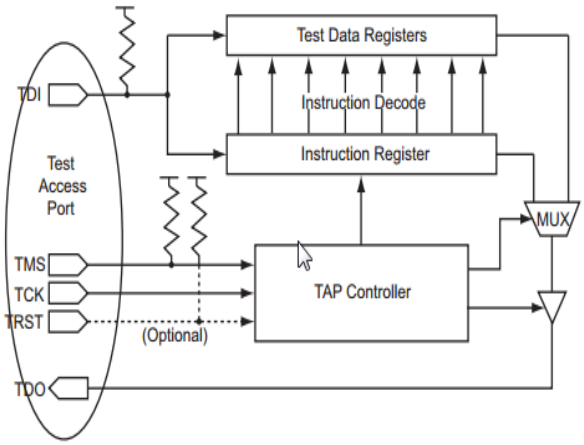


Figure 2: Simple JTAG Device1

2.1.2 Test Access Port (TAP)

Each test logic function is accessed through the TAP. The five pins associated with the TAP are listed on the **??** with their corresponding descriptions. Four pins - TMS, TCK, TDI, and TDO - are always required for JTAG operation. The fifth pin, TRST, is optional. These pins are dedicated pins - used only with the test logic.

Table 1: Test Access Port Descriptions

Port	Description
Test Mode Select (TMS)	Serial Input for the test logic control bits. Data is captured on the rising edge of the test logic clock (TCK). An internal pull-up resistor is present in dedicated mode but not in flexible mode.
Test Clock Input (TCK)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the the clock.
Test Data Input (TDI)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock. This pin is equipped with an internal pull-up resistor.
Test Data Output (TDO)	Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress.
Test Reset (TRST)	Active-low input which asynchronously resets the test logic. This pin is equipped with an internal pull-up resistor.

TRST overrides the behavior of the TMS and TCK. In other words, asserting TRST resets the TAP controller regardless of the the states of the TMS and TCK. Also, if TAP controller is held in the reset state, the state machine remains in the 'Test Logic Reset' condition.

2.1.3 TAP Controller

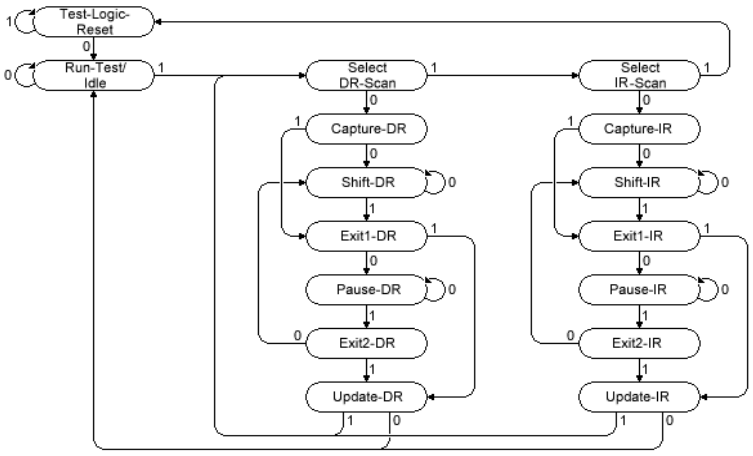


Figure 3: TAP CONTROLLER

The 16 states of the TAP controller finite state machine are shown in the fig **??**. The 1s and 0s shown adjacent to the state transitions represent the TMS values that must be present at the time of a rising edge at TCK for a state transition to occur. In the states that include the letters -IR, the instruction register operates. In the states that include the letters -DR, the test data registers operates (bypass, boundary scan).

By default, upon power up(or when TRST is asserted) the TAP controller enters the Test-Logic-Reset state. The TAP controller also has an inherent property for automatically reaching this state when the TMS signal is held high for atleast 5 clock signals.

The operation of each state is explained below:

- **Test-Logic-Reset**
  All test logic is disabled in this controller state enabling the normal operation of the IC.
- **Run-Test-Idle**
  In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it is executed when the controller enters this state. The test logic in the IC is idle otherwise.
- **Select-DR-Scan**
  This controller state controls whether to enter the Data Path or the Select-IR-Scan state.
- **Select-IR-Scan**
  This controller state controls whether or not to enter the Instruction Path. The controller can return to the Test-Logic-Reset state otherwise.
- **Capture-IR**
  In this controller state, the shift register bank in the Instruction register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits must always be '01'.
- **Shift-IR**
  In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in on to the instruction register.

- **Exit1-IR**
  This controller state controls whether to enter the Pause-IR state or Update-IR state.
- **Pause-IR**
  This state allows the shifting of the instruction register to be temporarily halted.
- **Exit2-IR**
  This controller state controls whether to enter either the Shift-IR state or Update-IR state.
- **Update-IR**
  In this controller state, the instruction in the instruction register is latched to the latch bank of the Instruction Register on every falling edge of TCK. The instruction becomes the current instruction once it is latched.
- **Capture-IR**
  In this controller state, the data is parallel-loaded into the data registers selected by the current instruction on the rising edge of TCK.
- **Shift-DR, Exit1-DR, Pause-DR, Exit2-DR and Update-DR**
  These controller states are similar to the Shift-IR, Exit1-IR, Pause-IR, Exit2-IR and Update-IR states in the Instruction Path.

2.1.4 Registers

- **Instruction Register** The instruction register allows an instruction to be shifted into the design. The instruction is used to select the test to be performed or the test data register to be accessed or both. Optionally, the instruction register allows examination of design-specific information generated within the component.

  Each IR cell in the Instruction Register has a shift-register stage and a latch stage for fault isolation of the board-level serial test data path.

Table 2: Supported Instructions

Instruction	IR-Code (IR3-IR0)	Instruction Type	Description
EXTEST	0000	Mandatory	Allows testing of off-line circuitry and board-level interconnections
SAMPLE/PRELOAD	0001	Mandatory	Allows a snapshot of the normal operation of the component to be taken and examined
IDCODE	0010	Optional	32-bit hard-wired Manufacturer ID, part number, and version number
BYPASS	1111	Mandatory	Provides minimum-length (1-bit) serial path between TDI and TDO pins of component when no test operation of that component is required
INTEST	XXXX	Optional	Allows testing of on-chip system logic while component is assembled on the board

- **Data Register**

I Boundary-Scan Register
The boundary-scan register allows testing of circuitry external to a component, for example, board interconnect or external components that do not conform to this standard. The register also permits the system signals flowing into and out of the system logic to be sampled and examined without causing interference with the normal (nontest) operation of the on-chip system logic. Optionally, additional test functions may be supported - for example, testing of the on-chip system logic.

II Bypass Register
This provides a single-bit serial connection through the circuit when none of the other test data registers is selected. This register can, for example, be used to allow test data to flow through a particular device to other components in a product without affecting the normal operation of the particular component.

III Device Identification Register
This is an optional test data register that allows the manufacturer, part number, and variant of a component to be determined.

2.2 Introduction to Verification Methodologies:

2.2.1 Classical verification vs Constraint based verification:

With the increasing complexity of the digital systems, comes the need to have smarter ways to verify the functionality of the designed DUT. Initially the digital were tested with tediously written test-benches and then observing the respective waveform. The higher complexity did no longer allow for the manual checks and there was a need to automate the verification methods.

Verification planning and management involves identifying the features of the DUT that need to be verified, prioritizing those features, measuring progress, and adjusting the allocation of verification resources so that verification closure can be reached on the required timescale. The mechanics of verification can be accomplished using static formal verification in the context of UVM focuses on the simulation-based verification environment.

There are two contrasting approaches to coverage-driven verification in current use. "Classical" constrained random verification starts with random stimulus and gradually tightens the constraints until coverage goals are met, relying on brute power of randomization and compute server farms to cover the state farms to cover the state space. More recently, graph-based stimulus generation (also known as Intelligent Testbench) starts from an abstract description of the legal transitions between the high-level states of the DUT, and automatically enumerates the minimum set of tests needed to cover the paths through this state space. For many application, graph-based stimulus is able to achieve high coverage in far fewer cycles than "classical" constrained random. UVM directly supports constrained random, whereas graph-based stimulus generation requires a separate, dedicated tool. Stimulus generated from the graph-based approach can be executed on a UVM verification environment.

Functional coverage and code coverage measure different things. Code coverage measures the execution of the actual RTL code (which must therefore exist before the code coverage can run at all). The collection of code coverage information, including statement and branch coverage, state coverage, and state transition coverage, is largely automatic. Functional coverage, on the other hand, attempts to measure whether the features described in the verification plan have actually been executed by the DUT. The feature to be measured have to be decided from the specification and implementation of the design to create the verification plan, and so functional coverage can be considered as a qualitative measure of DUT code execution.

The best practice is to create a verification plan that consists of a list of features to be tested as opposed to a list of direct test descriptions. All stakeholders in the verification process should contribute to the identification and prioritization of features in the verification plan, since this feature set will form the foundation for the subsequent verification process.

2.2.2 Advantages of Functional coverage

Functional coverage helps to identify

- the features in the verification plan that have been successfully tested
- the features in the verification plan that have yet to be tested
- the proportion of the features that have been tested and thus how close the verification process is to completion
- the set of tests that provide maximum coverage using the minimum number of CPU cycles

In contrast, in traditional directed testing methodology, the absence of further bugs being detected is taken as evidence that verification is nearly complete. This may overcome some scenarios in which the DUT might fail.

2.2.3 What is UVM?

Introduction to UVM
UVM is a methodology for functional verification using SystemVerilog, complete with a supporting library of SystemVerilog code. UVM stands for Universal Verification Methodology. It was created by Accelera based on the OVM(Open Verification Methodology) version 2.1.1.

It is basically a methodology for the functional verification of digital hardware, primarily using simulation. The hardware or system would be typically be described using Verilog, SystemVerilog, VHDL or SystemC at any appropriate abstraction level. This could be behavioral, Register-transfer level, or gate level. UVM is explicitly simulation-oriented, but UVM can also be used alongside assertion-based verification, hardware acceleration or emulation.

History
In December 2009, a technical subcommittee of Accellera - a standards organization in the electronic design automation (EDA) industry - voted to establish the UVM and decided to base this new standard on OVM 2.1.1, a verification methodology developed jointly in 2007 by Cadence Design Systems and Mentor Graphics. In February 21, 2011, Accelera approved the 1.0 version of UVM. It included a Reference Guide, a Reference Implementation in the form of SystemVerilof base class library, and a User Guide.

Checkers, Coverage and Constraints
Constrained random verificaiton relies on Checkers, Coverage and Constraints and these are supported by explicit features of the SystemVerilog language.

Firstly, checkers ensure functional correctness. Nothing is gained by throwing more and more random stimulus into a design to take functional coverage to ever higher levels unless the design-under test is being checked automatically for functional correctness. Checkers can be implemented by SystemVerilog assertions or using regular procedural code. UVM provides mechanisms and guidelines for building checkers into the verification environment and for logging reports.

Secondly, coverage provides a measure of the functional completeness of the testing, and tells us when we have met the goals set out in the verification plan, and thus when you have finished simulating. SystemVerilog offers two separate mechanisms for functional coverage collection; property-based coverage (cover directives) and sample-based coverage (covergroups). Both can be used in a UVM verification environment. The specification and the execution of the coverage information is intimately tied to the verification plan, and many simulation tools are able to annotate coverage information onto the verification plan document, facilitating tight management control.

Thirdly, constraints provide the means to reach coverage goals by shaping the random stimulus to push the DUT into interesting corner cases. Without shaping, random stimulus alone may be insufficient to exercise many of the deeper states of the DUT. Constrained random stimulus is still random, but the statistical distribution of the vectors is shaped to ensure that interesting cases are reached. Systemverilog has dedicated language features for expressing constraints, and UVM goes

further by providing mechanisms that allow constraints to be written as a part of a test rather than embedded within verification components. this and other features of UVM facilitate the creating of reusable verification components.

Verification Reuse

UVM facilitates the constructino of verification environments and tests, both by providing reusable machinery in the form of a library of SystemVerilog classes, and alos by providing a set of guidelines for best practice when using SystemVerilog for verification.

Verification productivity can be enhanced by reusing verification components, and this is an an important objective of UVM. Verification reuse is enabled by having a modular verification environment where each component has clearly defined responsibilities, by allowing flexibility in the wat in which components are configured and used, by having a mechanism to allow imported components to be customized to the application at hand, and by having well-defined coding guidelines to ensure consistency.

The architecture of UVM has been designed to encourage modular and layered verification environments, where verification components at all layers can be reused in different environments. Low-level driver and monitor components can be reused across multiple DUT. The whole verification environment can be reused by multiple tests and configured top-down by those tests. Finally, test scenarios can be reused from application to application. This degree of reuse is enabled by having UVM verification components able to be configured in a very flexible way without modification to their source code. This flexibility is built into the UVM class library.

3 Objective and Specifications

Development of a Universal Verification Methodology environment of the JTAG interface. It will contain the following functionality:

- Existing and verified IP core of a JTAG interface
- Execution of the following Instructions:
  EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE according to IEEE1149.1 standard
- Enhanced test bench(es) to fully test the DUT

The simulation runs as well as the occurring challenges are documented.
IDE used: Questa®Advanced Simulator, Mentor Graphics

4 Developed Modules:

Blocks in UVM

We have a DUT and to test the functionality we have to simulate it. To achieve this, we will need a block that generates sequences of bits to be transmitted to the DUT. This block in UVM is called the *Sequencer*.

Usually the sequencer is unaware of the communication bus and the physical connections to the DUT. The sequencer is responsible only for generating generic sequences of data and then it is sent to another block that has direct access to the physical pins of the DUT. This block that interacts directly with the DUT is called the *Driver*.

While the driver maintains activity with the DUT by feeding it data generated from the sequencers, it does not validate the applied stimuli. We need a block that will listen to the communication between the driver and the DUT. This block is called the *Monitor*. Monitors sample the inputs/outputs of the DUT.

The monitor tries to make a prediction of the expected result and send the prediction and result of the DUT to another block of UVM. This block, the *Scoreboard*, compares and evaluates these data from the monitor.

All these blocks together constitute a typical system used for verification and the same structure is used in UVM testbenches. This is represented in fig.**??**

Usually the sequence, the sequencer, the driver and the monitor compose an *Agent*. An agent together with the scoreboard constitute an *Environment*. All these blocks are controlled by a greater block denominated by *Test*. The test block controls all the blocks and sub blocks of the testbench. By changing just a few lines of code, we could add, remove and override blocks in our testbench and build different environments without rewriting the whole test.

UVM classes

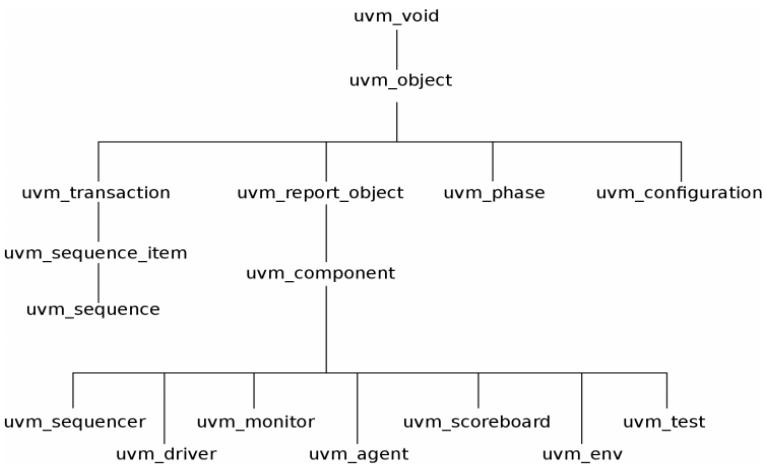


Figure 4: UVM Class Tree

The re-usability is one of the great advantages of UVM. This is mainly due to the concept of classes and objects from SystemVerilog.

In UVM, all the above mentioned blocks are represented as objects that are derived from the already existing classes.

A class tree of the most important UVM classes can be seen in the fig.**??**.

The data that travels to and from the DUT is stored in *uvm_sequence_item* and *uvm_sequence*. The sequencer is derived from the *uvm_sequencer*, the driver is derived from the *uvm_driver* and so on.

UVM Phases

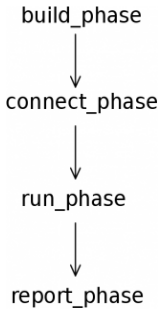


Figure 5: Instruction Register

All the above mentioned classes have simulation phases. Phases are ordered steps of execution implemented as methods. When we derive a new class, the simulation of our testbench goes through these different steps in order to construct, configure and connect the testbench.

- Build Phase:
  The build phase is used to construct components of the hierarchy. For example, the build phase of the agent class will construct the classes for the monitor, for the sequencer and for the driver.

- Connect Phase:
  The connect is used to connect the different sub components of a class. Using the same example, the connect phase of the agent connects the driver to the sequencer and the monitor is connected to an external port.

- Run Phase:
  The run phase is the main phase of the execution. This is where the actual code of a simulation will execute.

- Report Phase:
  Finally, the report phase is the phase where the results of the simulation are displayed.

UVM Macros

Macros are an important aspect of UVM. These macros implement some useful methods in classes

and in variables. Though they are optional to use, using them simplifies the process of code development and testing.

The most common ones are:

- ‘uvm_component_utils
  This macro registers the new class type. It is used when deriving new classes like a new agent, driver, monitor and so on.

- ‘uvm_fie‘ld_init
  This macro registers a variable in the UVM factory and implements some functions like copy(), compare() and print().

- ‘uvm_info
  This is a very useful macro which we have used to print messages from the UVM environment during simulation time.

4.1 Device Under Test with JTAG capability

The designed DUT is JTAG compliant. The objective of our project is to develop a UVM Test for a JTAG interface. We would design a basic full adder with JTAG capabilities. The full adder module can be replaced with any other DUTs and the same testbench would implement the same JTAG tests accurately.

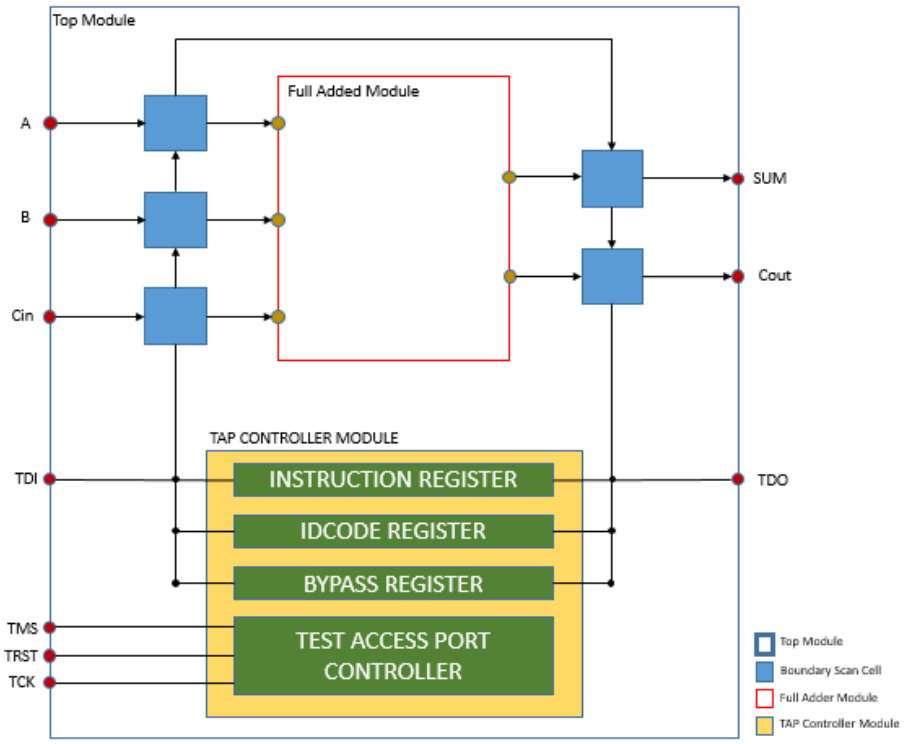


Figure 6: Developed Design Under Test

4.1.1 Boundary Scan Cells Modules

Located in: *InputCell.v* and *OutputCell.v*

The boundary-scan test architecture provides a means to test interconnects between integrated circuits on a board without using physical test probes. It adds a boundary-scan cell that includes a multiplexer and latches to each pin on the device. Boundary-scan cells in a device can capture data from pin or core logic signals, or force data onto pins. Captured data is serially shifted out and externally compared to the expected results. Forced test data is serially shifted into the boundary-scan cells. All of this is controlled from a serial data path called the scan path or scan chain. Figure 1 depicts the main elements of a boundary-scan cell. By allowing direct access to nets, boundary-scan eliminates the need for a large number of test vectors, which are normally needed to properly initialize sequential logic. Tens or hundreds of vectors may do the job that had previously required thousands of vectors. Potential benefits realized from the use of boundary-scan are shorter test times, higher test coverage, increased diagnostic capability and lower capital equipment cost.

Data is passed serially through the Boundary Scan Registers which help in debugging the state of the inputs and the outputs.

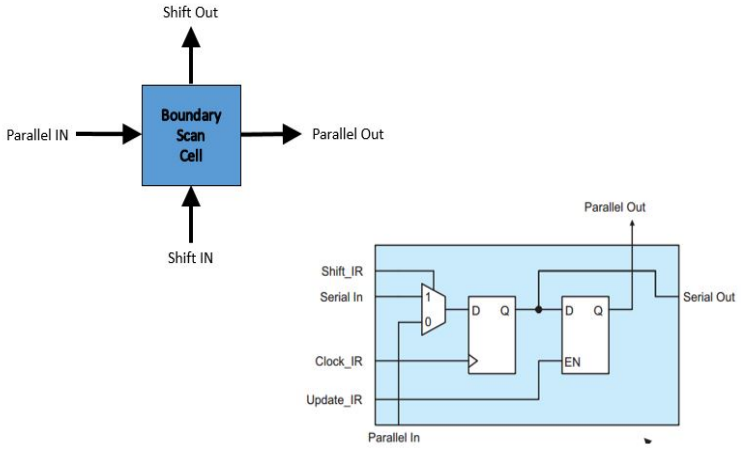


Figure 7: Boundary Scan Cell

Output Boundary Scan Cell: This is the Boundary Scan Cell that is connected to the output side of the Full Adder Module. When the DUT is running in JTAG mode, then the TDI and TDO are connected between the boundary scan registers and this path is called the 'Scan Path'. The JTAG mode, the value in the instruction register decides the flow of information from the Scan Path. In normal operation mode, these boundary scan cells pass the Full Adder outputs to the outputs of the DUT.

```
module OutputCell( FromCore, FromPreviousBSCell, CaptureDR, ShiftDR, UpdateDR, extest, TCK, ToNextBSCell, TristatedPin);
input  FromCore;
input  FromPreviousBSCell;
input  CaptureDR;
input  ShiftDR;
input  UpdateDR;
input  extest;
input  TCK;
output ToNextBSCell;
output TristatedPin;
```

Figure 8: Output Cell Code

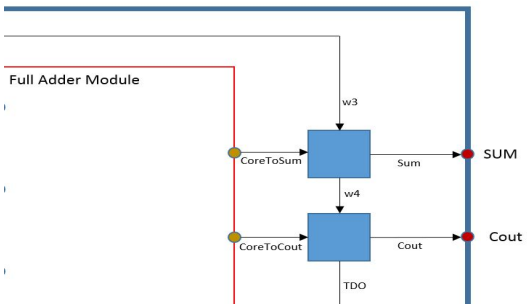


Figure 9: Output DUT

Input Boundary Scan Cell: This is the Boundary Scan Cell that is connected to the output side of the Full Adder Module. In normal operation mode, these boundary scan cells pass the input given to the DUT to the Full Adder input ports. The JTAG mode, the value in the instruction register decides the flow of information from the Scan Path.

```
module InputCell( InputPin, FromPreviousBSCell, CaptureDR, ShiftDR, TCK, ToNextBSCell, ToCore);
input  InputPin;
input  FromPreviousBSCell;
input  CaptureDR;
input  ShiftDR;
input  TCK;
output ToNextBSCell;
output ToCore;
```

Figure 10: Input Cell Code

In addition to the parallel in, parallel out, serial in and serial out lines, the captureDR, ShiftDR, UpdateDR and TCK pins are also passed to this module from the TAP controller module. These signals indicate the Boundary Scan of the mode in which the DUT is operating in.

InputCell.v and OutputCell.v are the files that contain the input boundary scan cell and output boundary scan cell respectively.

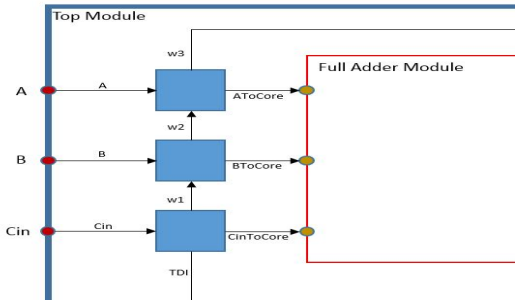


Figure 11: Input Cell Code

4.1.2 TAP Controller Module

Located in: *tap_top.v*

The TAP controller module controls all the operation of the DUT when in the JTAG test operation mode. The TCK, TDI, TRST and TMS are the inputs to this module. The TDO pin is the output from this module. The TAP controller also contains the instruction register, the BYPASS register and the IDCODE register.

When the instruction register contains the instruction for IDCODE operation, the TDI and TDO are connected between the IDCODE registers. On every falling edge of the TCK signal, the IDCODE register is shifted out bit by bit to the TDO pin.

The BYPASS register is a one bit register that is connected between the TDI and TDO pin when the BYPASS instruction is selected. So the TDO follows the TDI with one clock cycle delay.

The operation of the TAP controller is controlled by the TMS pin. Fig. **??** shows how the TAP controller states change. The Finite-State Machine for the TAP controller has been implemented and tested.

4.1.3 Full Adder Module

Located in: *full_adder.v*

The full adder module implements the basic operations of the Full adder. It has three inputs and Sum and Carry outputs. This module is written in the full_ addder.v file.

Ports of the full adder:

- A - input
- B - input
- Cin - input
- Sum - output
- Cout - output

```
module full_adder(
    input_a,
    input_b,
    input_cin,

    output_sum_o,
    output_cout_o
);

input input_a;
input input_b;
input input_cin;

output output_sum_o;
output output_cout_o;

reg output_sum;
reg output_cout;

assign output_sum_o = output_sum;
assign output_cout_o = output_cout;
assign {output_cout, output_sum} = input_cin + input_a + input_b;

endmodule
```

Figure 12: Full Adder Module Code

4.2 UVM Modules

This contains all the modules that are required for the verification environment

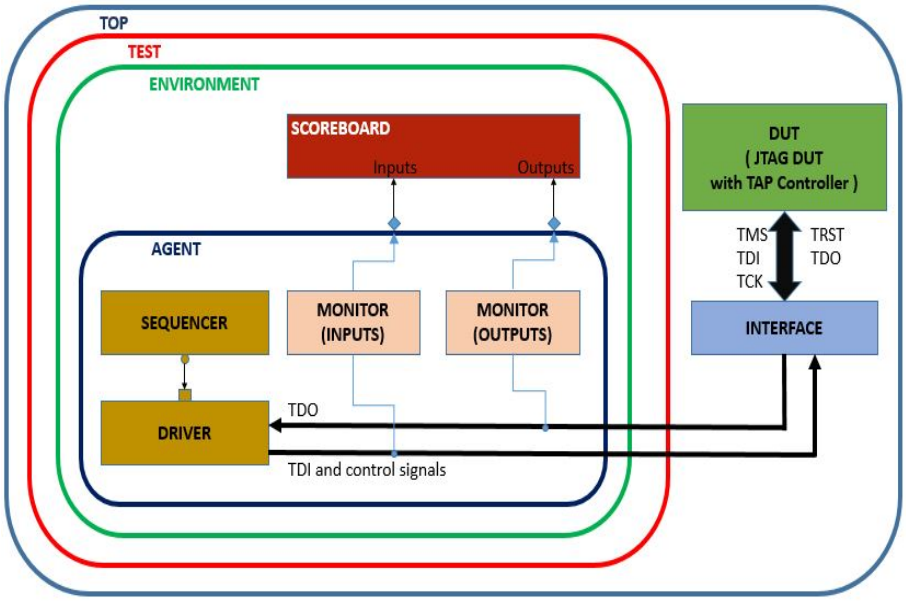


Figure 13: Designed Verification Environment

Each of these blocks are explained in detail below. It also contains actual snapshots of the code for easier understanding.

4.2.1 Top Block

Located in: *testbench.sv*

Generally the development of the DUT is done independently of the development of the testbench environment. The testbench top module connects the DUT to the verification components.

A virtual interface is defined and added to the database so that all the modules that have access to the DUT can invoke it from the database.

```
// ------------------------------------------------------------ //
//                                                              //
// TOP TEST MODULE                                              //
// The top module that contains the DUT and interface.          //
// This module starts the test.                                 //
//                                                              //
// ------------------------------------------------------------ //

module top;
  import uvm_pkg::*;
  import my_testbench_pkg::*;

  // Instantiate the interface
  dut_if dut_if1();

  // Instantiate the DUT and connect it to the interface
  dut dut1(.dif(dut_if1));

  // Clock generator
  initial begin
    dut_if1.tck_pad_i = 0;
    forever #5 dut_if1.tck_pad_i = ~dut_if1.tck_pad_i;
  end

  initial begin
    // Place the interface into the UVM configuration database
    uvm_config_db#(virtual dut_if)::set(null, "*", "dut_vif", dut_if1);
    // Start the test
    run_test("my_test");
  end

  // Dump waves
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(0, top);
  end

endmodule
```

Figure 14: Testbench Top Code

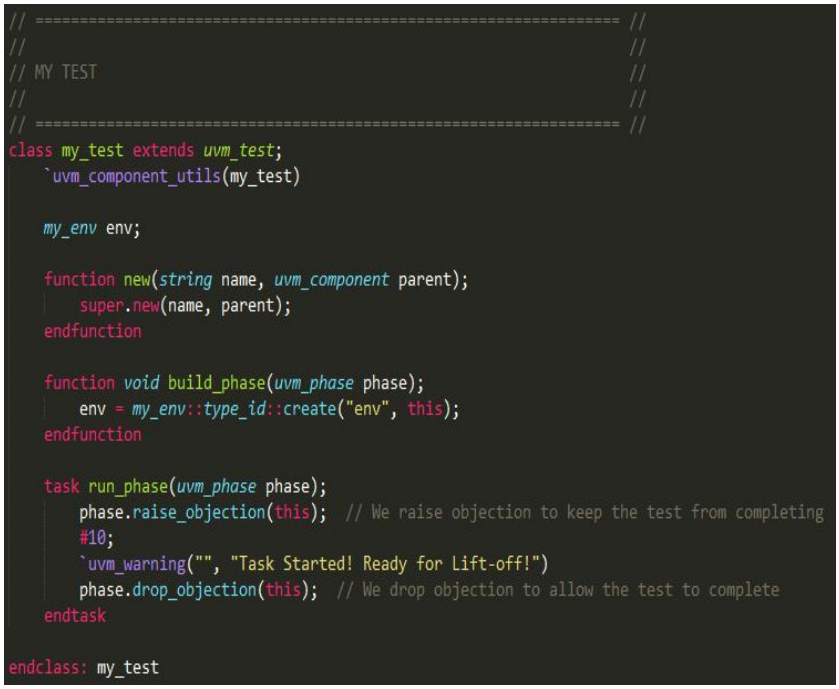
The Top contains the following:

- DUT Instance
- Interface instance
- Clock Generator block
- start the test
- set config_db
- waveform dump logic

4.2.2 Test Block

Located in: *my_testbench_pkg.svh*

The test file is derived from the uvm_test class. The test defines the test scenario for the testbench. It contains the environment, configuration properties, class overrides etc. A sequence can also be connected from this block. This test block runs when the run_test() function is called. Here, the test also defines the environment.



```
// ============================================================ //
//                                                              //
// MY TEST                                                      //
//                                                              //
// ============================================================ //
class my_test extends uvm_test;
    `uvm_component_utils(my_test)

    my_env env;

    function new(string name, uvm_component parent);
        super.new(name, parent);
    endfunction

    function void build_phase(uvm_phase phase);
        env = my_env::type_id::create("env", this);
    endfunction

    task run_phase(uvm_phase phase);
        phase.raise_objection(this);  // We raise objection to keep the test from completing
        #10;
        `uvm_warning("", "Task Started! Ready for Lift-off!")
        phase.drop_objection(this);  // We drop objection to allow the test to complete
    endtask

endclass: my_test
```

Figure 15: Test Code

4.2.3 Environment Block

Located in: *my_testbench_pkg.svh*

The environment is derived from the uvm_env class. The environment defines the Agent and the Scoreboard in the build phase. In the connect phase, the outputs from the monitor are connected to the scoreboard.

```
// ============================================================ //
//                                                              //
// ENVIRONMENT                                                  //
//                                                              //
// ============================================================ //
class my_env extends uvm_env;
    `uvm_component_utils(my_env)

        my_agent agent;
        jtag_scoreboard mem_scb;

        function new(string name, uvm_component parent);
            super.new(name, parent);
        endfunction

        function void build_phase(uvm_phase phase);
            agent   = my_agent::type_id::create("agent", this);
            mem_scb = jtag_scoreboard::type_id::create("mem_scb", this);
        endfunction

        function void connect_phase(uvm_phase phase);
            agent.mon_before.mon_ap_before.connect(mem_scb.sb_export_before);
            agent.mon_after.mon_ap_after.connect(mem_scb.sb_export_after);
        endfunction : connect_phase

endclass: my_env
```

Figure 16: Environment Code

4.2.4 Agent Block

Located in: *my_testbench_pkg.svh*

The build phase of the driver executes the following commands:

- Instantiate the ports that are used to connect to the monitor
- Instantiate the sequencer block
- Instantiate the agent block
- Instantiate the monitor block for reading TDI
- Instantiate the monitor block for reading TDO

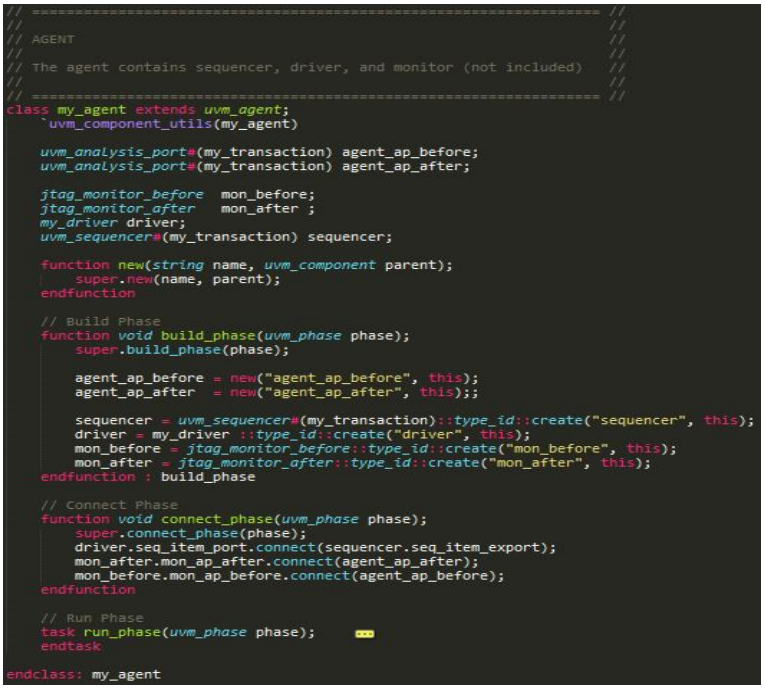
The connect phase of the driver executes the following commands:

- The seq_item_port of the driver is connected to the seq_item_export of the sequencer
- The uvm_analysis_port of TDI monitor is connected to the uvm_analysis_port of the agent
- The uvm_analysis_port of TDO monitor is connected to the uvm_analysis_port of the agent

The agent also contains the following blocks:

- Sequence or Transaction Block
- Sequencer Block
- Driver Block
- Monitors Block

These blocks and their snapshots are explained more in detail further.



```
// ============================================================ //
//                                                              //
// AGENT                                                        //
//                                                              //
// The agent contains sequencer, driver, and monitor (not included)   //
//                                                              //
// ============================================================ //
class my_agent extends uvm_agent;
    `uvm_component_utils(my_agent)

    uvm_analysis_port#(my_transaction) agent_ap_before;
    uvm_analysis_port#(my_transaction) agent_ap_after;

    jtag_monitor_before  mon_before;
    jtag_monitor_after   mon_after ;
    my_driver driver;
    uvm_sequencer#(my_transaction) sequencer;

    function new(string name, uvm_component parent);
        super.new(name, parent);
    endfunction

    // Build Phase
    function void build_phase(uvm_phase phase);
        super.build_phase(phase);

        agent_ap_before = new("agent_ap_before", this);
        agent_ap_after  = new("agent_ap_after", this);;

        sequencer = uvm_sequencer#(my_transaction)::type_id::create("sequencer", this);
        driver = my_driver ::type_id::create("driver", this);
        mon_before = jtag_monitor_before::type_id::create("mon_before", this);
        mon_after = jtag_monitor_after::type_id::create("mon_after", this);
    endfunction : build_phase

    // Connect Phase
    function void connect_phase(uvm_phase phase);
        super.connect_phase(phase);
        driver.seq_item_port.connect(sequencer.seq_item_export);
        mon_after.mon_ap_after.connect(agent_ap_after);
        mon_before.mon_ap_before.connect(agent_ap_before);
    endfunction

    // Run Phase
    task run_phase(uvm_phase phase);
    endtask

endclass: my_agent
```

Figure 17: Agent code

Sequence or Transaction Block
Located in: *my_sequence.svh*

The first step in testing our RTL design is to decide what kind of transaction is to be passed to the Driver. The transaction is designed by extending the uvm_ sequence_ item class. This includes the information needed to model the communication between the UVM components.

```
// ============================================================ //
//                                                              //
// TRANSACTION                                                  //
//                                                              //
// ============================================================ //
class my_transaction extends uvm_sequence_item;

    `uvm_object_utils(my_transaction)

    rand bit tms;
    rand bit tdi;
    rand bit trstn;
    rand bit tdo;
    rand bit A;
    rand bit B;
    rand bit Cin;

    function new (string name = "");
        super.new(name);
    endfunction

endclass: my_transaction
```

Figure 18: Transaction code

Sequencer Block
Located in: *my_sequence.svh*

After a basic transaction has been defined, the verification environment will need to generate a collection of them and get them ready to be sent to the driver. This is the job of the sequencer. Sequencer is extended from the uvm_ sequence and its main job is to generate multiple transactions. Sequences are an ordered collection of transactions and they shape transactions to our needs and also generate as many as we need. We could also constrain the range of randomization to the valid range to reduce simulation time in invalid values. These transactions are then transferred to the driver module.

```
// ============================================================ //
//                                                              //
// SEQUENCER                                                    //
//                                                              //
// ============================================================ //
class my_sequence extends uvm_sequence#(my_transaction);

    `uvm_object_utils(my_sequence)

    function new (string name = "");
        super.new(name);
    endfunction

    task body;
        repeat(80)
        begin
            req = my_transaction::type_id::create("req");

            start_item(req);
            if(!req.randomize())
            begin
                `uvm_warning("", "Randomization failed!")
            end
            finish_item(req);  // Waiting for the driver to send the item_done() command
        end
    endtask: body

endclass: my_sequence
```

Figure 19: Sequencer code

Driver Block
Located in: *my_sequence.svh*

The role of the driver block is to directly interact with the DUT. The driver pulls transactions from the sequencer and sends them repetitively to the signal-level interface. This interaction will be observed and evaluated by another block, the monitor. The driver toggles the TMS and the TDI pins to traverse through the TAP controller. The values of the TDI are shifted into the IR or the DR register depending on the state of the TAP controller. The driver module is extended from the uvm_ driver class. The run phase of the driver does the following:

- Gets a sequence item from sequencer
- Drive the sequence item to the DUT
- Wait for a possible few clock cycles for the DUT to respond
- Tell the sequencer that the current process is complete
- Ask the sequencer to send the next sequence item

The config_db places the defined virtual interface in the database so that it can be accessed by the driver module. Using the similar process, the interface can be loaded into any block which accesses the DUT directly.

UVM Driver Methods:
get_next_item
This method blocks the driver till a sequence_item is available at the sequencer
item_done
The non-blocking item_done()method will return a null pointer if there is no sequence_item available in the sequencer.

Tests implemented in the driver:
Bypass Instruction
The selection of the Bypass instruction is done by declaring *'define BYPASS_INSTR.*
Note: Do not run two tests simultaneously.
The tests for the bypass instruction are added in the run phase of the driver. The comments in the code mention exactly what each step does. Variable data stream length can be defined. A global variable *DATA_LENGTH* is defined in the *my_sequence.svh* file. The value will correspond to the length of the data stream that is sent from the TDI to the TDO.

The values of the TDI and TDO are stored by the monitor and then written into the scoreboard. The function *compareForBypass()* compares the TDI and TDO values and the result is printed in the console of the QuestaSim during simulation.

To introduce error into the bypass instruction the variable *introduceErrorBypass* should be set to 1. This introduces a stuck-at-1 error at TDO pin. The function *compareForBypass()* compares the two data streams and gives out an error on the console as the TDO and the TDI values do not match.

Idcode Instruction

The selection of the Idcode instruction is done by declaring *'define IDCODE_INSTR.*
The tests for the IDCODE are also defined in the run phase of the driver. The comments in the code mention exactly what each step does. Here, variable data streams cannot be defined as the length of the IDCODE register is defined in the IEEE Standard 1149.1

The values of the TDI and TDO are stored by the monitor and then written into the scoreboard. The function *compareForIdcode()* compares the TDO values with the values of the IDCODE defined in the DUT . The result is printed in the console of the QuestaSim during simulation. Incase of an error, the IDCODE that is read by the verification environment is also printed out on the console.

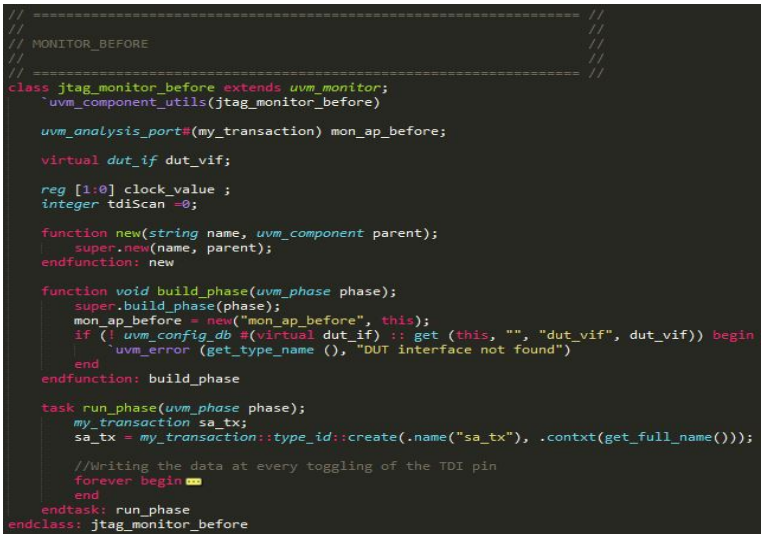
To introduce error into the IDCODE instruction the variable *introduceErrorIdcode* should be set to 1. This introduces an error in the value that is read from the IDCODE register. The function *compareForIdcode()* compares the two data streams and gives out an error on the console as the TDO values and the IDCODE register values do not match.

```
// ============================================================ //
//                                                              //
// DRIVER                                                       //
//                                                              //
// ============================================================ //
class my_driver extends uvm_driver #(my_transaction);
    `uvm_component_utils(my_driver)
    virtual dut_if dut_vif;

    function new(string name, uvm_component parent);
        super.new(name, parent);
    endfunction

    function void build_phase(uvm_phase phase);
        // Get interface reference from config database
        if(!uvm_config_db#(virtual dut_if)::get(this, "", "dut_vif", dut_vif))
        begin
            `uvm_error("", "uvm_config_db::get failed")
        end
        else
        begin
            `uvm_warning("", "Configuration database successfully accessed!")
        end
    endfunction

    task run_phase(uvm_phase phase); ...
    endtask

    virtual function void compareForBypass(); ...
    endfunction: compareForBypass

    virtual function void compareForIdcode(); ...
    endfunction: compareForIdcode

    function void report_phase(uvm_phase phase); ...
    endfunction
endclass: my_driver
```

Figure 20: Driver code

Monitors Block
Located in: *my_sequence.svh*
The monitor is derived from the uvm_monitor. Monitor is a passive block that observes the communication of the DUT with the verification environment. The monitor also returns an error if the response of the DUT does not match with the expected results. It is passive because it does not drive any signals to the DUT. The monitor samples the DUT signals through the virtual interface and converts the signal level activity to transaction level activity.

Monitor uses TLM ports to point to the DUT signals. There are two monitors that have been defined in out verification environment. One monitor is used to sample the inputs that are driven from the driver to the DUT(TDI). The second monitor samples the response of the DUT (TDO) and converts in into transaction level activity. All these are written to the scoreboard.



```
// ============================================================ //
//                                                              //
// MONITOR_BEFORE                                               //
//                                                              //
// ============================================================ //
class jtag_monitor_before extends uvm_monitor;
    `uvm_component_utils(jtag_monitor_before)

    uvm_analysis_port#(my_transaction) mon_ap_before;

    virtual dut_if dut_vif;

    reg [1:0] clock_value ;
    integer tdiScan =0;

    function new(string name, uvm_component parent);
        super.new(name, parent);
    endfunction: new

    function void build_phase(uvm_phase phase);
        super.build_phase(phase);
        mon_ap_before = new("mon_ap_before", this);
        if (! uvm_config_db #(virtual dut_if) :: get (this, "", "dut_vif", dut_vif)) begin
            `uvm_error (get_type_name (), "DUT interface not found")
        end
    endfunction: build_phase

    task run_phase(uvm_phase phase);
        my_transaction sa_tx;
        sa_tx = my_transaction::type_id::create(.name("sa_tx"), .contxt(get_full_name()));

        //Writing the data at every toggling of the TDI pin
        forever begin ...
        end
    endtask: run_phase
endclass: jtag_monitor_before
```

Figure 21: Monitor code for TDI

```
// ============================================================ //
//                                                              //
// MONITOR_AFTER                                                //
//                                                              //
// ============================================================ //
class jtag_monitor_after extends uvm_monitor;
    `uvm_component_utils(jtag_monitor_after)

    uvm_analysis_port#(my_transaction) mon_ap_after;

    virtual dut_if dut_vif;

    reg [1:0] clock_value ;
    integer tdoScan =0;

    function new(string name, uvm_component parent);
        super.new(name, parent);
    endfunction: new

    function void build_phase(uvm_phase phase);
        super.build_phase(phase);
        mon_ap_after = new(.name("mon_ap_before"), .parent(this));
        if (! uvm_config_db #(virtual dut_if) :: get (this, "", "dut_vif", dut_vif))
        begin
            `uvm_error (get_type_name (), "DUT interface not found")
        end
    endfunction: build_phase

    task run_phase(uvm_phase phase); ...
    endtask: run_phase
endclass: jtag_monitor_after
```

Figure 22: Monitor code for TDO

4.2.5 Scoreboard Block

Located in: *my_sequence.svh*

```
// ============================================================== //
//                                                                //
// SCOREBOARD                                                     //
//                                                                //
// ============================================================== //
class jtag_scoreboard extends uvm_scoreboard;
    `uvm_component_utils(jtag_scoreboard)

    uvm_analysis_export #(my_transaction) sb_export_before;
    uvm_analysis_export #(my_transaction) sb_export_after;

    uvm_tlm_analysis_fifo #(my_transaction) before_fifo;
    uvm_tlm_analysis_fifo #(my_transaction) after_fifo;

    my_transaction transaction_before;
    my_transaction transaction_after;

    function new(string name, uvm_component parent);
        super.new(name, parent);
        transaction_before = new("transaction_before");
        transaction_after = new("transaction_after");
    endfunction: new

    function void build_phase(uvm_phase phase);...
    endfunction: build_phase

    function void connect_phase(uvm_phase phase);...
    endfunction: connect_phase

    task run();...
    endtask: run
endclass: jtag_scoreboard
```

Figure 23: Scoreboard code

5 Testing and Problems faced

5.1 Phase I: Basic communication

In this phase, the DUT that we use is a dummy DUT. Its only work is to print out the data as it receives it. The interface of the DUT is similar to that of an 8-bit memory block with data address and data registers. A transaction is defined and a sequence is passed to a sequencer. This sequence then calls on to the driver to access the DUT. The environment used to develop the code is EDAPlayground. EDAPlayground is an online simulator where there is no download required to run the code. For initial testing, this was easier to use as the samples codes are readily available. The work-flow is given below:

- Classes for sequence, sequencer and driver are written
- UVM builds, connects and runs these classes
- A transaction is created
- A randomized and constrained sequence (address and data) is sent to the DUT
- Sequencer sends the sequence to the Driver and waits for item_done signal from the driver
- Driver toggles these data on to the DUT through the interface and then sends item_done signal to the sequencer
- UVM reporting is activated as long as the system does not receive a reset signal
- Repeat sending sequences to the driver and observe the signals

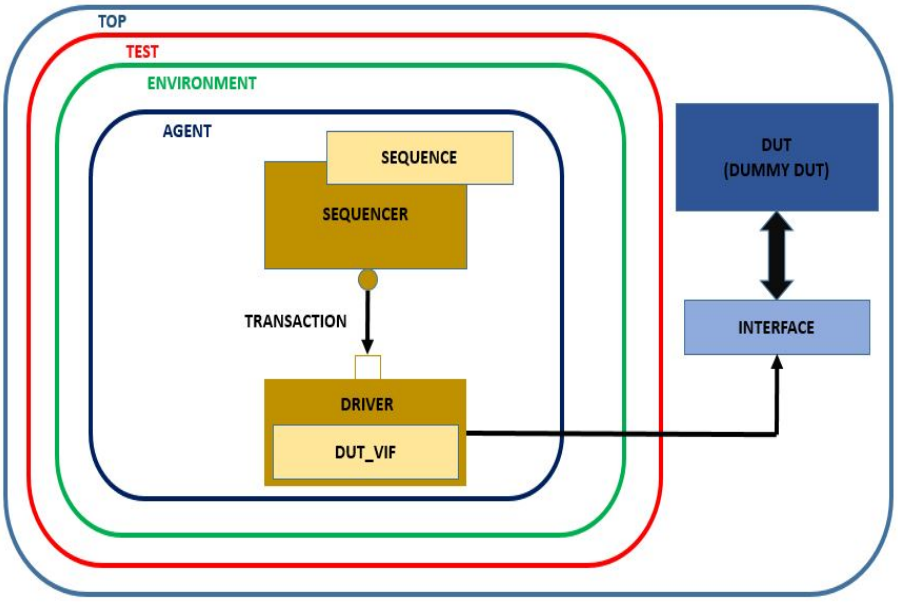


Figure 24: Basic Communication Environment

5.1.1 Testing Results for Phase I

The system reset is held low and normal operations are let to run. Randomized data and address is sent. From the waveform in Fig.**??**, we can see that these signals are toggling with the input.

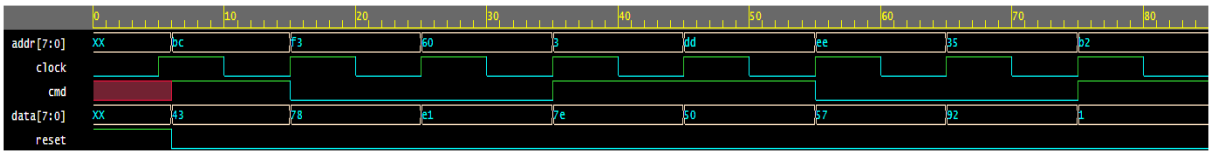


Figure 25: Phase I testing

The input parameters are randomized using the default *randomize()* command in SystemVerilog. The input to the DUT here is a 8-bit data bus and the constraint on the value of the input is from 0 to 255.

5.1.2 Testing Conclusion for Phase I

With this we have established a one-directional communication with our DUT. Also, the UVM Phases(build, connect, run and report) were tested. Our further developments have been built upon this basic building blocks. Here, we have not yet connected a monitor and scoreboard block. This would be included in phase III.

5.2 Phase II: Adding JTAG DUT

Phase 2 development was built over the existing architecture in Phase 1. Here we have added

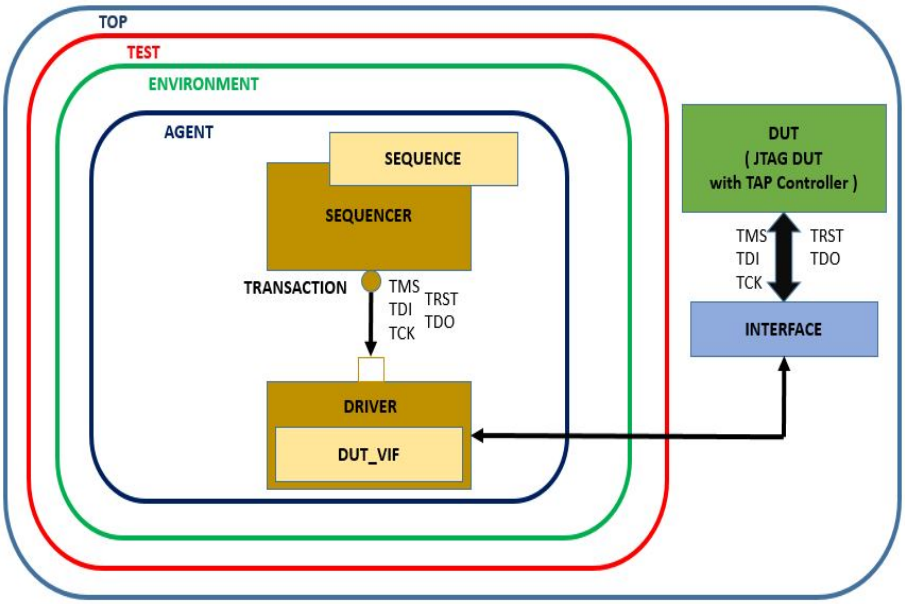


Figure 26: Environment after JTAG DUT addition

5.2.1 Testing Results for Phase II

5.2.2 Testing Conclusion for Phase II

5.3 Phase III: Adding Monitor and Scoreboard

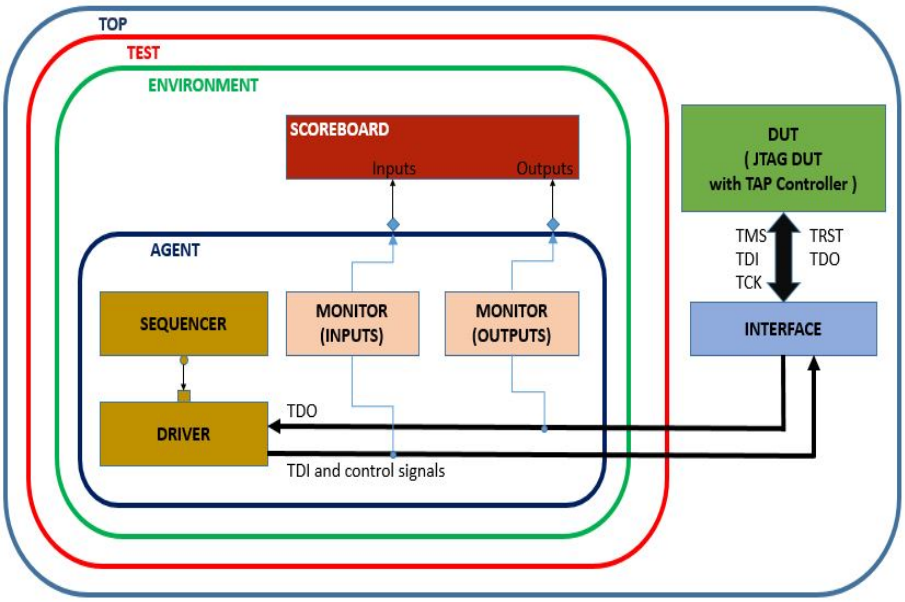


Figure 27: Complete Environment with Monitors and Scoreboard

5.3.1 Testing Results for Phase III

5.3.2 Testing Conclusion for Phase III

6 Results

6.1 Instruction: IDCODE

6.2 Instruction: BYPASS

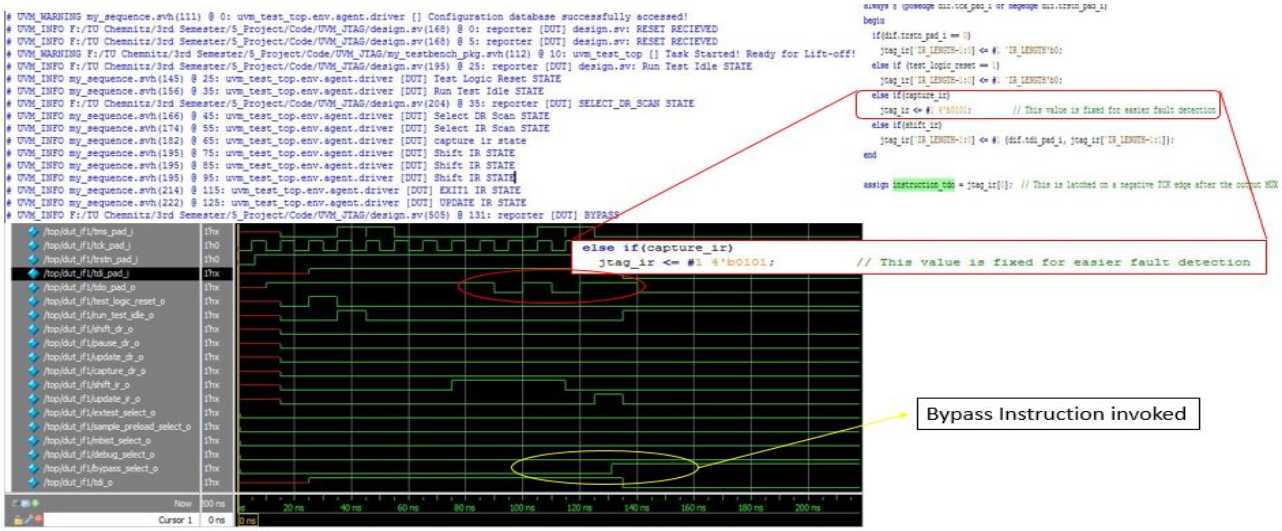


Figure 28: Result of the BYPASS instruction testing

6.3 Instruction: EXTEST

6.4 Instruction: INTEST

6.5 Instruction: SAMPLE/HOLD

7 Conclusion

We have now implemented a Device under test with JTAG capabilities. This can now be further extended to any DUT that is designed by replacing the *full_adder.v* file with any file that has the DUT to be tested. Only *top_module.v* needs to be modified for the instantiation of the modules. The UVM environment would remain the same and we could test the complete functionality of the JTAG instructions.

The tests have been carried out to see the responses of the DUT to the BYPASS and IDCODE instructions. The UVM environment compares the received and the expected values and gives an output on the console of the IDE. The user does not have to use the waveforms to manually verify the integrity of the signals. This reduces the time and effort that goes into testing of modules.

Provision has also been made to intentionally introduce errors into the testing modes. This gives us an idea of how the response would be when there is something wrong with the DUT. Also, this functionality helps cross verify our verification environment.

References

[1] *The Test Access Port and Boundary-Scan Architecture*, Colin M Maunder, et al., IEEE Computer Society Press, Los Alamitos

[2] *IEEE Std 1149.1-1993*, IEEE Standard Test Access Port, and Boundary-Scan Architecture, IEEE, Inc., New York

[3] *The Boundary-Scan Handbook*, Kenneth P. Parker, Kluwer Academic Publishers, Norwell

[4] *High-Level Guide to JTAG*, https://www.xjtag.com/about-jtag/jtag-high-level-guide/

[5] *IEEE Standard 1149.1*, https://www.microsemi.com/document-portal/doc_view/130050-ac160-ieee-standard-1149-1-jtag-in-the-sx-rtsx-sx-a-ex-rt54sx-s-families-app-not

[6] *JTAG - General Description of the TAP Controller states*, https://www.xilinx.com/support/answers/3203.html

[7] *IEEE Standard Test Access Port and Boundary Scan Architecture*, IEEE-SA Standards Board, 14 June 2001

[8] *Coverage driven Verification Methodology*, https://www.doulos.com/knowhow/sysverilog/uvm/easier_uvm_guidelines/coverage-driven/

[9] *UVM Verification Primer*, John Aynsley https://www.doulos.com/knowhow/sysverilog/uvm/tutorial_0/

[10] *Accellera's UVM User's Guide 1.1*

[11] *Accellera's UVM 1.1 Class Reference*

[12] *Verification Academy's UVM Cookbook*

[13] *SystemVerilog for Verification: A Guide to Learning the TestBench Language Features*, Chris Spear

[14] *Comprehensive Functional Verification: The Complete Industry Cycle*, John Goss

[15] *UVM guide for Beginners* https://www.colorlesscube.com/uvm-guide-for-beginners/

[16] *EDA Playground* https://www.edaplayground.com

[16] *corelis.com* http://www.corelis.com/education/Boundary-Scan_Tutorial.htm