Application Report
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Multiple TLV320ADCx140 Devices With Shared TDM and I²C Bus

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ABSTRACT

The TLV320ADCx140 device family (TLV320ADC3140, TLV320ADC5140, and TLV320ADC6140) is a quad-channel, high-performance, analog-to-digital converter (ADC) for audio applications. This document describes how to configure multiple TLV320ADCx140 devices to share a single TDM and I²C Bus.

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Trademarks

1 Introduction

For TLV320ADx140 applications requiring more than four channels, multiple TLV320ADCx140 devices can share a common bus. For systems with up to 16 analog input channels or up to 32 digital microphone inputs, up to four TLV320ADCx140 devices can share a single control and audio data bus to minimize board routing area. TLV320ADCx140 supports a control bus using the I²C interface and an audio serial bus using a time-division multiplexed (TDM), Inter-IC Sound (I²S), or Left-justified (LJ) interface. Figure 1 shows a diagram of four TLV320ADCx140 devices sharing the control and audio data buses.

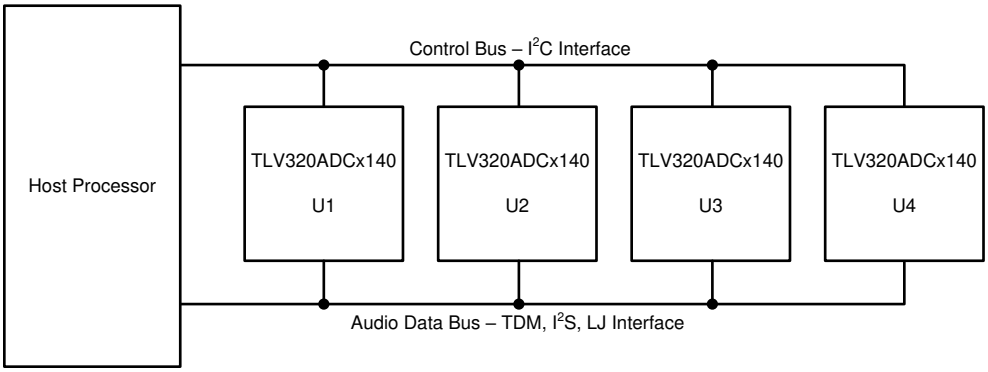

Figure 1. Four TLV320ADCx140 Devices With Shared Control and Audio Data Buses

Each channel of the TLV320x140 device follows the signal chain shown in Figure 2. Each channel of the TLV320ADCx140 supports an analog differential or single-ended signal or a digital pulse density modulation (PDM) digital microphone. In TLV320ADCx140 device families, the analog input signal is amplified by a Programmable Gain Amplifier (PGA) and then converted by a high-performance ADC into a digital signal. The PGA gains the input signal to match the full scale of the ADC. The digital signal has a programmable phase calibration to adjust the phase delay of each channel in steps of one modulator clock cycle. This allows the system to match the phase across different channels. The phase-calibrated digital signal is then decimated through a set of linear phase filters or low-latency filters. DC offset is removed from the decimated signal through a Digital High Pass Filter (HPF) with three pre-set cutoff frequencies or a fully programmable cutoff frequency. Note that DC shifts are caused by mismatches in common-mode voltages. The output of the HPF is gain calibrated with 0.1 dB steps and summed with other channels. The gain calibration matches the gain across different channels, particularly if the channels have microphones with varying gain values. The output is then filtered by the Digital Biquad Filters and gained by the volume control.

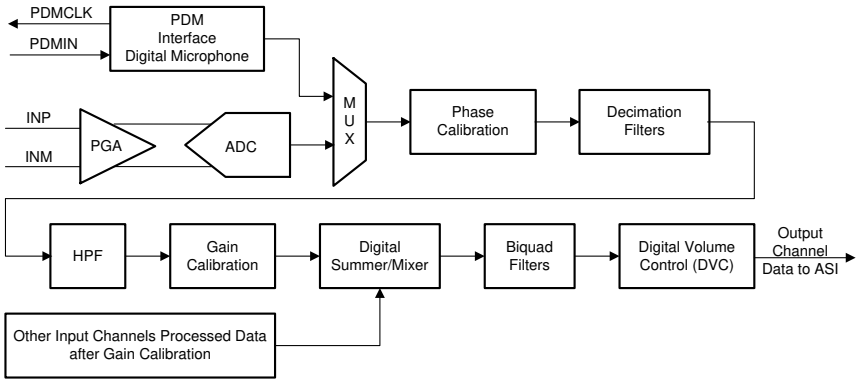

Figure 2. TLV320ADCx140 Channel Signal Chain Processing Flow Chart

This application note concentrates on how to configure the TLV320ADCx140 to share a single control and audio data bus between the devices.

2 Sharing the Control Bus

The TLV320ADCx140 devices are controlled through an I^2C bus operating in standard mode, fast mode, and fast mode plus. This I^2C control bus requires a 7-bit slave address whose two least significant bits are programmable by pulling the ADDR0_SCLK and ADDR1_MISO pins to VSS or IOVDD. By programming different I^2C slave addresses through these pins, several TLV320ADCx140 devices can share a single I^2C control bus. Moreover, a programmable broadcast enable feature allows you to temporarily change the I^2C slave address to 1001100 for TLV320ADCx140. This temporary slave address allows for simultaneous broadcasting I^2C communication to all TLV320ADCx140 devices in the system. Table 1 lists the four possible TLV320ADCx140 device addresses resulting from these pin and broadcast configuration options. In these table entries for ADDR1_MISO and ADDR0_SCLK, the notation '0' refers to pulling the pin to VSS, while notation '1' refers to pulling the pin to IOVDD. The notation 'X' refers to pulling the pin to either VSS or IOVDD.

Table 1. TLV320ADCx140 I^2C Slave Address Settings

ADDR1_MISO	ADDR0_SCLK	I2C_BRDCAST_EN BIT FIELD OF SLEEP_CFG REGISTER	I^2C SLAVE ADDRESS (BINARY)
0	0	0 (default)	1001 100
0	1	0 (default)	1001 101
1	0	0 (default)	1001 110
1	1	0 (default)	1001 111
X	X	1	1001 100

3 Sharing the Audio Bus

TLV320ADCx140 devices send the digitized audio data through a Time Division Multiplexed (TDM) audio bus. A set of channel transfers starts at the rising edge of FSYNC with the first slot of data (slot 0), followed by the remaining data slots in increasing order (slot1, slot2, and so forth). A slot contains the converted data from an ADC channel. Each slot transmits a bit on the rising or falling edge of BCLK, starting with the most significant bit first. Figure 3 shows an example for TDM bus operation with eight slots when TX_OFFSET is set to 0. In this figure, FSYNC is the frame sync signal from the host processor, BCLK is the bit clock signal from the host processor, and SDOUT is the bus from the TLV320ADCx140 devices. TLV320ADCx140 supports up to 64 slots in the SDOUT output.

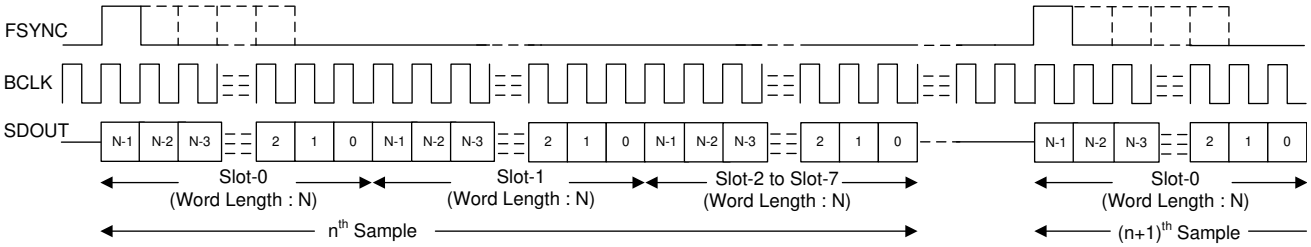

Figure 3. TDM Mode Standard Protocol Timing (TX_OFFSET = 0)

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the programmed word length of the output channel data, as shown in Equation 1. For the example shown in Figure 1 with four devices, each with four channels, at a 48-KHz sampling rate and 32-bit word length, BCLK ≥ 4 × 4 × 48 000 × 32 = 24.576 MHz. Since the maximum supported BCLK is 25 MHz, the maximum number of devices is dependent on the number of channels used, sample rate, and word length that maintains a bit clock (BCLK) under 25 MHz.

25 MHz ≥ bit clock ≥ (# channels/device) × (# devices) × (sample rate) × (word length) (1)

NOTE: For BCLK periods greater than 18.5 MHz (for corresponding sampling rates, see the Supported FSYNC and BCLK Frequencies table of the data sheet), one of the following conditions must be satisfied:

- The microprocessor must latch DOUT data on same edge clock polarity by adding a one BCLK cycle delay to allow capturing of DOUT transmission.
- The ADC must add a half cycle delay to DOUT from DOUT transmission at BCLK edge by setting TX_EDGE = 1 in ASI_CFG0 register (Figure 9). This setting adds a 1-bit offset in the data capture to the microprocessor.

Failure to observe these conditions might result in the microprocessor capturing corrupted data from DOUT.

The TLV320ADCx140 supports two methods of wiring several devices together: Shared TDM or Daisy Chain TDM. The following two sections detail the registers that need to be programmed to configure the TLV320ADCx140 devices to share the TDM bus in these methods.

3.1 ASI Configuration for Shared TDM

In Shared TDM bus configuration, the ASI buses of multiple TLV320ADCx140 devices are connected together into a single shared bus, as shown in Figure 4.

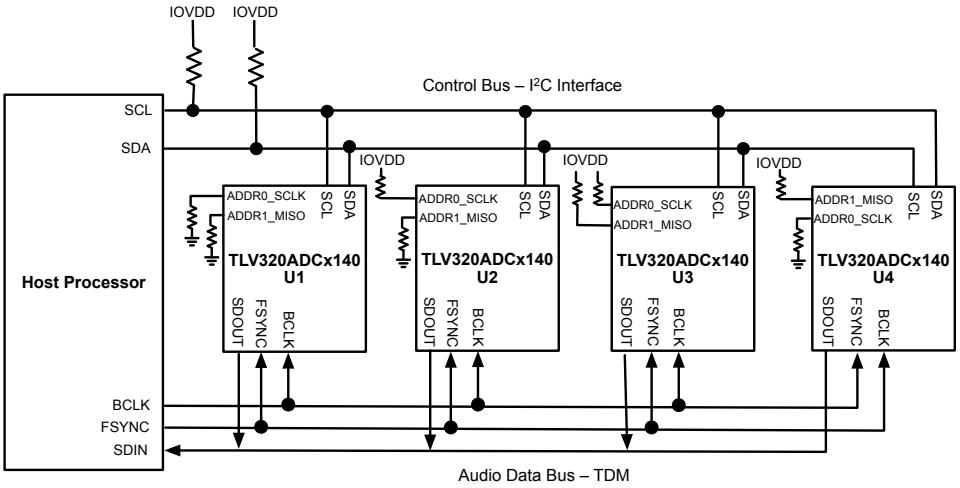

Figure 4. TLV320ADCx140 Shared TDM Connection Diagram

To avoid multiple devices transmitting output data in the same slot, the TLV320ADCx140 supports mapping the input channels of a device to a programmable slot using the following registers:

- ASI_CH1 (Page 0x00, Register 0x0B), shown in Figure 5
- ASI_CH2 (Page 0x00, Register 0x0C), shown in Figure 6
- ASI_CH3 (Page 0x00, Register 0x0D), shown in Figure 7
- ASI_CH4 (Page 0x00, Register 0x0E), shown in Figure 8

This allows any channel to be mapped to any slot in any order. Furthermore, the TLV320ADCx140 also supports a secondary SDOUT output (SDOUT2) configured through the GPO_CFG0 register, bit field GPIO1_CFG with value of 0x03, as shown in Figure 16. This allows one or more devices outputting slots through two pins: primary output (SDOUT) and secondary output (SDOUT2). The ASI_CHx register bit field CHx_OUTPUT maps a slot to the primary (SDOUT) or secondary output (SDOUT2).

Figure 5. ASI_CH1 Register

7	6	5	4	3	2	1	0
Reserved	CH1_OUTPUT	CH1_SLOT[5:0]					
R-0h	R/W-0h	R/W-0h					

Table 2. ASI_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH1_OUTPUT	R/W	0h	Channel 1 output line 0d = Channel 1 output is on the ASI primary output pin (SDOUT) 1d = Channel 1 output is on the ASI secondary output pin (GPIO1 or GPOx)
5-0	CH1_SLOT[5:0]	R/W	0h	Channel 1 slot assignment 0d = TDM is slot 0 or I²S, LJ is left slot 0 1d = TDM is slot 1 or I²S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I²S, LJ is left slot 31 32d = TDM is slot 32 or I²S, LJ is right slot 0 33d = TDM is slot 33 or I²S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I²S, LJ is right slot 31

Figure 6. ASI_CH2 Register

7	6	5	4	3	2	1	0
Reserved	CH2_OUTPUT	CH2_SLOT[5:0]					
R-0h	R/W-0h	R/W-1h					

Table 3. ASI_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH2_OUTPUT	R/W	0h	Channel 2 output line 0d = Channel 2 output is on the ASI primary output pin (SDOUT) 1d = Channel 2 output is on the ASI secondary output pin (GPIO1 or GPOx)
5-0	CH2_SLOT[5:0]	R/W	1h	Channel 2 slot assignment 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

Figure 7. ASI_CH3 Register

7	6	5	4	3	2	1	0
Reserved	CH3_OUTPUT	CH3_SLOT[5:0]					
R-0h	R/W-0h	R/W-2h					

Table 4. ASI_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH3_OUTPUT	R/W	0h	Channel 3 output line 0d = Channel 3 output is on the ASI primary output pin (SDOUT) 1d = Channel 3 output is on the ASI secondary output pin (GPIO1 or GPOx)
5-0	CH3_SLOT[5:0]	R/W	2h	Channel 3 slot assignment 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is left slot 31 32d = TDM is slot 32 or I^2S, LJ is right slot 0 33d = TDM is slot 33 or I^2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I^2S, LJ is right slot 31

Figure 8. ASI_CH4 Register

7	6	5	4	3	2	1	0
Reserved	CH4_OUTPUT	CH4_SLOT[5:0]					
R-0h	R/W-0h	R/W-3h					

Table 5. ASI_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CH4_OUTPUT	R/W	0h	Channel 4 output line 0d = Channel 4 output is on the ASI primary output pin (SDOUT) 1d = Channel 4 output is on the ASI secondary output pin (GPIO1 or GPOx)

Table 5. ASI_CH4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	CH4_SLOT[5:0]	R/W	3h	Channel 4 slot assignment 0d = TDM is slot 0 or I²S, LJ is left slot 0 1d = TDM is slot 1 or I²S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I²S, LJ is left slot 31 32d = TDM is slot 32 or I²S, LJ is right slot 0 33d = TDM is slot 33 or I²S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I²S, LJ is right slot 31

For the example of Figure 4, the following I²C script configures the input channels of U1–U4 into slots 0–15 for TLV320ADCx140, respectively. Note that slots are not assigned to the input channels of each device in sequence to show the flexibility of channel assignments to TDM slots:

```
w 98 0B 04  # Set U1 Ch1 mapped to slot 4 of SDOUT
w 98 0C 06  # Set U1 Ch2 mapped to slot 6 of SDOUT
w 98 0D 01  # Set U1 Ch3 mapped to slot 1 of SDOUT
w 98 0E 00  # Set U1 Ch4 mapped to slot 0 of SDOUT

w 9A 0B 03  # Set U2 Ch1 mapped to slot 3 of SDOUT
w 9A 0C 05  # Set U2 Ch2 mapped to slot 5 of SDOUT
w 9A 0D 02  # Set U2 Ch3 mapped to slot 2 of SDOUT
w 9A 0E 07  # Set U2 Ch4 mapped to slot 7 of SDOUT

w 9C 0B 08  # Set U3 Ch1 mapped to slot 8 of SDOUT
w 9C 0C 09  # Set U3 Ch2 mapped to slot 9 of SDOUT
w 9C 0D 0A  # Set U3 Ch3 mapped to slot 10 of SDOUT
w 9C 0E 0C  # Set U3 Ch4 mapped to slot 12 of SDOUT

w 9E 0B 0F  # Set U4 Ch1 mapped to slot 15 of SDOUT
w 9E 0C 0D  # Set U4 Ch1 mapped to slot 13 of SDOUT
w 9E 0D 0E  # Set U4 Ch1 mapped to slot 14 of SDOUT
w 9E 0E 0B  # Set U4 Ch1 mapped to slot 11 of SDOUT
```

This configuration requires that all the devices place their outputs in high-impedance mode, so another device can drive the bus. TLV320ADCx140 supports driving the output line low or placing it in high-impedance during unused bit clock cycles through the ASI_CFG0 register bit field TX_FILL, shown in Figure 9. Setting the TX_FILL places the primary (SDOUT) and secondary output line (SDOUT2) in high-impedance. Note the reset value configures SDOUT and SDOUT2 to drive low during unused bit clock cycles.

Figure 9. ASI_CFG0 Register

7	6	5	4	3	2	1	0
ASI_FORMAT[1:0]		ASI_WLEN[1:0]		FSYNC_POL	BCLK_POL	TX_EDGE	TX_FILL
R/W-0h		R/W-3h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 6. ASI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ASI_FORMAT[1:0]	R/W	0h	ASI protocol format 0d = TDM mode 1d = I²S mode 2d = LJ (left-justified) mode 3d = Reserved
5-4	ASI_WLEN[1:0]	R/W	3h	ASI word or slot length 0d = 16 bits 1d = 20 bits 2d = 24 bits 3d = 32 bits
3	FSYNC_POL	R/W	0h	ASI FSYNC polarity 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol

Table 6. ASI_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BCLK_POL	R/W	0h	ASI BCLK polarity 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
1	TX_EDGE	R/W	0h	ASI data output (on the primary and secondary data pin) transmit edge 0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL) 1d = Inverted following edge (half cycle delay) with respect to the default edge setting
0	TX_FILL	R/W	0h	ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles

TLV320ADCx140 also supports tri-stating unused channels slots through the ASI_OUT_CH_EN register, as shown in Figure 10.

Figure 10. ASI_OUT_CH_EN Register

7	6	5	4	3	2	1	0
ASI_OUT_CH1_EN	ASI_OUT_CH2_EN	ASI_OUT_CH3_EN	ASI_OUT_CH4_EN	ASI_OUT_CH5_EN	ASI_OUT_CH6_EN	ASI_OUT_CH7_EN	ASI_OUT_CH8_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7. ASI_OUT_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_OUT_CH1_EN	R/W	0h	ASI output channel 1 enable setting 0d = Channel 1 output slot is in a tri-state condition 1d = Channel 1 output slot is enabled
6	ASI_OUT_CH2_EN	R/W	0h	ASI output channel 2 enable setting 0d = Channel 2 output slot is in a tri-state condition 1d = Channel 2 output slot is enabled
5	ASI_OUT_CH3_EN	R/W	0h	ASI output channel 3 enable setting 0d = Channel 3 output slot is in a tri-state condition 1d = Channel 3 output slot is enabled
4	ASI_OUT_CH4_EN	R/W	0h	ASI output channel 4 enable setting 0d = Channel 4 output slot is in a tri-state condition 1d = Channel 4 output slot is enabled
3	ASI_OUT_CH5_EN	R/W	0h	ASI output channel 5 enable setting 0d = Channel 5 output slot is in a tri-state condition 1d = Channel 5 output slot is enabled
2	ASI_OUT_CH6_EN	R/W	0h	ASI output channel 6 enable setting 0d = Channel 6 output slot is in a tri-state condition 1d = Channel 6 output slot is enabled
1	ASI_OUT_CH7_EN	R/W	0h	ASI output channel 7 enable setting 0d = Channel 7 output slot is in a tri-state condition 1d = Channel 7 output slot is enabled
0	ASI_OUT_CH8_EN	R/W	0h	ASI output channel 8 enable setting 0d = Channel 8 output slot is in a tri-state condition 1d = Channel 8 output slot is enabled

To minimize power consumption by preventing pins from floating, the TLV320ADCx140 also supports enabling bus-keepers on SDOUT and SDOUT2 outputs. Register ASI_CFG1 controls the bus-keeper on the outputs through the TX_KEEPER bit field, as shown in Table 8. This register also controls the length of time SDOUT and SDOUT2 strongly drives the least significant bit (LSB) on the bus. This allows fine control so that two devices do not drive different signals on the same bus line at the same time, avoiding bus contention. For example, the LSB of U2 could be set to transmit on the first half of the bit clock cycle, while the MSB of U3 is driving without any offset. Moreover, selecting TX_KEEPER value of 0x2 or 0x3 adds robustness to the system by ensuring the LSB is latched properly by the host processor, since bus-keepers continue holding the bus with the last value driven. Note that this register also controls the number of bit clocks the most significant bit (MSB) is delayed.

Figure 11. ASI_CFG1 Register

7	6	5	4	3	2	1	0
TX_LSB	TX_KEEPER[1:0]		TX_OFFSET[4:0]				
R/W-0h	R/W-0h		R/W-0h				

Table 8. ASI_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_LSB	R/W	0h	ASI data output (on the primary and secondary data pin) for LSB transmissions 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle
6-5	TX_KEEPER[1:0]	R/W	0h	ASI data output (on the primary and secondary data pin) bus keeper 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles
4-0	TX_OFFSET[4:0]	R/W	0h	ASI data MSB slot 0 offset (on the primary and secondary data pin) 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol

To support a greater number of slots than Equation 1 allows, multiple host processor TDM busses can split the TLV320ADCx140 devices connected, as shown in Figure 12. This connection method not only decreases the bit clock (BCLK) speed by half, but also reduces the load capacitance on the data lines SDIN1 and SDIN2 of the host processor.

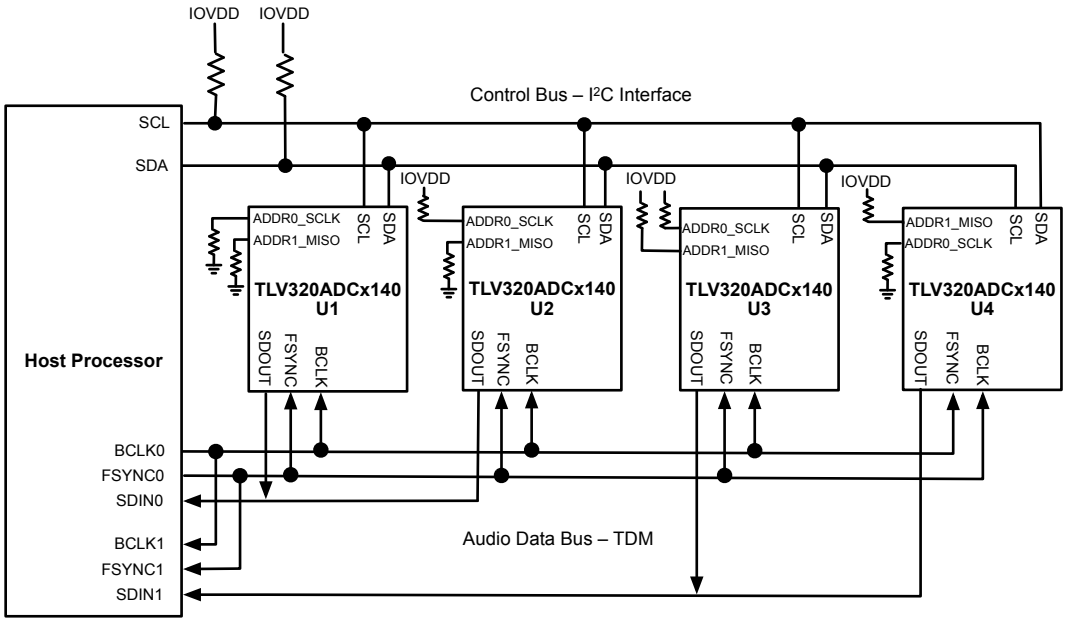

Figure 12. TLV320ADCx140 Shared Split TDM Connection Diagram

Another option is to use the secondary output to map slots of a single device to the primary and secondary output. For example, a system with 12 channels, 32-bit data words, and running with a 96-KHz sample rate requires a bit clock of 36.864 MHz (three devices * four channels/device * 32 bit words * 96 kHz), violating the maximum BCLK speed of 25 MHz. Dividing the 12 channels by assigning six channels to a primary bus and six channels to a secondary bus keeps the BCLK under 25 MHz. Since each device has four channels, one device has two channels assigned to the primary bus and two channels assigned to the secondary bus, as shown in Figure 13.

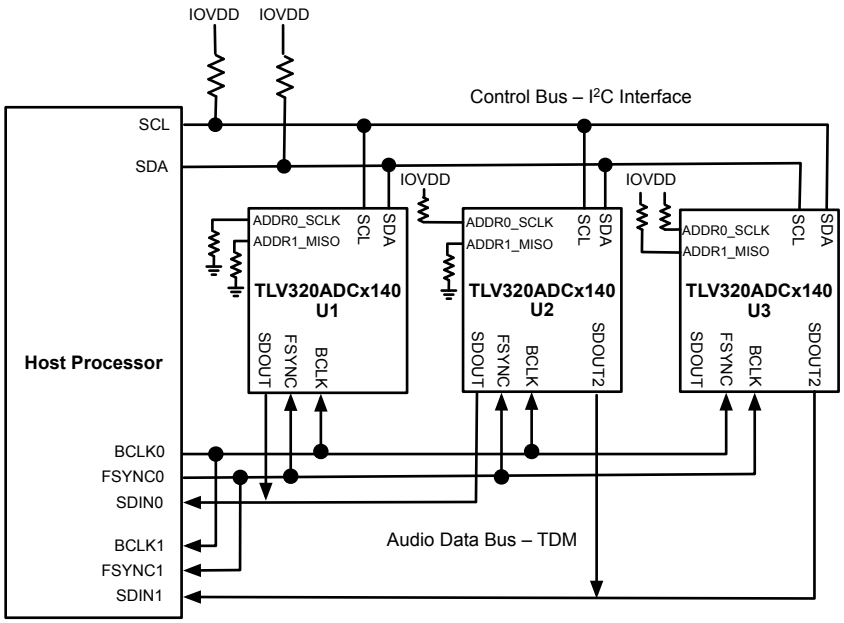

Figure 13. TLV320ADCx140 Shared Split TDM With Primary and Secondary Bus Connection Diagram

For the example of Figure 13, the following I²C script configures U1, U2, and U3 for Shared TDM with primary and secondary bus.

```
w 98 0B 00  # Set U1 Ch1 mapped to slot 0 of SDOUT
w 98 0C 01  # Set U1 Ch2 mapped to slot 1 of SDOUT
w 98 0D 02  # Set U1 Ch3 mapped to slot 2 of SDOUT
w 98 0E 03  # Set U1 Ch4 mapped to slot 3 of SDOUT

w 9A 0B 04  # Set U2 Ch1 mapped to slot 4 of SDOUT
w 9A 0C 05  # Set U2 Ch2 mapped to slot 5 of SDOUT
w 9A 22 30  # Set U2 GPIO1 as SDOUT2
w 9A 0D 40  # Set U2 Ch3 mapped to slot 0 of SDOUT2
w 9A 0E 41  # Set U2 Ch4 mapped to slot 1 of SDOUT2

w 9C 22 30  # Set U3 GPIO1 as SDOUT2
w 9C 0B 42  # Set U3 Ch1 mapped to slot 2 of SDOUT2
w 9C 0C 43  # Set U3 Ch2 mapped to slot 3 of SDOUT2
w 9C 0D 44  # Set U3 Ch3 mapped to slot 4 of SDOUT2
```

3.2 ASI Configuration for Daisy Chain TDM

To simplify board routing and TDM bus timing requirements, or to avoid high SDOUT line load capacitance, TLV320ADCx140 devices offer a daisy-chain mode that routes data output (SDOUT) of one device as input to the GPI1 pin (GPIO1) of another device. Each device internally combines the data into the appropriate slot in the TDM bus and passes it to the next device.

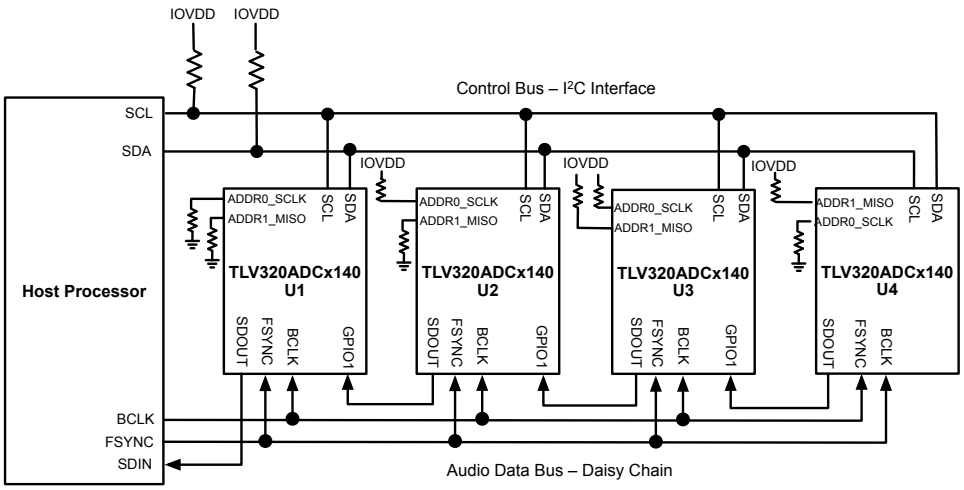

Figure 14. TLV320ADCx140 Daisy Chain TDM Connection Diagram

Setting the ASI_DAISY bit field of the ASI_CFG2 Register shown in Table 9 configures the devices for daisy chain configuration.

Figure 15. ASI_CFG2 Register

7	6	5	4	3	2	1	0
ASI_DAISY	Reserved	ASI_ERR	ASI_ERR_RCOV	Reserved			
R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h			

Table 9. ASI_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ASI_DAISY	R/W	0h	ASI daisy-chain connection 0d = All devices are connected in the common ASI bus 1d = All devices are daisy-chained for the ASI bus
6	Reserved	R	0h	Reserved

Table 9. ASI_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ASI_ERR	R/W	0h	ASI bus error detection 0d = Enable bus error detection 1d = Disable bus error detection
4	ASI_ERR_RCOV	R/W	0h	ASI bus error auto resume 0d = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remains powered down until the host configures the device
3-0	Reserved	R	0h	Reserved

For all the devices that take the SDOUT as input from another device into the GPIO1 pin, the bit filed GPIO1_CFG of the GPIO_CFG0 register must be set to "ASI Input for daisy chain (SDIN)," as shown in Table 10.

Figure 16. GPIO_CFG0 Register

7	6	5	4	3	2	1	0
GPIO1_CFG[3:0]				Reserved	GPIO1_DRV[2:0]		
R/W-2h				R-0h	R/W-2h		

Table 10. GPIO_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO1_CFG[3:0]	R/W	2h	GPIO1 configuration 0d = GPIO1 is disabled 1d = GPIO1 is configured as a general-purpose output (GPO) 2d = GPIO1 is configured as a device interrupt output (IRQ) 3d = GPIO1 is configured as a secondary ASI output (SDOUT2) 4d = GPIO1 is configured as a PDM clock output (PDMCLK) 5d to 7d = Reserved 8d = GPIO1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO1 is configured as a general-purpose input (GPI) 10d = GPIO1 is configured as a master clock input (MCLK) 11d = GPIO1 is configured as an ASI input for daisy-chain (SDIN) 12d = GPIO1 is configured as a PDM data input for channel 1 and channel 2 (PDMDIN1) 13d = GPIO1 is configured as a PDM data input for channel 3 and channel 4 (PDMDIN2) 14d = GPIO1 is configured as a PDM data input for channel 5 and channel 6 (PDMDIN3) 15d = GPIO1 is configured as a PDM data input for channel 7 and channel 8 (PDMDIN4)
3	Reserved	R	0h	Reserved
2-0	GPIO1_DRV[2:0]	R/W	2h	GPIO1 output drive configuration (not used when GPIO1 is configured as SDOUT2) 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved

For the example of Figure 14, the following I^{2}C script configures U1, U2, and U3 for daisy chain, taking input from the next device in the SDOUT through GPIO1 of the chain. Note that channels of each device are mapped to slots 0-3. However, the SDOUT of U1 has slots 0-3 with the U1 channels, slots 4-7 with the U2 channels, slots 8-11 with the U3 channels, and slots 12-15 with the U4 channels. Note that the last device in the daisy chain does not need to be configured for daisy chain mode since it is not taking input on GPIO1 from another device.

```
w 98 0B 00  # Set U1 Ch1 mapped to slot 0 of SDOUT
w 98 0C 01  # Set U1 Ch2 mapped to slot 1 of SDOUT
w 98 0D 02  # Set U1 Ch3 mapped to slot 2 of SDOUT
w 98 0E 03  # Set U1 Ch4 mapped to slot 3 of SDOUT
```

```
w 9A 0B 00  # Set U2 Ch1 mapped to slot 0 of SDOUT
w 9A 0C 01  # Set U2 Ch2 mapped to slot 1 of SDOUT
w 9A 0D 02  # Set U2 Ch3 mapped to slot 2 of SDOUT
w 9A 0E 03  # Set U2 Ch4 mapped to slot 3 of SDOUT

w 9C 0B 00  # Set U3 Ch1 mapped to slot 0 of SDOUT
w 9C 0C 01  # Set U3 Ch2 mapped to slot 1 of SDOUT
w 9C 0D 02  # Set U3 Ch3 mapped to slot 2 of SDOUT
w 9C 0E 03  # Set U3 Ch4 mapped to slot 3 of SDOUT

w 9E 0B 00  # Set U4 Ch1 mapped to slot 0 of SDOUT
w 9E 0C 01  # Set U4 Ch1 mapped to slot 1 of SDOUT
w 9E 0D 02  # Set U4 Ch1 mapped to slot 2 of SDOUT
w 9E 0E 03  # Set U4 Ch1 mapped to slot 3 of SDOUT

w 98 09 80  # Set U1's ASI to daisy chain
w 98 21 B0  # Set U1's GPIO1 input as ASI input for daisy chain

w 9A 09 80  # Set U2's ASI to daisy chain
w 9A 21 B0  # Set U2's GPIO1 input as ASI input for daisy chain

w 9C 09 80  # Set U3's ASI to daisy chain
w 9C 21 B0  # Set U3's GPIO1 input as ASI input for daisy chain
```

4 Configuring PurePath™ Console for Multiple TLV320ADCx140 EVMs

The PurePath Console supports multiple TLV320ADCx140 devices connected to a single AC-MB. However, the AC-MB connector can only be connected to one TLV320ADCx140. To connect additional devices to a single AC-MB, externally wire power, ground, I^2C, and TDM signals of the board connected to a single AC-MB to the respective signals of the other TLV320ADCx140 EVMs. Connect only one EVM to the AC-MB while connecting the other signals through their respective headers or jumpers as follows:

- Connect together IOVDD from all the TLV320ADCx140 EVMs through the JMP2 jumper.
- Connect together AVDD from all the TLV320ADCx140 EVMs through the JMP1 jumper.
- Connect together SHDNz from all the TLV320ADCx140 devices through the SHDNz test point.
- Connect together the SCL pins from all TLV320ADCx140 devices through the SCL test point.
- Connect together the SDA pins from all TLV320ADCx140 devices through the SDA test point.
- Connect together the BCLK pins from all TLV320ADCx140 devices through the BCLK test point.
- Connect together the FSYNC pins from all TLV320ADCx140 devices through the FSYNC test point.
- SDOUT connections depend on Shared TDM or Daisy-Chain TDM mode:
  - For Shared TDM mode, connect together the SDOUT pins from all TLV320ADCx140 devices through the DOUT test point.
  - For Daisy-Chain TDM mode, connect the TLV320ADCx140 EVMs in a daisy chain fashion:
    - Connect the GPIO1 signal at the header J13, pin1 (GPIO1) from the board connected to the AC-MB to the SDOUT pin of the second board through the DOUT test point.
    - Connect the signal of the second board at the header J13, pin1 (GPIO1) to the SDOUT pin of the third board through the DOUT test pin, if using three devices or more.
    - Connect the signal of the third board at the header J13, pin1 (GPIO1) to the SDOUT pin of the fourth board through the DOUT test pin, if using four devices.

These signals can be tapped at the respective digital test points of the TLV320ADCx140 EVMs, as shown in Figure 17.

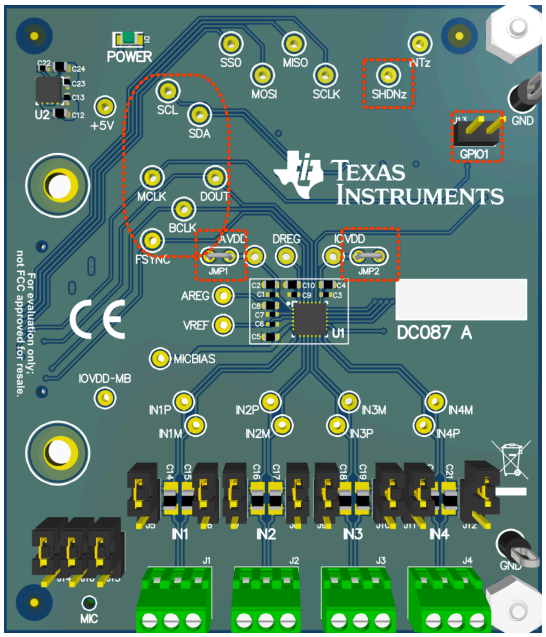

Figure 17. Location of TLV320ADCx140 EVM I²C and TDM signals

4.1 Changing the Default I²C Address of the TLV320ADCx140 EVM

When multiple TLV320ADCx140 EVMs are connected to a single I2C bus, each EVM must have a unique I²C address. The I²C address is set by pullups and pulldowns on the Control and GPIO Selection at the underside of the board, as shown in Figure 18. Placement of the resistors in this section, as shown in Table 11, controls the I2C address of each TLV320ADCx140 device.

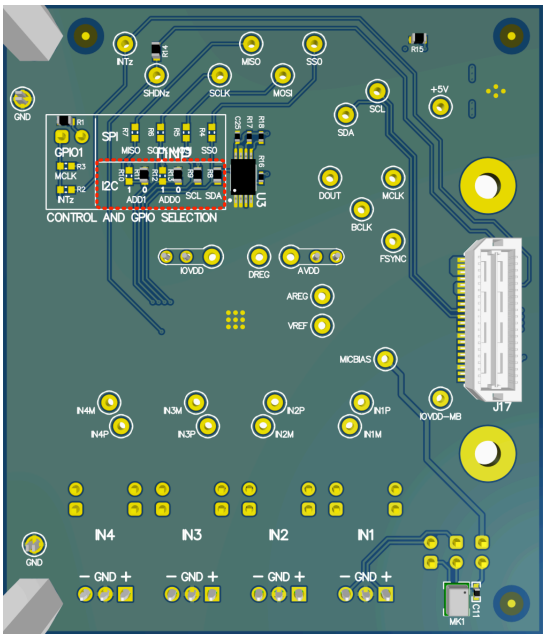

Figure 18. I²C Address Configuration for the TLV320ADx140 EVM

Table 11. TLV320ADCx140 EVM I²C Slave Address

ADD1		ADD0		I²C SLAVE ADDRESS (BINARY)
1	0	1	0	
Not Installed	Installed	Not Installed	Installed	1001 100
Not Installed	Installed	Installed	Not Installed	1001 101
Installed	Not Installed	Not Installed	Installed	1001 110
Installed	Not Installed	Installed	Not Installed	1001 111

4.2 Launching PurePath Console with Multiple Devices

When PurePath Console is launched, it queries the user on how many devices are connected to an AC-MB, as shown in Figure 19. In this dialog window, after selecting two TLV320ADC5140 devices and clicking on Next, the main window shown in Figure 20 launches.

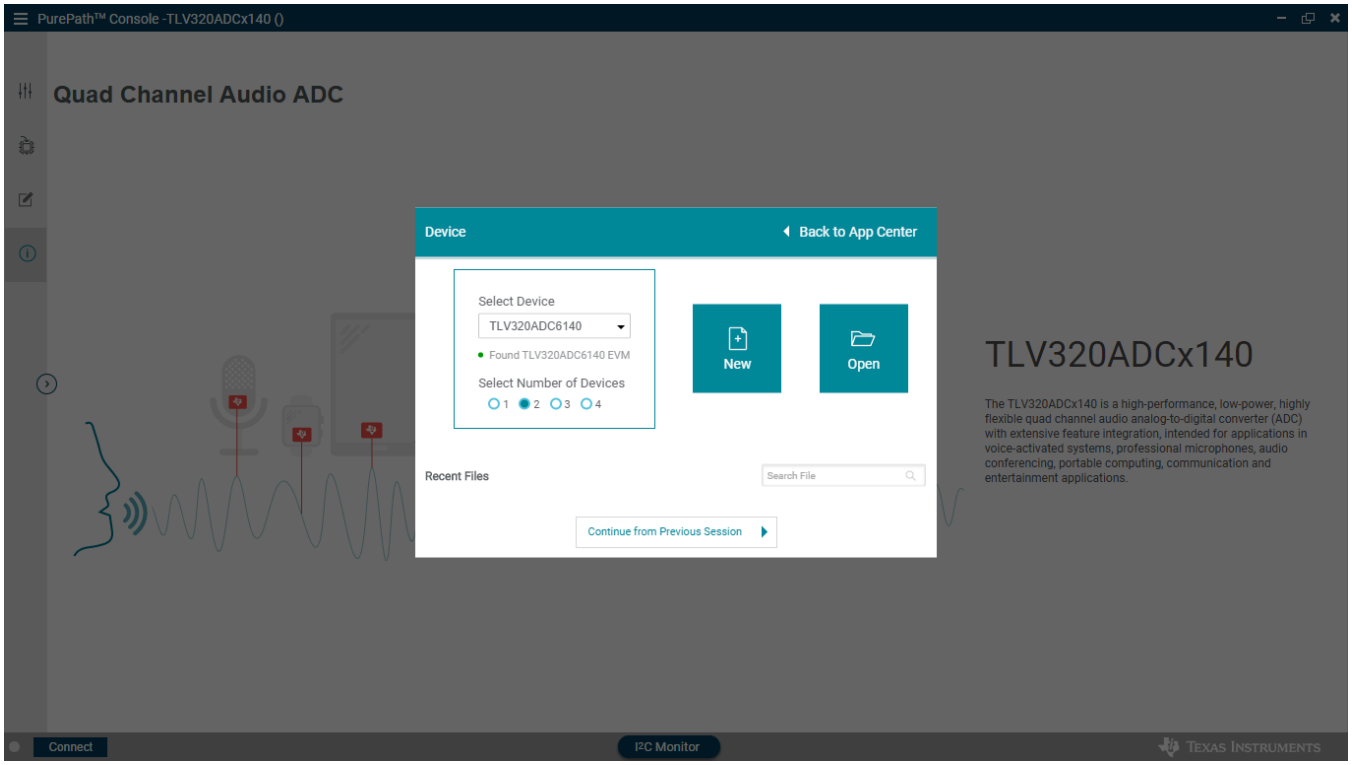

Figure 19. PurePath Console Input Number of Devices Dialog

PurePath Console configures only one device at a time. The devices are labeled by a device icon with a letter at the top of the screen, as shown in Figure 20. Clicking on device icon A programs the lower number I²C address, B programs the next I²C address, and so forth.

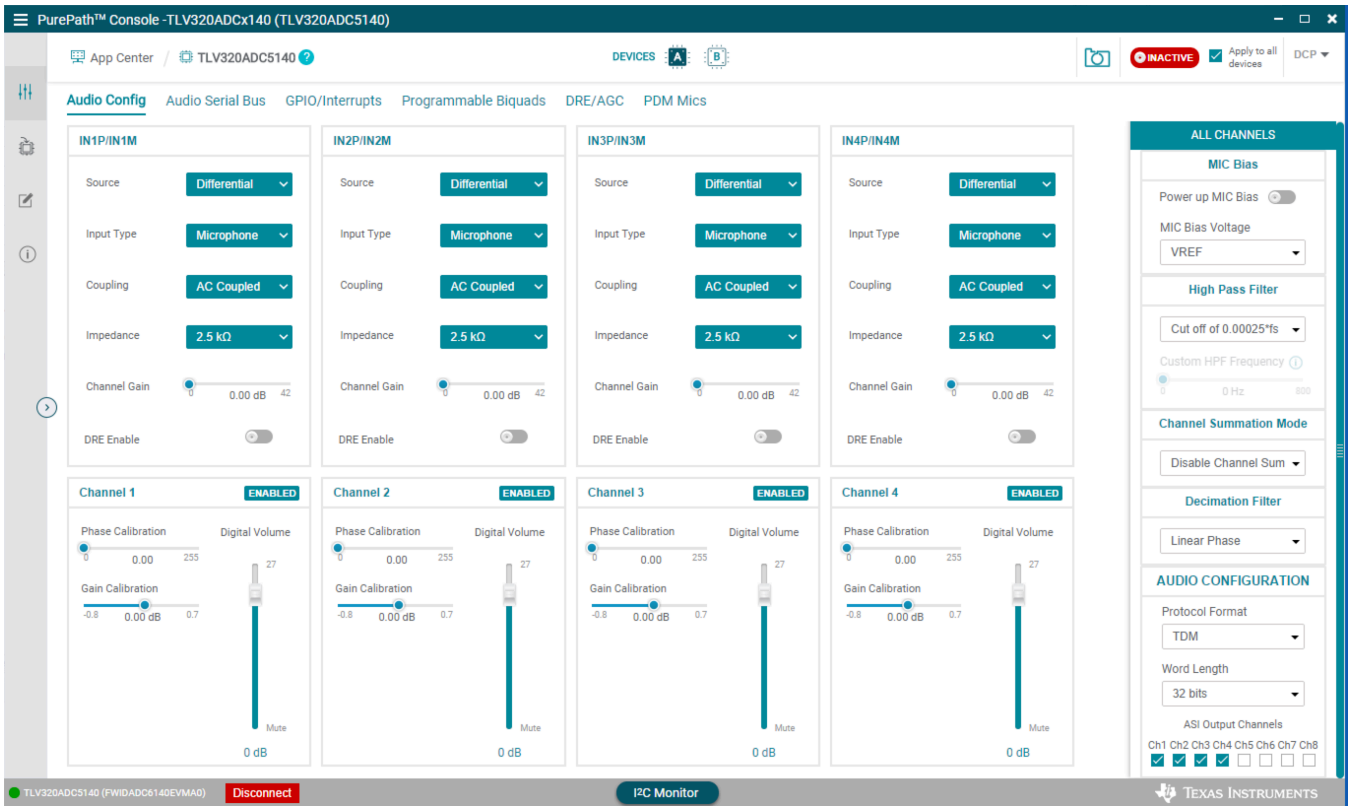

Figure 20. PurePath Console Main Window

The Audio Serial Bus tab assigns each channel of a device to a slot. In Figure 21, the device A input channels 1-4 are assigned to slots 0-3, respectively. In Figure 22, the device B input channels 1-4 are assigned to slots 4-7. Note that the previous slots in the TDM bus are not shown, but an ellipsis at the beginning of the audio interface signal line plot in BCLK, FSYNC, and SDOUT signifies that other slots precede these slots.

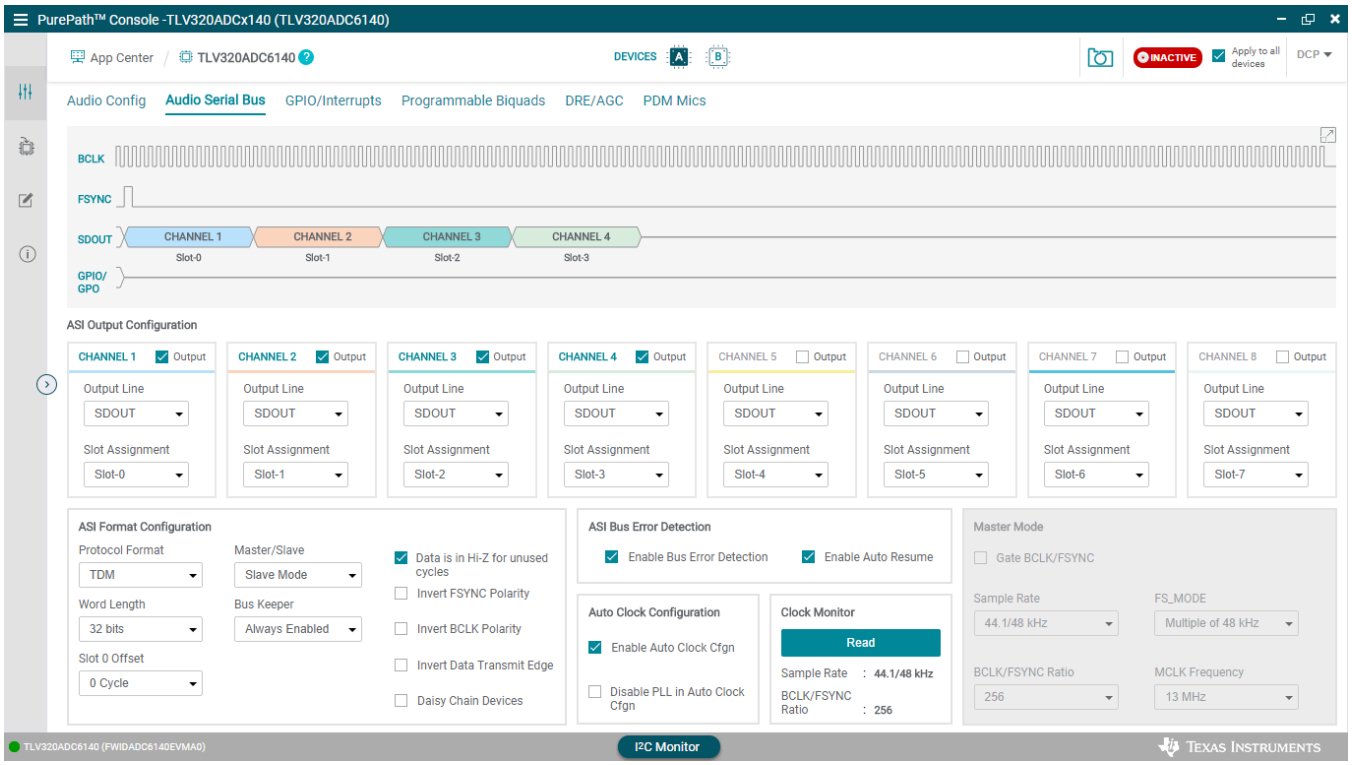

Figure 21. PurePath Console Device A Channel to Slot Mapping

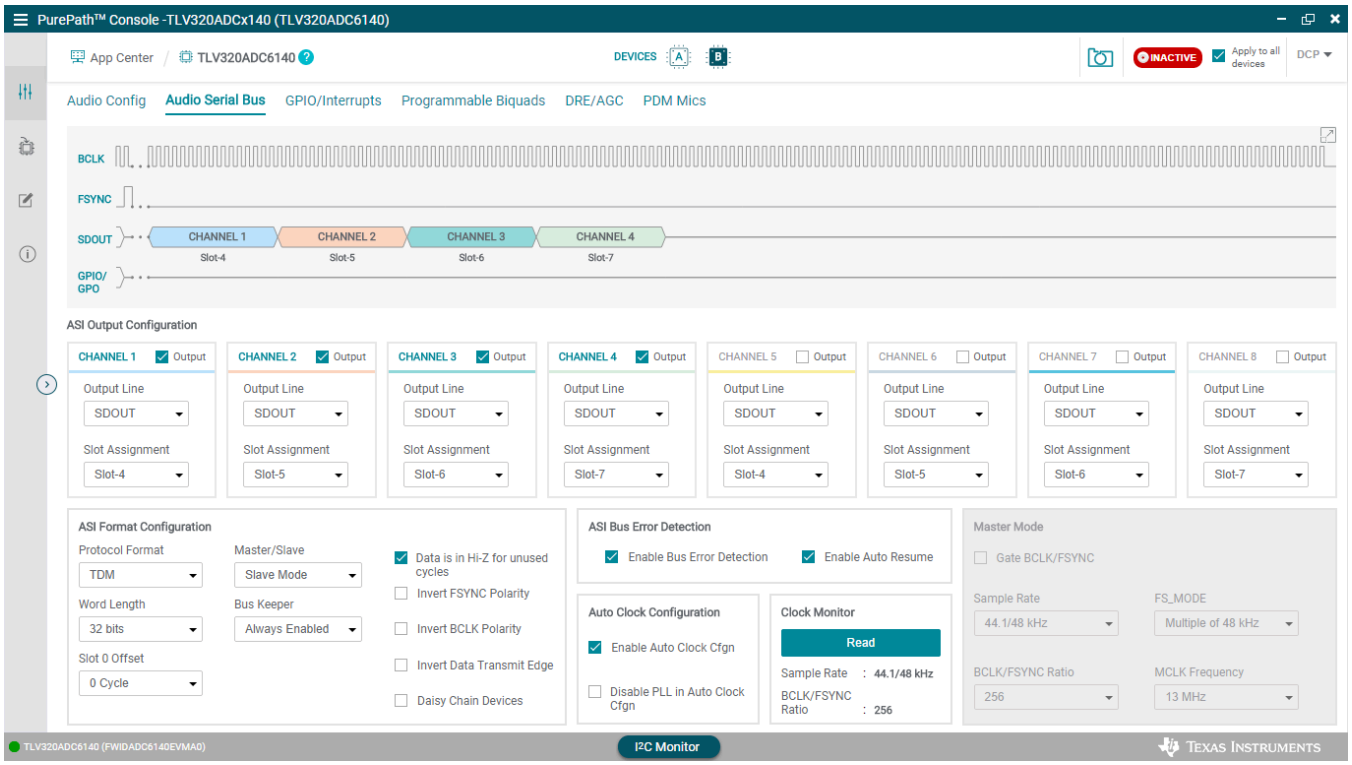

Figure 22. PurePath Console Device B Channel to Slot Mapping

Clicking on the upper right window expansion icon of the Audio Serial Bus graphic shows all slots and all devices, as shown in Figure 23.

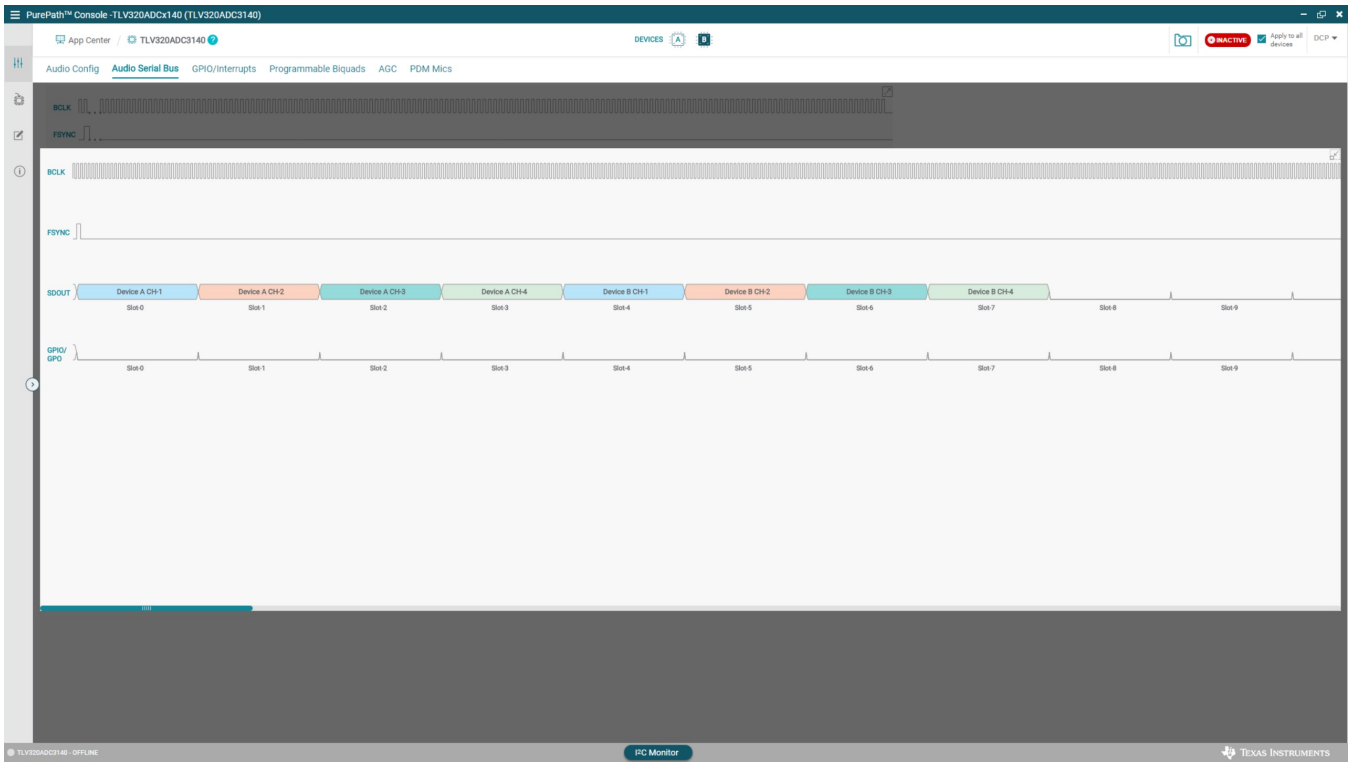

Figure 23. PurePath Console Channel to Slot Mapping for Device A and B

PurePath Console I²C Scripts

A.1 TLV320ADCx140 I²C Scripts for Shared TDM

The following I²C scripts sets four devices for shared TDM mode, after devices are reset:

```
# Key: w NN YY ZZ ==> write to I2C address 0xNN, to register 0xYY, data 0xZZ
#               # ==> comment delimiter
#
# I2C programming script for four devices sharing a TDM bus
#  U4(SDOUT) -> U3 (SDOUT) -> U2 (SDOUT) -> U1 (SDOUT) -> Host Processor
#
##############################################################################
# Power-up Sequence:
# Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Release SHDNZ to HIGH.
# Wait for 1ms.
##############################################################################

# Wake-up devices
w 98 02 81  # Wake-up Device U1
w 9A 02 81  # Wake-up Device U2
w 9C 02 81  # Wake-up Device U3
w 9E 02 81  # Wake-up Device U4
d 10        # 10 ms delay

# Program Device A (U1)
w 98 00 00  # Set Device page register to Page 0
w 98 07 31  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity,
            # default TX edge, Hi-Z for unused cycles
w 98 08 A0  # ASI transmit LSB for 1st half cycle, Hi-Z for second half cycle,
            # bus keeper always enabled
w 98 0B 00  # ASI primary output (SDOUT) with CH1 assigned to slot 0
w 98 0C 01  # ASI primary output (SDOUT) with CH2 assigned to slot 1
w 98 0D 02  # ASI primary output (SDOUT) with CH3 assigned to slot 2
w 98 0E 03  # ASI primary output (SDOUT) with CH4 assigned to slot 3
w 98 73 F0  # Enable Ch1-4 of Device A
w 98 74 F0  # Enable Ch1-4 ASI output of Device A

# Program Device B (U2)
w 9A 00 00  # Set Device page register to Page 0
w 9A 07 31  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity,
            # default TX edge, Hi-Z for unused cycles
w 9A 08 80  # ASI transmit LSB for 1st half cycle, Hi-Z for second half cycle,
            # bus keeper disabled
w 9A 0B 04  # ASI primary output (SDOUT) with CH1 assigned to slot 4
w 9A 0C 05  # ASI primary output (SDOUT) with CH2 assigned to slot 5
w 9A 0D 06  # ASI primary output (SDOUT) with CH3 assigned to slot 6
w 9A 0E 07  # ASI primary output (SDOUT) with CH4 assigned to slot 7
w 9A 73 F0  # Enable Ch1-4 of Device B
w 9A 74 F0  # Enable Ch1-4 ASI output of Device B

# Program Device C (U3)
w 9C 00 00  # Set Device page register to Page 0
w 9C 07 31  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity,
            # default TX edge, Hi-Z for unused cycles
```

```
w 9C 08 80  # ASI transmit LSB for 1st half cycle, Hi-Z for second half cycle,
            # bus keeper disabled
w 9C 0B 08  # ASI primary output (SDOUT) with CH1 assigned to slot 8
w 9C 0C 09  # ASI primary output (SDOUT) with CH2 assigned to slot 9
w 9C 0D 0A  # ASI primary output (SDOUT) with CH3 assigned to slot 10
w 9C 0E 0B  # ASI primary output (SDOUT) with CH4 assigned to slot 11
w 9C 73 F0  # Enable Ch1-4 of Device C
w 9C 74 F0  # Enable Ch1-4 ASI output of Device C

# Program Device D (U4)
w 9E 00 00  # Set Device page register to Page 0
w 9E 07 31  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity,
            # default TX edge, Hi-Z for unused cycles
w 9E 08 80  # ASI transmit LSB for 1st half cycle, Hi-Z for second half cycle,
            # bus keeper disabled
w 9E 0B 0C  # ASI primary output (SDOUT) with CH1 assigned to slot 12
w 9E 0C 0D  # ASI primary output (SDOUT) with CH2 assigned to slot 13
w 9E 0D 0E  # ASI primary output (SDOUT) with CH3 assigned to slot 14
w 9E 0E 0F  # ASI primary output (SDOUT) with CH4 assigned to slot 15
w 9E 73 F0  # Enable Ch1-4 of Device D
w 9E 74 F0  # Enable Ch1-4 ASI output of Device D

# Power-up Devices A, B, C, & D
w 98 75 60  # Power up ADC and PLL of Device A
w 9A 75 60  # Power up ADC and PLL of Device B
w 9C 75 60  # Power up ADC and PLL of Device C
w 9E 75 60  # Power up ADC and PLL of Device D
```

A.2 TLV320ADCx140 I²C Scripts for Daisy Chain TDM

The following I²C scripts sets four devices for Daisy-Chain TDM mode, after devices are reset:

```
# Key: w NN YY ZZ ==> write to I2C address 0xNN, to register 0xYY, data 0xZZ
#               # ==> comment delimiter
#
# I2C programming script for four devices in daisy chain TDM mode
#  U4(SDOUT) -> (GPIO1) U3 (SDOUT) -> (GPIO1) U2 (SDOUT) -> (GPIO1) U1 (SDOUT) -> Host Processor
#
##############################################################################
# Power-up Sequence:
# Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Release SHDNZ to HIGH.
# Wait for 1ms.
##############################################################################

# Wake-up devices
w 98 02 81  # Wake-up Device U1
w 9A 02 81  # Wake-up Device U2
w 9C 02 81  # Wake-up Device U3
w 9E 02 81  # Wake-up Device U4
d 10        # 10 ms delay

# Program Device A (U1)
w 98 00 00  # Set Device A page register to Page 0
w 98 07 31  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity,
            # default TX edge, Hi-Z for unused cycles
w 98 08 A0  # ASI transmit LSB for 1st half cycle, Hi-Z for second half cycle,
            # bus keeper always enabled
w 98 09 80  # ASI to daisy chain connection with bus error detection and
            # auto resume after bus error recovery
w 98 21 B0  # GPIO1 input as ASI input for daisy chain
w 98 0B 00  # ASI primary output (SDOUT) with CH1 assigned to slot 0
w 98 0C 01  # ASI primary output (SDOUT) with CH2 assigned to slot 1
w 98 0D 02  # ASI primary output (SDOUT) with CH3 assigned to slot 2
w 98 0E 03  # ASI primary output (SDOUT) with CH4 assigned to slot 3
```

```
w 98 73 F0  # Enable Ch1-4 of Device A
w 98 74 F0  # Enable Ch1-4 ASI output of Device A

# Program Device B (U2)
w 9A 00 00  # Set Device page register to Page 0
w 9A 07 31  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity,
            # default TX edge, Hi-Z for unused cycles
w 9A 08 80  # ASI transmit LSB for 1st half cycle, Hi-Z for second half cycle,
            # bus keeper disabled
w 9A 09 80  # ASI to daisy chain connection with bus error detection and
            # auto resume after bus error recovery
w 9A 21 B0  # GPIO1 input as ASI input for daisy chain
w 9A 0B 04  # ASI primary output (SDOUT) with CH1 assigned to slot 4
w 9A 0C 05  # ASI primary output (SDOUT) with CH2 assigned to slot 5
w 9A 0D 06  # ASI primary output (SDOUT) with CH3 assigned to slot 6
w 9A 0E 07  # ASI primary output (SDOUT) with CH4 assigned to slot 7
w 9A 73 F0  # Enable Ch1-4 of Device B
w 9A 74 F0  # Enable Ch1-4 ASI output of Device B

# Program Device C (U3)
w 9C 00 00  # Set Device page register to Page 0
w 9C 07 31  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity,
            # default TX edge, Hi-Z for unused cycles
w 9C 08 80  # ASI transmit LSB for 1st half cycle, Hi-Z for second half cycle,
            # bus keeper disabled
w 9C 09 80  # ASI to daisy chain connection with bus error detection and
            # auto resume after bus error recovery
w 9C 21 B0  # GPIO1 input as ASI input for daisy chain
w 9C 0B 08  # ASI primary output (SDOUT) with CH1 assigned to slot 8
w 9C 0C 09  # ASI primary output (SDOUT) with CH2 assigned to slot 9
w 9C 0D 0A  # ASI primary output (SDOUT) with CH3 assigned to slot 10
w 9C 0E 0B  # ASI primary output (SDOUT) with CH4 assigned to slot 11
w 9C 73 F0  # Enable Ch1-4 of Device C
w 9C 74 F0  # Enable Ch1-4 ASI output of Device C

# Program Device D (U4)
w 9E 00 00  # Set Device page register to Page 0
w 9E 07 31  # ASI Format TDM with 32-bit word length, default FSYNC and BCLK polarity,
            # default TX edge, Hi-Z for unused cycles
w 9E 08 80  # ASI transmit LSB for 1st half cycle, Hi-Z for second half cycle,
            # bus keeper disabled
w 9E 0B 0C  # ASI primary output (SDOUT) with CH1 assigned to slot 12
w 9E 0C 0D  # ASI primary output (SDOUT) with CH2 assigned to slot 13
w 9E 0D 0E  # ASI primary output (SDOUT) with CH3 assigned to slot 14
w 9E 0E 0F  # ASI primary output (SDOUT) with CH4 assigned to slot 15
w 9E 73 F0  # Enable Ch1-4 of Device D
w 9E 74 F0  # Enable Ch1-4 ASI output of Device D

# Power-up Devices A, B, C, & D
w 98 75 60  # Power up ADC and PLL of Device A
w 9A 75 60  # Power up ADC and PLL of Device B
w 9C 75 60  # Power up ADC and PLL of Device C
w 9E 75 60  # Power up ADC and PLL of Device D
```

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (November 2019) to B Revision	Page
• Added note describing constraints on systems with BCLK > 18.5 MHz in *Section 3*	4

Changes from Original (April 2019) to A Revision	Page
• Reworded *Section 1*	2

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