SAE STANDARD J1850

CLASS B DATA COMMUNICATION NETWORK INTERFACE

2/15/94

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1 OBJECTIVES AND SCOPE

1.1 Objectives - This document constitutes the requirements for a vehicle data communications network. These requirements are related to the lowest two layers of the ISO Open System Interconnect (OSI) model (Ref. ISO 7498). These layers are the Data Link Layer and the Physical Layer. This network has been described using the ISO conventions in ISO/TC 22/SC 3/WG1 N429 E, dated October, 1990. Both documents are intended to describe the same network requirements but using different descriptive styles. If any technical differences are identified, the very latest revision of these documents should be used.

This is an SAE Recommended Practice which has been submitted as an American National Standard. As such, its format is somewhat different from the formal ISO description in that descriptions have been expanded, but are in no way less precise. A more textual format has been adopted herein to allow explanations to be included.

The vehicle application for this class of data communication (Class B) network is defined (Reference SAE J1213 APR88) to allow the sharing of vehicle parametric information. Also per the definition, this Class B network shall be capable of performing Class A functions.

1.2 Scope - This document establishes the requirements for a Class B Data Communication Network Interface applicable to all On and Off-Road Land Based Vehicles. It defines a minimum set of data communication requirements such that the resulting network is cost effective for simple applications and flexible enough to use in complex applications. Taken in total, the requirements contained in this document specify a data communications network that satisfies the needs of automotive manufacturers.

This specification describes two specific implementations of the network, based on media / Physical Layer differences. One Physical Layer is optimized for a data rate of 10.4 Kbps while the other Physical Layer is optimized for a data rate of 41.6 Kbps (see Appendix A for a checklist of application specific features).

Although devices may be constructed that can be configured to operate in either of the two primary implementations defined herein, it is expected that most manufacturers will focus specifically on either the 10.4 Kbps implementation or the 41.6 Kbps implementation depending on their specific application and corporate philosophy toward network usage. However, low volume users of network interface devices are expected to find it more effective to use a generic interface capable of handling either of the primary implementations specified in this document.

This SAE document is under the control and maintenance of the Vehicle Networks for Multiplexing and Data Communications (Multiplex) Committee. This committee will periodically review and update this document as needs dictate.

2 REFERENCES AND RELATED DOCUMENTS

2.1 SAE Documents

J1113 AUG87 Electromagnetic Susceptibility Measurements Procedures for Vehicle Components

J1211 NOV78 A Recommended Environmental Procedure for Electronic Equipment Design

J1213/1 APR88 Glossary of Vehicle Networks for Multiplexing and Data Communications

J1547 OCT88 Electromagnetic Susceptibility Measurement Procedures for Common Mode Injection

J1879 OCT88 General Qualification and Production Acceptance Criteria for Integrated Circuits in Automotive Applications

J1930 SEP91 Electrical/Electronic Systems Diagnostic Terms, Definitions, Abbreviations, & Acronyms

J1962 JUN92 Diagnostic Connector

J1979 DEC91 E/E Diagnostic Test Modes

J2012 MAR92 Diagnostic Codes/Messages

J2178/1 JUN92 Class B Data Communication Network Messages

J2190 JUN93 Enhanced E/E Diagnostic Test Modes

2.2 ISO Documents

ISO/TC22/SC3/WG1 N429E OCT. 90 Road Vehicles - Serial Data Communication for Automotive Applications, Low Speed (125 Kbps and Below)

ISO 7498 Data Processing Systems - Open Systems Interconnection - Standard Reference Model

2.3 CISPR Documents

CISPR/D/WG2 (Secretariat) 19 Sept 1989 Radiated Emissions Antenna and Probe Test

2.4 Definitions and Abbreviations

2.4.1 Definitions

Active State - The state of a bus wire which results when one or more nodes have "turned on" their physical layer circuitry. This is V_{oh} volts for Bus + (PWM and VPW) and V_{ol} volts for Bus - (PWM only). Refer to Tables 4 (PWM DC Parameters) and 6 (VPW DC Parameters) for the values of V_{oh} and V_{ol}. The active state voltage level is determined by the source voltage of the physical layer drive circuitry.

Arbitration - The process of resolving which frame, or In-Frame Response data, continues to be transmitted when two or more nodes begin transmitting frames, or In-Frame Response data, simultaneously.

Class A Data Communications - A system whereby vehicle wiring is reduced by the transmission and reception of multiple signals over the same signal bus between nodes that would have been accomplished by individual wires in a conventionally wired vehicle. The nodes used to accomplish multiplexed body wiring typically did not exist in the same or similar form in a conventionally wired vehicle.

Class B Data Communications - A system whereby data (e.g., parametric data values) is transferred between nodes to eliminate redundant sensors and other system elements. The nodes in this form of a multiplex system typically already existed as stand-alone modules in a conventionally wired vehicle. A Class B network shall also be capable of performing Class A functions.

Class C Data Communications - A system whereby high data rate signals typically associated with real time control systems, such as engine controls and anti-lock brakes, are sent over the signal bus to facilitate distributed control and to further reduce vehicle wiring. A Class C network shall also be capable of performing Class A and Class B functions.

Dominant Bit - A bit which wins arbitration when contending for the bus. For SAE J1850, a logic "0" is the dominant bit.

Dual Wire - Two wires that are routed adjacently throughout the network and can be either a twisted or a parallel pair of wires.

Fault Tolerance - The ability of a system to survive a certain number of failures with allowance for possible down-graded performance while maintaining message transmission capability at the specified data rate.

Frame - One complete transmission of information, which may or may not include an "in-frame response." For this network, each frame contains one and only one message. A frame is delineated by the Start of Frame (SOF) and End of Frame (EOF) symbols.

Functional Addressing - Labeling of messages based on their operation code or data content. See paragraph 5.1.2 for an example of the typical usage for functional addressing.

Message - All of the data bytes contained in a frame. The message is what is left after the frame symbols have been removed from the frame. As such, the message is the sequence of bytes contained in the frame.

Passive State - The state of a bus wire which results when all nodes have "turned off" their physical layer circuitry. This is V_{ol} volts for Bus + (PWM and VPW) and V_{oh} volts for Bus - (PWM only). Refer to Tables 4 (PWM DC Parameters) and 6 (VPW DC Parameters) for the values of V_{oh} and V_{ol}. The passive state voltage level is determined by the reference voltage of the bus wire termination resistor(s).

Physical Addressing - Labeling of messages for the physical location of their source and/or destination(s). See paragraph 5.1.1 for an example of the typical usage for physical addressing.

Pulse Width Modulation (PWM) - A data bit format, where the width of a pulse of constant voltage or current determines the value (typically one or zero) of the data transmitted.

Recessive Bit - A bit which loses arbitration when contending for the bus with a dominant bit. For SAE J1850, a logic "1" is the recessive bit.

Sleep-Mode - Node behavior in a low power consumption standby state waiting to be switched on by a frame or other activity. This is distinct from an off mode where the node is disconnected from the power supply.

Variable Pulse Width (VPW) Modulation - A method of using both the state of the bus and the width of the pulse to encode bit information. This encoding technique is used to reduce the number of bus transitions for a given bit rate. One embodiment would define a "ONE" (1) as a short active pulse or a long passive pulse while a "ZERO" (0) would be defined as a long active pulse or a short passive pulse. Since a frame is comprised of random 1's and 0's, general byte or frame times cannot be predicted in advance.

2.4.2 Abbreviations / Acronyms

BRK: Break
CRC: Cyclic Redundancy Check
E/E: Electrical and Electronic
EMC: Electromagnetic Compatibility
EMI: Electromagnetic Interference
EOD: End of Data
EOF: End of Frame
IFR: In-Frame Response (Byte/Bytes)
IFS: Inter-Frame Separation
ISO: International Standards Organization
Kbps: Kilo bits per second
NA: Not Applicable
NB: Normalization Bit
OSI: Open System Interconnect
SOF: Start of Frame

3 DESCRIPTION OF THE ARCHITECTURE

3.1 General - It is the intent of this network to interconnect different electronic modules on the vehicle using an "Open Architecture" approach. An open architecture network is one in which the addition or deletion of one or more modules (data nodes) has minimal hardware and/or software impact on the remaining modules.

In order to support an open architecture approach, the Class B network utilizes the concept of Carrier Sense Multiple Access (CSMA) with non-destructive contention resolution. Additionally this network supports the prioritization of frames such that, in the case of contention, the higher priority frames will always win arbitration and be completed.

3.2 Network Topology

3.2.1 Data Bus Topology - Data bus topology is the map of physical connections of the data bus nodes to the data bus. It includes all nodes and data buses involved in the data bus integration of the vehicle. A single-level bus topology, the simplest bus topology, is currently being used in several automotive applications. In a single-level bus topology, all nodes are interconnected via the same data bus. The redundancy requirements of a particular application may require a single-level topology to be implemented using multiple interconnecting cables operating in various modes (active or passive). However, the requirement to use multiple buses for redundancy purposes does not change the single-level bus topology definition if the following criteria are maintained:

a. All nodes/devices transmit and receive from a single path.
b. All nodes/devices receive all frames at the same time.
c. Communication on each data bus is identical.

3.2.2 Data Bus Control - Although various methods of data bus control can be used, this Class B network is intended for "masterless" bus control. The principal advantage of the masterless bus control concept is its ability to provide the basis for an open architecture data communications system. Since a master does not exist, each node has an equal opportunity to initiate a data transmission once an idle bus has been detected. However, not all nodes and/or data are of equal importance, prioritization of frames is allowed and the highest priority frame will always be completed. This also implies that frame/data contention will not result in lost data. Two disadvantages of the masterless bus concept are that data latency cannot be guaranteed, except for the single highest system priority frame, and bus utilization extremes are difficult to evaluate.

3.3 References to the OSI Model - Although this document focuses on the data link layer and the physical layer, references are included for the application layer since this needs to be included for emission related, diagnostic communication legislation requirements. The Class B network maps into the OSI model as described in the following paragraphs. This "mapping" is illustrated in Figure 1.

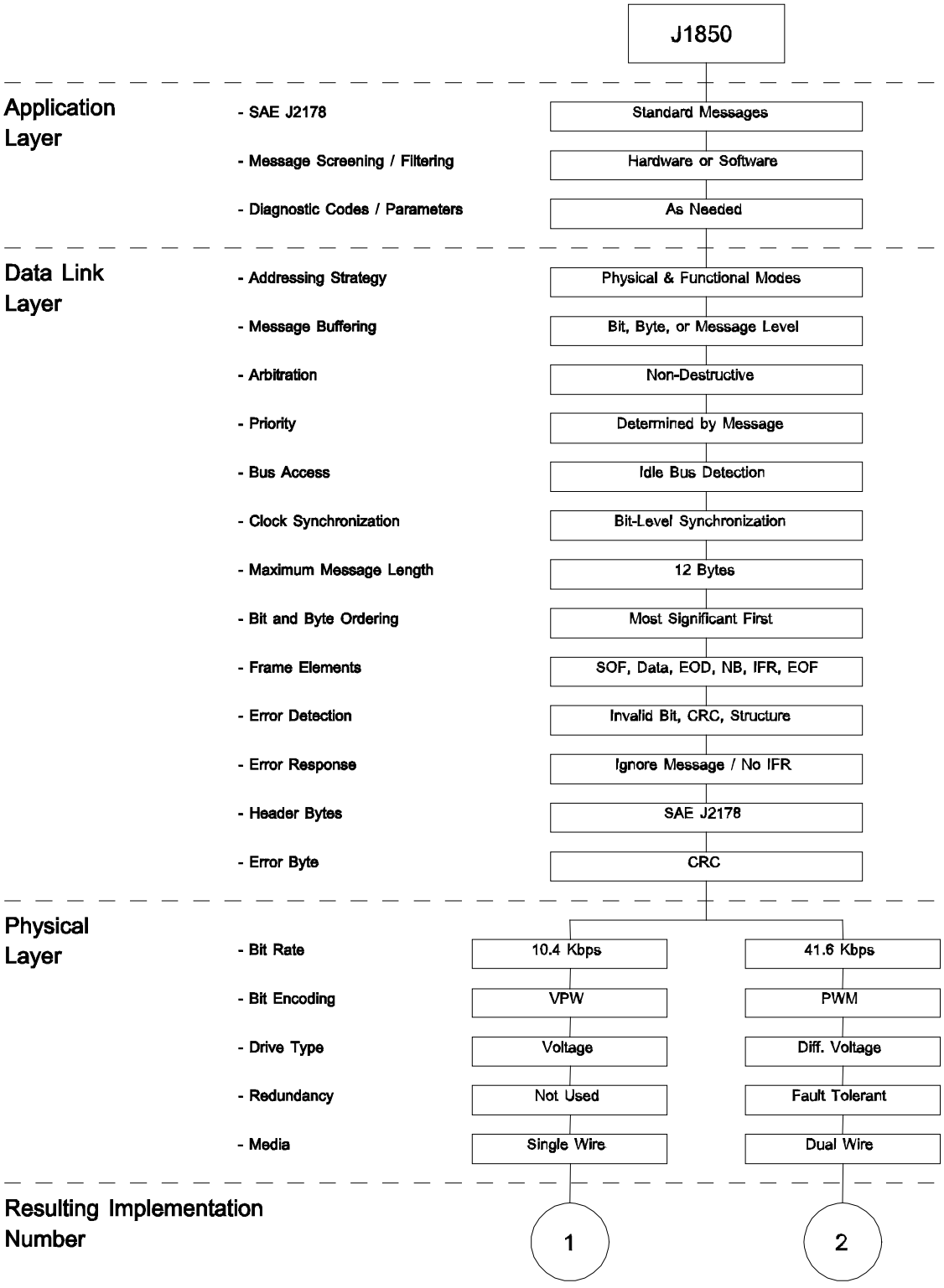


FIGURE 1 - Map of SAE J1850 to the ISO OSI Model

3.3.1 Application Layer - At the top of the OSI reference model is the Application Layer. This layer establishes the relationship between the various application input and output devices, including what is expected of human operators. This layer documents the high level description of the function including control algorithms if appropriate. An example of an Application Layer functional description might be; "Pressing the head lamp button shall cause the low beam head lamp, marker and tail lamp filaments to be energized." Legislated diagnostics is another area in which application layer requirements need to be specified.

3.3.2 Data Link Layer - The primary function of the Data Link Layer is to convert bits and/or symbols to validated error free frames/data. Typical services provided are serialization (parallel to serial conversion) and clock recovery or bit synchronization. An important additional service provided by the Data Link Layer is error checking. When errors are detected, they may be corrected or higher layers may be notified.

3.3.3 Physical Layer - The Physical Layer and its associated wiring form the interconnecting path for information transfer between Data Link Layers. Typical Physical Layer protocol elements include, voltage/current levels, media impedance, and bit/symbol definition and timing.

3.4 Network Implementation - The network implementations based on this document have been reduced to commonize hardware, software, messages and tools. The consolidation of messages has been documented in SAE J2178. The first byte or the first three bytes of these messages are called the "Header" byte(s). These header bytes fully define the associated requirements of this network interface, which previously had been optional. Figure 2 shows the general format for single byte header forms. Figure 3 shows the three byte header form. Figure 4 shows the specific bit assignments for priority, In-Frame Response, and Functional / Physical Address mapping in the three byte header format. For a complete description of the "KYZZ" bits shown in Figure 4 refer to SAE J2178/1.

Single Byte Header:

Bit 7	6	5	4	3	2	1	0
Message ID (256)							

One Byte Form of Consolidated Header:

Bit 7	6	5	4	3	2	1	0
x	x	x	H=1	x	x	x	x
Message ID (128)							

FIGURE 2 - Single Byte Header & One Byte Form of Consolidated Header

Three Byte Form of Consolidated Header:

Byte 1	Byte 2	Byte 3
See Figure 4 Below	Target Address	Source Address

FIGURE 3 - Three Byte Form of Consolidated Header

Byte 1 of Three Byte Form of Consolidated Header:

Bit 7	6	5	4	3	2	1	0
P	P	P	0	K	Y	Z	Z
Priority (0 to 7)			H=0	Message Type (see below)			

Bit	Meaning	Value	Meaning
K	In-Frame Response (IFR)	0 1	IFR Required IFR Not Allowed
Y	Addressing Mode	0 1	Functional Addressing Physical Addressing
ZZ	Specific Message Type	0 0 0 1 1 0 1 1	The meaning for these values are dependant on K & Y above. These meanings can be found in J2178/1.

FIGURE 4 - First Byte of Three Byte Form of Consolidated Header

4 APPLICATION LAYER DETAILS

The application of this communication network is the transfer of information from one node of the network to one or more other nodes. This transfer of information supports both operational and diagnostic needs. SAE has developed documents describing each of these types of applications, consistent with this document.

4.1 Normal Vehicle Operation (Down the Road) Messages - The messages sent during non-diagnostic operations are called normal vehicle operation messages. These normal vehicle operation messages are used for communication from a transmitter to one or more receivers across this network. The normal operation messages have been developed by the SAE for this communication network and are defined in SAE J2178. SAE defined messages and the "Reserved" messages of SAE J2178 shall remain specific to those definitions. In SAE J2178, there is also a set of "Reserved - Manufacturer" messages which, if used, will have meanings specific to a vehicle manufacturer but are likely to be different between manufacturers.

4.2 Diagnostic Messages - It is expected that this network will be used for diagnostics of the devices utilizing the network. These diagnostic procedures may include legislated diagnostics, industry standard diagnostics, or manufacturer specific diagnostic procedures.

Legislated diagnostics, and some level of voluntary industry standard diagnostics, that reference this recommended practice, should only specify procedures and frames that conform to this recommended practice. SAE J1979 and SAE J2190 define the set of recognized test modes that are available and have been reserved for diagnostic purposes.

Manufacturer specific test procedures utilizing this network may specify procedures that do not conform to the requirements of this recommended practice.

4.2.1 Diagnostic Parametric Data - SAE J1979 and SAE J2190 define test modes and frame formats for use by off-vehicle test equipment to obtain diagnostic data from the vehicle. SAE J1979 and SAE J2190 messages conform to the requirements and limitations of this document.

4.2.2 Diagnostic Malfunction Codes - SAE J2012 defines trouble codes to be assigned to various vehicle system malfunctions, and also assigns ranges of codes to be used for manufacturer specific codes. SAE J1979 and SAE J2190 includes messages to be used to retrieve these codes from the on-vehicle systems. When trouble codes are to be assigned to system malfunctions, the code structure of SAE J2012 should be used.

4.3 Frame Filtering - The network interface device may be capable of filtering frames on the network to select those appropriate to a given node. Because this Class B protocol may use more than one type of frame addressing (e.g., functional and physical; see Paragraph 5.1 below), the criteria for these filtering operations may include multiple byte comparisons occurring over the first several frame bytes. Regardless of the exact technique used for frame filtering, the objective is to reduce the software and processing burden associated with network operations by limiting the number of received frames to just those necessary for any given node.

5 DATA LINK LAYER DETAILS

This section defines the requirements on the following Data Link Layer attributes:

a. Addressing Strategy
b. Network Access and Data Synchronization
c. Frame Elements and Structure
d. Error Detection
e. Error Response

5.1 Addressing Strategy - Two types of addressing strategies are defined and can coexist on this network. The two strategies serve different types of tasks and the flexibility to use both types on the same network provides a major benefit.

5.1.1 Physical Addressing - Frames are exchanged only between two devices based on their "Physical" address within the network. Each node must be assigned a unique physical address within the network. This type of addressing strategy is used when the communications involve specific nodes and not the others that may be on the network. Diagnostic access would be one case where identification of a specific module is important.

5.1.2 Functional Addressing - Frames can be transmitted between many devices based on the function of that frame on the network. Each node is assigned the set of functions that it cares about, either as transmitter or receiver, and can be located anywhere in the network. This type of addressing strategy is used when the physical location of the function is not important but could move around from one module to another. In the case of functional addressing, the function of the message is important and not the physical addresses of the nodes.

5.2 Network Access and Data Synchronization - The network interface shall implement a multiple access arbitration based protocol using nondestructive bit-by-bit arbitration to transparently resolve simultaneous access to the bus. Network access is allowed after detection of an idle bus. The definition of an idle bus is contained in Paragraph 6.6.1.7.

Since a discrete clock wire is not used with this network, node synchronization can be derived from bit/symbol transitions on the bus.

5.2.1 Full Message Buffering - One or more messages exist in their entirety in the interface device. This approach reduces software burden at the expense of hardware costs. Message filtering (or screening) is possible in such a device which reduces software burden even further.

5.2.2 Byte Buffering - Each byte of a received message (or transmit message) is stored individually in the interface device. The controlling device is responsible for the timely servicing of the interface device to keep up with frame traffic.

5.3 Network Elements and Structure

The general format is:

idle, SOF, DATA_0, ..., DATA_N, CRC, EOD, NB, IFR_1, ..., IFR_N, EOF, IFS, idle:

The preceding acronyms are defined as follows:

idle: Idle Bus (occurs before SOF and after IFS)
SOF: Start of Frame
DATA: Data bytes (each 8 bits long)
EOD: End of Data (only when IFR is used)
CRC: CRC Error Detection Byte (may occur in IFR as well)
NB: Normalization Bit (10.4 Kbps only)
IFR: In-Frame Response Byte(s)
EOF: End of Frame
IFS: Inter-Frame Separation

Note: Break (BRK) can occur (be sent) on a network at any time.

5.3.1 Frame Elements - The frame elements other than the symbols SOF, EOD, NB, EOF, IFS, and BRK will be byte oriented and must end on byte boundaries. Each byte will be 8 bits in length.

5.3.2 Bit Ordering - The first bit of each byte transmitted on the network shall be the most significant bit (i.e., MSB first).

5.3.3 Maximum Frame Length - The maximum number of continuous bit times that a single node is able to control the bus shall not exceed the value specified in Section 7.2.

5.3.4 Function of SOF, EOD, EOF, IFS, NB, and BRK - In addition to actual data bytes (i.e., data, CRC, IFR) frame delimiter symbols are defined to allow the data bus to function properly in a multitude of different applications. An overview of these symbols is provided here. Detailed timing requirements on each symbol can be found in Section 7.3

5.3.4.1 Start of Frame (SOF) - The SOF mark is used to uniquely identify the start of a frame. The SOF mark shall not be used in the calculation of the CRC error detection code.

5.3.4.2 End of Data (EOD) - End of Data (EOD) is used to signal the end of transmission by the originator of a frame. The in-frame response (IFR) section of the frame, if used, begins after the EOD time but before the EOF. If the IFR feature (see Paragraph 5.3.7) is not used, then the bus would remain in the passive state thereby resulting in an End of Frame (EOF). If a frame includes an IFR, the originator of the frame will expect the recipient(s) of the frame to drive the network with one or more in-frame response bytes immediately following EOD.

5.3.4.3 End of Frame (EOF) - The completion of the EOF defines the end of a frame. After the last transmission byte (including in-frame response bytes where applicable), the bus will be left in a passive state. When EOF has expired, all receivers will consider the transmission complete.

5.3.4.4 Inter-Frame Separation (IFS) - Inter-Frame Separation is used to allow proper synchronization of various nodes during back-to-back frame transmissions. A transmitter must not initiate transmission on the bus before the completion of the IFS minimum period. However, receivers must synchronize to any other SOF occurring after the EOF minimum period in order to accommodate individual clock tolerances.

A transmitter that desires bus access must wait for either of two conditions before transmitting a SOF:

a. IFS minimum have expired.
b. EOF minimum has expired and another rising edge has been detected.

5.3.4.5 Normalization Bit (NB) - Only applicable to 10.4 Kbps implementation - For Variable Pulse Width Modulation, the first bit of In-Frame Response data is also passive and therefore it is necessary to generate a Normalization Bit to follow the EOD symbol. This Normalization Bit shall define the start of the in-frame response. The Normalization Bit is defined in Paragraph 6.6.2.5.

5.3.4.6 Break (BRK) - BRK is allowed to accommodate those situations in which bus communication is to be terminated and all nodes reset to a "ready-to-receive" state. If BRK is used, it must adhere to the requirements as specified in Section 6.6.

5.3.5 Idle Bus (idle) - Idle bus is defined as any period of passive bus state occurring after IFS. During an idle bus, any node may transmit immediately. Contention may still occur when two or more nodes transmit nearly simultaneously; therefore, re-synchronization to rising edges must continue to occur.

5.3.6 Data Byte(s) - A number of data bytes, each eight (8) bits in length, can be transmitted at the discretion of the system designer. However, the total message length (from SOF to EOF) shall not exceed the limit defined in Section 7.2.

5.3.7 In-Frame Response (IFR) - For In-Frame Response, the response byte(s) are transmitted by the responders and begin after EOD. If the first bit of the in-frame response byte does not occur at this point and the bus remains passive for a period of time defined as EOF, then the originator and all receivers must consider the frame complete. In-frame response bytes may take one of the following forms (refer to Figure 5):

a. None

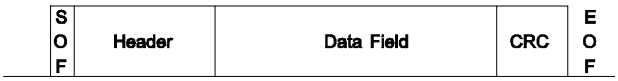
b. A single byte transmitted from a single recipient, typically a unique identifier (ID) or address.

c. Multiple bytes, a single byte transmitted from each recipient. The effect is to concatenate the individual response bytes into a response "stream". The response byte from each recipient must be unique, typically a physical address (ID n). Arbitration takes place during the response process so that each recipient, if arbitration is lost during its response byte, will retransmit the single byte until the recipient observes its unique byte in the response stream. Once a given recipient observes its own unique response byte, it discontinues the transmission process to allow any remaining responders to transmit their byte.

d. One or more data bytes, all from a single recipient. A CRC byte may be appended to the data byte(s). The CRC byte is calculated as described in Paragraph 5.4.1, except only the data in the response is used for the CRC calculation.

Refer to SAE J2178/1 for a detailed discussion of the different IFR types and for determination of which message types utilize which IFR types.

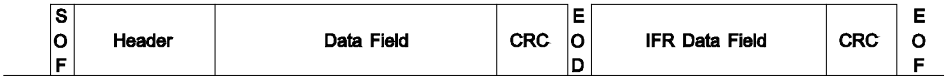
If in-frame response bytes are used, the overall frame / message length limit remains in effect. The sum total of data bytes, CRC bytes, and in-frame response bytes shall not exceed the frame length as specified in Section 7.2.



Type 0 - None

Type 1 - Single Byte From a Single Responder

Type 2 - Single Byte From Multiple Responders



Type 3 - Multiple Bytes From a Single Responder

FIGURE 5 - Types of In-Frame Response

5.3.7.1 Normalization Bit - If the In-Frame Response is employed in the 10.4 Kbps implementation then a "Normalization Bit" is required. The Normalization Bit is described in Paragraph 6.6.2.5.

5.4 Error Detection - The error descriptions in this document are loosely defined and classified. In general, the action taken after an error condition has been detected is manufacturer specific unless it has been specified in this document.

5.4.1 Cyclic Redundancy Check (CRC) - The CRC is required with either of the header byte systems used. The method of calculating and checking the CRC byte is defined below. An invalid CRC byte may constitute a detected error.

a. The CRC calculation and the CRC checker shift registers (or memory locations) will be located in the sender and receiver nodes, respectively, and shall be initially set to the "all ones" state during SOF. (The setting to "ones" prevents an "all zeros" CRC byte with an all zero data stream.)

b. All frame bits that occur after SOF and before the CRC field are used to form the Data Segment Polynomial which is designated as D(X). For any given frame, this number can be interpreted as an "n-bit" binary constant, where n is equal to the frame length, counted in bits.

c. The CRC division polynomial is $X^8 + X^4 + X^3 + X^2 + 1$. This polynomial is designated as P(X).

d. The Remainder Polynomial R(X) is determined from the following Modulo 2 division equation:

Install Equation Editor and double-click here to view equation.

Note: Q(X) is the quotient resulting from the division process.

e. The CRC byte is made equal to $\overline{R(X)}$, where $\overline{R(X)}$ is the ones complement of R(X).

f. The Frame Polynomial M(X) that is transmitted is:

Install Equation Editor and double-click here to view equation.

g. The receiver checking process shifts the entire received frame, including the transmitted CRC byte, through the CRC checker circuit. An error free frame will always result in the unique constant polynomial of $X^7 + X^6 + X^2$ (C4 hex) in the checker shift register regardless of the frame content.

h. Examples of frames with the appropriate CRC bytes are listed in Table 1.

i. A status flag may be used to indicate the occurrence of a received CRC error.

j. When In-Frame Response data is protected by a CRC field, the previous rules are used to define the CRC, except that the sender and receiver nodes are interchanged. The CRC calculation only includes the in-frame response bytes. (Note that the SOF, EOD, EOF, and NB are not used in the CRC calculation and serve as data delimiters.)

TABLE 1 - Examples of Frames & Appropriate CRC Bytes

Data Bytes (hex)	CRC (hex)
00 00 00 00	59
F2 01 83	37
0F AA 00 55	79
00 FF 55 11	B8
33 22 55 AA BB CC DD EE FF	CB
92 6B 55	8C
FF FF FF FF	74

Note: Figure 6 illustrates a typical CRC generator and Figure 7 illustrates a typical CRC checker. With appropriate gating, the two circuits may be combined to use only a single shift register for both CRC generation and CRC checking.

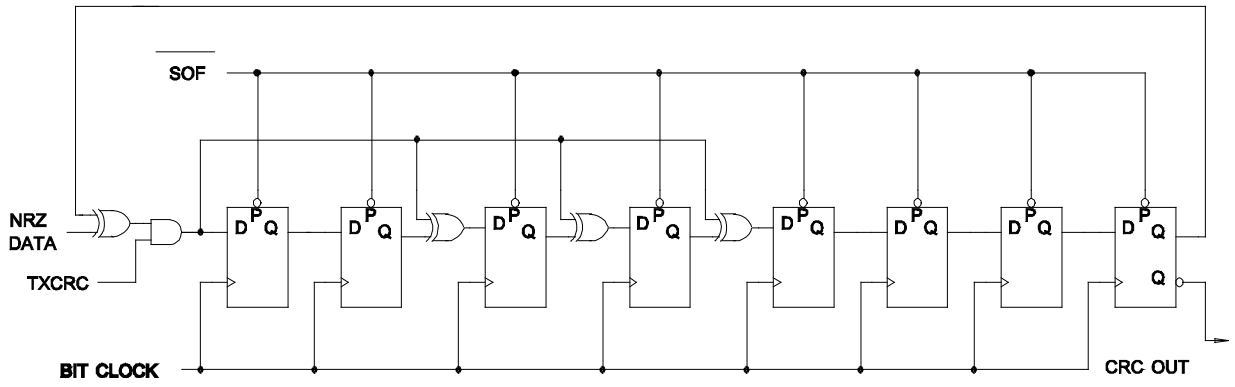


FIGURE 6 - CRC Generator

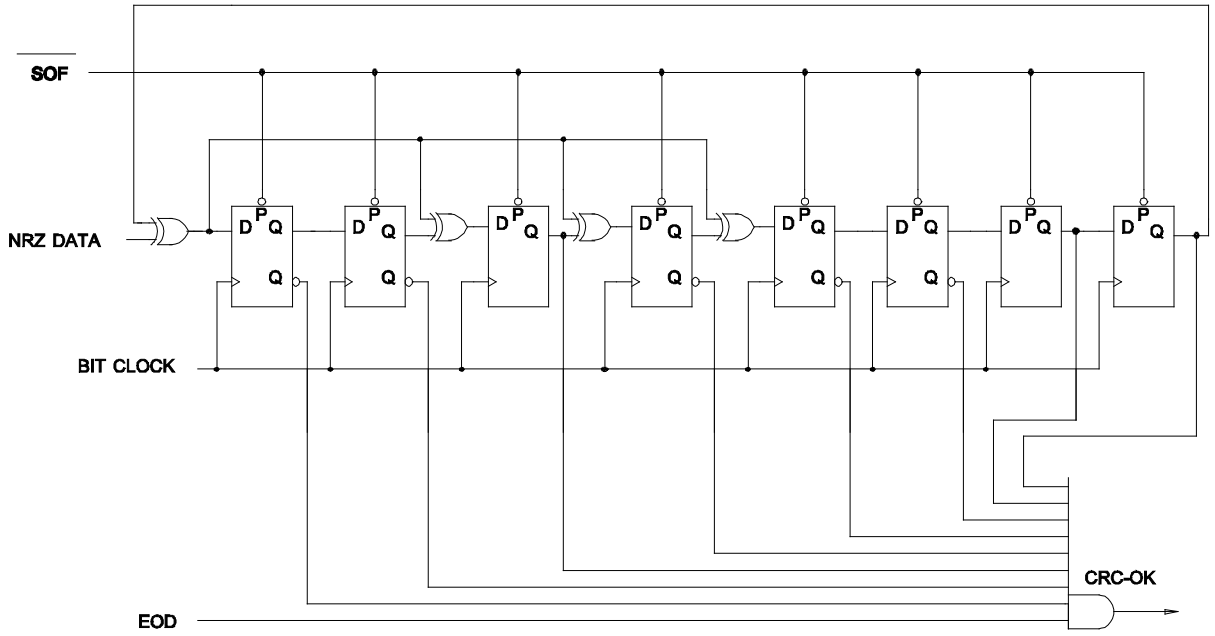


FIGURE 7 - CRC Checker

5.4.2 Frame / Message Length - A frame exceeding its defined length limit may constitute a detected error.

5.4.3 Out-of-Range - Data is corrupted in a vehicle network when transient interference is large enough to drive the receiver out of its dynamic range of operation. This out-of-range condition, where the receiver can no longer accurately decode the data, may be detected by an out-of-range detector. The following defines the operation of an out-of-range detector:

a. Data is recovered by holding the receiver output in the state it was prior to the out-of-range condition for the duration of the interference.

b. If the interfering transient is long enough to corrupt a desired bus symbol, accurate data recovery may not occur. This may constitute a detected error.

5.4.4 Concept of Valid / Invalid Bit / Symbol Detection

5.4.4.1 Invalid Bit Detection - In some cases, data integrity may be increased by detecting the condition in the data stream where the received data bit does not match the specifications for either a "one" or a "zero" bit.

5.4.4.2 Invalid Frame Structure Detection - Regardless of data encoding, data integrity may be increased by detecting the condition when an EOD or EOF occurs on a non-byte boundary within the data stream, or the frame exceeds the maximum frame length.

5.5 Error Response

5.5.1 Transmit - When an originator of a frame detects an error condition on the network (i.e., one of the error conditions defined in paragraph 5.4), the originator must discontinue the transmit operation prior to the start of the next bit. After the specified period of IFS or reception of an edge after EOF, the originator is allowed to retransmit the frame.

5.5.2 Receive - If a frame is received which contains an error (i.e., one of the error conditions defined in paragraph 5.4), the frame is to be ignored. If "In-Frame Response" is being used, the receiver must not respond to a received frame containing an error. This lack of response serves as a signal to the originator that an error was detected by the receiver.

6 PHYSICAL LAYER DETAILS

This section defines the requirements on the following physical layer attributes:

a. Media
b. Unit Load Specifications
c. Maximum Number of Nodes
d. Maximum Network Length
e. Media Characteristics
f. Data Bit/Symbol Definition/Detection
g. Network Wake-Up Via Physical Layer
h. Physical Layer Fault Considerations
i. EMC Requirements

Specific parametric values associated with the physical layer are contained in Section 7.

6.1 Physical Layer Media - Although this specification focuses on the data carrying media, it is assumed that each node shall be supplied with appropriate power and ground.

6.1.1 Single Wire - The network medium for the single wire voltage drive shall be a single random lay wire.

6.1.2 Dual Wires - The network medium for the dual wire voltage drive shall be either a parallel wire pair separated by a constant distance, or a twisted pair of wires.

6.1.3 Routing - No Restrictions

6.2 Unit Load Specifications - The electrical loading effect of each device connected to this network will be measured in terms of unit loads. A unit load is a nominal value which, if all nodes correspond to one unit load, will allow the maximum specified number of nodes to be connected to the network. There is no requirement that a given node must be equal to a standard unit load, but the combination of all load values must not exceed the limits for any given system.

6.3 Maximum Number of Nodes - The maximum number of nodes, assuming each node is the equivalent of a standard unit load, is specified in Section 7.

6.4 Maximum Network Length - The maximum medium length between any two nodes shall not exceed the value specified in Section 7.

6.4.1 On-Vehicle / Off-Vehicle - The maximum network length, maximum capacitance value and minimum load / termination resistance values for any off-vehicle equipment have been specified in Section 7.3. Because all applications must allow for such off-vehicle equipment, the allowed maximum on-vehicle loads shall be limited to account for this level of off-vehicle loading.

6.5 Media Characteristics - The characteristics of the media are as specified in Section 7.

6.6 Data Bit / Symbol Definition / Detection - The data bus can be in one of two valid states, active or passive. For clarity in the following sections, a rising edge is a transition from the passive to active state, and a falling edge is a transition from the active to the passive state.

There are two methods of bit encoding specified in this document, Pulse Width Modulation (PWM) and Variable Pulse Width (VPW) modulation. The timing diagrams that follow represent the requirements for the logical waveform. It is the transmitter's responsibility to transmit bits / symbols which are valid (i.e., meets these specifications). In some contention situations, the transmitter will have to re-synchronize to ensure that the falling edge is within specification. The requirements associated with the reception of these bits and symbols are not stated explicitly in this specification, but are to be derived from transmitter specifications by the module or circuit designer. It is expected that the receiver will employ a simple clock-driven digital filter and digital integrator or majority vote sampling circuit for decoding data and maintaining "clock" synchronization. All timing requirements are specified in Section 7.

The following bits/symbols are defined for both PWM and VPW:

a. One "1" bit
b. Zero "0" bit
c. Start of Frame (SOF)
d. End of Data (EOD)
e. End of Frame (EOF)
f. Inter-Frame Separation (IFS)

The Normalization Bit (NB), is only applicable for VPW implementations and is therefore only defined for VPW.

6.6.1 Pulse Width Modulation (PWM) - The following values represent nominal timing, detailed timing requirements for each bit/symbol can be found in Section 7.

6.6.1.1 The One "1" and Zero "0" Bits (See Figures 8 and 9):

a. "1" Bit - A "1" bit is characterized by:

(1) A rising edge that follows the previous rising edge by at least Tp3. Two rising edges shall never be closer than Tp3.

(2) A falling edge that occurs Tp1 after the rising edge.

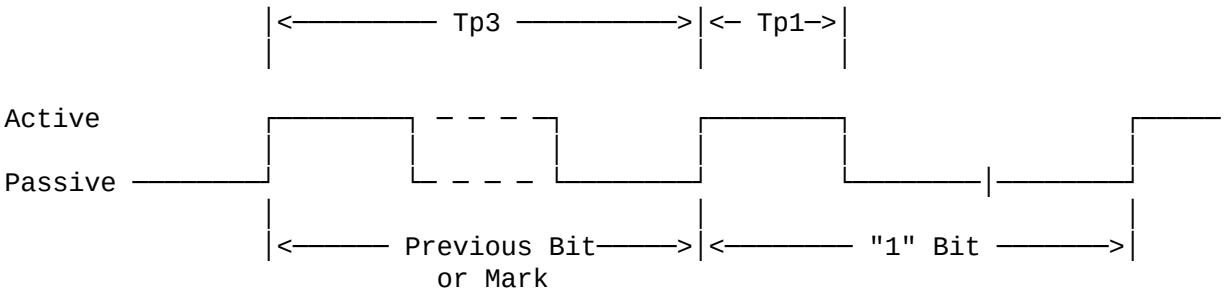


FIGURE 8 - "1" Bit Definition

b. "0" Bit - A "0" bit is characterized by:

(1) A rising edge that follows the previous rising edge by at least Tp3. Two rising edges shall never be closer than Tp3.

(2) A falling edge that occurs Tp2 after the rising edge.

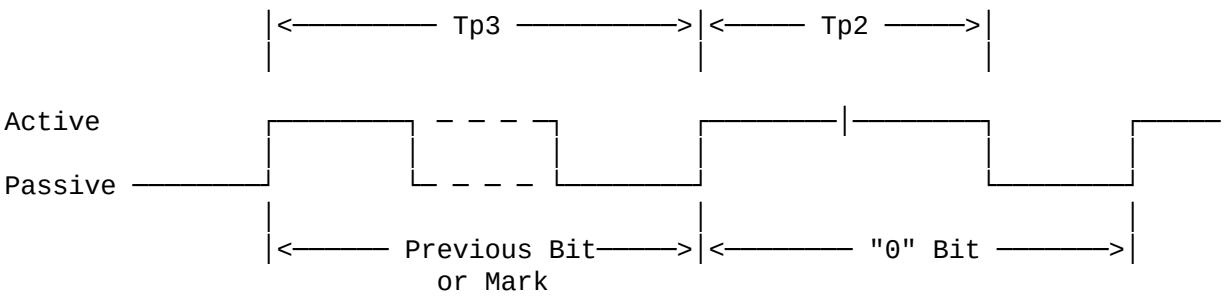


FIGURE 9 - "0" Bit Definition

6.6.1.2 Start of Frame (SOF) - The Start of Frame (SOF) mark has the distinct purpose of uniquely determining the start of a frame (see Figure 10). The SOF is characterized by:

a. A reference rising edge that follows the previous rising edge by at least Tp5.

b. A falling edge that occurs Tp7 after the reference rising edge.

c. The rising edge of the first data bit will occur at Tp4 after the reference rising edge.

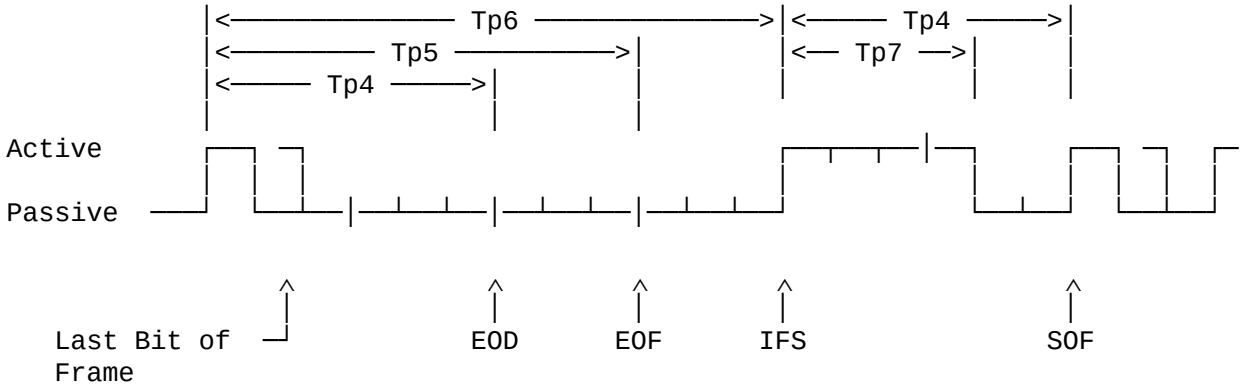


FIGURE 10 - Frame Symbols

Note: Last bit of a frame may be the last data bit, last CRC bit, or last In-Frame Response bit.

6.6.1.3 End of Data (EOD) - End of Data is used to signal the end of transmission by the originator of a frame. The In-Frame Response (IFR) section of the frame, if used, begins immediately after the EOD bit (see Figure 11). If the In-Frame Response feature is not used, then the bus would remain in the passive state for an additional bit time, thereby signifying an End of Frame (EOF).

For In-Frame Response, the response byte(s) are driven by the responders and begin with the rising edge of the first bit of the response, Tp4 after the rising edge of the last bit sent from the originator of the frame.

If the first bit of the response byte does not occur at Tp4, and the bus remains passive for one additional bit time (total time Tp5) then the originator and all receivers must consider the frame complete (i.e., EOD has been transformed into an EOF).

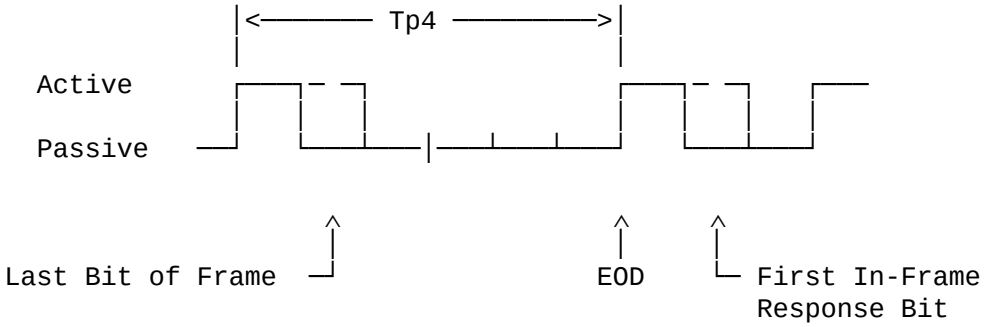


FIGURE 11 - End of Data Symbol

Note: Last bit of a frame may be the last data bit, last CRC bit, or last In-Frame Response bit.

6.6.1.4 End of Frame (EOF) - The completion of the EOF defines the end of a frame (by definition, an EOD forms the first part of the EOF - see Figure 13). After the last transmission byte (including in-frame response bytes where applicable), the bus will be left in a passive state. When EOF has expired (Tp5 after the rising edge of the last bit), all receivers will consider the transmission complete.

6.6.1.5 Inter-Frame Separation (IFS) - Inter-Frame Separation allows proper synchronization of various nodes during back-to-back frame operation.

A transmitter that desires bus access must wait for either of two conditions before transmitting a SOF:

a. IFS minimum has expired (Tp6 after the rising edge of the last bit).

b. EOF minimum and another rising edge has been detected.(Tp5 after the rising edge of the last bit).

6.6.1.6 Break (BRK) - BRK is allowed to accommodate those situations in which bus communication is to be terminated and all nodes reset to a "ready-to-receive" state (see Figure 12). The PWM Break symbol is an extended SOF symbol and will be detected as an "invalid" symbol to some devices, which will then ignore the current frame, if any. Following the break symbol, an IFS following BRK perioid (Tp9 after the rising edge of the break) is needed to resynchronize the receivers. If the "Breaking" device wishes to obtain guaranteed access to the bus, the highest priority frame must then be sent, otherwise, other frames may gain access under the normal rules of arbitration.

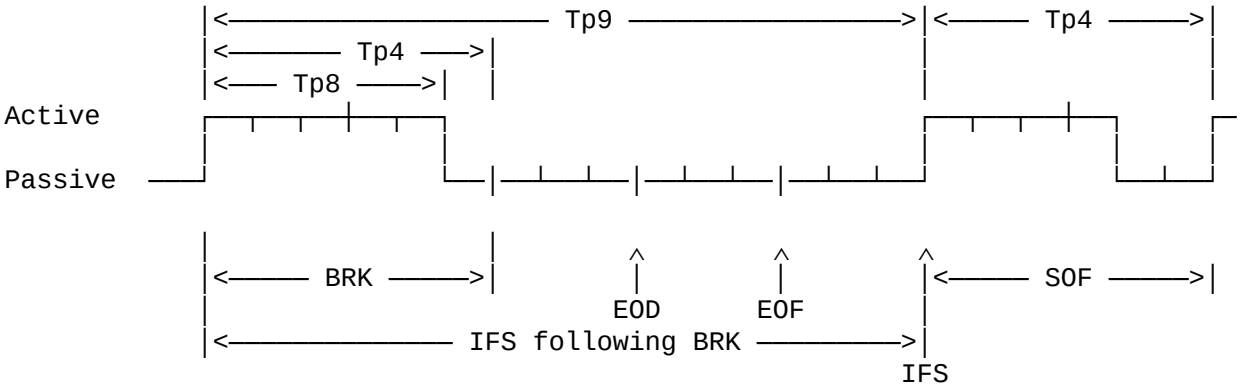


FIGURE 12 - PWM Break Sequence

6.6.1.7 Idle Bus (Idle) - Idle bus is defined as any period of passive bus state occurring after IFS minimum (see Figure 13). A node may begin transmission at any time during idle bus.

During an idle bus, any node may transmit immediately. Contention may still occur when two or more nodes transmit nearly simultaneously; therefore, resynchronization to rising edges must continue to occur.

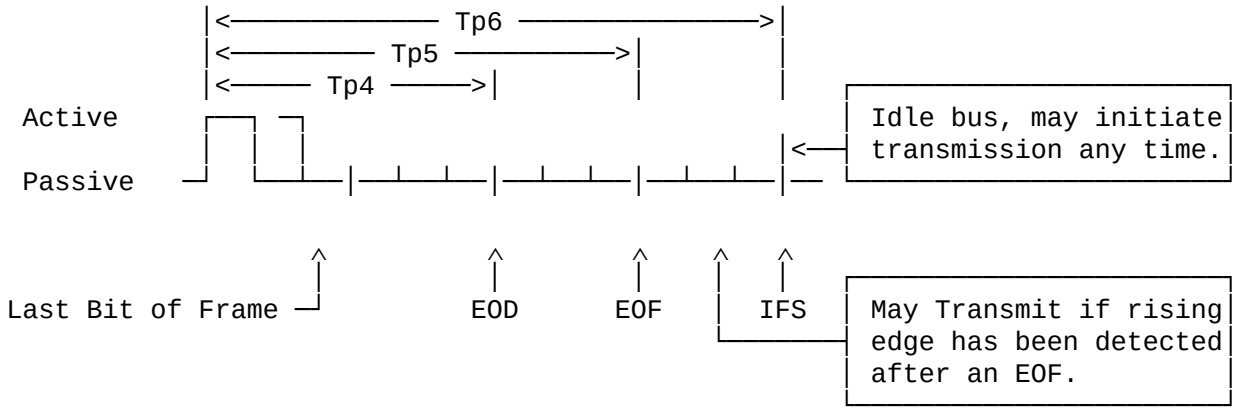


FIGURE 13 - EOF and Idle Bus Definition

Note: Last bit of a frame may be the last data bit, last CRC bit, or last In-Frame Response bit.

6.6.1.8 PWM Symbol Timing Requirements - The symbol timing reference for PWM encoding is based on transitions from the passive state to the active state. The SOF and each data bit in PWM has a "leading edge" from which all subsequent timing is derived. The transition from active to passive (which occurs within the SOF or data bits) is not used as a timing reference. The leading edge is used as the only reference because the transition from passive to active appears on the bus wires as a fast clean edge while the transition from active to passive is slow and ambiguous due to variations in network capacitance.

Paragraph 7.3.2.1 defines the timing values for PWM at 41.6 Kbps. Values are provided for the transmitter and receiver (based on the suggested bit decoder implementation).

6.6.2 Variable Pulse Width Modulation - The SOF symbol, "0" bit, and "1" bit are defined by the time between two consecutive transitions and the level of the bus, active or passive. The EOD, EOF, IFS, and Break symbols are defined simply by the amount of time that has expired since the last transition. EOD, EOF, and IFS are all passive symbols and the Break is an active symbol. Therefore, there is one symbol per transition and one transition per symbol. The end of the previous symbol starts the current symbol. The following values represent nominal timing, detailed timing requirements for each bit / symbol can be found in Section 7.

6.6.2.1 The One "1" and Zero "0" Bits - A "1" bit is either a Tv2 passive pulse or a Tv1 active pulse. Conversely, a "0" bit is either a Tv1 passive pulse or a Tv2 active pulse (see Figure 14). The pulse widths change between passive and active bus states in order to accommodate the arbitration and priority requirements as specified in Section 6.7.

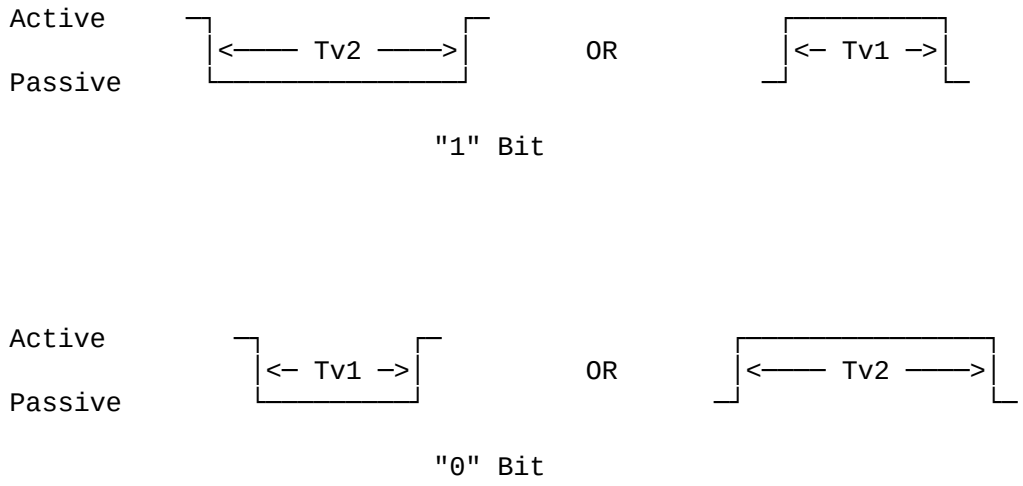


FIGURE 14 - One and Zero Bit Definitions

6.6.2.2 Start Of Frame (SOF) - SOF is a active pulse, Tv3 in duration (see Figure 15)

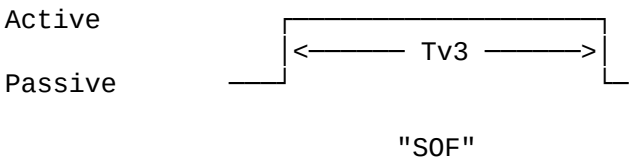


FIGURE 15 - Start Of Frame (SOF) Symbol

6.6.2.3 End Of Data (EOD) - EOD is a passive pulse, Tv3 in duration (see Figure 16)

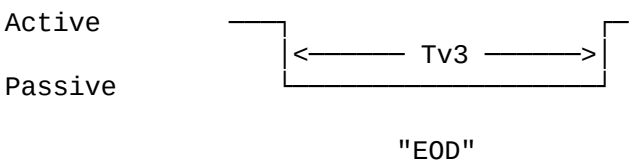


FIGURE 16 - End of Data (EOD) Symbol

6.6.2.4 End of Frame (EOF) - EOF is a passive pulse, Tv4 in duration (see Figure 17)

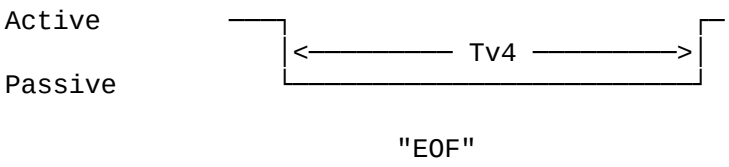


FIGURE 17 - End of Frame (EOF) Symbol

6.6.2.5 In-Frame Response Byte(s) / Normalization Bit - The "In-Frame Response" (IFR) is transmitted by the responder and begins after the passive EOD symbol. For Variable Pulse Width Modulation, the first bit of the IFR data is also passive. Therefore, it is necessary to generate a normalization bit to follow the EOD symbol. The responding device generates the normalization bit prior to sending the IFR data. This normalization bit defines the start of the IFR and can take two forms. The first form is an active short period (Tv1) and the second form is an active long period (Tv2). Figure 18 illustrates the IFR using the normalization bit. The normalization bit can also be used to indicate what type of response is expected during the IFR portion of the frame. The preferred method is to use an active short bit (Tv1) to indicate that the IFR DOES NOT contain a CRC (i.e., IFR types 1 or 2). An active long bit (Tv2) would therefore indicate that the IFR DOES contain a CRC (i.e., IFR type 3). This is only a preferred method, and individual manufacturers are allowed to implement the normalization bit per their requirements. However, all future SAE J1850 applications are urged to implement the normalization bit using the preferred method described above.

If in-frame response bytes are used, the overall frame / message length limit remains in effect. The sum total of data bytes, CRC byte, and in-frame response bytes shall not exceed the value specified in Section 7.

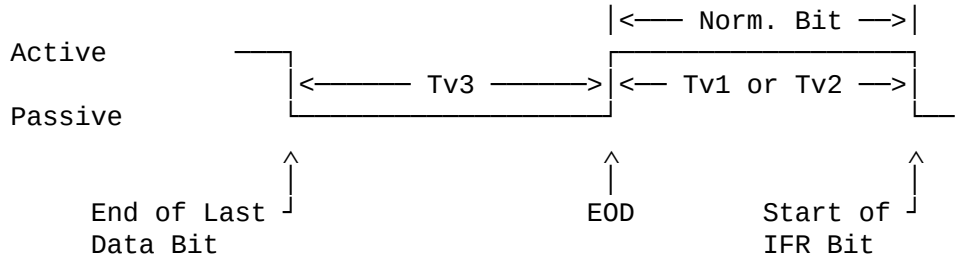


FIGURE 18 - Normalization Bit

6.6.2.6 Inter-Frame Separation (IFS) - Inter-Frame Separation is used to allow proper synchronization of various nodes during back-to-back frame operation.

A transmitter that desires bus access must wait for either of two conditions before transmitting a SOF (see Figure 19):

a. IFS minimum has expired (Tv6).

b. EOF minimum and another rising edge has been detected (Tv4).

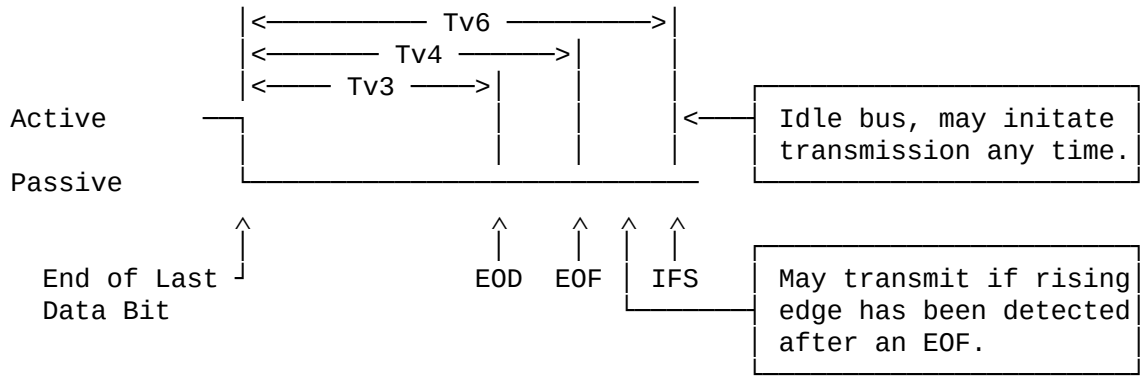


FIGURE 19 - Inter-Frame Seperation

6.6.2.7 Break (BRK) - BRK is allowed to accommodate those situations in which bus communication is to be terminated and all nodes reset to a "ready-to-receive" state (see Figure 20). The VPW Break symbol will be detected as an "invalid" symbol to some devices, which will then ignore the current frame, if any. The VPW Break symbol is a long active period ($\geq$ Tv5). Following the break symbol, an IFS period (Tv6) is needed to resynchronize the receivers and the normal IFS rules for transmitting a SOF during back-to-back operation apply. If the "Breaking" device wishes to obtain guaranteed access to the bus, the highest priority frame must then be sent, otherwise, other frames may gain access under the normal rules of arbitration.

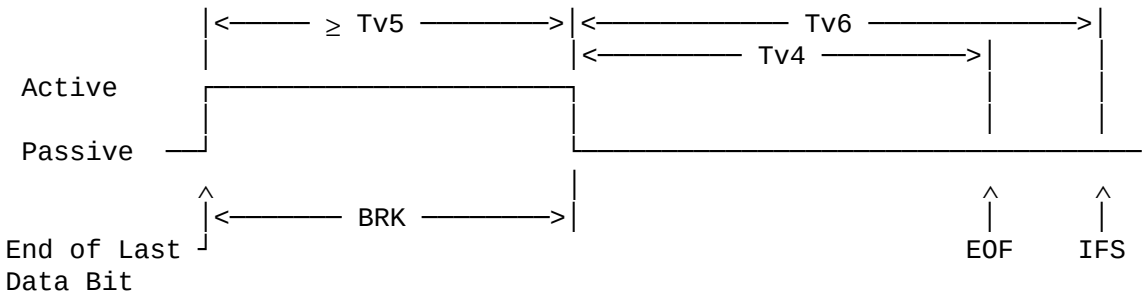


FIGURE 20 - Break signal

6.6.2.8 Idle Bus (Idle) - Idle bus is defined as any period of passive bus state occurring after IFS. A node may begin transmission at any time during idle bus.

An idle bus will exist after IFS (Tv6). Contention may still occur when two or more nodes transmit nearly simultaneously; therefore, resynchronization to rising edges must continue to occur.

6.6.2.9 VPW Symbol Timing Requirements - The most important factor in symbol timing uncertainty is the edge position uncertainty due to the time taken to make a transition between $V_{ol,max}$ and $V_{oh,min}$ (in either direction). The maximum allowable transition time,$T_{t,max}$ (the area between $V_{ol,max}$ and $V_{oh,min}$), bounds the time span between the earliest and latest node to recognize a transition and is a key design parameter. As $T_{t,max}$ is reduced it becomes more and more difficult to design a driver which also meets the necessary EMI requirements. In this manner, the corners of the waveform, which are a major contributor to the radiated contents of the signal do not fall within the limits imposed by $T_{t,max}$. as found in Section 7.

Other factors that affect the transmitted pulse width are oscillator tolerance and variations in delay through the receiver, noise filter, and driver. For a fixed oscillator and a well designed digital filter, most of the variation is in the time it takes the driver to leave the current state and start the transition. The various factors (plus some guard band and allowance for alternative implementations) can be lumped into a single set of limits, $T_{x,min}$ and $T_{x,max,}$ for each symbol. Each is measured from the trip point of the previous transition as seen by the transmitting node (assuming a step input) to the beginning or end of the transition at $V_{oh,min}$ or $V_{ol,max.}$

The pulse width as seen by another node, which may perceive the leading edge either sooner or later than the transmitting node, can range from $T_{x,min}$ - $T_{t,max}$ to $T_{x,max}$ + $T_{t,max}$ in absolute terms. This range represents a receiver's required acceptance range for a given symbol. The actual acceptance range must be wider to allow for receiver oscillator tolerance and any implementation dependent uncertainties or constraints. The necessary guard band limits how close together symbols can be defined. To keep the symbols short, there is no space allocated for an unambiguous (with normal tolerances) forbidden zone between symbols.

The time windows are not affected by multiple nodes trying to transmit at the same time during arbitration. This is because a single node effectively dominates each transition. It is either the first node to leave the passive state or the last node to leave the active state. Although the fastest or slowest node dominates a particular transition, the contention scheme assures that the highest priority frame always wins regardless of which node started transmitting first.

The purpose of the noise filter is to eliminate impulse noise which may exceed the steady state noise margin and to minimize the need for hysteresis at the receiver input. The delay through the filter is compensated for in the timing logic. A specific implementation of the filter is not required for compatibility so long as the delay is properly compensated and the uncertainty bounds are not exceeded. In the presence of arbitrary noise during the transition period, the filter should respond as though a single step input had occurred at some point within that period.

The symbol limits defined in Section 7 are consistent with $T_{t,max}$ and the specified oscillator tolerance. T_{nom} is the nominal symbol time with no oscillator error and the receiver detecting the transition at V_t (see analysis in Appendix D).

6.7 Contention / Arbitration / Priority - A contention situation arises when more than one node attempts to access the bus at essentially the same time.

6.7.1 Contention Detection - Contention detection is the recognition of conflicting symbols or bits. The process of bit-by-bit arbitration allows conflicting frame transmissions to be detected. A node that detects a difference between the symbol or bit it receives and the symbol or bit it is currently transmitting, has detected contention to the transmission of its frame. Only the one frame that wins all conflicts of different symbols and bits with all the other nodes that began transmitting during that frame will not detect contention.

6.7.2 Bit-by-Bit Arbitration - The bit-by-bit arbitration scheme described below settles the conflicts that occur when multiple nodes attempt to transmit frames simultaneously. This scheme is applied to each symbol / bit of the frame, starting with the SOF symbol and continuing until the end of the frame. Bit-by-bit arbitration is based on the use, at the physical layer, of two values of the bus, called the active state and the passive state. All symbols and bits are encoded on the bus by the physical layer as combinations of active and passive state signals. During simultaneous transmissions of active state and passive state signals on the bus, the resultant state on the bus is always active (active state dominates). If the transmitting node detects a signal state on the bus that is different from the state being transmitted by the node during the header portion of the frame, the node must discontinue the transmit operation prior to the start of the next bit. If the transmitting node detects a signal state on the bus that is different from the state being transmitted by the node during the data portion of the frame (following the header), the process used to cease transmission is implementation specific. Some possible options are:

a. Discontinue the transmit operation prior to the start of the next bit (similar to the action taken if contention is detected during the header phase). If transmission of a message is prematurely terminated on a byte boundary due to unexpected contention detection following the header, care must be taken by receiving nodes not to accept the message as a valid one. There is a 1 in 256 chance that the last byte received is the CRC of the previous bytes and would therefore appear to be a valid message. In this case, a node may need to validate the received message to ensure it is of the correct length.

b. Transmit additional bits (< 8) when contention is detected on a byte boundary. This ensures that a framing error will be received by all other receivers in the case of unexpected contention detection possibly due to noise.

Bus access is granted to nodes sending an active state signal over nodes sending a passive state signal. Figure 21 shows this operation on the physical layer, based on the two forms of modulation allowed (PWM and VPW).

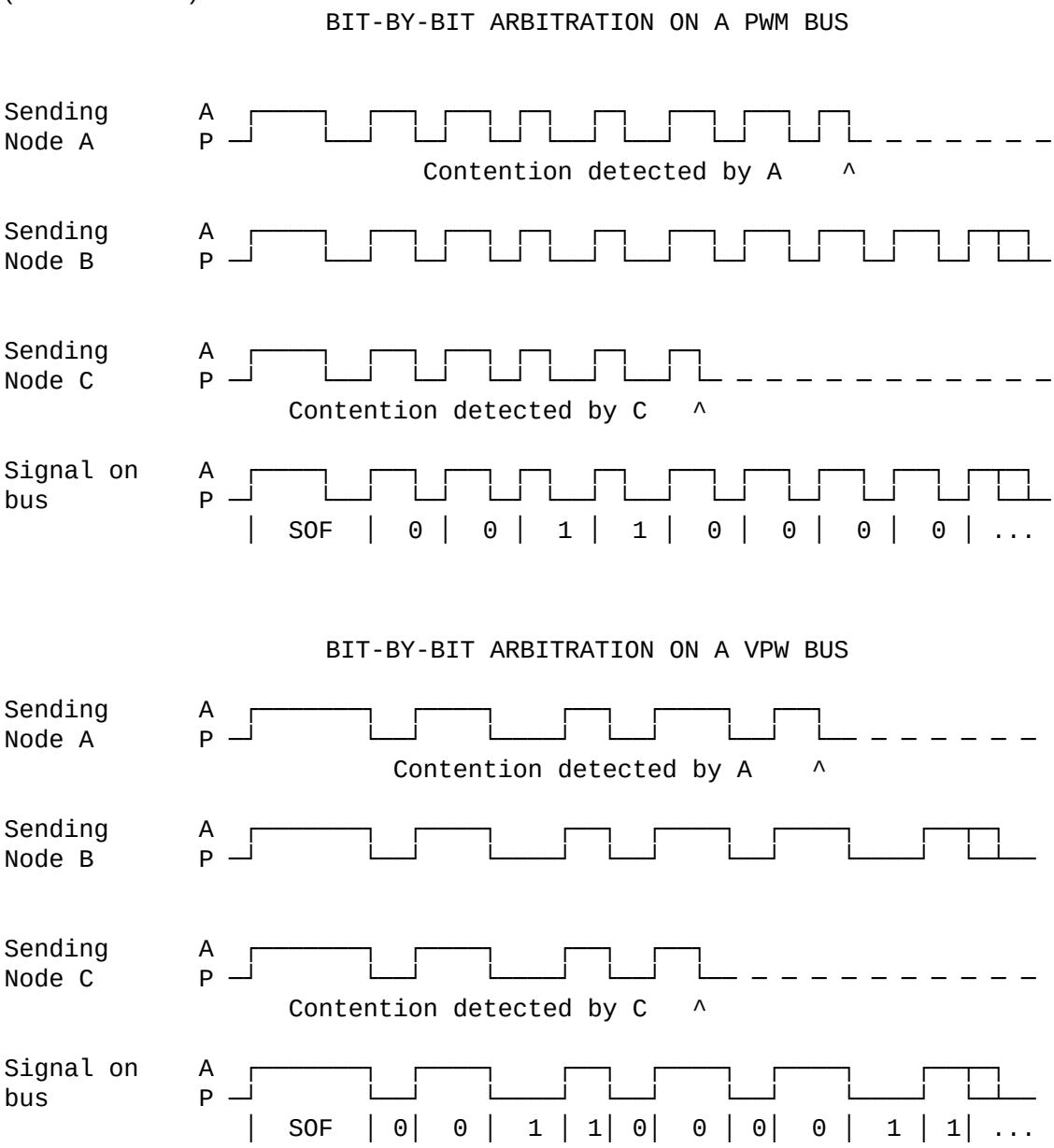


FIGURE 21 - Arbitration

The arbitration process begins with the SOF and continues through all the bits of the frames being sent. As each symbol or bit of all the simultaneous frames is transmitted, all of the nodes still transmitting after the last symbol or bit will detect whether any contention is taking place. Nodes that detect contention have, by definition, lost arbitration and will discontinue sending any further symbols or bits. Any remaining nodes will continue to send their symbols / bits until the next contention is detected. The node which obtains sole access to the medium is that which sends its symbols and bits without detecting any contention.

6.7.3 Arbitration Area - The arbitration resolution described above concerns all the symbols and bits between the SOF and the EOF including, in the case of an in-frame response, all the symbols and bits of the in-frame response. In other words, arbitration acts throughout the frame.

6.7.4 Frame Priority - The bit-by-bit arbitration mechanism allows the implementation of a frame priority system. When unique frames or, more particularly, when arbitration is resolved down to a single transmitter prior to any data values within the frame, a structure of relative frame priority is inherent.

Should two or more nodes attempt to access the bus within the same frame synchronization window (see IFS in Sections 6.6.1.5 and 6.6.2.7), nondestructive arbitration will occur based on the bit value within each frame. The bus allows two states - active and passive. If a active state bit and a passive state bit are transmitted on the bus simultaneously, then the active state bit will override the passive state bit. Hence, frame arbitration occurs in a bit-wise manner. The result of the arbitration is that the node(s) sending lower priority frame(s) will recognize that they have lost arbitration and will discontinue transmitting before the next bit time. The node transmitting the highest priority frame will continue transmitting uninterrupted.

Based on the bit definitions contained in Section 6.6, the lowest value bytes immediately following the SOF will have the highest priority. Therefore, regardless of the number of bits allocated for "frame prioritization," the numerical value of zero will have the absolutely highest priority (that is, 000 is higher priority than 001 or 111).

6.8 Node Wake-Up Via Physical Layer - The transition to a functional/operating network from an unpowered or standby state is a common occurrence in vehicle multiplex systems. In the context of this document the Session Layer controls the transitions between the operating and the standby states.

Two perspectives are used to define the session layer:

a. the view of the media itself, without regard to the individual nodes on the network
b. the view from an individual node

Both are required for a complete definition of the possible states of network operation.

It is expected that a typical vehicle multiplex system may contain a mixture of unpowered and powered nodes, and that the individual nodes may themselves have both powered and standby states.

6.8.1 Network Media

6.8.1.1 Unbiased Network - An unbiased network is all conductors at ground voltage and the impedance of the conductors not controlled. No communication is possible on an unbiased network. The media must first be brought to the biased state before communication can take place. The transition of the network from the unbiased to the biased state may serve as a node wake-up signal for certain applications, but this is not a requirement (i.e., it is possible for individual nodes to be in the sleep state on a fully biased network or in the awake state on an unbiased network).

6.8.1.2 Biased Network - A biased network is all conductors at the "passive" voltage level (with no communciation occurring) and with appropriate impedances capable of supporting communication. Individual nodes on the network may exist in any of the three states described below. Note that nodes which use the optional sleep state are required to wake up from the appropriate network signal within a defined wake-up period. In other words, all nodes which are capable of wake-up from network signals must do so; otherwise these nodes are considered "unpowered". This requirement assures a finite and limited delay to establish communication with nodes which may be in the sleep state.

The time required for the media to make the transition from the unbiased to the biased state is not defined in this document, since this parameter is largely application dependent, and, in fact, may not even occur (e.g., media always biased). For the same reason the time required for a node to make the transition between the unpowered state and the sleep or awake state is also not defined.

6.8.2 Individual Nodes

6.8.2.1 Unpowered Node - An unpowered node is not capable of network communication, nor wake-up from network signal transitions.

6.8.2.2 Sleeping Node - A sleeping node may have an optional low power standby mode capable of detecting network signal transitions for the purpose of wake-up. Any interface device in the sleep state can be awakened by any other interface device via network activity or awakened by its host via its interface to the host. There is no specified requirement for the transition from the awake state to the sleep state, since this is an implementation specific issue.

6.8.2.3 Awake / Operational - An awake / operational node is fully capable of receiving and transmitting frames on the network. The maximum amount of time from the wake-up stimulus until the node is capable of communicating is implementation specific. A transition of the bus from the passive state to the active state shall be considered a "wake-up" signal to a sleeping node. Proper bus bias must be supplied by all nodes designated to supply bias when the network is powered.

6.9 Physical Layer Fault Considerations

6.9.1 Required Fault Tolerant Modes - The network must meet the requirements as defined per the following failure modes:

a. Node Power Loss - All nodes must continue to meet the network leakage current requirement during a loss of power (or low voltage) condition.

b. Bus Short to Ground - Network data communications may be interrupted but there shall be no damage to any node when the bus is shorted to ground.

c. Bus Short to Battery - Network data communications may be interrupted but there shall be no damage to any node when the bus is shorted to battery power.

d. Loss of Node Connection to Ground - When a node loses its ground connection, the remaining nodes shall remain capable of communications.

6.9.2 Optional Fault Tolerant Modes - The network may optionally meet the requirements as defined per the following failure modes:

a. Loss of Termination / Bias - Biasing and termination resistors shall be redundant such that no single point failure will cause the network to become inoperative.

b. Loss of Connection to Network - When a node becomes disconnected from the network, the remaining nodes shall remain capable of communications.

c. Dual Wire Fault Tolerant Operation - Nodes on a dual wire bus may be capable of full communication (sending and receiving frames) at the specified bit rate in the presence of any one of the following faults occurring anywhere on the network:

(1) Bus "+" wire Open Circuit

(2) Bus "-" wire Open Circuit

(3) Bus "+" wire Shorted to Ground

(4) Bus "-" wire Shorted to Ground

(5) Bus "+" wire Shorted to Battery + (V_{batt})

(6) Bus "-" wire Shorted to Battery + (V_{batt})

(7) Bus "+" wire Shorted to any voltage between Ground and Battery

(8) Bus "-" wire Shorted to any voltage between Ground and Battery

Noise immunity and emissions may be somewhat degraded during the faulted period but shall return to normal after the fault is removed.

All nodes shall be protected from damage during the presence of these faults such that recovery to normal operation occurs automatically upon removal of the fault (i.e., faults shall not propagate through the network).

Continued communication is not required for the "Double Fault" condition of the Bus "+" wire shorted to the Bus "-" wire.

6.10 EMC Requirements - The vehicle manufacturer shall specify a minimum EMC level of operation for a module that utilizes this network interface device. A philosophical method for classification of functional performance can be found in SAE J1113 Part 1 Appendix B (formerly SAE J1113 Appendix B). A component manufacturer that designs the interface device to conform to the most severe classification of Class C Region I, for example, could be assured of adequate performance for all conditions.

The modules that communicate with each other via this interface device shall not generate levels of noise emissions (EMI) large enough to interfere with each other. For reference the levels defined by CISPR/D/WG2 (Secretariat) 19 Sept 1989 may be used. In general the specifications on wave shaping and transition rise and fall times control the EMI levels.

The vehicle manufacturers may find SAE J1211 A Recommended Environmental Procedure for Electronic Equipment Design helpful in specifying their multiplex systems. SAE J1879 A Recommended Practice for General Qualification and Production Acceptance Criteria For Integrated Circuits in Automotive Application also may be utilized for specifying components.

This document recommends the vehicle manufacturers use the following documents and the outlined EMC test plan defined in Appendix B. EMC and voltage "level" requirements specified by the Test Plan are given for reference only and the vehicle manufacturer specifications shall be used for compliance testing.

a. Radiated Emissions Antenna & Probe Test (CISPR/D/WG2(Secretariat) 19Sept1989)
b. Transfer Function, Current probe monitoring (SAE J1113 Part 2)
c. Transfer Function, Antenna monitoring (SAE J1113 Part 3)
d. RF Susceptibility (SAE J1113 Part 13)
e. Transient Susceptibility (SAE J1113 Part 10)

7 PARAMETERS

7.1 Application Layer - The following Application Layer requirements shall exist whenever the network is used.

Bit Dominance - A "0" bit dominates over a "1" bit.

7.2 Data Link Layer

7.2.1 Pulse Width Modulation (PWM) at 41.6 Kbps - The maximum frame length from SOF to EOF inclusive is 101 bit times. The maximum number of message bytes (i.e., excluding frame delimiters SOF, EOD, EOF, and IFS) is 12 bytes.

7.2.2 Variable Pulse Width (VPW) at 10.4 Kbps - The maximum number of message bytes (i.e., excluding frame delimiters SOF, EOD, EOF, and IFS) is 12 bytes.

7.3 Physical Layer

7.3.1 General Network Requirements (see Table 2)

TABLE 2 - General Network Parameters

Parameter Description	Parameter Value
On-Vehicle Network Length	35 meters
Off-Vehicle Network Length	5 meters
Total Vehicle Network Length	40 meters
Maximum number of standard unit loads (including off-vehicle equipment)	32 nodes
Off-vehicle load resistance	10.6 Kohms min.
Off-vehicle capacitance (each bus wire to signal or chassis ground, as measured at the SAE J1962 connector)	500 pF max.

7.3.2 Pulse Width Modulation (PWM)

7.3.2.1 PWM Timing Requirements - The following requirements, Table 3, are for a nominal bit time of 24 µs or 41.6 Kbps

TABLE 3 - PWM Pulse Width Times (µsec)

Symbol	Tx,min	Tx,nom	Tx, max	Rx,min	Rx,max
Tp1: Active phase "1"	≥ 6	7	≤ 8	≥ 4	≤ 10
Tp2: Active phase "0"	≥ 14	15	≤ 16	≥ 12	≤ 18
Tp3: Bit time	≥ 23	24	≤ 25	≥ 21	≤ 27
Tp4: SOF / EOD time	≥ 47	48	≤ 49	≥ 42	≤ 54
Tp5: EOF time	≥ 70	72	N/A [1]	≥ 63	N/A [1]
Tp6: IFS time	≥ 93	96	N/A [2]	≥ 84	N/A [2]
Tp7: Active SOF	≥ 29	31	≤ 32	≥ 27	≤ 34
Tp8: Active BRK	≥ 37	39	≤ 41	≥ 35	≤ 43
Tp9: BRK to IFS time	≥ 116	120	N/A [2]	≥ 105	N/A [2]

Notes: [1] EOF transitions into IFS and is not actually a "transmitted" symbol.

[2] Maximum IFS ends at next SOF.

Transmit tolerances include oscillator tolerances, physical layer delays (i.e., turn-on and turn-off delays), and other miscellaneous tolerances. Receive tolerances include considerations for voltage offsets between transmitter and receiver and other miscellaneous tolerances.

Symbols received in the "gray" areas above can be decoded as either the symbol before or after that of the "gray" area. For example, an active pulse of 11 µsec can be decoded as either an active phase "1" (Tp1) or an active phase "0" (Tp2). An incorrect decision will be detected in the CRC error detection byte. Figure 22 below gives an example of how a signal should be decoded based on the received pulse width.

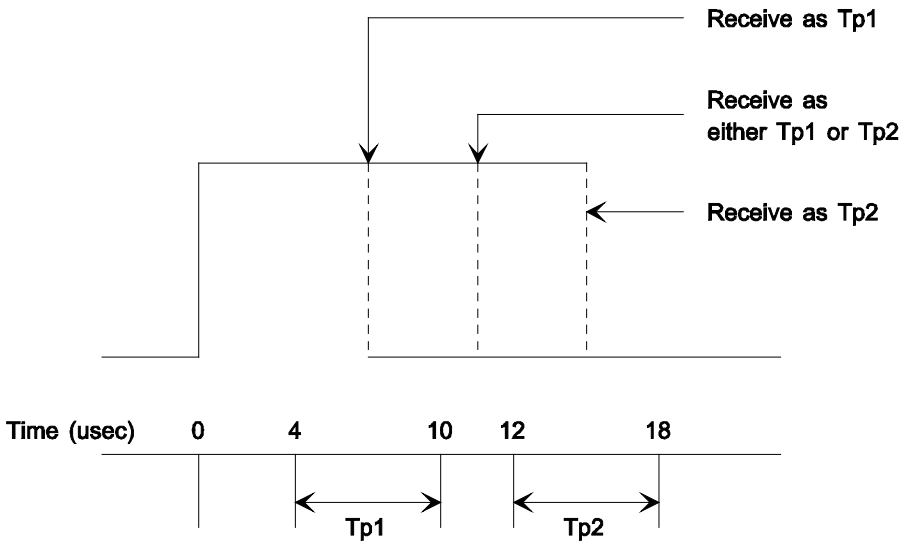


FIGURE 22 - Example of Receiving a Tp1 or Tp2 Symbol

Note that a pulse width detected between Tp1(min) and Tp1(max) must be decoded as an active phase "1" and a pulse width detected between Tp2(min) and Tp2(max) must be decoded as an active phase "0" However, a pulse width detected between Tp1(max) and Tp2(min) can be decoded as either an active phase "1" or active phase "0".

7.3.2.2 PWM DC Parameters (see Table 4)

TABLE 4 - PWM DC Parameters [1]

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage	V_{ih}	2.80	---	6.25	volts
Input Low Voltage	V_{il}	-1.00	---	2.20	volts
Output High Voltage	V_{oh}	3.80	---	5.25	volts
Output Low Voltage	V_{ol}	0.00	---	1.20	volts
Absolute Ground Offset Voltage	V_{go}	0.00	---	1.00	volts
Bus (+) Driver & Bus (-) Termination Supply Voltage	V_{sup}	4.75	5.00	5.25	volts
Receiver Input Common Mode Operating Range	V_{cm}	1.80	---	2.75	volts
Receiver Hysteresis & Overdrive	V_{hys}	---	---	180	mvolts
Network Resistance (each wire)	R_{load}	85	---	378	ohms
Network Capacitance (each wire)	C_{load}	500	---	15,000	pF
Network Time Constant [2]	T_{load}	---	---	1.35	µsec
Signal Transition Time	T_t	---	---	1.75	µsec
Node Resistance (unit load, each wire)	R_{ul}	---	2,880	---	ohms
Node Capacitance (unit load, each wire to ground)	C_{ulg}	---	250	---	pF
Node Capacitance (unit load, wire-to-wire)	C_{ulw}	---	10	---	pF
Node Leakage Current (each wire - active state)	I_{leakA}	---	---	100	µAmp
Node Leakage Current (each wire - passive state, unpowered node)	I_{leakPU}	---	---	100	µAmp
Node Leakage Current (each wire - passive state, powered node)	I_{leakPP}	---	---	20	µAmp

Notes: [1] Refer to Appendix D for an analysis of the PWM waveform.

[2] The network time constant (T_{load}) is the product of R_{load} and C_{load}. Therefore, some combinations of network resistance and network capacitance are not allowed. The product of R_{load} and C_{load} must always be less than $T_{.load,max}$.

7.3.3 Variable Pulse Width Modulation (VPW)

7.3.3.1 VPW Timing Requirements - The following requirements, Table 5, show the VPW timing values.

TABLE 5 - VPW Pulse Width Times (µsec)

Symbol	Tx,min	Tx,nom	Tx, max	Rx,min	Rx,max
Tv1: Short Pulse	≥ 49	64	≤ 79	> 34	≤ 96
Tv2: Long Pulse	≥ 112	128	≤ 145	> 96	≤ 163
Tv3: SOF / EOD time	≥ 182	200	≤ 218	> 163	≤ 239
Tv4: EOF time	≥ 261	280	N/A [1]	> 239	N/A [1]
Tv5: BRK time	≥ 280	300	≤ 5 msec	> 239	≤ 1.0 sec
Tv6: IFS time	≥ 280	300	N/A [2]	> 280	N/A [2]

Notes: [1] EOF transitions into IFS and is not actually a "transmitted" symbol.

[2] Maximum IFS ends at next SOF.

7.3.3.2 VPW DC Parameters (see Table 6)

TABLE 6 - VPW DC Parameters [1]

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage [2]	V_{ih}	4.25	---	20.00	volts
Input Low Voltage	V_{il}	---	---	3.50	volts
Output High Voltage	V_{oh}	6.25	---	8.00	volts
Output Low Voltage	V_{ol}	0.00	---	1.50	volts
Absolute Ground Offset Voltage	V_{go}	0.00	---	2.00	volts
Network Resistance	R_{load}	315	---	1,575	ohms
Network Capacitance	C_{load}	2,470	---	16,544	pF
Network Time Constant [3]	T_{load}	---	---	5.2	µsec
Signal Transition Time	T_t	---		18.0	µsec
Node Resistance (unit load)	R_{ul}	---	10,600	---	ohms
Node Capacitance (unit load)	C_{ul}	---	470	---	pF
Node Leakage Current	I_{leak}	---	---	10	µAmp

Notes: [1] Refer to Appendix C for an analysis of the VPW waveform.

[2] Individual manufacturers may require a higher upper limit ($V_{ih,max}$).

[3] The network time constant (T_{load}) is the product of R_{load} and C_{load}. Therefore, some combinations of network resistance and network capacitance are not allowed. The product of R_{load} and C_{load} must always be less than $T_{.load,max}$.

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APPENDIX A - CHECKLIST OF APPLICATION SPECIFIC FEATURES

A The following checklist is provided as an aid to highlight the communication features of J1850.

TABLE A1 - Checklist of Application Specific Features

FEATURES	Tx	Rx	Comments
FRAME ELEMENTS			
General Frame Elements : IFS, SOF, Data, CRC, EOF.			
End of Data (EOD)			
Normalization Bit (NB) - Tv1/Tv2			
BUS ACCESS			
Idle Bus			
Break (BRK)			
IN-FRAME RESPONSE			
Type 0 (None)			
Type 1 (Single Byte, Single Responder)			
Type 2 (Single Byte, Multiple Responder)			
Type 3 (Multiple Byte, Single Responder)			
ERROR DETECTION			
Cyclic Redundancy Check (CRC)			
Out of Range			
Invalid Bit			
Invalid Symbol			
Invalid Structure			
Invalid Message Length			
Number of Arbitration Bytes			
FAULT TOLERANCE			
Node Power Loss			
Bus Short to Ground			
Bus Short to Battery			
Loss of Node Ground Connection			
Loss of Termination Resistance			
Loss of Network Connection			

TABLE A1 - Checklist of Application Specific Features, (continued)

FEATURES	Tx	Rx	Comments
Dual Wire Fault Tolerance			
HEADER BYTES			
Single Byte			
One Byte Consolidated			
Three Byte Consolidated			
RATE / SYMBOL ENCODING			
10.4 Kbps Variable Pulse Width Modulation (VPWM)			
41.6 Kbps Pulse Width Modulation (PWM)			
FEATURE ELEMENTS			
Maximum Frame Size			
Wake-Up Capability			

APPENDIX B - I/O EMC TEST PLAN

B I/O EMC Test Plan

B.1 Radio Disturbance From Vehicle Components - (CISPR/D/WG2(Secretariat) 19 Sept 1989) - See Figure B1 for diagram

B.1.1 Radiated Emissions Antenna Test

B.1.1.1 Frequency Range - 10 KHz to 1.0 GHz

B.1.1.2 Bandwidth Setting

a. Frequency - 10 KHz to 149 KHz, Bandwidth - 1 KHz
b. Frequency - 150 KHz to 1 GHz, Bandwidth - 3 KHz

B.1.1.3 Test Data

B.1.1.3.1 Ambient Reference

a. 10 KHz modulation off
b. Both transmitter and receiver power off
c. Sweep signal off

B.1.1.3.2 Idle Bus State

a. 10 KHz modulation off
b. Both transmitter and receiver power on
c. Sweep signal off

B.1.1.3.3 Active Bus State

a. 10 KHz modulation on
b. Both transmitter and receiver power on
c. Sweep signal off

B.1.2 Radiated Emissions Probe Test

B.1.2.1 Frequency Range - 10 KHz to 200 MHz

B.1.2.2 Bandwidth Setting

a. Frequency - 10 KHz to 149 KHz, Bandwidth - 1 KHz
b. Frequency - 150 KHz to 1 GHz, Bandwidth - 3 KHz

B.1.2.3 Probe Type - As required to make measurements

a. Recommended probe type - Tektronix A6302 (0 - 29 MHz)
b. Recommended probe type - Ailtech 94111-1 (30 - 200 MHz)

B.1.2.4 Probe Distance - 5 cm from part

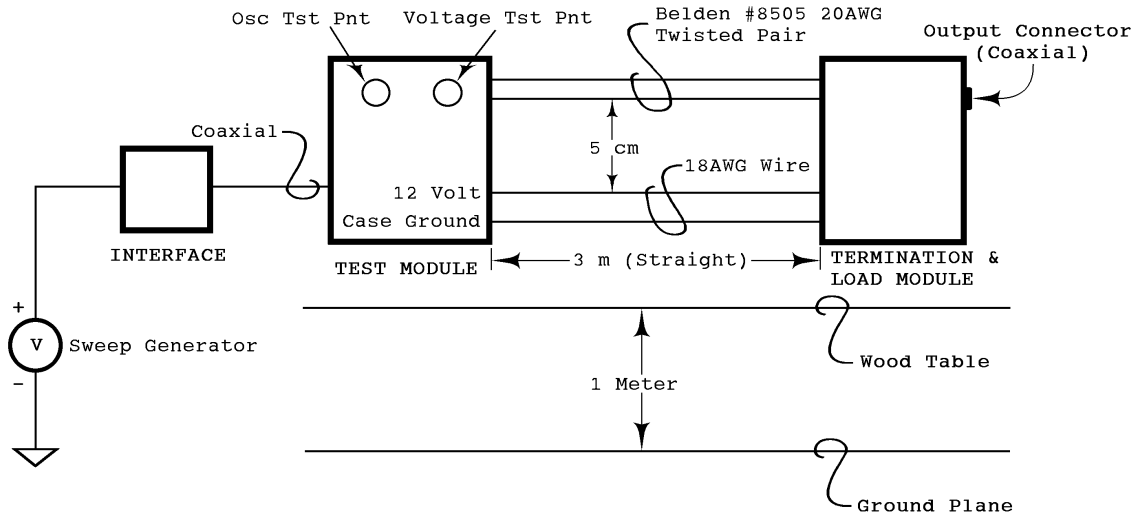

FIGURE B1 - EMC Test Setup

B.1.2.5 Test Data

B.1.2.5.1 Ambient Reference

a. 10 KHz modulation off
b. Both transmitter and receiver power off
c. Sweep signal off

B.1.2.5.2 Idle State

a. 10 KHz modulation off
b. Both transmitter and receiver power on
c. Sweep signal off

B.1.2.5.3 Active Bus

a. 10 KHz modulation on
b. Both transmitter and receiver power on
c. Sweep signal off

B.2 Transfer Function - Electromagnetic Susceptibility Measurement Procedures for Vehicle Components

B.2.1 Current Probe Monitoring - Adapted from SAE J1113 Part 2 (Formerly SAE J1113 (Aug 87) Section 2).

a. Frequency - 30 Hz to 250 KHz
b. Amplitude - 1 V peak to peak at test point

B.2.2 Antenna Monitoring - Adapted from SAE J1113 Part 3 (Formerly SAE J1113 (Aug 87) Section 3).

a. Frequency - 250 KHz to 200 MHz
b. Attenuator input power - $\approx$ 25 milliwatts to generate 1 V peak to peak at test point

B.2.3 Test Data

B.2.3.1 Transfer Function from Vcc to Bus

a. 10 KHz modulation on
b. Both transmitter and receiver power on
c. Sweep signal on

B.2.3.2 Transfer Function from Ground to Bus

a. 10 KHz modulation on
b. Both transmitter and receiver power on
c. Sweep signal on

B.3 RF Susceptibility

Electromagnetic Susceptibility Measurement Procedures for Common Mode Injection for compliance, test per SAE J1113 Part 13 (Formerly SAE J1547)

B.3.1 Frequency Range - 1 MHz to 200 MHz

B.3.2 Max Level - 100 mA RMS

B.3.3 Procedure - Injection and monitoring to be applied to Bus pair only

B.3.4 Test Data - Record the nature of any interaction occurring below the test level along with the current and frequency

B.4 Transient Susceptibility - Test per SAE J1113 Part 10 (Adapted from ISO 7637/3)

Test Pulse Amplitude

a. Test Pulse 1: -30 volts (Reference)
b. Test Pulse 2: +30 volts (Reference)
c. Test Pulse 3a: -60 volts (Reference)
d. Test Pulse 3b: +40 volts (Reference)

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APPENDIX C - VPW WAVEFORM ANALYSIS

C VPW Waveform Analysis

Figure C1 shows a drawing of a bus waveform with various voltage levels and trip points. The voltage levels and trip points are defined as follows:

C.1 Voltage Levels and Trip Points

C.1.1 $V_{oh,min}$ - Minimum guaranteed output high voltage. This is also the highest trip point, with the source having no ground offset noise, and the receiver having 2V of noise.

C.1.2 $V_{ol,max}$ - Maximum guaranteed output low voltage. This is also the highest trip point, with the receiver having no ground offset noise, and the source having 2V of noise.

C.1.3 V_t - Ideal receiver trip point.

C.1.4 $V_{ih,min}$ - Minimum guaranteed input high voltage, and is also the highest trip point with no offset noise.

C.1.5 $V_{il,max}$ - Maximum guaranteed input low voltage, and is also the lowest trip point with no offset noise.

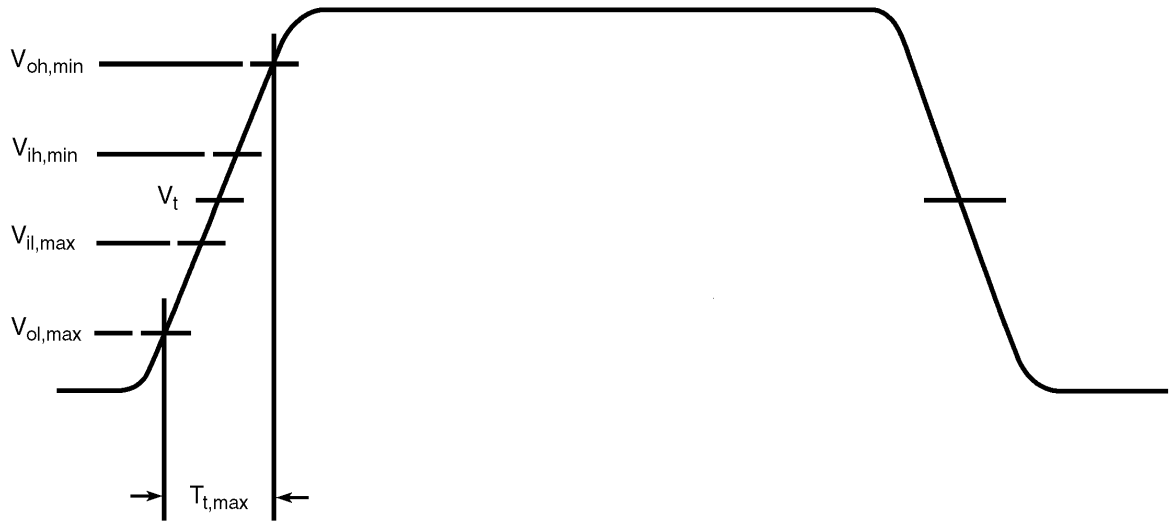

FIGURE C1 - Voltage Levels and Trip Points

C.2 VPW Pulse Width Analysis

Factors that affect the transmitted pulse width are oscillator tolerance and variations in delay through the source driver, and the medium. These factors, along with some guard banding, are lumped into a single set of limits called $T_{x,min}$ and $T_{x,max}$ for each bus symbol.

The equations C1 and C2 are used to generate the transmitted pulse values shown in Table C1:

$$T_{x,min} = (T_{nom} - T_{t,max}/2) * 0.98 - T_{x,mar} \quad \text{(Eq. C1)}$$

$$T_{x,max} = (T_{nom} + T_{t,max}/2) * 1.02 + T_{x,mar} \quad \text{(Eq. C2)}$$

The $(T_{nom} \pm T_{t,max}/2) * 2\%$ factor covers the 2% oscillator tolerance. The $T_{x,nom}$ and $T_{t,max}$ factors are given in section 7. The $T_{x,mar}$ factor is assumed to be 7.0 which covers the rest of the factors (lumped variation in delay through the source driver and medium).

For VPW, mode synchronization is an integral part of symbol timing. All transmitting nodes reference their transmit timing from their receiver's perception of the previous edge, without regard to whether that edge was due to their own or another transmitter.

Figure C2 shows a plot of T_x, $T_{x,min}$ and $T_{x,max}$. Each is measured from the ideal trip point on the leading edge of the waveform. The fact that what is seen at the source's own receiver contributes to the transmitted pulse width, implies that the source device could be using echoed back information to shape what is transmitted.

The pulse width seen by another node (receiver) can range from $T_{x,min} - T_{t,max}$ to $T_{x,max} + T_{t,max}$. This range comes from the variations in the transmitted pulse width combined with possible noise offset affects on the transmitted and receiving node. The $T_{x,min} - T_{t,max}$ situation occurs when a $T_{x,min}$ pulse width is transmitted by a source node with no ground offset noise, and received by a receiving node with a 2V of ground offset noise. This sets up the possibility of the receiver tripping at $V_{oh,min}$ on the leading and trailing edge of the waveform. Therefore the pulse width seen by another node for the this $T_{x,min} - T_{t,max}$ situation including the oscillator tolerance and guard banding is given by equation C4. Equation C5 is derived by substituting equation C1 for $T_{x,min}$ in equation C4. The $T_{t,max}/2$ factor is equal to zero since an ideal trip point and no ground offset was assumed. The $T_{x,max} + T_{t,max}$ situation occurs with a $T_{x,max}$ pulse being transmitted, the source node having 2V of noise, and the receiver having no offset. This sets up the possibility of the receiving node tripping at $V_{ol,max}$. Again the actual acceptance range must be wider to allow for the receiving node's oscillator tolerance and any implementation dependent uncertainties or constraints. Similarly equations C7 and C8 are derived.

The receiving node may perceive the leading edge sooner or later than the transmitting node (source node). This range represents a receiver's required acceptance range for a given bus symbol. Figure C2 shows a drawing of this acceptance range.

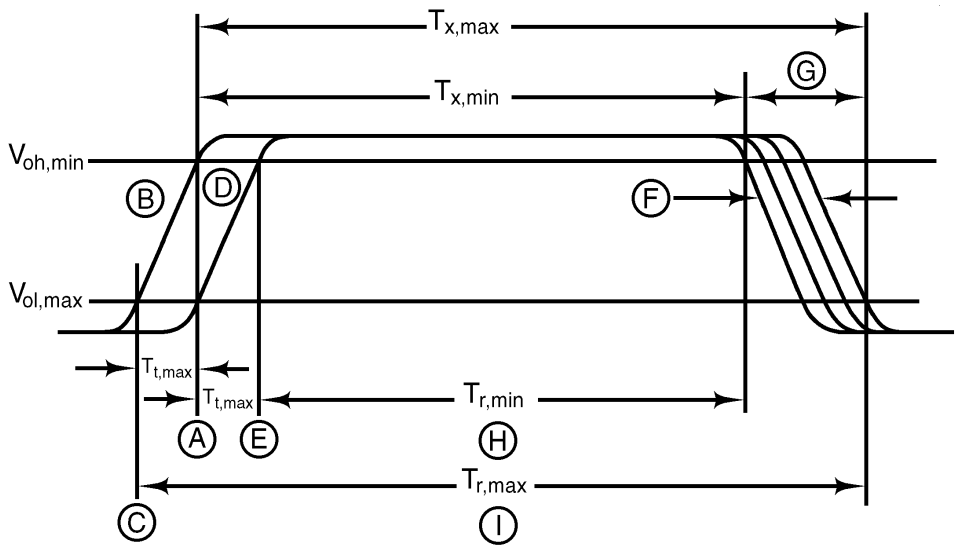

FIGURE C2 - Waveform Timing Parameters

A - The trigger point on waveform "B" or "D" where the transmitting node sees the transition ending the previous symbol, and starts timing the current symbol. Take note that a node could trigger at any level of a transition between $V_{ol,max}$ and $V_{oh,min}$. The maximum and minimum trigger points of any given transition are illustrated by showing line A cutting through two different waveform transitions. This method of illustration allows separating the uncertainties of nodes sensing the beginning and ending of a symbol.

B - The earliest waveform that could trigger the transmitter at point A.

C - The earliest point on waveform "B" that could trigger any other node.

D - The latest waveform that could trigger the transmitter at point A.

E - The latest point on waveform "D" that could trigger any other node.

F - The waveform dispersion due to transmitter tolerances in oscillator, driver, etc.

G - The total transmitter spread when transition time limits are combined with the other tolerances in "F".

H - The shortest legitimate symbol time which can legitimately be seen under worst case conditions.

I - The longest legitimate symbol time which can legitimately be seen under worst case conditions.

Notes: $T_{x,max}$ - Starts at $V_{oh,min}$ on wave "B"; $T_{x,min}$ - Starts at $V_{ol,max}$ on wave "D"

The calculations for the received $T_{r,min}$ and $T_{r,max}$ are derived using the factors specified in section 7 for a 2 V ground offset range and a transition rise time of $T_{t,max}$. The transmitting node $T_{t,max}$ factor would be zero (0) if it was a perfect receiver and sensed a transition at the ideal trip point. However, for a real receiver the trip point $T_{tp,max}$ can be approximated by equation B3 assuming a liner waveform rise time.

$$T_{tp,max} = T_{t,max} * ((V_{ih,min} - V_{il,max})/(V_{oh,min} - V_{ih,min})) \quad \text{(Eq. C3)}$$

The values for this range shown in Table C1 were arrived at using equations C6 and C9. Note these values compare favorably with the values specified in Section 7, Table 5.

$$T_{r,min} = (T_{x,min} - T_{t,max}) * 0.98 - T_{r,mar} \quad \text{(Eq. C4)}$$

$$T_{r,min} = ([(T_{nom} - T_{t,max}/2) * 0.98 - T_{x,mar}] - T_{t,max}) * 0.98 - T_{r,mar} \quad \text{(Eq. C5)}$$

$$T_{r,min} = ([(T_{nom} - T_{tp,max}/2) * 0.98 - T_{x,mar}] - T_{t,max}) * 0.98 - T_{r,mar} \quad \text{(Eq. C6)}$$

$$T_{r,max} = (T_{x,max} + T_{t,max}) * 1.02 + T_{r,mar} \quad \text{(Eq. C7)}$$

$$T_{r,max} = ([(T_{nom} + T_{t,max}/2) * 1.02 + T_{x,mar}] + T_{t,max}) * 1.02 + T_{r,mar} \quad \text{(Eq. C8)}$$

$$T_{r,max} = ([(T_{nom} + T_{tp,max}/2) * 1.02 + T_{x,mar}] + T_{t,max}) * 0.98 + T_{r,mar} \quad \text{(Eq. C9)}$$

The 2% guard bands cover the oscillator tolerances of both transmitter and receiver and $T_{r,mar}$ = 4.0 covers the other uncertainties, including receiver delay and digital filter delay. VPW bus symbols allow no forbidden zones between symbols.

Table C1 shows the VPW Pulse Width Timing Requirements

TABLE C1 - VPW Pulse Width Times (µsec)

Symbol	Tx,min	Tx,nom	Tx, max	Rx,min	Rx,max
Tv1: Short Pulse	49	64	79	34	96
Tv2: Long Pulse	112	128	145	95	162
Tv3: SOF / EOD time	182	200	218	164	237
Tv4: EOF time	261	280	N/A	241	N/A

Filter Compensation - The reason for choosing a synchronous data encoding technique is to synchronize at every valid state transition. If the delays through the filter, receiver, and output drivers can be characterized into a constant value this delay can be compensated for by the timing logic. If variations in delay caused by this Filter and I/O Hardware cannot be easily compensated for, then the Source Interface device variations should be included in the ± 5.0 µs factor defined in $T_{x,min}$ and $T_{x,max}$. All further, variations in delay and including a safety factor for dead zones between symbols for the Receiving device should be included in the ± 4.0 µs factor defined in $T_{r,min}$ and $T_{r,max}$.

D PWM Waveform Analysis

Figure D1 shows a drawing of a typical bus waveform with various voltage levels and trip points. Table D1 contains the DC parameter specifications.

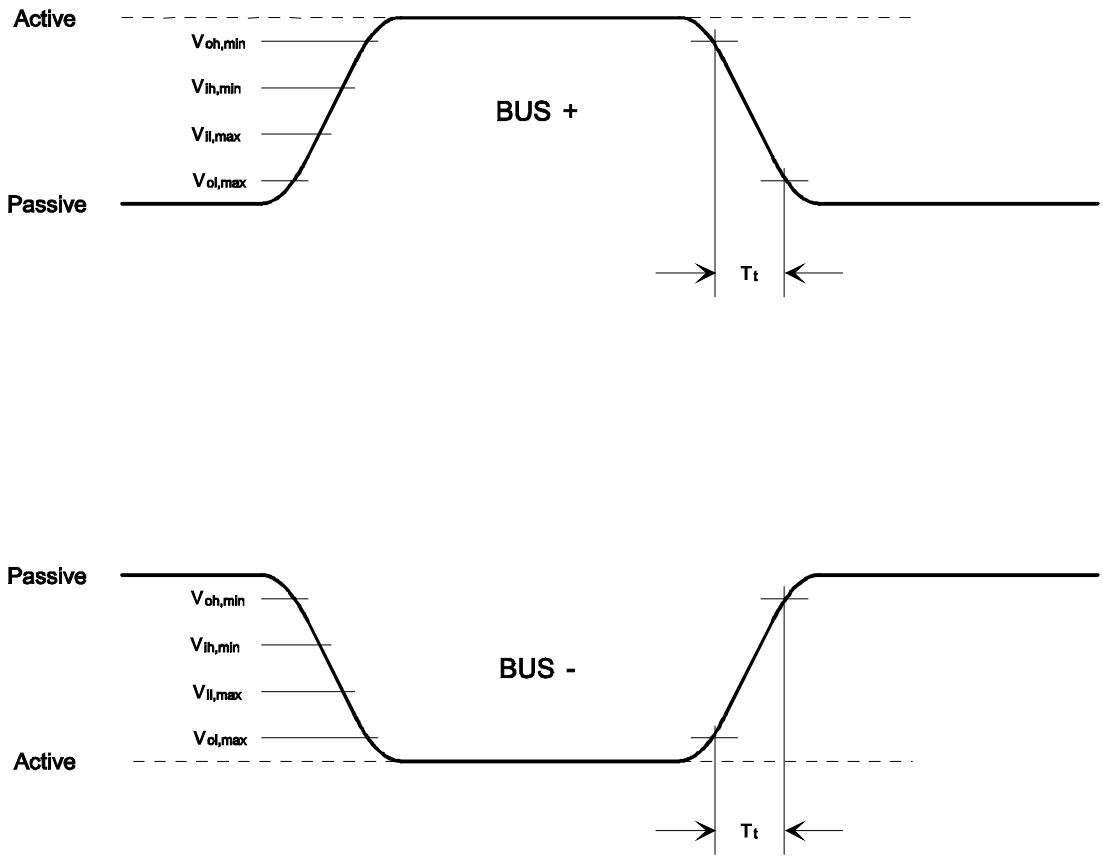

FIGURE D1 - Typical PWM Waveform

TABLE D1 - PWM DC Parameters

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage	V_{ih}	2.80	---	6.25	volts
Input Low Voltage	V_{il}	-1.00	---	2.20	volts
Output High Voltage	V_{oh}	3.80	---	5.25	volts
Output Low Voltage	V_{ol}	0.00	---	1.20	volts
Absolute Ground Offset Voltage	V_{go}	0.00	---	1.00	volts
Bus (+) Driver & Bus (-) Termination Supply Voltage	V_{sup}	4.75	5.00	5.25	volts
Receiver Input Common Mode Operating Range	V_{cm}	1.80	---	2.75	volts
Receiver Hysteresis & Overdrive	V_{hys}	---	---	180	mvolts
Network Resistance (each wire)	R_{load}	85	---	378	ohms
Network Capacitance (each wire)	C_{load}	500	---	15,000	pF
Network Time Constant [1]	T_{load}	---	---	1.35	µsec
Signal Transition Time	T_t	---	---	1.75	µsec
Node Resistance (unit load, each wire)	R_{ul}	---	2,880	---	ohms
Node Capacitance (unit load, each wire to ground)	C_{ulg}	---	250	---	pF
Node Capacitance (unit load, wire-to-wire)	C_{ulw}	---	10	---	pF
Node Leakage Current (each wire - active state)	I_{leakA}	---	---	100	µAmp
Node Leakage Current (each wire - passive state, unpowered node)	I_{leakPU}	---	---	100	µAmp
Node Leakage Current (each wire - passive state, powered node)	I_{leakPP}	---	---	20	µAmp

Notes: [1] The network time constant (T_{load}) is the product of R_{load} and C_{load}. Therefore, some combinations of network resistance and network capacitance are not allowed. The product of R_{load} and C_{load} must always be less than $T_{load,max}$.

D.1 Voltage Levels and Trip Points

D.1.1 V_{ih} - This is the input high voltage which a receiver must detect as an active state on bus (+) and as a passive state on bus (-).

D.1.2 V_{il} - This is the input low voltage which a transmitter must detect as an active state on bus (-) and as a passive state on bus (+).

D.1.3 V_{oh} - This is the output high voltage which a transmitter must drive bus (+) and the voltage which bus (-) must passively return to. Note that $V_{oh,min}$ is $V_{ih,min}$ plus the absolute maximum ground offset voltage ($V_{go,max}$).

D.1.4 V_{ol} - This is the output low voltage which a transmitter must drive bus (-) and the voltage which bus (+) must passively return to. Note that $V_{ol,max}$ is $V_{il,max}$ minus the absolute maximum ground offset voltage ($V_{go,max}$).

D.1.5 V_{og} - This is the absolute ground offset voltage that can exist between any two nodes on the network.

D.1.6 V_{sup} - This is the supply voltage which a transmitter must use to drive bus (+) and terminate bus (-).

D.1.7 V_{cm} - This is the receiver input common mode operating range. In order for the differential receiver to recognize a valid signal transition, the bus (+) and bus (-) signals must cross at a voltage within this range.

D.1.8 V_{hys} - This is the receiver hysteresis and overdrive voltage including any power supply reference tolerance.

D.1.9 R_{load} - This is the equivalent network resistance from each bus wire to the corresponding passive voltage source.

D.1.10 C_{load} - This is the equivalent network capacitance from each bus wire to ground.

D.1.11 T_{load} - This is the network time constant for each bus wire. This is the product of R_{load} and C_{load} of each bus wire. The time constant determines the maximum active-to-passive transition time.

D.1.12 T_t - This is the signal transition time for each bus wire from either the active-to-passive state or passive-to-active state. The passive-to-active edge is driven by the transmitter and shall be no more than $T_{t,max}$. The active-to-passive edge is determined by the network time constant, bus voltage levels, and the passive state supply voltage level.

D.1.13 C_{ulg} - This is the unit load node capacitance of each wire to ground. This capacitance along with the unit load node capacitance wire-to-wire results in the total network capacitance referred to in paragraph C.1.10.

D.1.14 C_{ulw} - This is the unit load node capacitance wire-to-wire. This capacitance along with the node capacitance of each wire to ground results in the total network capacitance referred to in paragraph C.1.10.

D.1.15 I_{leakA} - This is the leakage current of each wire when the bus in in the active state.

D.1.16 I_{leakPU} - This is the leakage current of each wire when the bus in in the passive state and the node is unpowered.

D.1.17 I_{leakPP} - This is the leakage current of each wire when the bus in in the passive state and the node is powered.

D.2 Input Voltage Limits

Given the Bus (+) Driver & Bus (-) Termination Supply Voltage (V_{sup}) and the maximum Receiver Hysteresis & Overdrive Voltage (V_{hys}), V_{ih} and V_{il} can be derived.

$V_{il,min}$ = (Ground Reference) - V_{go} = 0.00 - 1.00 = -1.00 V (Eq. D1)

$V_{il,max}$ = ½ ($V_{sup,min}$) - $V_{hys,min}$ = ½ (4.75) - 0.18 = 2.20 V (Eq. D2)

$V_{ih,min}$ = ½ ($V_{sup,max}$) + $V_{hys,max}$ = ½ (5.25) + 0.18 = 2.81 V (Eq. D3)

$V_{ih,max}$ = $V_{sup,max}$ + V_{go} = 5.25 + 1.00 = 6.25 V (Eq. D4)

where the ½ factor in $V_{il,max}$ and $V_{ih,min}$ assumes a receive comparator voltage level of one-half of the supply voltage. It turns out this is a good trade-off for voltage ground offset capability versus output drive requirements.

D.3 Output Voltage Limits

Output voltage limits can be derived directly from the input voltage limits.

$V_{ol,min}$ = $V_{il,min}$ + V_{go} = -1.00 + 1.00 = 0 V (Ground Reference) (Eq. D5)

$V_{ol,max}$ = $V_{il,max}$ - V_{go} = 2.20 - 1.00 = 1.20 V (Eq. D6)

$V_{oh,min}$ = $V_{ih,min}$ + V_{go} = 2.80 + 1.00 = 3.80 V (Eq. D7)

$V_{oh,max}$ = $V_{ih,max}$ - V_{go} = 6.25 - 1.00 = 5.25 ($V_{sup,max}$) (Eq. D8)

D.4 Network Time Constant & Signal Transition Time

In order to guarantee signal cross over in the Receiver Input Common Mode Operating Range (V_{cm}) the signal transition time must be less than 2.20 µsec. This is $T_{t,max}$ + the worst case transition time from $V_{ol,min}$ to $V_{ol,max}$ for Bus (-), or $V_{oh,max}$ to $V_{oh,min}$ for Bus (+). Therefore, given Δt = 2.20 µsec, the following relationship for $V_{oh,min}$ must be satisfied for Bus (-) and $V_{ol,max}$ for Bus (+).

$V_{oh,min} = V_{sup,min} (1 - e^{-(\Delta t / Tload,max)})$ for Bus (-) (Eq. D9)

$V_{ol,max} = V_{oh,max} (e^{-(\Delta t / Tload,max)})$ for Bus (+) (Eq. D10)

From this, the maximum network time constant ($T_{load,max}$) can be derived.

$$T_{load,max}(\text{Bus-}) = -\Delta t \div \ln(1-(V_{oh,min} / V_{sup,min})) \quad \text{(Eq. D11)}$$

$$= -2.20 \div \ln(1-(3.80/4.75)) = 1.37\ \mu\text{sec}$$

$$T_{load,max}(\text{Bus+}) = -\Delta t \div \ln(V_{ol,max} / V_{oh,max})) \quad \text{(Eq. D12)}$$

$$= -2.20 \div \ln(1.20/5.25) = 1.49\ \mu\text{sec}$$

Choosing a $T_{load,max}$ of 1.35 µsec satisfies both equations. Given a maximum network time constant of 1.35 µsec, the signal transition time $T_{t,max}$ can be found by subtracting the time from $V_{ol,min}$ to $V_{ol,max}$ (for Bus -) or the time from $V_{oh,max}$ to $V_{oh,min}$ (for Bus +) from 2.20 µsec.

Bus (-):

$$T(V_{ol,min} \text{ to } V_{ol,max}) = -T_{load,max} (\ln(1-(V_{ol,max} / V_{sup,min}))) \quad \text{(Eq. D13)}$$

$$= -1.35 (\ln(1-(1.20/4.75))) = 0.39\ \mu\text{sec}$$

$$T_{load,max} = 2.20 - T(V_{ol,min} \text{ to } V_{ol,max}) \quad \text{(Eq. D14)}$$

$$= 2.20 - 0.39 = 1.81\ \mu\text{sec}$$

Bus (+):

$$T(V_{oh,max} \text{ to } V_{oh,min}) = -T_{load,max} (\ln(V_{oh,min} / V_{oh,max})) \quad \text{(Eq. D15)}$$

$$= -1.35 (\ln(3.80/5.25))) = 0.44\ \mu\text{sec}$$

$$T_{load,max} = 2.20 - T(V_{oh,max} \text{ to } V_{oh,min}) \quad \text{(Eq. D16)}$$

$$= 2.20 - 0.44 = 1.76\ \mu\text{sec}$$

Therefore, choosing a network time constant $T_{load,max}$, of 1.35 µsec and a signal transition time $T_{t,max}$ of 1.75 µsec ensures that the two bus signals will cross within the Common Mode Operating Range.

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