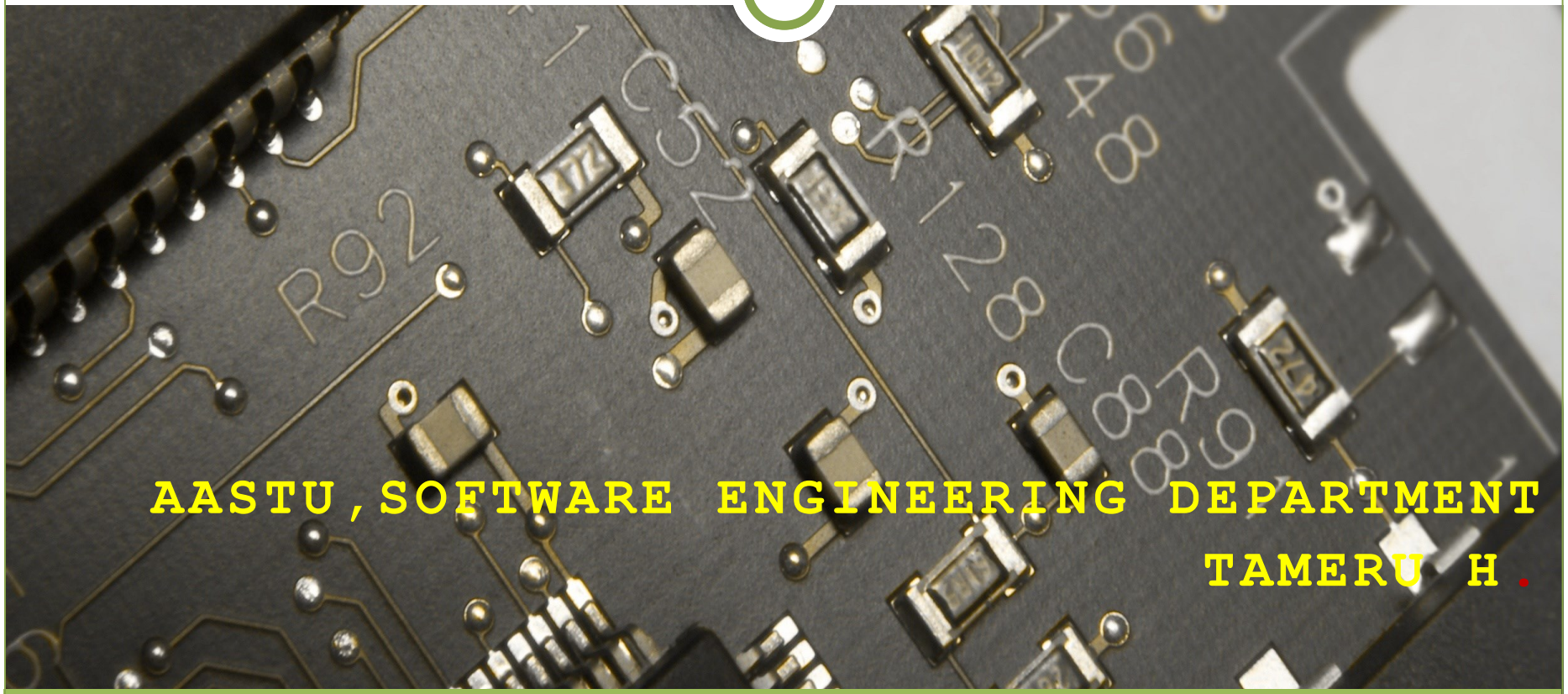
# Chapter Three

## Top Level View of Computer Function and Interconnection

## Part 1

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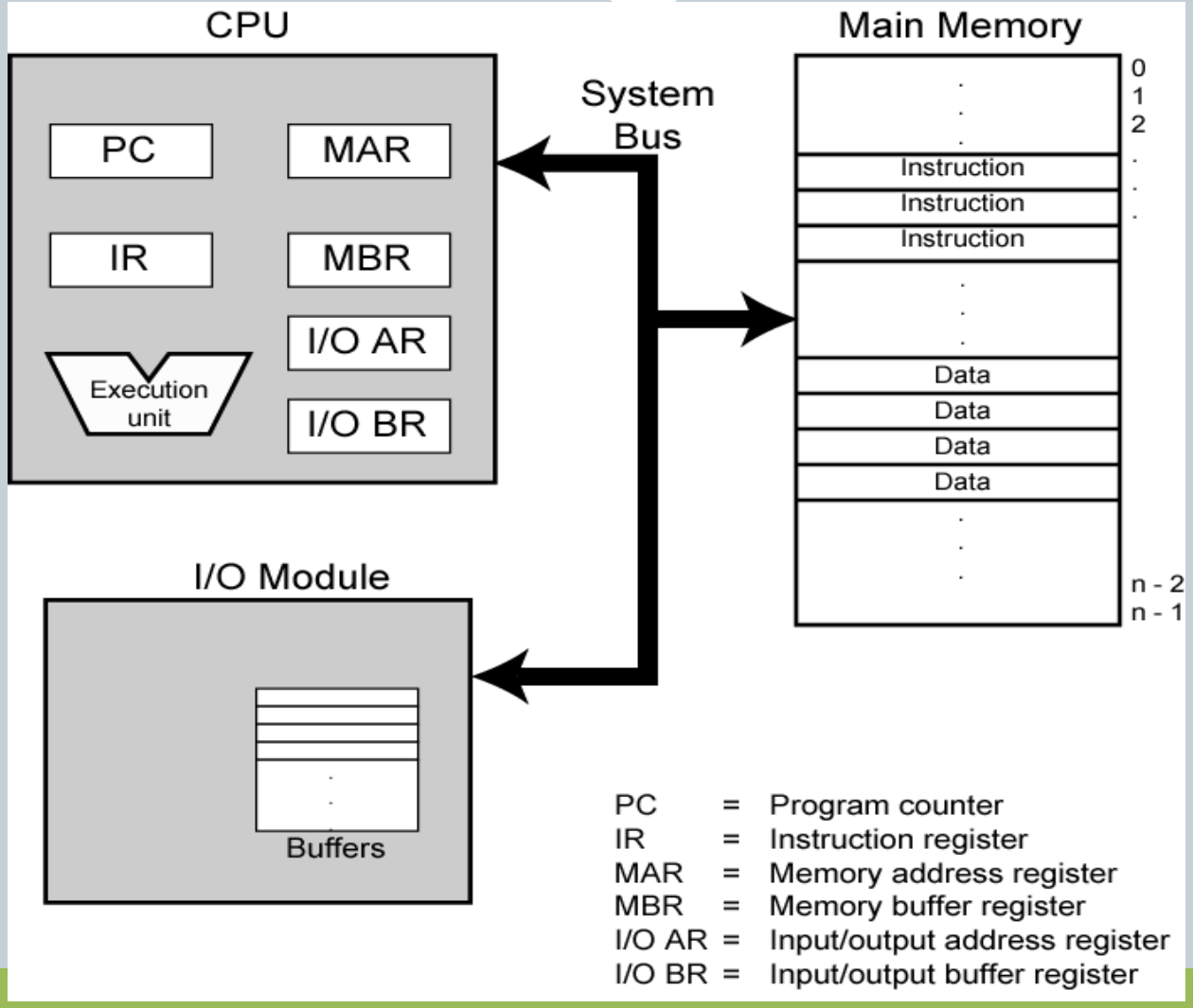
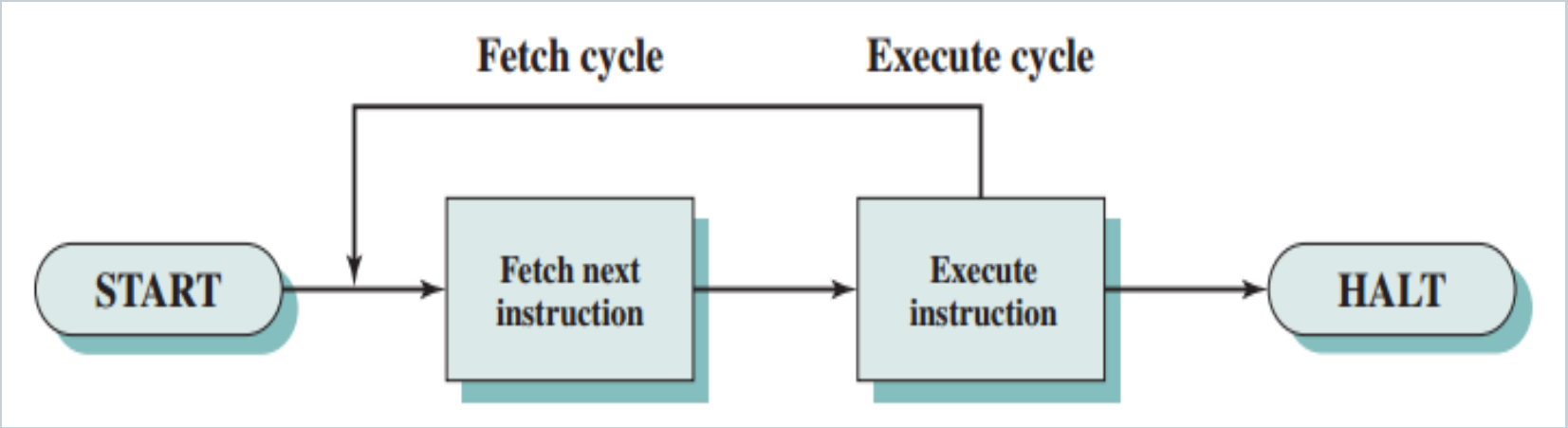
# Computer Components



# Instruction Cycle

Two steps:

- Fetch
- Execute



# Fetch Cycle

- Program Counter (PC) holds address of next instruction to fetch
- Processor fetches instruction from memory location pointed to by PC
- Increment PC

  Unless told otherwise
- Instruction loaded into Instruction Register (IR)
- Processor interprets instruction and performs required actions

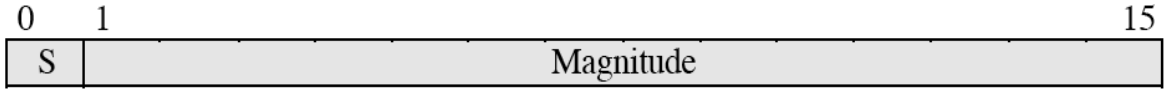
# Execute Cycle

- **Processor-memory**
  - ✓data transfer between CPU and main memory
- **Processor I/O**
  - ✓Data transfer between CPU and I/O module
- **Data processing**
  - ✓Some arithmetic or logical operation on data
- **Control**
  - ✓Alteration of sequence of operations

  e.g. jump
- **Combination of above**

# Hypothetical Machine


(a) Instruction format




(b) Integer format

Program Counter (PC) = Address of instruction
Instruction Register (IR) = Instruction being executed
Accumulator (AC) = Temporary storage

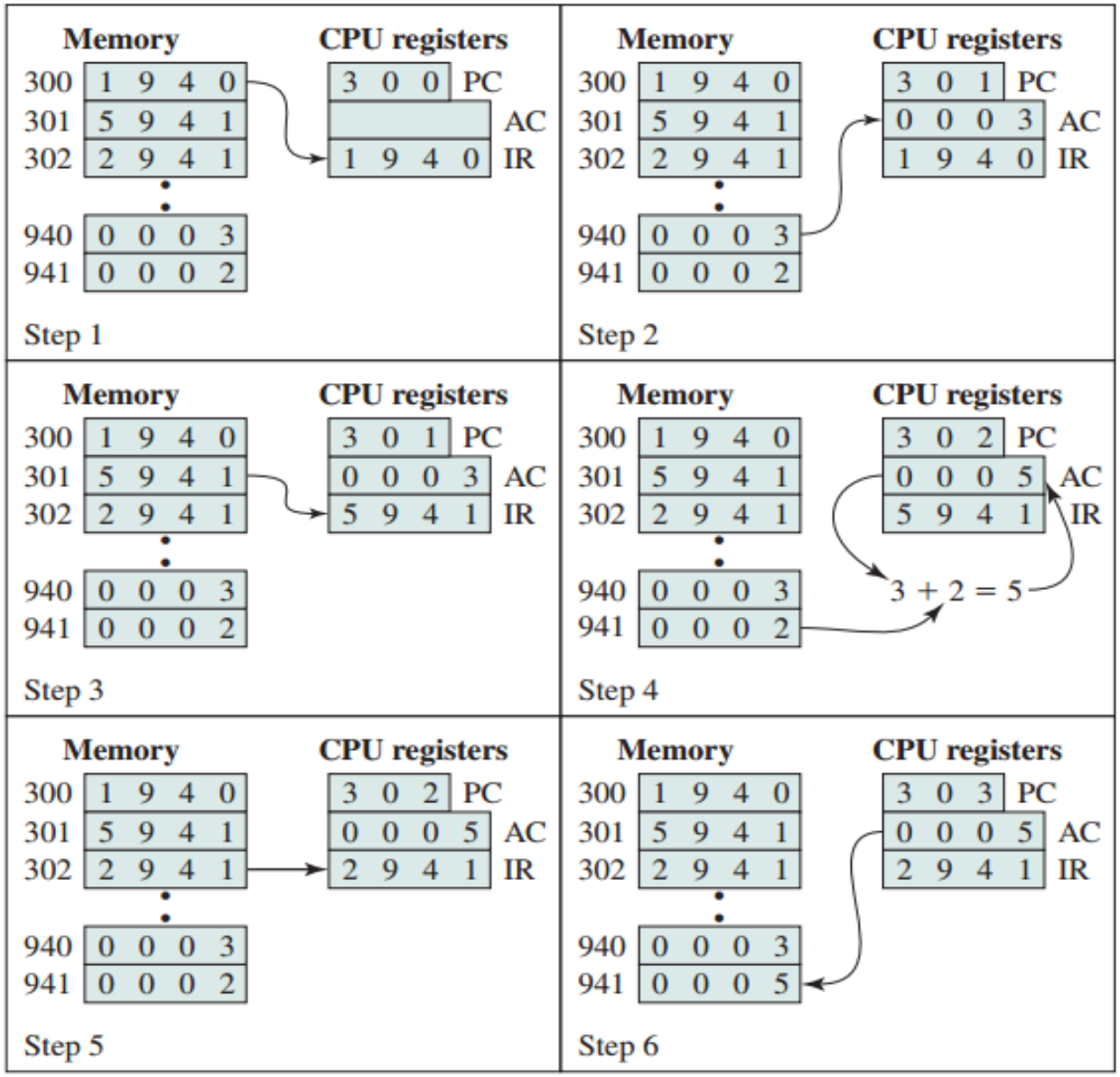
(c) Internal CPU registers

0001 = Load AC from Memory
0010 = Store AC to Memory
0101 = Add to AC from Memory

(d) Partial list of opcodes

**Figure 3.4 Characteristics of a Hypothetical Machine**

# Example


Memory
CPU registers
300 1 9 4 0
301 5 9 4 1
302 2 9 4 1
940 0 0 0 3
941 0 0 0 2
3 0 0 PC
AC
1 9 4 0 IR
Step 1
3 0 1 PC
0 0 0 3 AC
1 9 4 0 IR
Step 2
5 9 4 1 IR
Step 3
3 0 2 PC
0 0 0 5 AC
3 + 2 = 5
Step 4
2 9 4 1 IR
Step 5
3 0 3 PC
Step 6

# Instruction State Diagram