Analog Integrated System Design – Cadence Tools

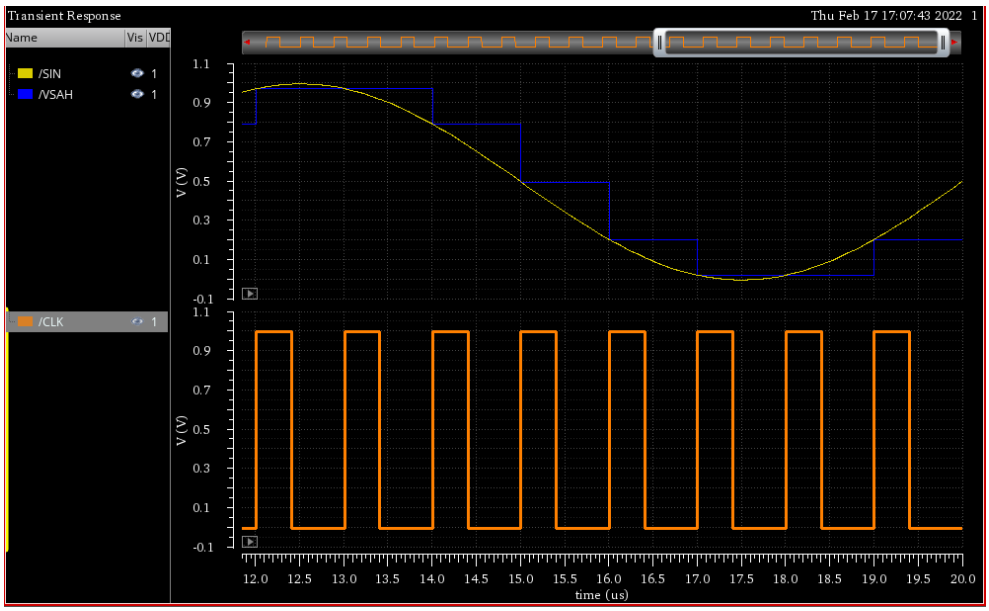
LAB 08 Solution (Mini-Project 01)

SAR ADC

Part 1: Verilog-A Behavioral Models

Testing Blocks:

1-Ideal_sah_switch:

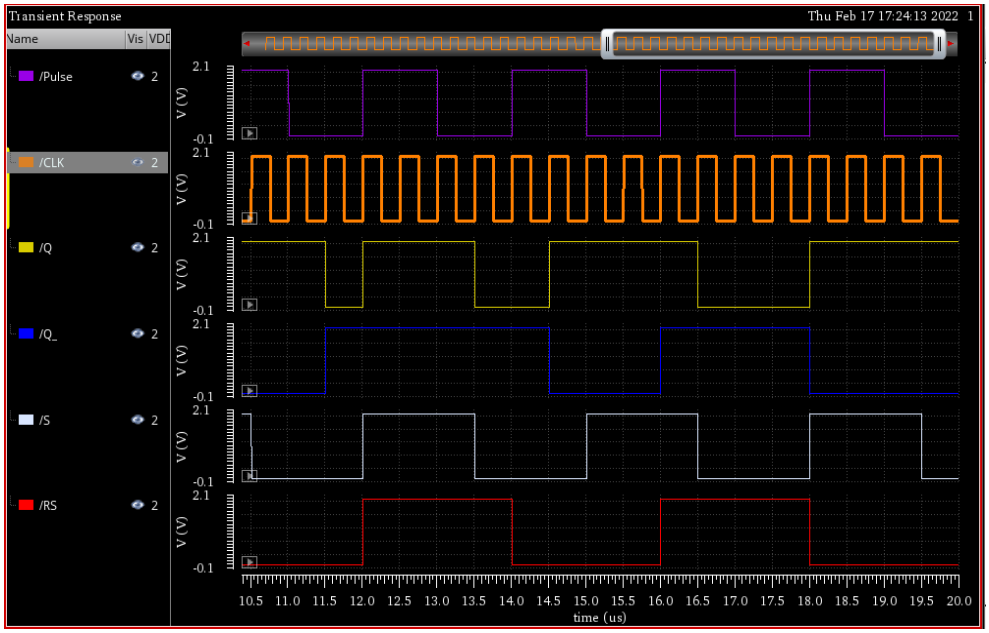


2-DFF:

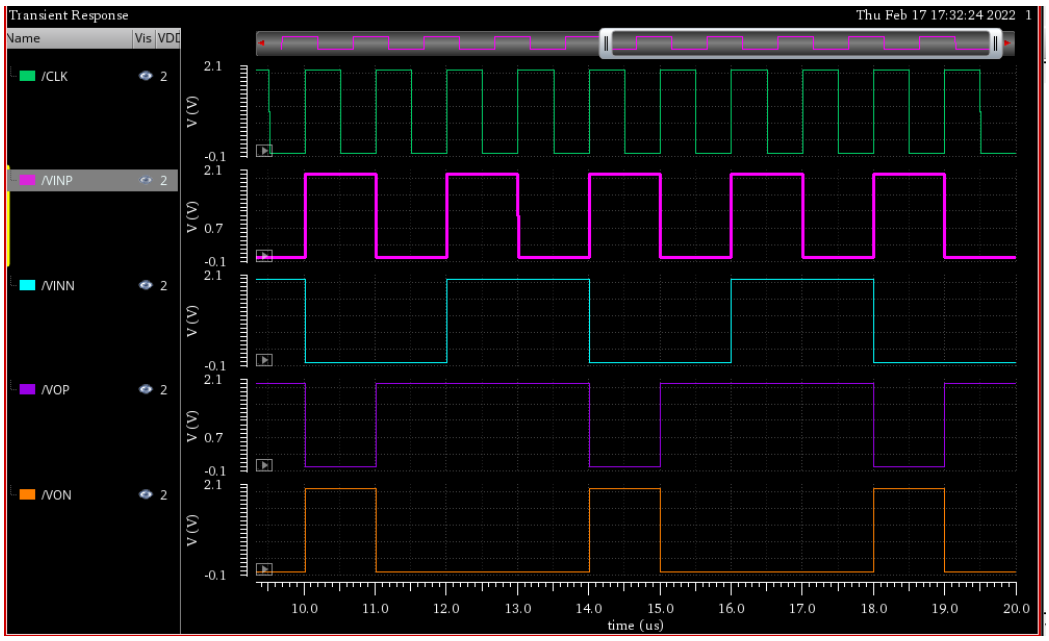
-When no set or reset, clock edges fetch D to Q.

-When Set, Q is 1.

-When Reset, Q is 0.



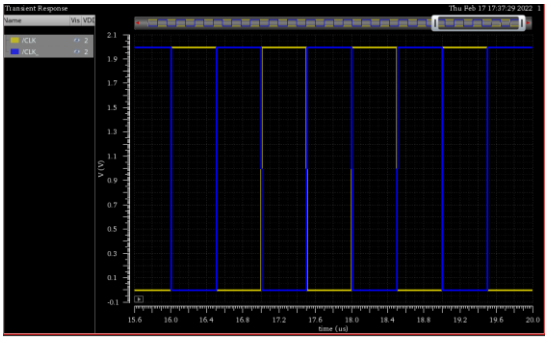
3-Comprator:



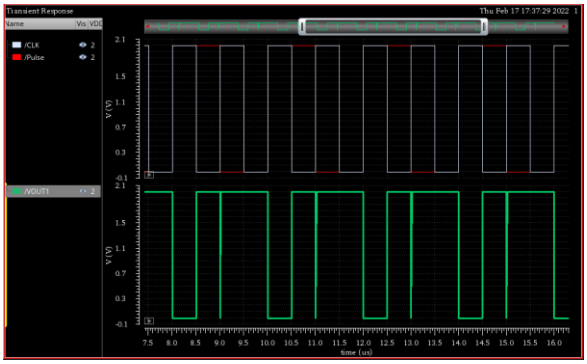
-We can see at clock edges when VINP > VINN, VOP > VON.

4-

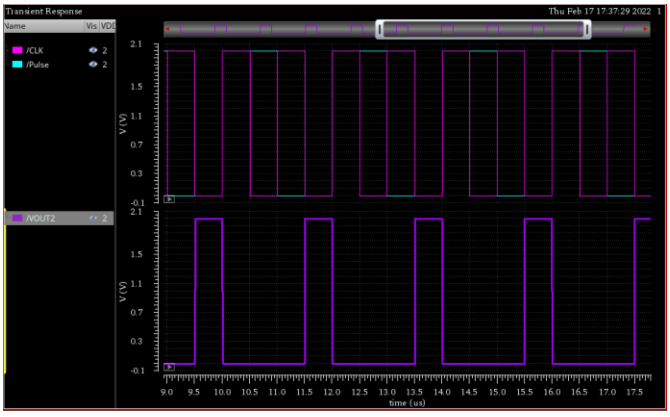
Inverter



NAND



NOR

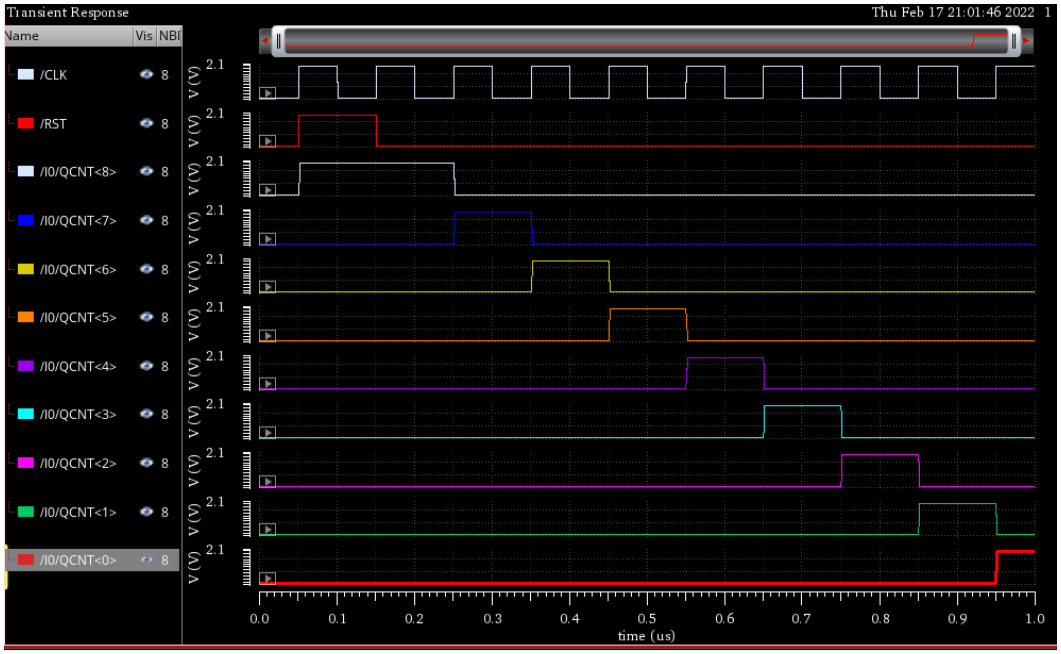


PART 2: SAR Logic

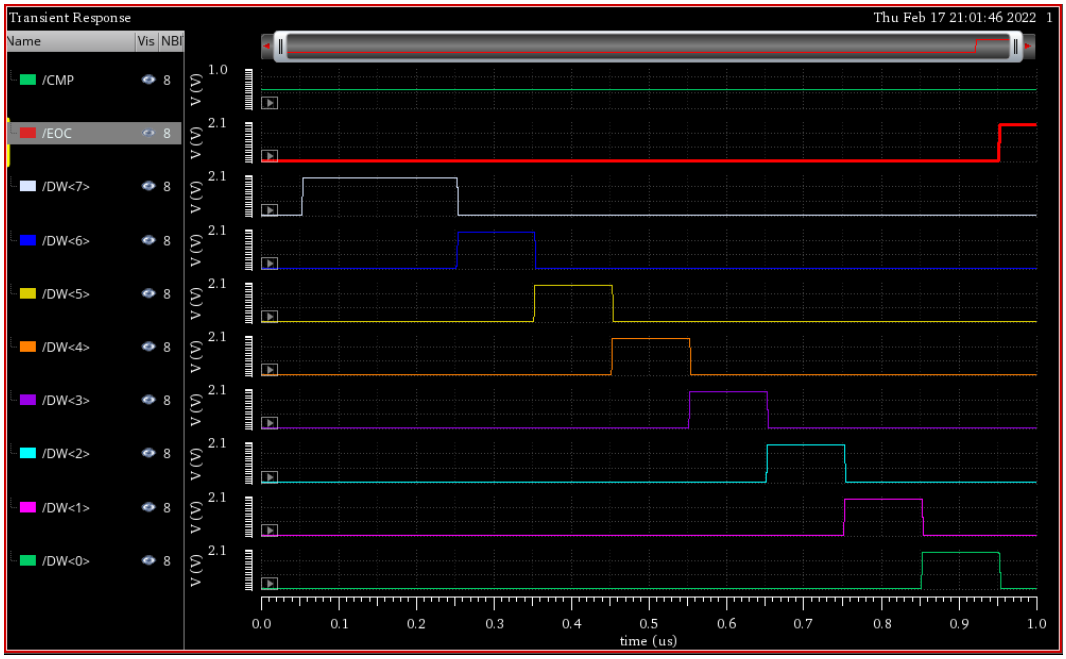
1-Transiet Simulations:

1-When CMP is all zero:

The ring counter output

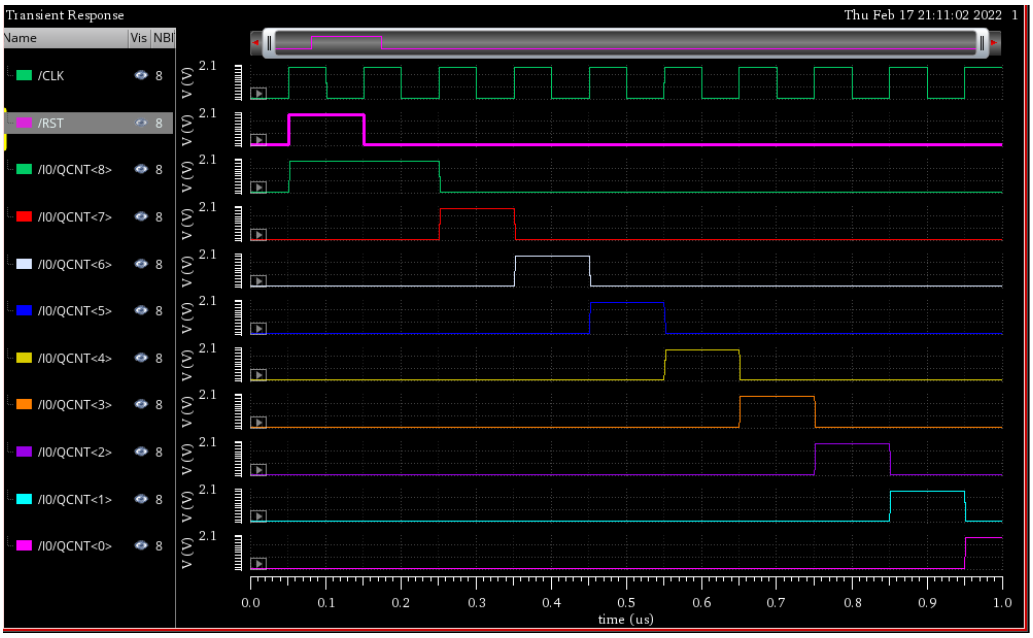


The Code register output and EOC

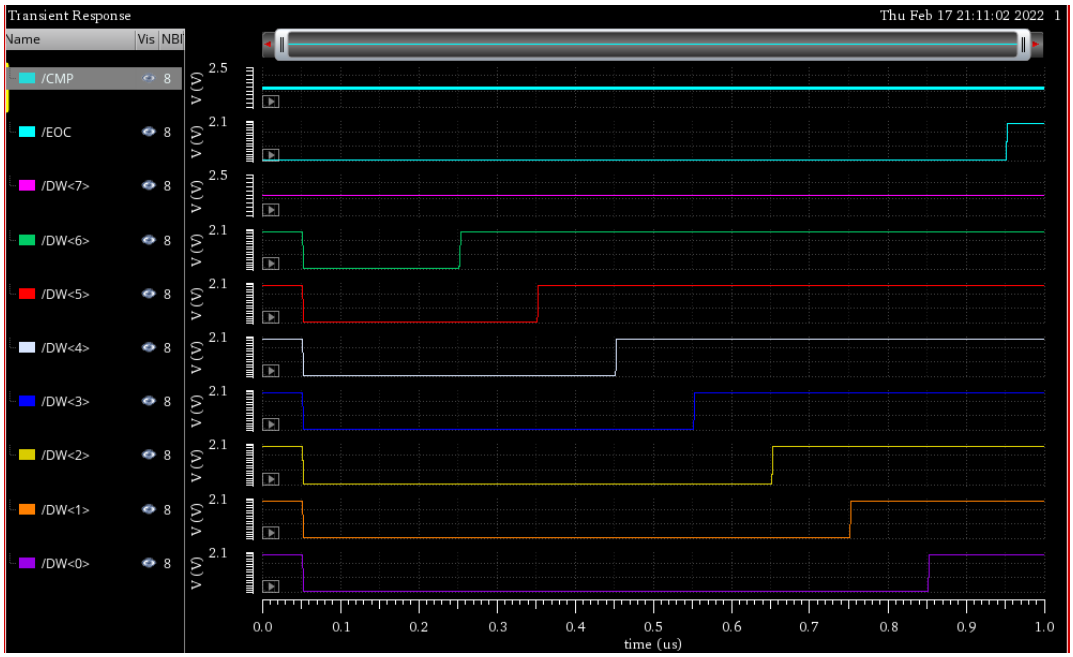


2-When CMP is all ones:

The ring counter output

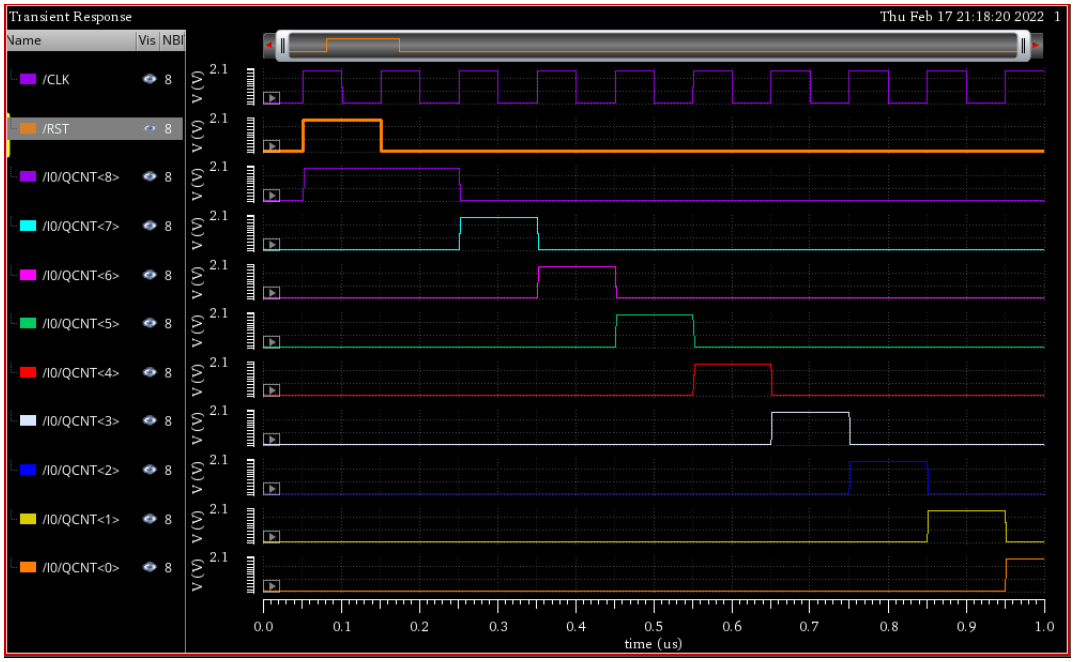


The Code register output and EOC

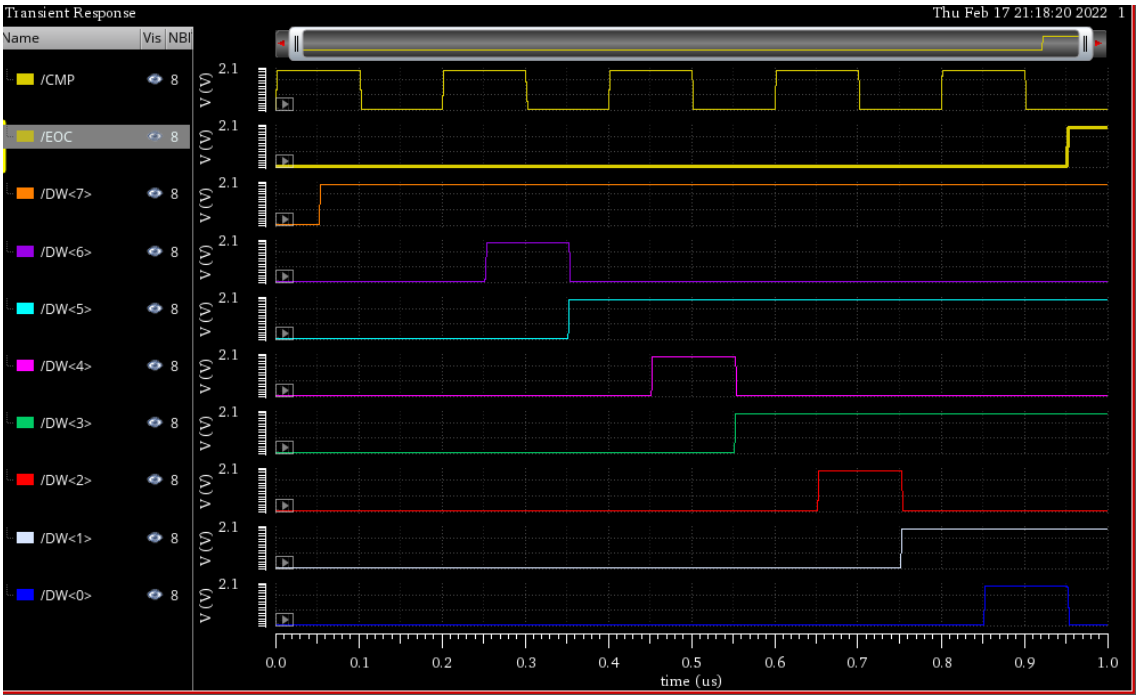


3- CMP is alternating ones and zeros

The ring counter output



The Code register output and EOC



CLock	DW<7>	DW<6>	DW<5>	DW<4>	DW<3>	DW<2>	DW<1>	DW<0>	CMP
1(reset)	1	0	0	0	0	0	0	0	
2	B7	1	0	0	0	0	0	0	B7
3	B7	B6	1	0	0	0	0	0	B6
4	B7	B6	B5	1	0	0	0	0	B5
5	B7	B6	B5	B4	1	0	0	0	B4
6	B7	B6	B5	B4	B3	1	0	0	B3
7	B7	B6	B5	B4	B3	B2	1	0	B2
8	B7	B6	B5	B4	B3	B2	B1	1	B1
9	B7	B6	B5	B4	B3	B2	B1	B0	B0
10	B7	B6	B5	B4	B3	B2	B1	B0	

Brief Explain the logic:

-We have the ring counter or we can say the shift register that shifts the reset pulse to all the flipflops, the outputs of the flipflops of the shift register are connected to the Set Pin of the flipflops of the code register in order to initially activate the binary output bits

-The reset pulse activates the first flipflop of the shift register (Qcnt8) that initially activate the MSB of the code register, the binary output of a flipflop is used as a clock for the previous flipflop in order to evaluate and load the output of the comparator.

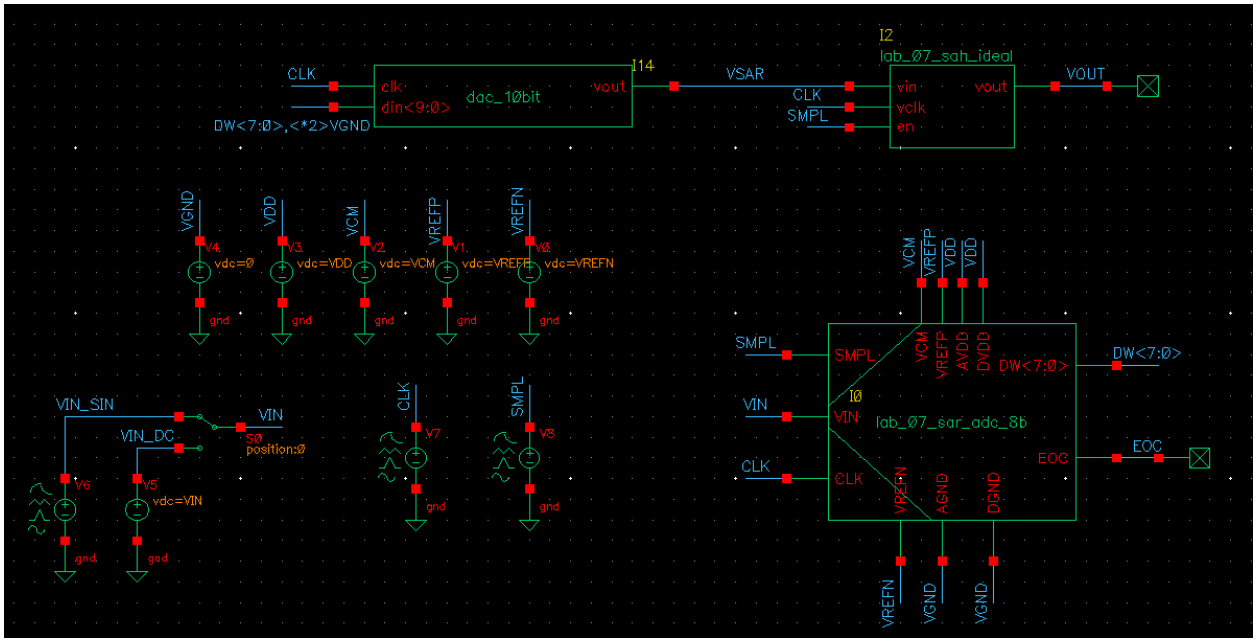
-For ex, when DW<6> is activated by (Qcnt7) , that causes DW<7> to load the comparator output.

-And so on, reaching the LSB, that initially activated and wait to evaluate by the end of conversion (EOC) pulse that comes from the last flipflop in the shift register (Qcnt0) that indicates the EOC.

-Now we have the loaded output binary bits, we apply a reset signal again to repeat evaluation.

PART 3: SAR ADC Testbench

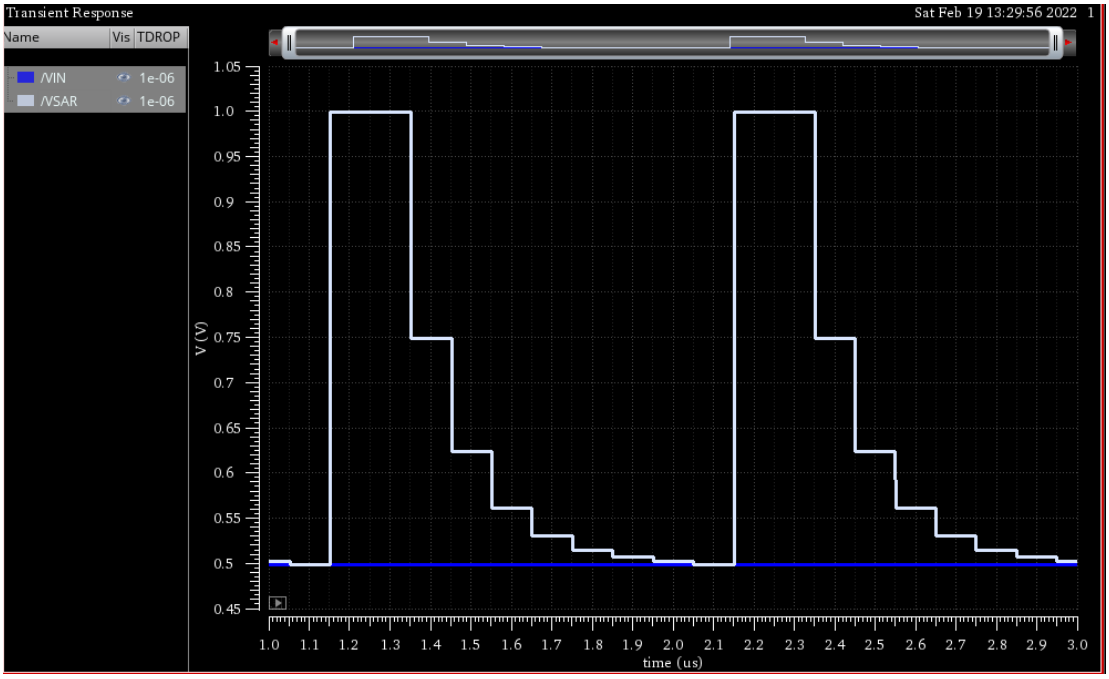
Only creating the schematics included in PDF.



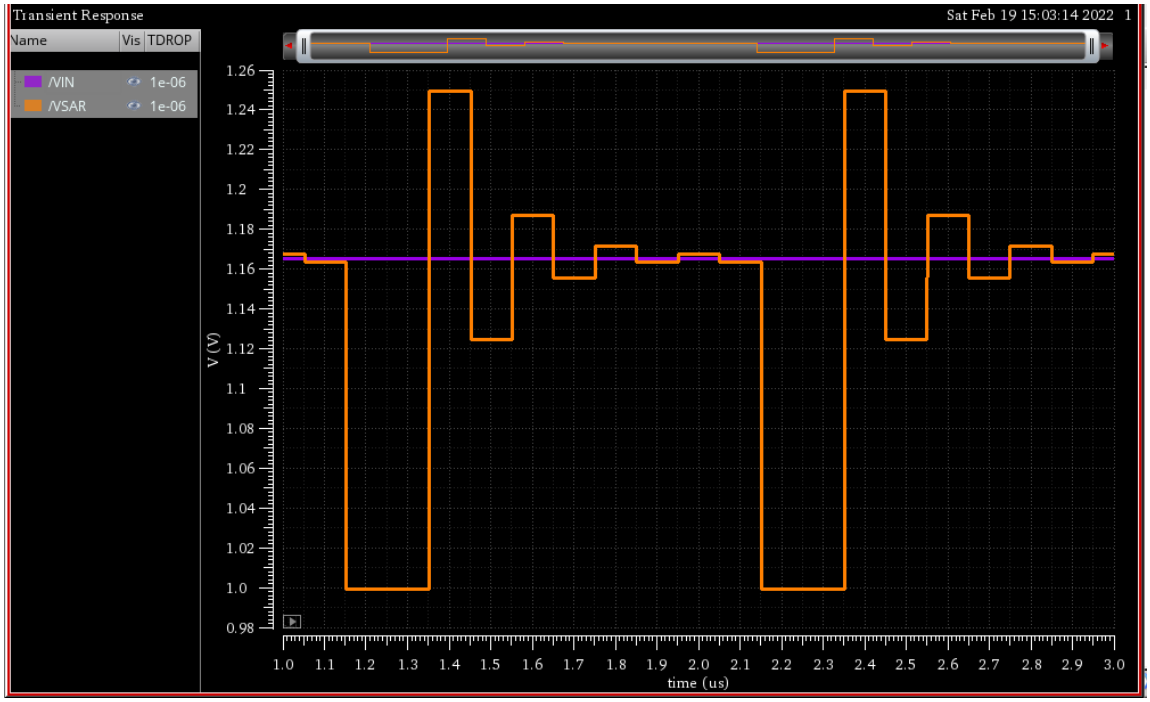
-skipping the actual comparator circuit

PART 4: DC Functional Test:

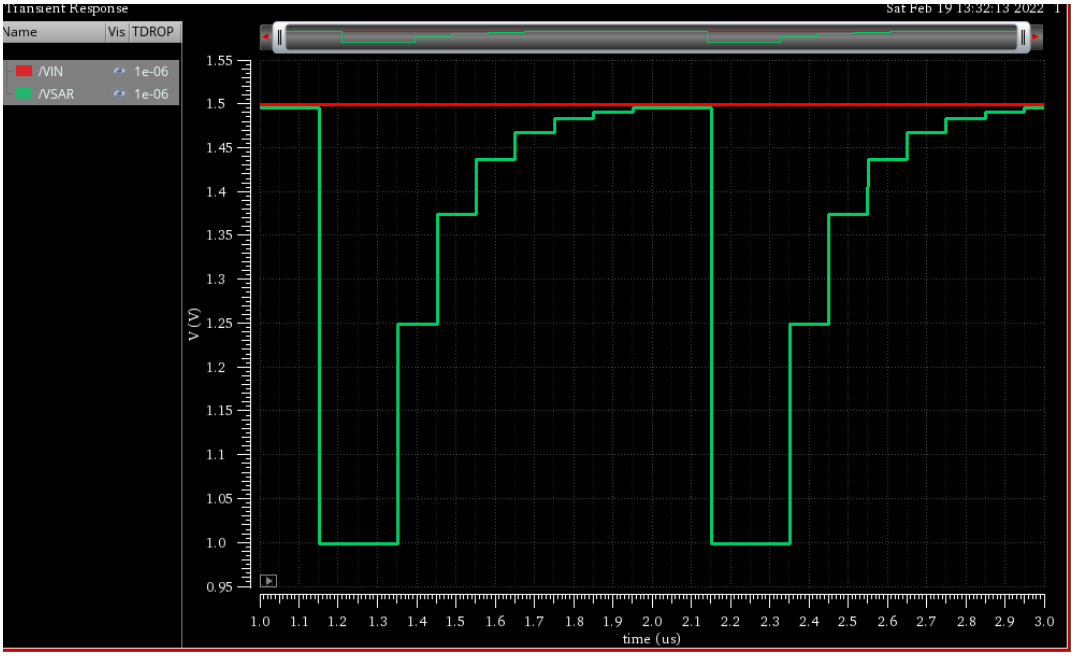
1-VIN = VREFN



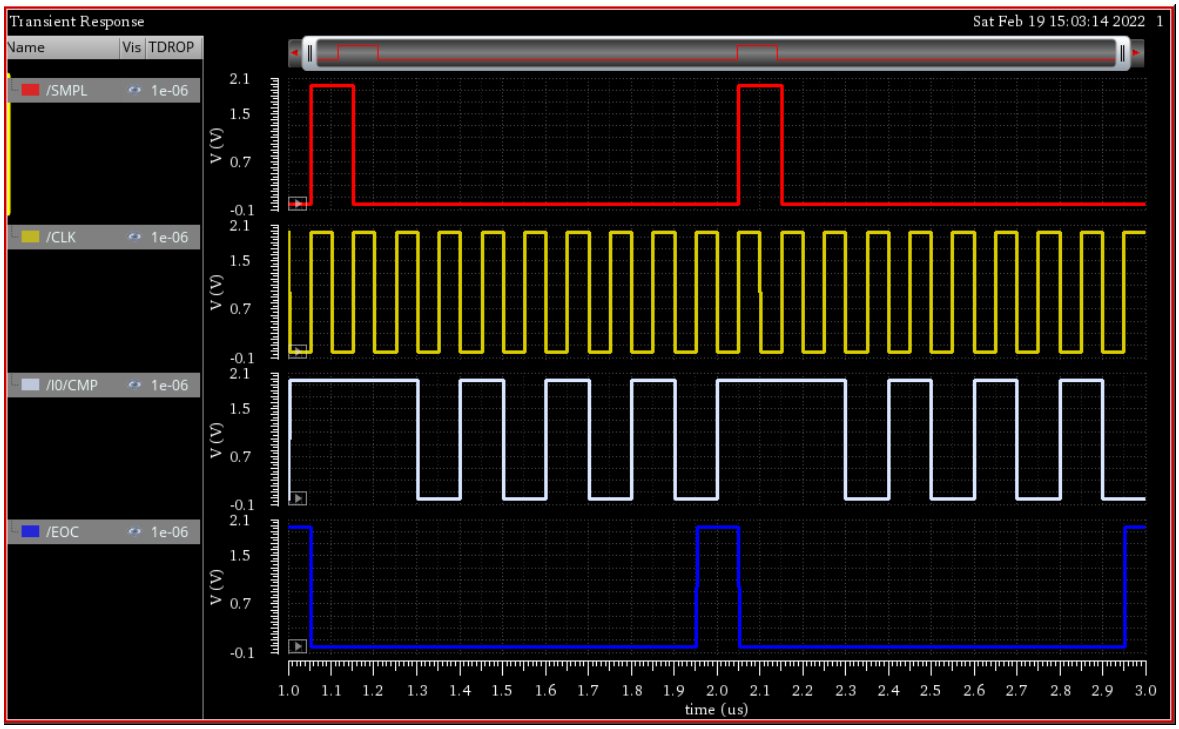
2- VIN = VREFN + (128+32+8+2+0.5)*VLSB



3-VIN = VREFP

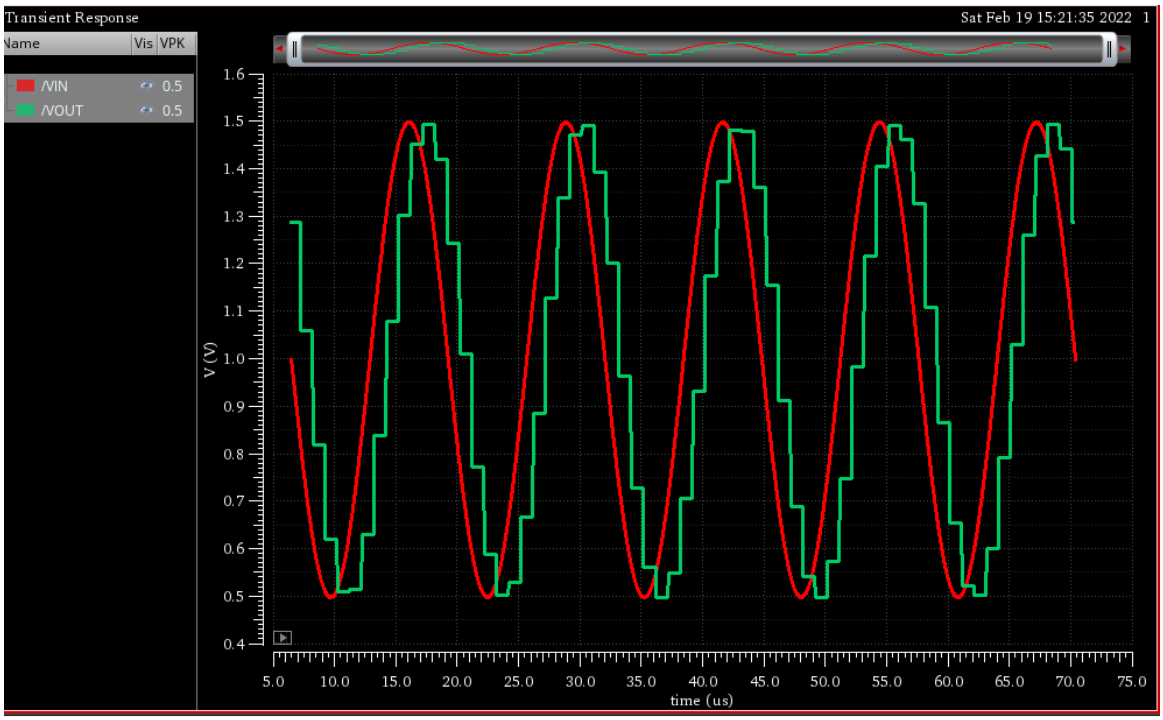


4- SMPL, CLK, CMP, and EOC for the second case:



PART 5: Sine Wave Test

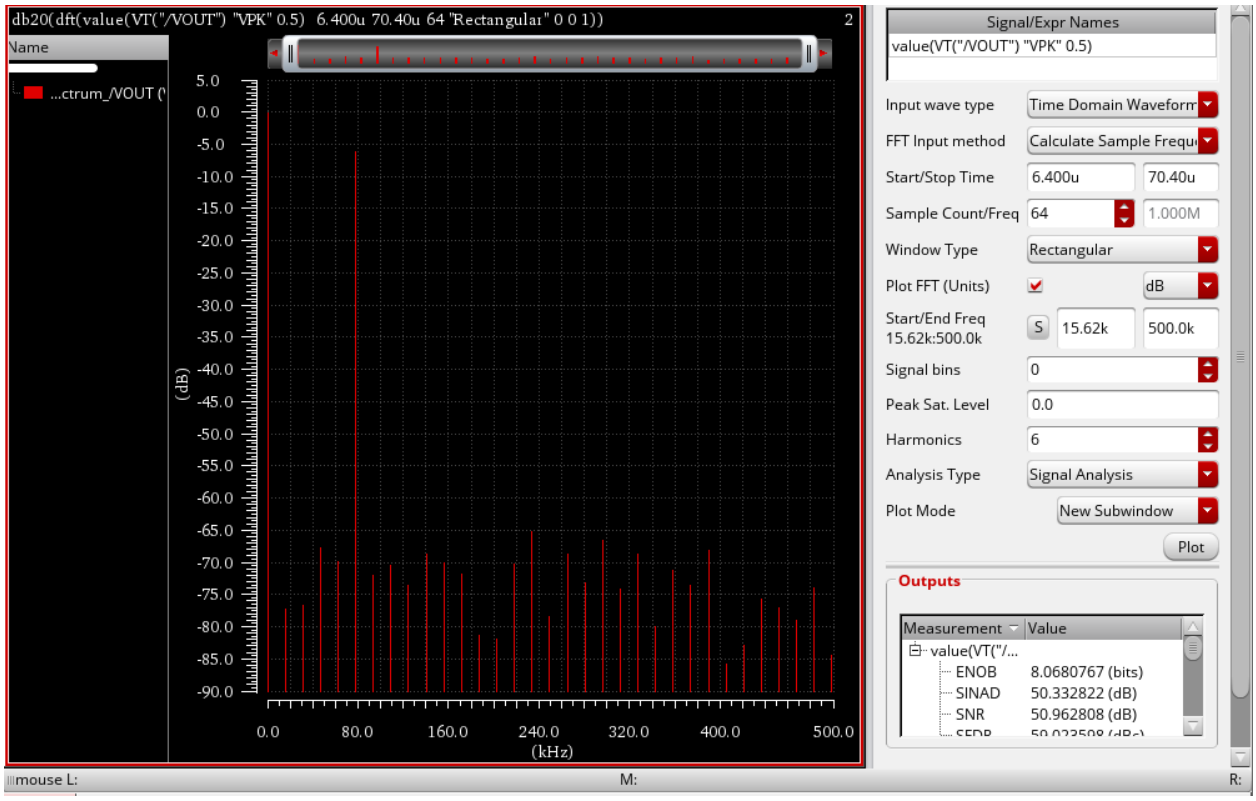
1-VIN and VOUT vs time:



-We can see that VOUT try to reach VIN with some delay.

Note: sine wave with VPK = 1V and no dc level can’t be input here because this is out of range so the circuit doesn’t work so we need to add a dc offset = 1V, for sine being in range.

2-FFT of VOUT:



Comments:

-We can see dc power = 1V = 0dB, Signal power = 20log(0.5) = -6dB

-NCYC = 5, We satisfy coherent condition so no harmonic components or spectral leakage.

-ENOB = 8.06, yes, we do most of things ideal but I think it can’t be higher than 8!

-SNR = 50dB as expected.

-Highest spurious tone at -65dB so SFDR = 59dBc

-Noise Floor at -72dB as we didn’t take higher FFT points.

-SNR is close to SNDR as we have here only the quantization noise.

Measurement	Value
SNR	50.962808 (dB)
SFDR	59.023598 (dBc)
THD	0.15819268 (%)
THD	-56.016272 (dB)
Signal P...	-6.0230266 (dB)
DC Pow...	-0.018574909 (dB)
Noise Fl...	-72.037335 (dB)
Noise Fl...	-113.83765 (dB)

-At the end, Thanks much for everything.