Analog IC Design – Cadence Tools
Lab 09 (Mini Project 01)
Two-Stage Miller OTA

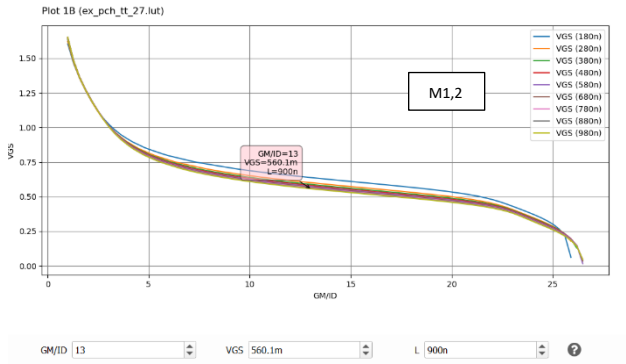
-Two-stage Miller-compensated OTA Design:

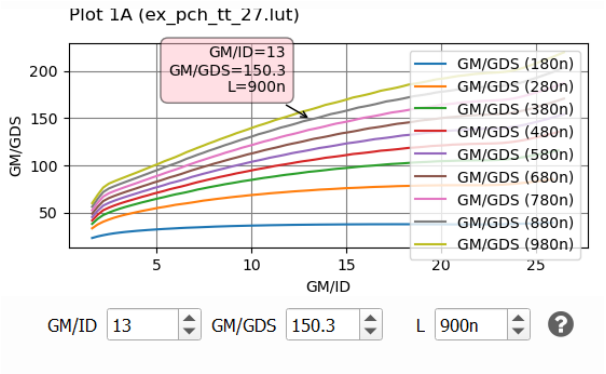
Required specs:

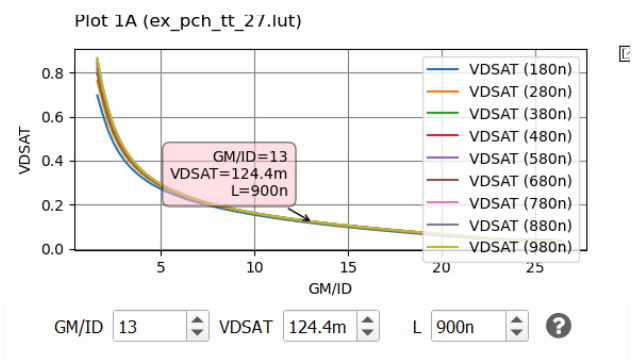
Technology	0.13um	0.18um
Supply voltage	1.2V	1.8V
Static gain error	<= 0.05%	<= 0.05%
CMRR @ DC	>= 74dB	>= 74dB
Phase margin (avoid pole-zero doublets)	>= 70°	>= 70°
OTA current consumption	<= 60uA	<= 60uA
CMIR – high	>= 0.6V	>= 1V
CMIR – low	<= 0.2V	<= 0.2V
Output swing	0.2 – 1V	0.2 – 1.6V
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns	<= 70ns
Slew rate (SR)	$5V/\mu s$	$5V/\mu s$

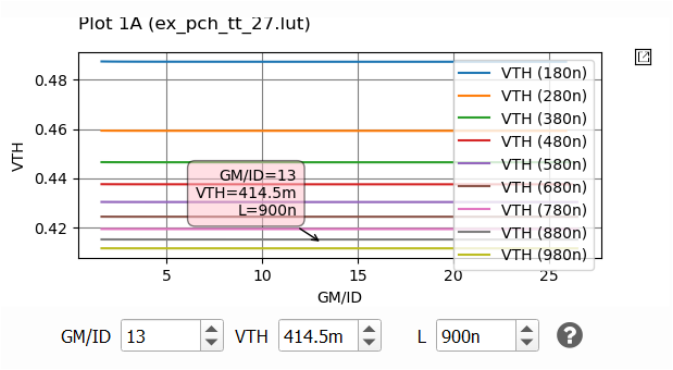
1-Design Charts:

1-Input Pair M1,2:

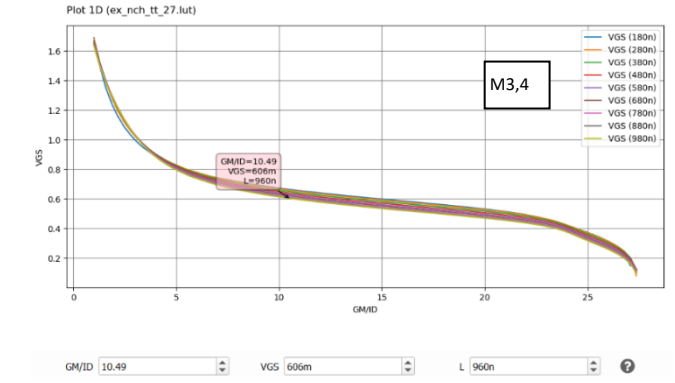


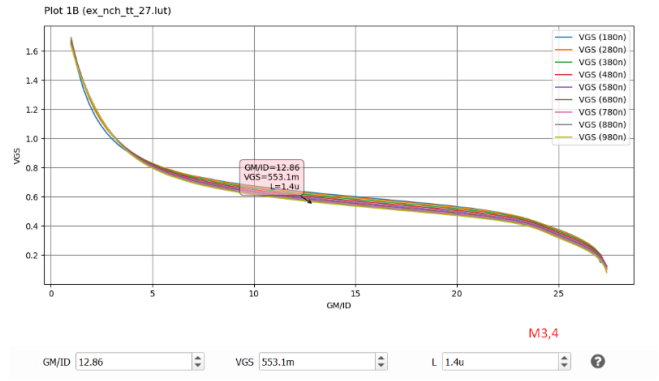


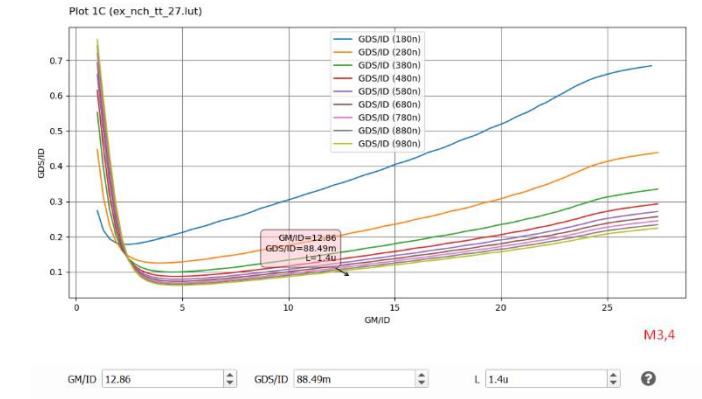


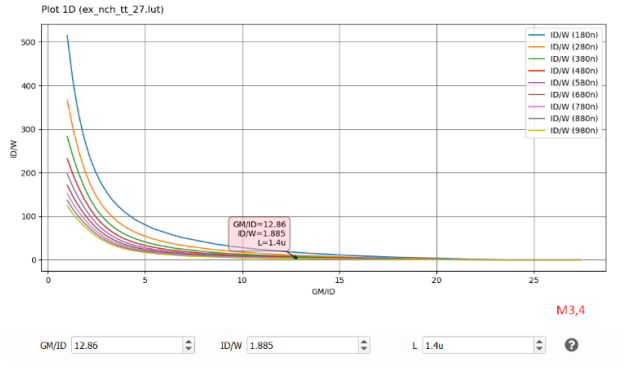


2-Current mirror load M3,4:

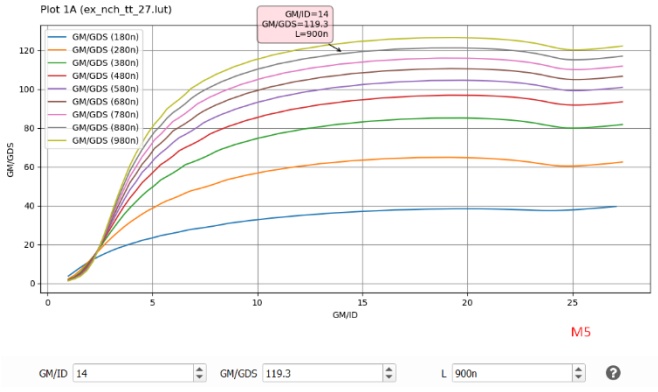


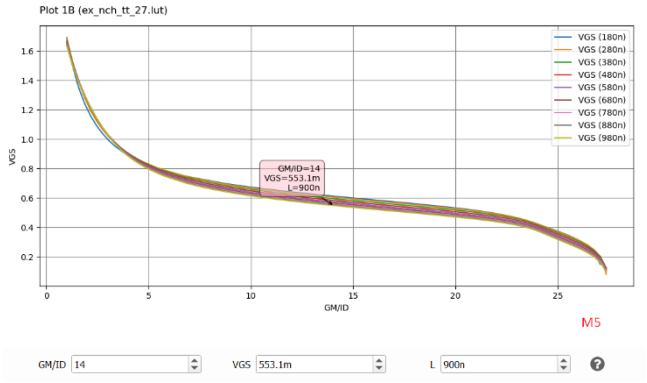


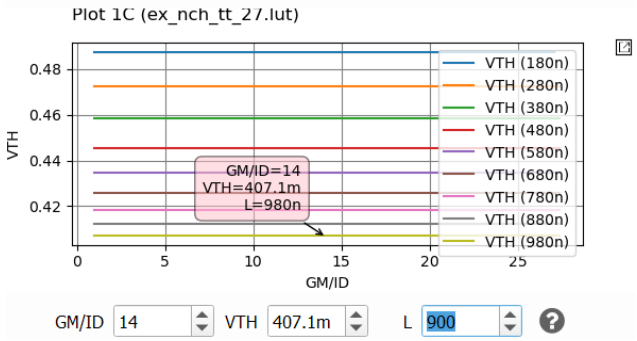


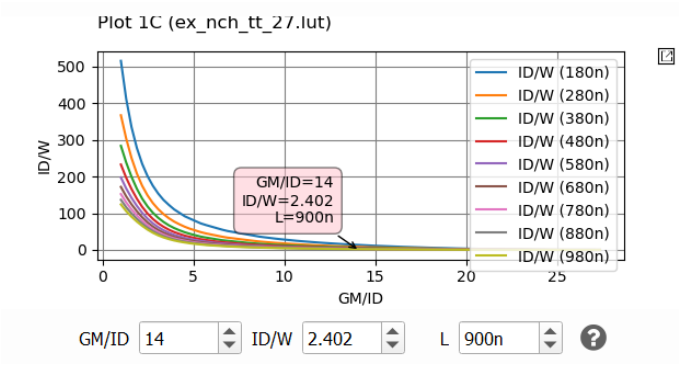


3-Input transistor of second stage M5:

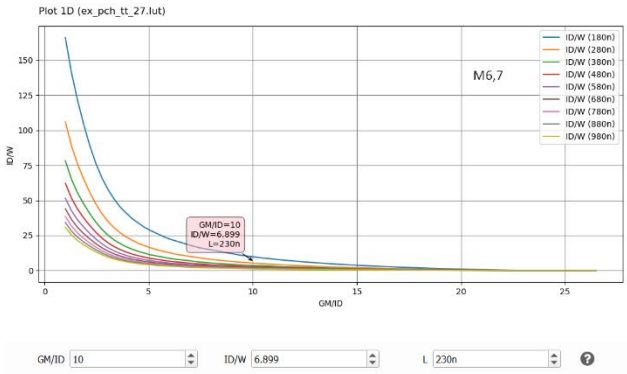


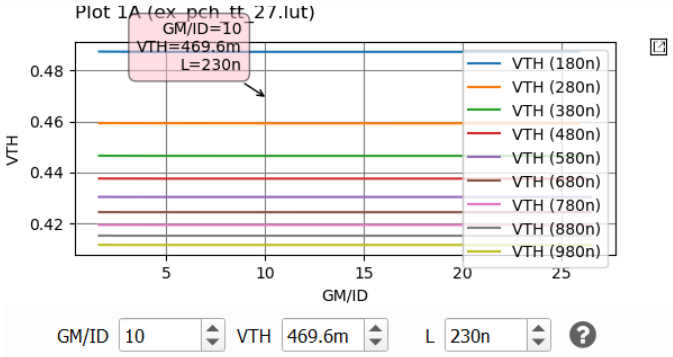


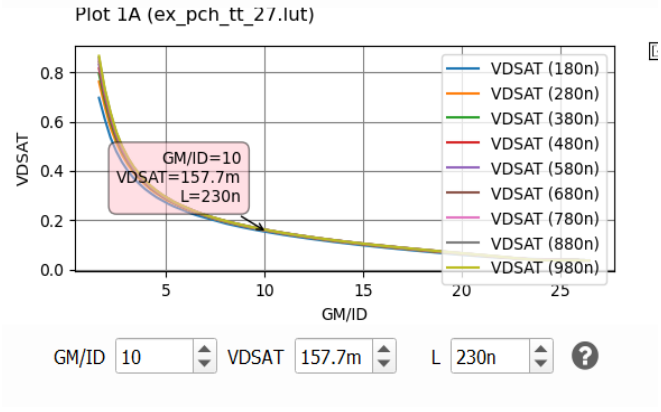


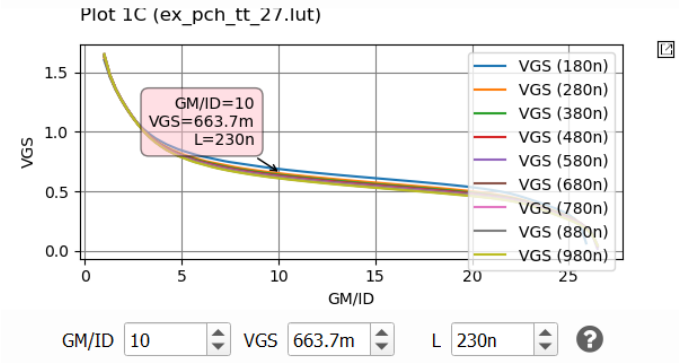


4-Tail current source M6,7:









Reporting the following:

1-Detailed design procedure and hand analysis:

-We use PMOS input pair as the CMIR is close to VDD and that reachable by PMOS

Design procedure:

1- $$trise = 2.2 * taw <= 70ns$$

$$Taw <= 3.18 * 10(-8) = 1/wu$$

$$Wu = \frac{gm1}{Cc} \geq 31.42Mrad$$

$$gm1{,}2 \geq 78.57$$

2- $$slewrate = \frac{IB1}{Cc} = 5\frac{v}{us}, \quad Cc = 2.5pf, \quad IB1 \leq 12.5uA, \quad IB2 \leq 47.5uA$$

3- $$\left(\frac{gm}{ID}\right)1{,}2 \geq 12.57$$

4- $$Acl = \frac{Aol}{1+BAol} = \frac{Aol+1-1}{1+Aol} = 1 - \frac{1}{Aol}$$

$$SGE = \frac{1}{LG} = Aol, \quad Aol \geq 2000, \quad Aol \geq 66dB$$

5- Assume the first stage gain is twice that of the second stage:

$$Av1 \geq 36dB \geq 63.095, \quad Av2 \geq 30dB \geq 31.622$$

$$\left(\frac{gm}{gds}\right)1{,}2 \geq 126.19, \quad From\ Chart\ \left(\frac{gm}{ID}\right)1{,}2 = 13, \quad L1{,}2 = 900n$$

$$From\ Chart, \frac{ID}{w} = 733.6m, \quad ID1 = 6.25uA, \quad W1{,}2 = 8.5um$$

6- $$Assume\ \left(\frac{gm}{ID}\right)3{,}4 = 15, \quad gds1{,}2{,}3{,}4 = .628us, \quad \frac{gds}{ID} = 100m$$

$$From\ chart, \quad L3{,}4 = 1.4um$$

7- $$PM \geq 70, \quad assume\ wp2 = 4wu, \quad \frac{GM2}{Cl} = \frac{4GM1}{Cc},$$

$$gm5 = 650us, \quad (\frac{gm}{ID})5min = 13.68$$

8- $$CMIRHigh \geq 1v$$

$$1 \geq -|Vgs1| + Vdsat7 + VDD$$

$$1 \geq 1.8 - .56 - |Vdsat7|$$

$$Vdsat7max = 240mv = V *$$

$$From\ Chart, \quad \frac{gm}{ID}6{,}7min = 8.3, \quad \left(\frac{gm}{ID}\right)6{,}7 = 10$$

9- $$CMRR \geq 74dB = AvddB - AvCMdB, \quad AvCM \leq -38dB, \quad .0125 \geq \frac{gds6}{2*gm3{,}4}$$

$$gds6 \leq 2us, \quad \frac{gm}{gds}6{,}7 \geq 62.5, \quad From\ chart, \quad L6{,}7 = 280n$$

10- $$\left(\frac{gm}{gds}\right)7 = 31.64, \quad gm7 = 475us, \quad gds7 = 15us$$

11- $$Av2 = gm5(ro5||ro7) = gm5\left(\frac{1}{gds5+gds7}\right) \geq 31.62$$

$$gds5 \leq 5.55, \quad \left(\frac{gm}{gds}\right)5 \geq 117.11 \quad From\ Chart, \quad L5 = 900n$$

12- $$\left(\frac{gm}{ID}\right)5 = 14, \quad \left(\frac{gm}{gds}\right)5 = 119.3, \quad L5 = 900n \quad From\ Chart, \quad VGS5 = 553.1m$$

$$From\ chart, \quad \left(\frac{ID}{W}\right)5 = 2.4, \quad W5 = 19.79um$$

13- $$VGS3{,}4 = VGS5 = 553.1mv, \ L3{,}4 = 1.4um, \ From\ chart\ \left(\frac{gm}{ID}\right)3{,}4 = 12.86$$

$$From\ Chart, \left(\frac{ID}{w}\right)3{,}4 = 1.885, \quad W3{,}4 = 3.3um$$

14-CMIRLow verify:

$$.2 \geq -|VGS1| + V * 1 + VGS3$$

$$VGS3max = 606mv, \quad From\ chart, \quad \left(\frac{gm}{ID}\right)3{,}4min = 10.49$$

Verified, $\left(\frac{gm}{ID}\right)3{,}4 = 12.86$

15-Peak to Peak output swing verification:

$$Voutmin = 0.2, \qquad \left(\frac{gm}{ID}\right)5 = 14, \quad V * 5 = .142mv < Voutmin$$

$$Voutmax = 1.6v, \qquad \left(\frac{gm}{ID}\right)7 = 10, \quad V * 7 = 0.2 = Voutmax$$

16-$Wz = \frac{1}{Cc(\frac{1}{GM2-RZ})}, \quad to\ throw\ zero\ to\ infinity, \quad Rz = \frac{1}{GM2} = \frac{1}{gm5} = 1.538Kohm$

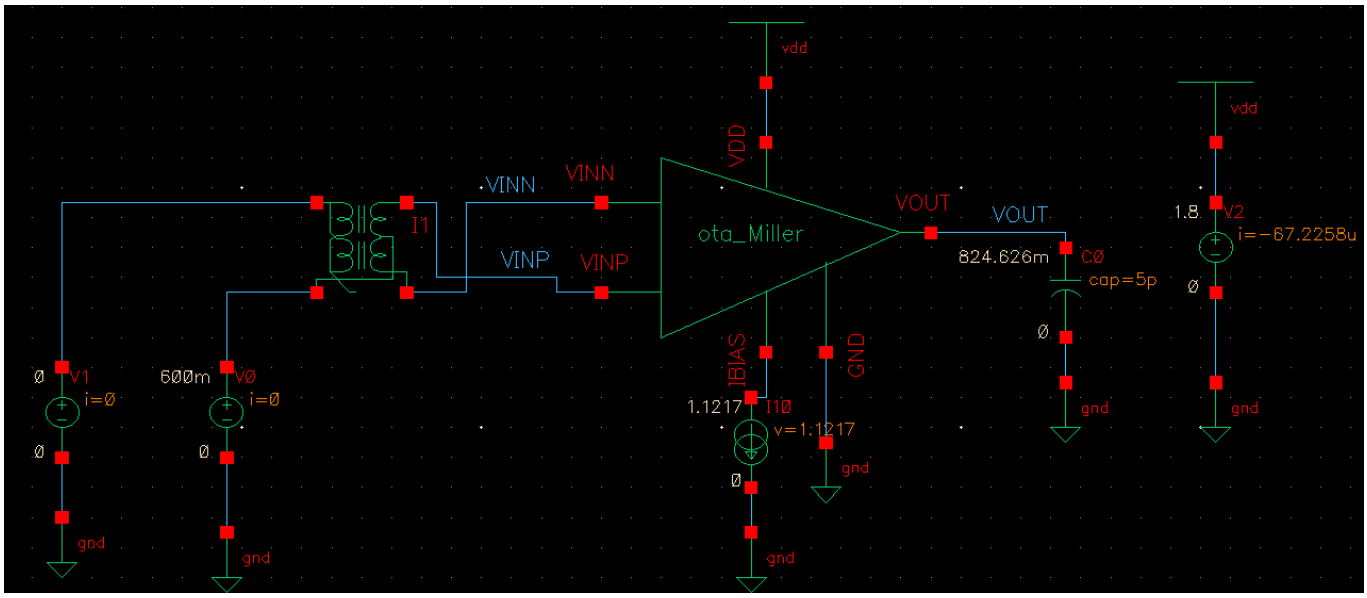
17-We tuned after simulation to $Cc = 2.3pF$ to get UGF spec

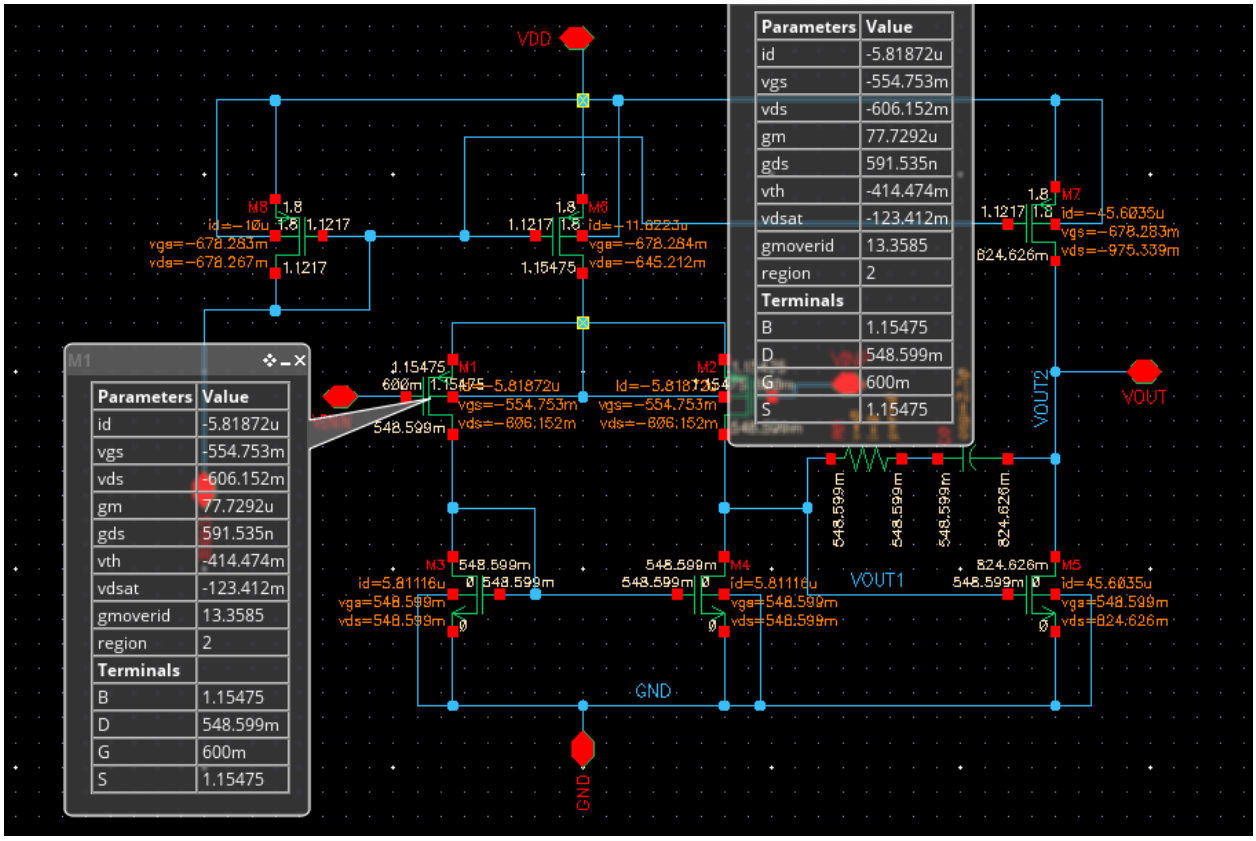
And $W3{,}4 = 3.1um, \quad W6 = 1.7um, \quad , W7 = 6.4um, \ W8 = 1.44um$ to tune the tail current.

	W	L	gm	ID	gm/ID	Vdsat	Vov	V*
M0,M1 Input pair	5.519um	900nm	81.25us	6.25uA	13	124.4mv	146mv	153mv
M3,M4 Current mirror	3.1um	1.4um	80.37us	6.25uA	12.86	125mv	407mv	155mv
M6,7 Tail current	W6=6.52um W7=6.4um	280nm	gm6=122us gm7=472us	ID6=12.2uA ID7=47.2uA	10	188mv	146mv	200mv
2nd stage input M5	19.79um	900n	660.8	47.2uA	14	115.1mv	194.1mv	142mv

PART 3: Open-Loop OTA Simulation:

1-Schematic of the OTA and bias circuit with DC node voltages clearly annotated:





-Yes, The current (and gm) in the input pair exactly equal.

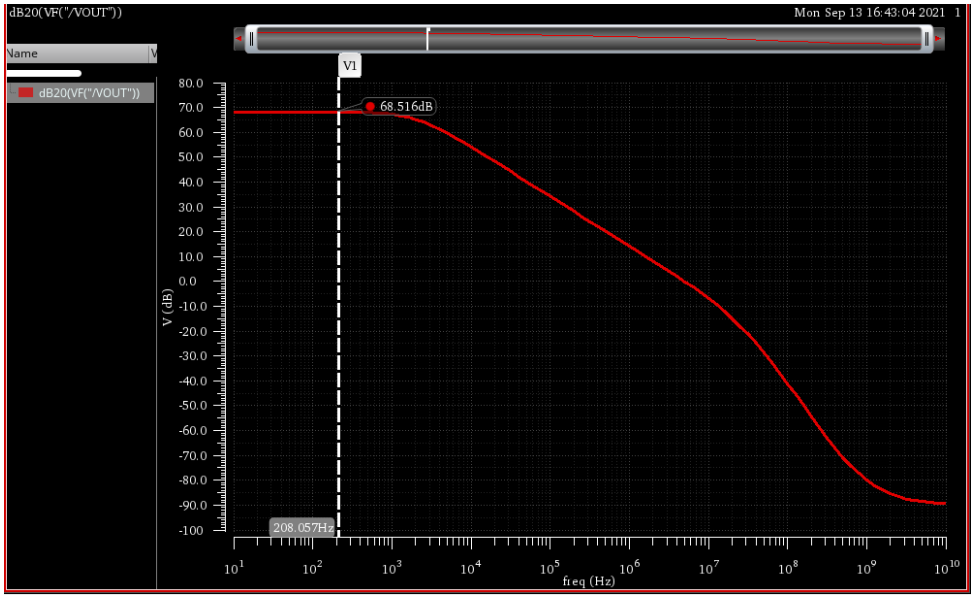
-VOUT1 = 548.59mv, because at CMInput Vout follows the mirror node Vf that equal to

$$VOUT1 = Vf = VDD - VDS6 - VDS1 = 1.8 - .645 - .606 \approx 549mv$$

-VOUT2=691.64mv, because at CMInput:

$$VOUT2 = VDD - VDS7 = 1.8 - .975 = 825mv$$

1) Diff small signal ccs:



Output	Nominal	Spe
/VOUT		
dB20(VF("/VOUT"))		
bandwidth(VF("/VOUT") 3 "lo...	1.973k	
unityGainFreq(VF("/VOUT"))	5.161M	
gainBwProd(VF("/VOUT"))	5.302M	

Hand analysis:

$$Avd = Av1 * Av2 = (gm1(ro2||ro4)) * (gm5(ro5||ro7) = 68.8 * 50.7$$

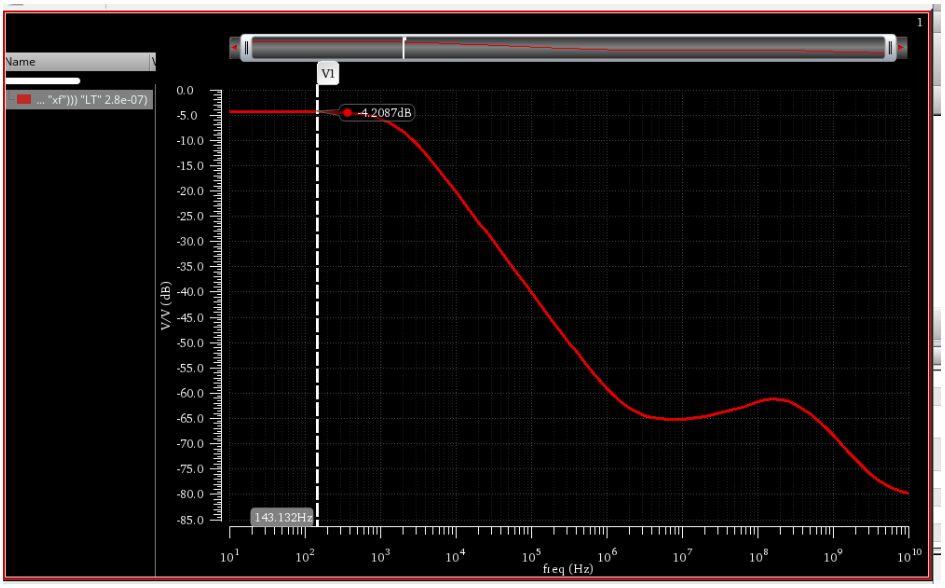
$$Avd = 3488.16 = 70.1dB$$

$$BW = \frac{1}{Rout1 gm5 Rout2 Cc} = 1.8K$$

$$GBW = UGF = Avd * BW = 5.5M$$

	simulation	analysis
Avd	68.5dB	70.1dB
BW	1.9K	1.8K
Wu	5.161M	5.5M
GBW	5.3M	5.5M

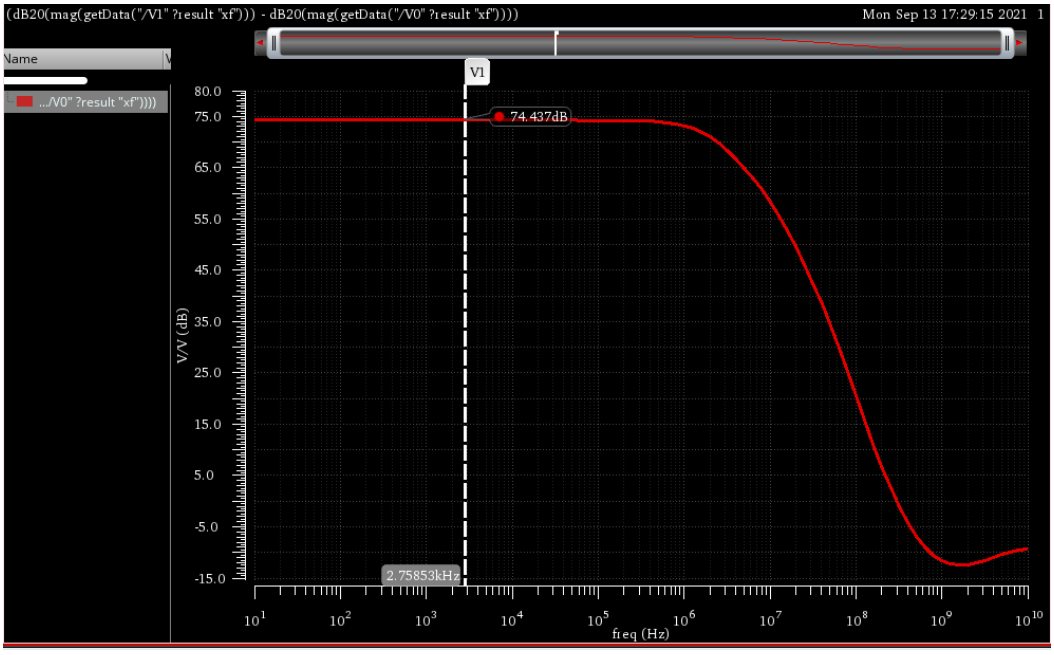
2) CM small signal ccs:



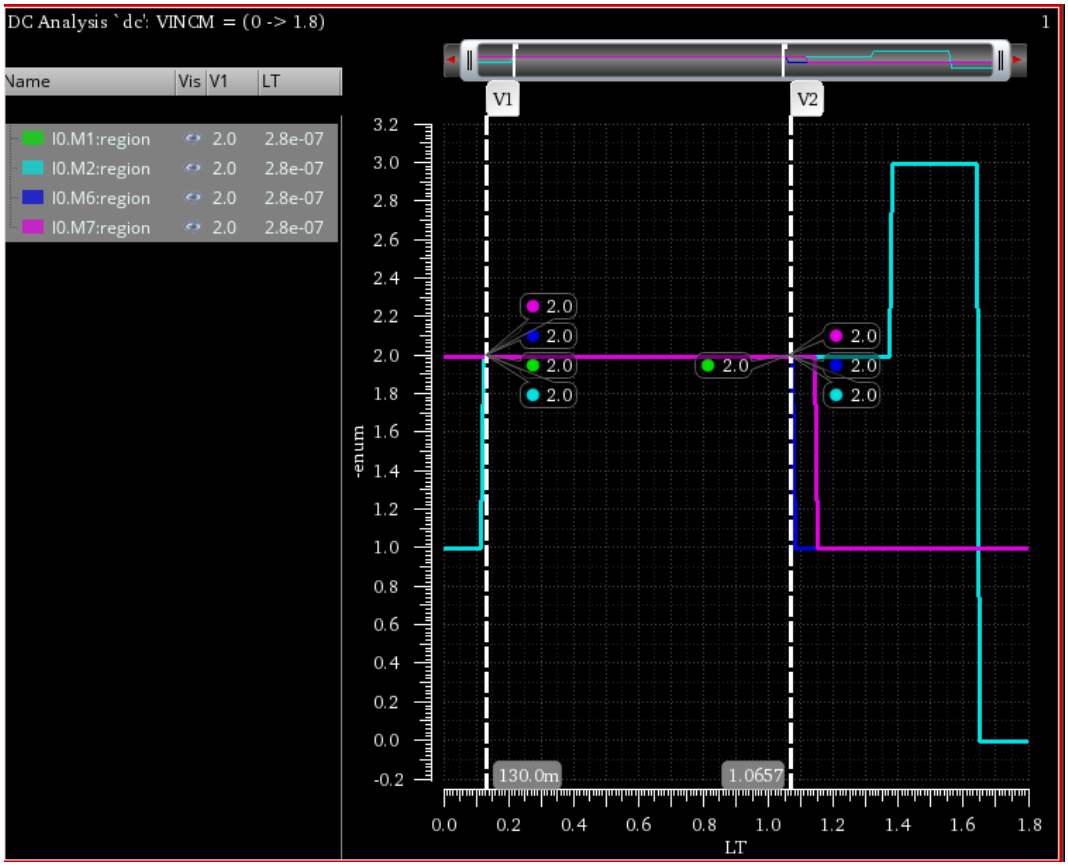
$$AvCM = -\frac{1}{2gm3 * ro6} * Av2 = -1.5 = -3.8B$$

	Simulation	Analysis
AvCM	-4.2dB	-3.8dB

3) (Optional) CMRR:



4) CM large signal ccs (region vs VICM):



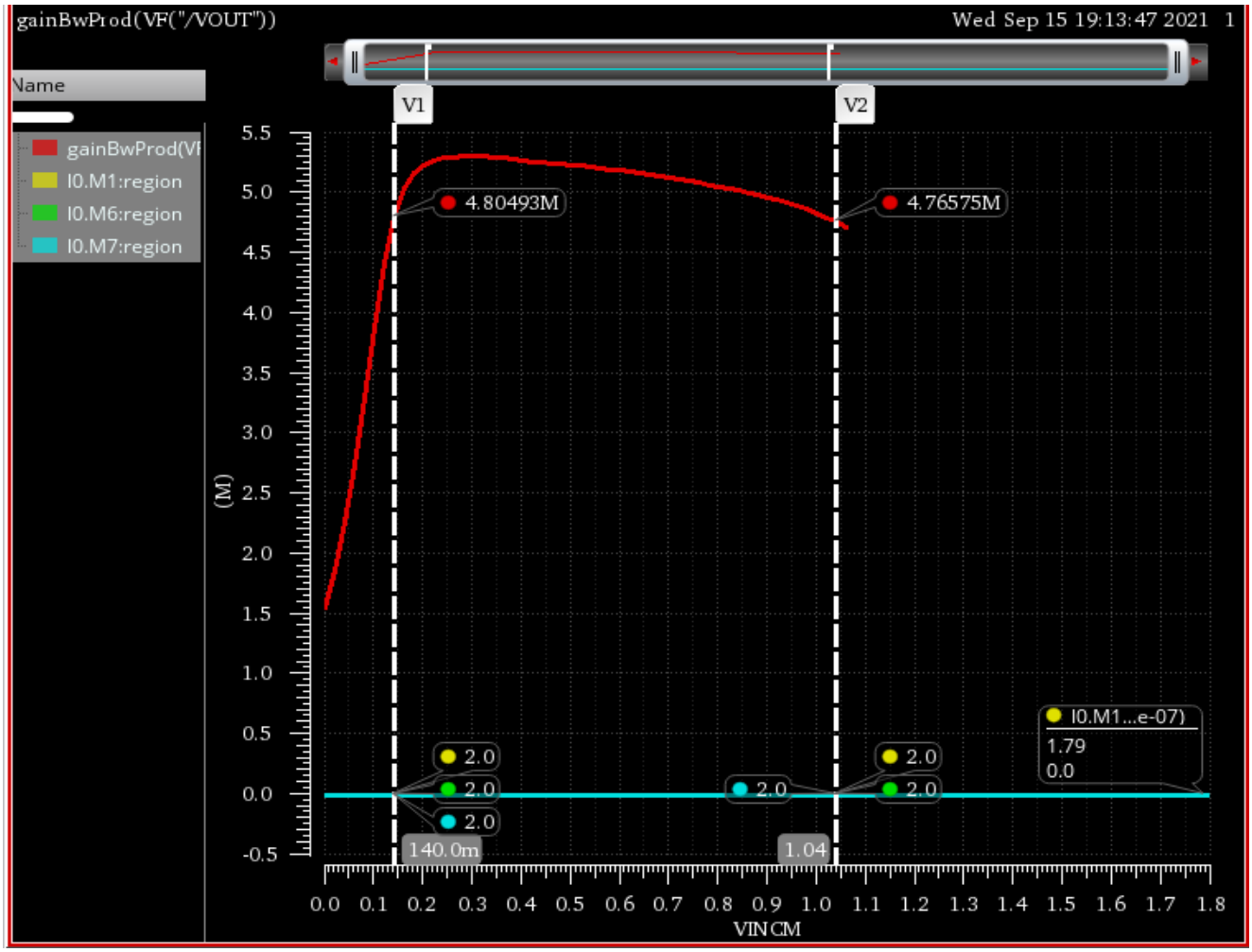
$$CMIR = 0.13 : 1.06$$

$$VINCMlow = -|VGS1| + |V * 1| + VGS3 = 0.153$$

$$VINCMHigh = -|VGS1| - |Vdsat7| + VDD = 1.068$$

	Simulation	Calculation
VINCMmin	0.13v	0.153v
VINCMmax	1.06v	1.068v

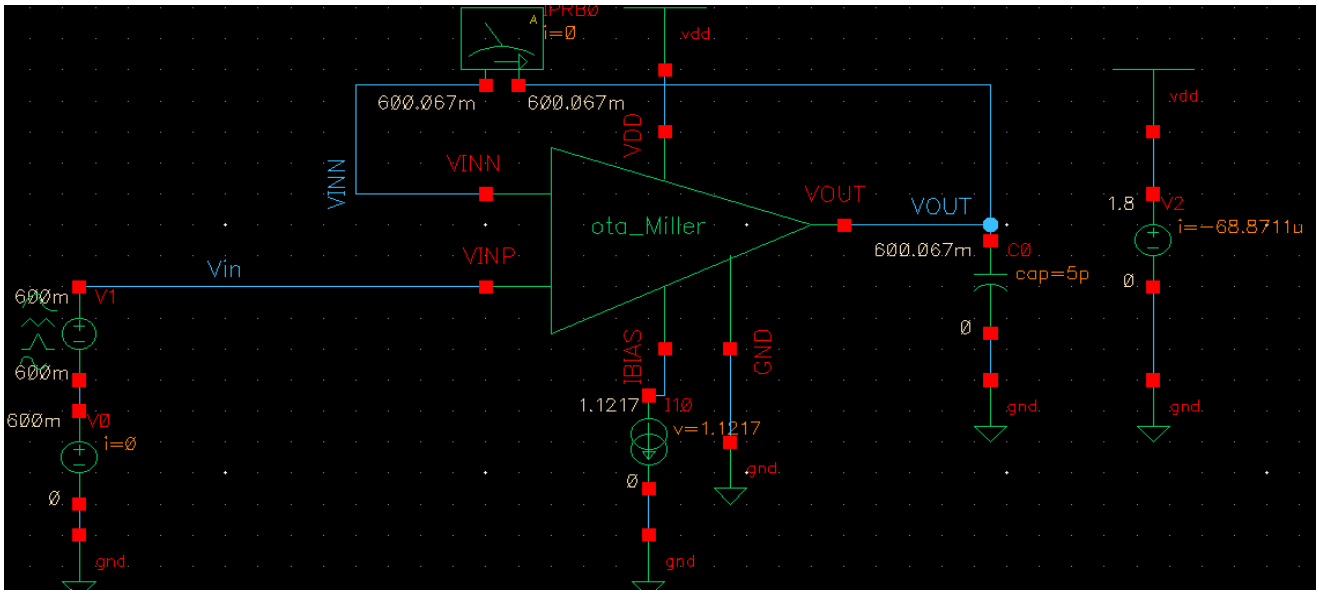
5) (Optional) CM large signal ccs (GBW vs VICM):

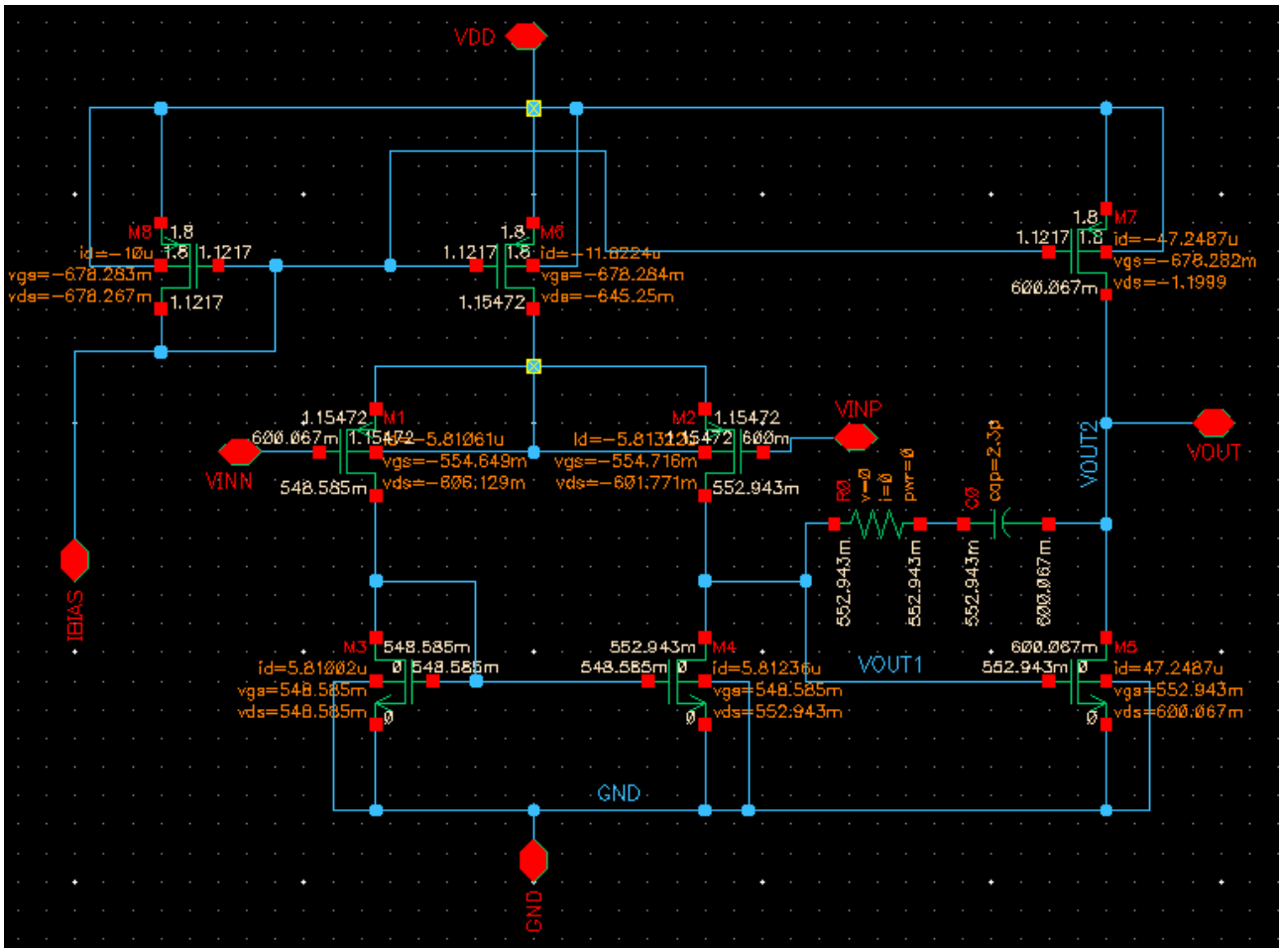


$$CMIR = 0.14 : 1.04$$

PART 4: Closed-Loop OTA Simulation

1) Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration



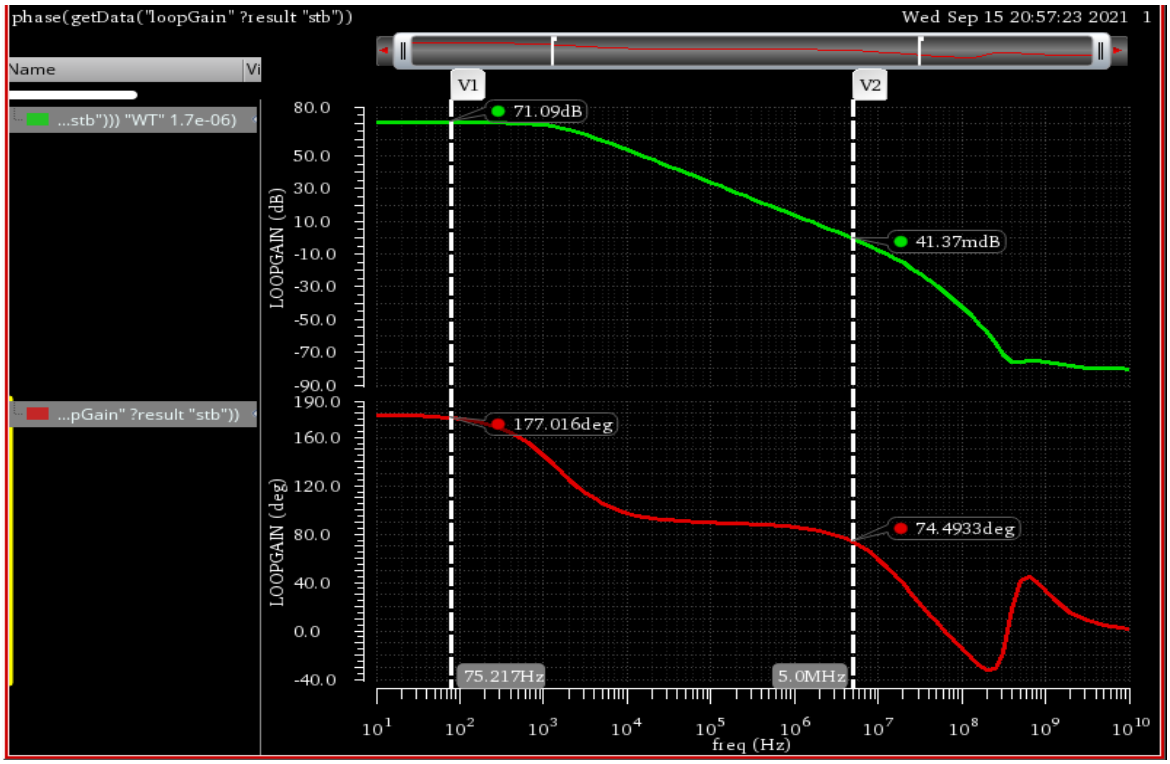


-DC Voltages at the input terminals of the op amp aren't exactly equal because in closed-loop, the output will follow the input. The output voltage deviates from its CM level (the voltage at the mirror node for the 5T OTA Miller) in order to match the input voltage. Since the gain is finite, that will cause Verr between terminals of the op amp that causes the small deviation

-Vout1(open loop) =548.59mv, Vout1(closed loop) =552.94mv, they aren't exactly equal due to the feedback connection with a finite gain that causes Vout2 to deviate from its CM level to match the input terminal of the op amp, that also causes some deviation in Vout1 from its CM level.

- The current (and gm) in the input pair aren't exactly equal because in closed-loop OTA, the output will follow the input. The output voltage deviates from its CM level in order to match the input voltage. Since the gain is finite, that will cause a small imbalance in the circuit that act as a mismatch.

2) Loop gain:



Output	Nominal	Spec
/VOUT		
dB20(mag(getData("loopGai...		
getData("/phaseMargin" ?res...	74.11	
ymax(mag(getData("loopGai...	3.278k	
unityGainFreq(mag(getData(...	5.133M	
gainBwProd(mag(getData("l...	5.285M	

Comparing DC gain and GBW with those obtained from open-loop simulation:

	Open-Loop	Loop gain
DC gain	68dB	71dB
Wu	5.161M	5.133M
GBW	5.3M	5.28M

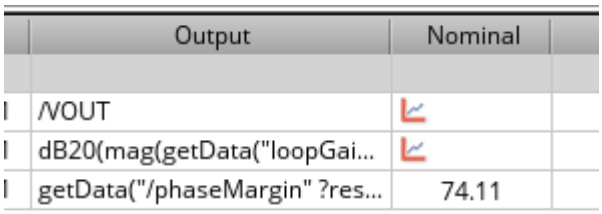
Comment:
-We can notice that feedback with unity gain correction (*B*=1) gives a loop gain equal to the open loop gain and doesn't affect GBW.

-Report PM. Compare with hand calculations. Comment:

$$Wu = \frac{gm1}{Cc} = 33.79MHz$$

$$Wp2 = \frac{gm5}{Cl} = 129.48$$

$$PM = 90 - \tan^{-1}\frac{Wu}{Wp2} = 75.7$$



	Output	Nominal
	/VOUT	
	dB20(mag(getData("loopGai...	
	getData("/phaseMargin" ?res...	74.11

Comment:
-We assumed that Wp2=4Wu and that gives PM=76 but we use Cc=2.3pf that reduce Wu
-Results are almost equal.

Hand analysis:

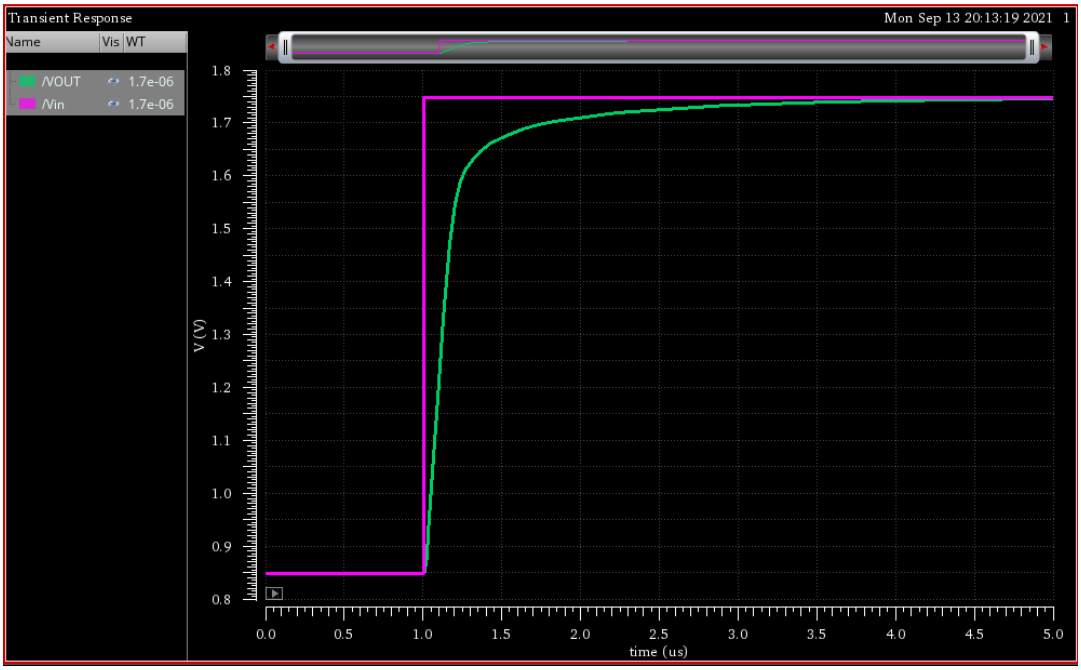
$$LG = BAol = Aol = 68.5dB$$

$$GBW = UGF = LG * BW = LG * Wpout = 5.5M$$

	Simulation	analysis
DC gain	71dB	68.5dB
Wu	5.133M	5.5M
GBW	5.28M	5.5M

3) Slew rate:

Report Vin and Vout overlaid



/VOUT	
/Vin	
slewRate(VT("/VOUT") 0.25 ni...	4.666M

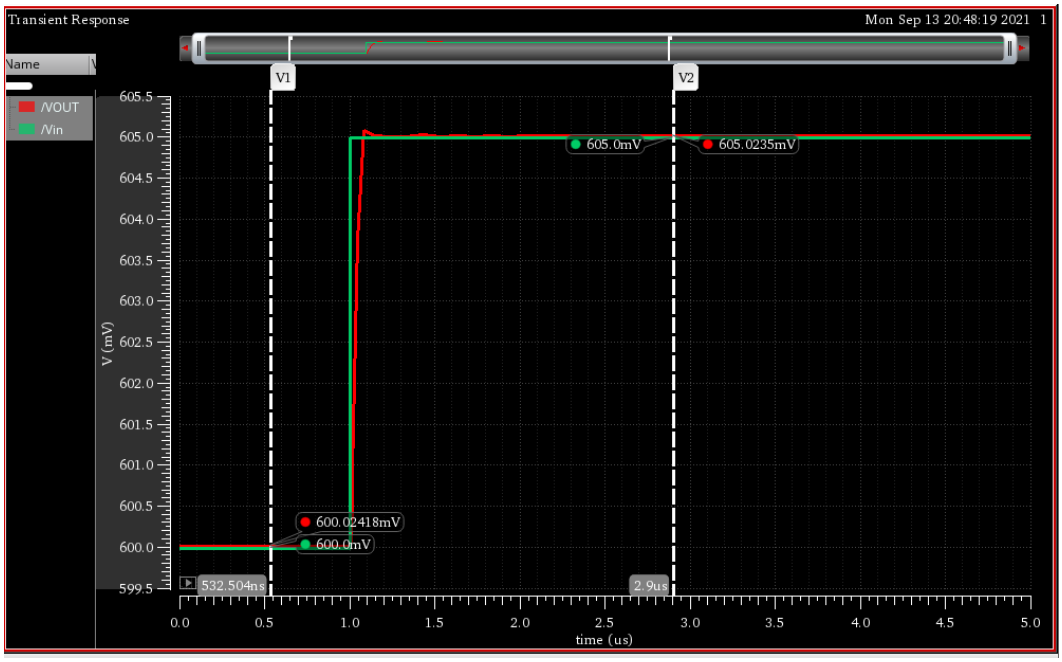
$$Slew\ rate = \frac{IB1}{Cc} = \frac{11.62uA}{2.3pf} = 5.05Mv/s$$

	Simulation	Analysis
Slew rate	4.66M	5.05M

Comment:

-I don't exactly know why the deviation between the two results, maybe we neglect parasitic capacitances that shunts Cc or some thing else. **May be TA tells us at a comment or at WhatsApp.**

4) Settling time:



Output	Nominal
/VOUT	
/Vin	
riseTime(VT("/VOUT") 0.6 nil ...	52.03n

$$trise = 2.2taw = \frac{2.2}{Wu} = \frac{2.2}{33.79M} = 65.1n$$

	Simulation	Analysis
Rise time	52.03n	65.1n

Comment:

-The deviation may be due to the approximate expression of UGF.

-Actually there is a very small ringing that we have PM = 74 < 76 in this case causes this small ringing.