# Analog IC Design – Cadence Tools
# Lab 12
# Design Problem

## The Design Challenge

- Part 1:
  - Two-stage SE output OTA
  - NMOS input stage
  - VDD = 1.8V
  - CL = 1pF
  - DC Gain > 60 dB
  - UGF > 200MHz
  - PM = 70-80 degree
  - Cgg of input stage < 100 fF
  - Minimize bias current

1-First we do a very rough hand analysis to get an initial point

$$Wu = \frac{gm1}{2piCc} > 200MHz, \qquad assume\ Cc = 0.5pf$$

$$gm1 > 628.3us$$

$$For\ Cgg < 100f,$$

$$assume\ \left(\frac{gm}{ID}\right)1 = 14, \qquad ID > 44.87uA, \qquad IB1 > 89.75uA$$

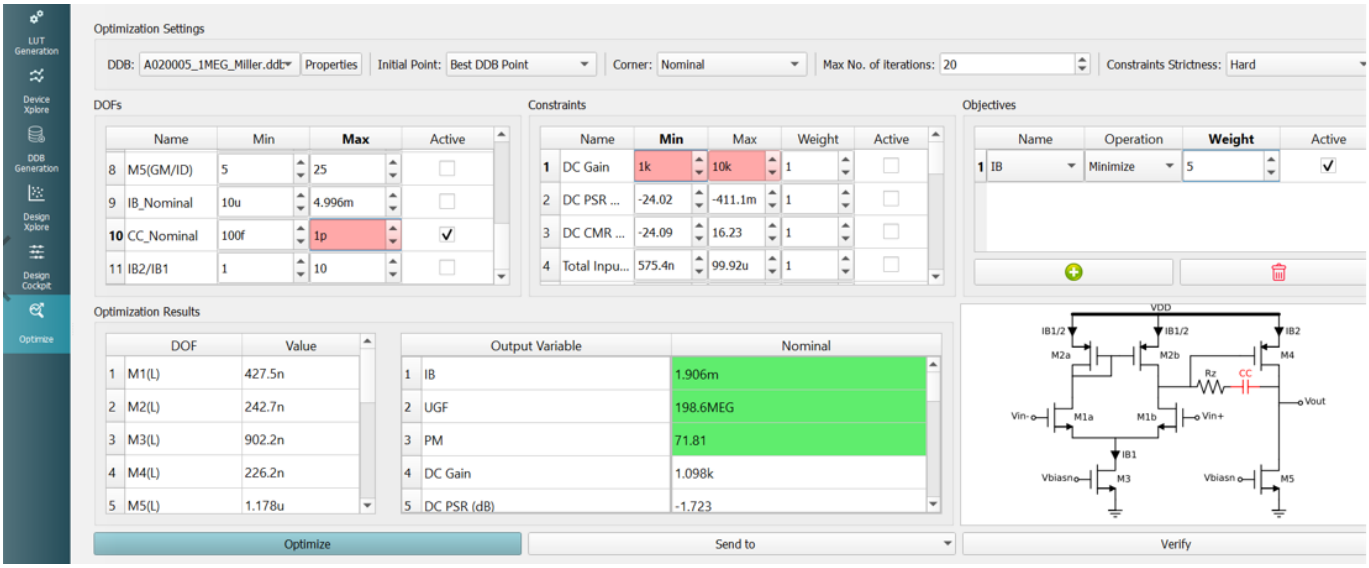
$$assume\ PM = 76, \quad Wp2 = 4Wu, \qquad \frac{gm2}{Cl} = \frac{4gm1}{Cc}$$

$$gm2 > 5026.4us$$

$$assume\ \left(\frac{gm}{ID}\right)2 = 14, \qquad IB2 > 359uA$$

$$IB > 448uA, \quad so\ we\ need\ a\ large\ current\ here$$

2-Then We go to ADT to make an initial guess from Design Cockpit, then to the optimization interface to get an optimum point with my ranges that gives:



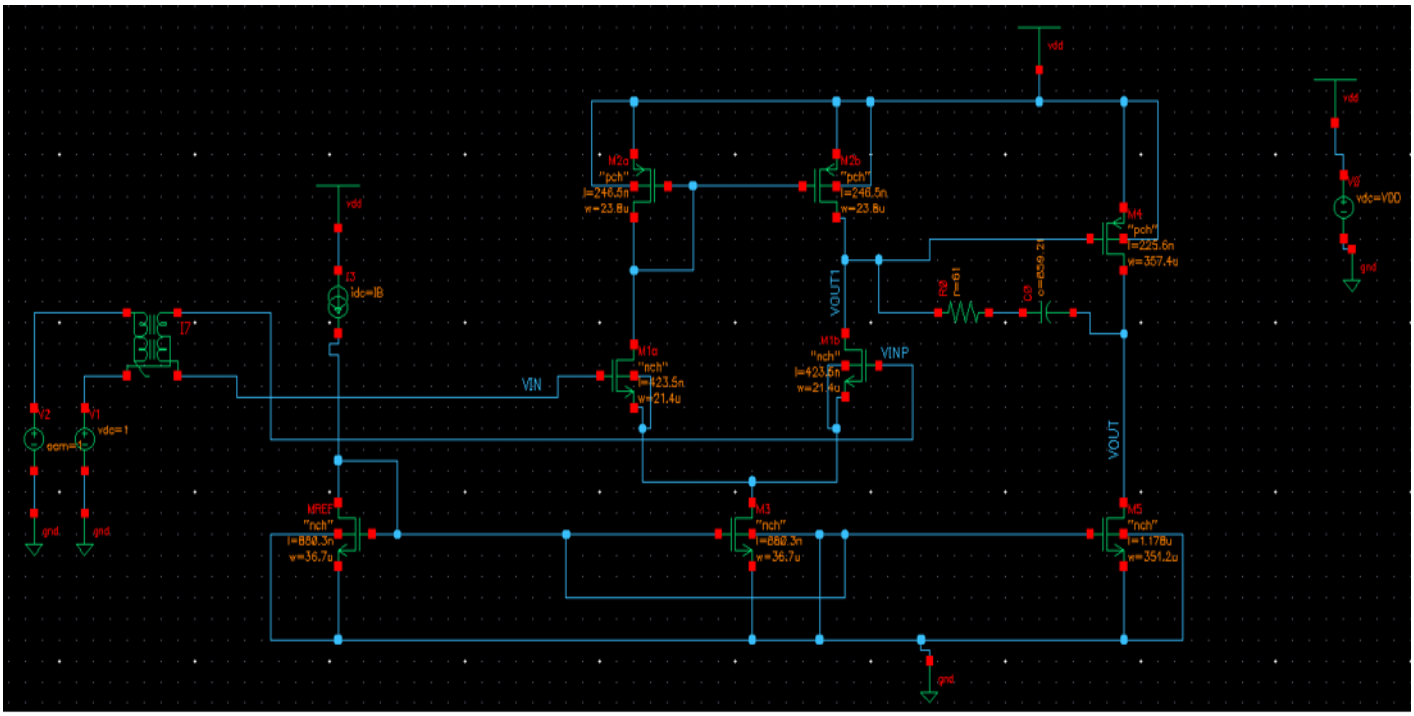

That point meets the specs with a large current but that's acceptable for now.

3-Then went to cadence to simulate this point and tune:

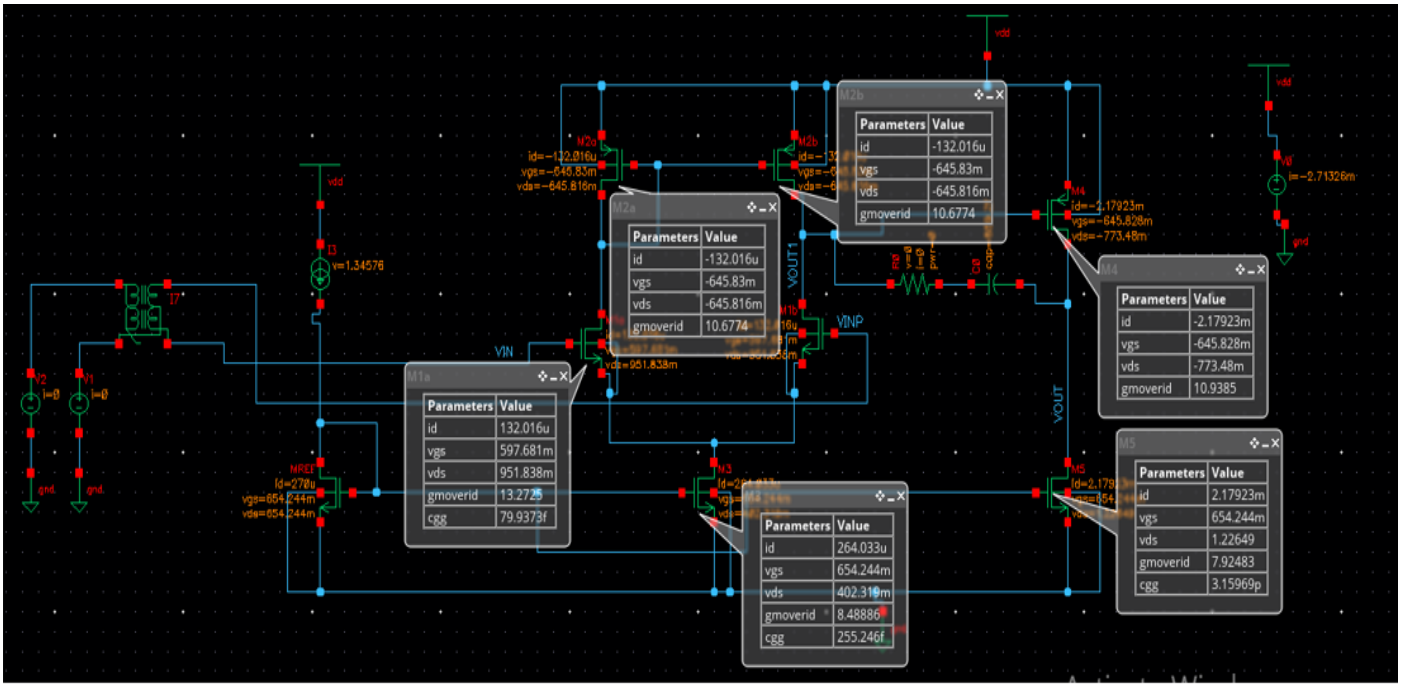
-That point gives UGF smaller than expected so we tuned to increase the current much again to meet the specs

-Finally, we reached that point:

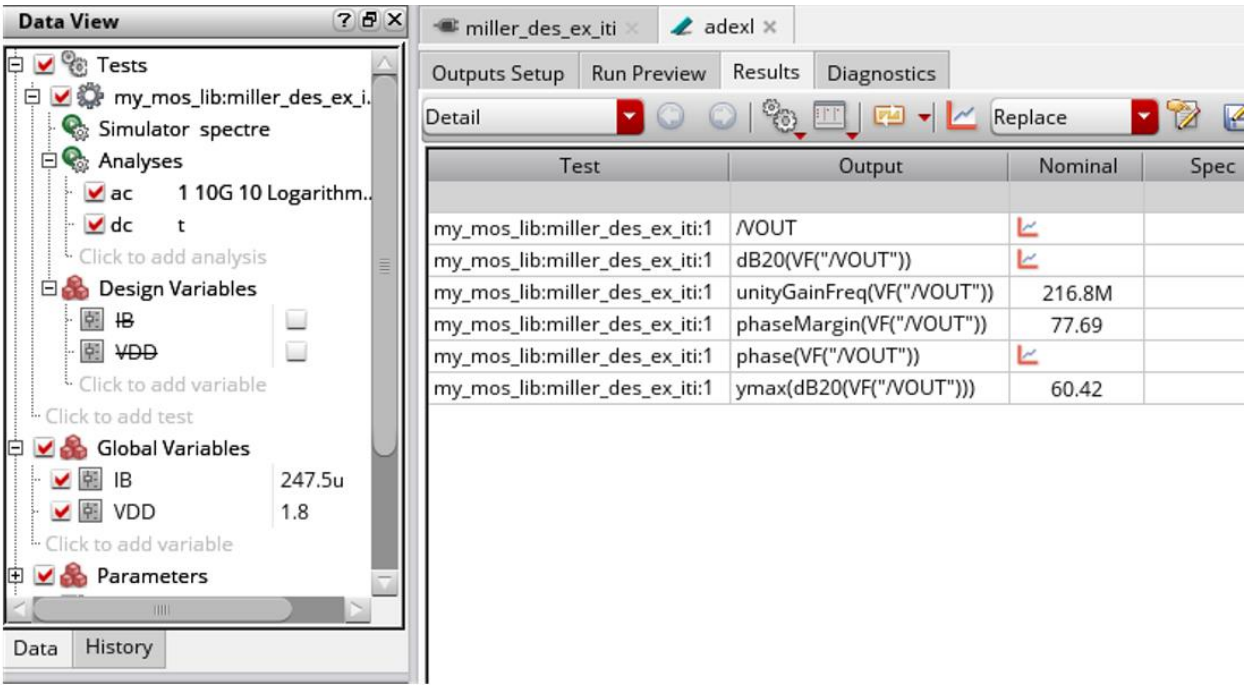
-Schematic with sizing:



-OP Point:



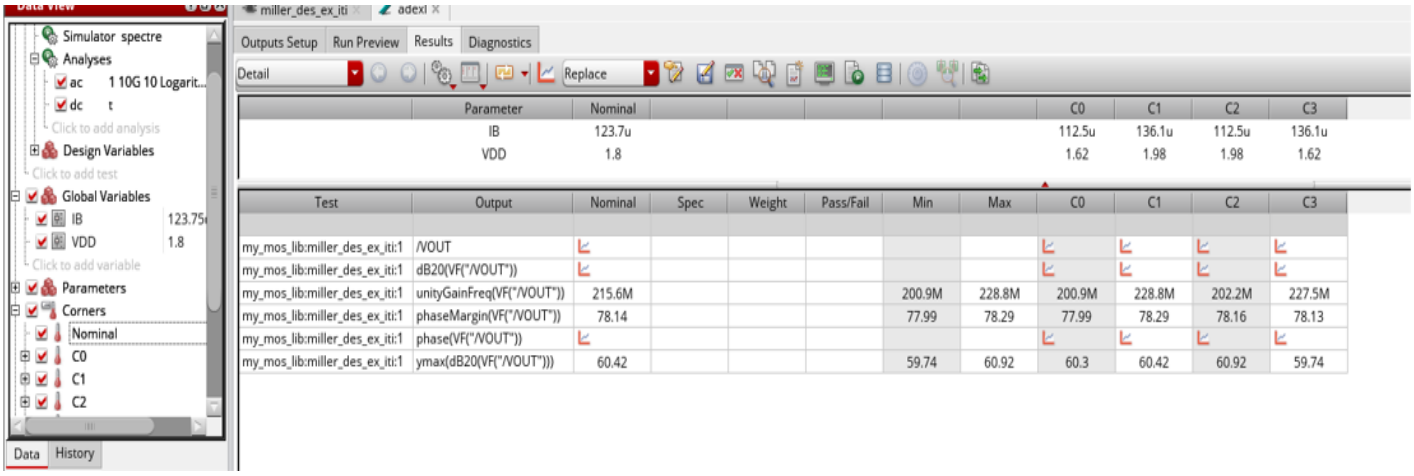

-Result:



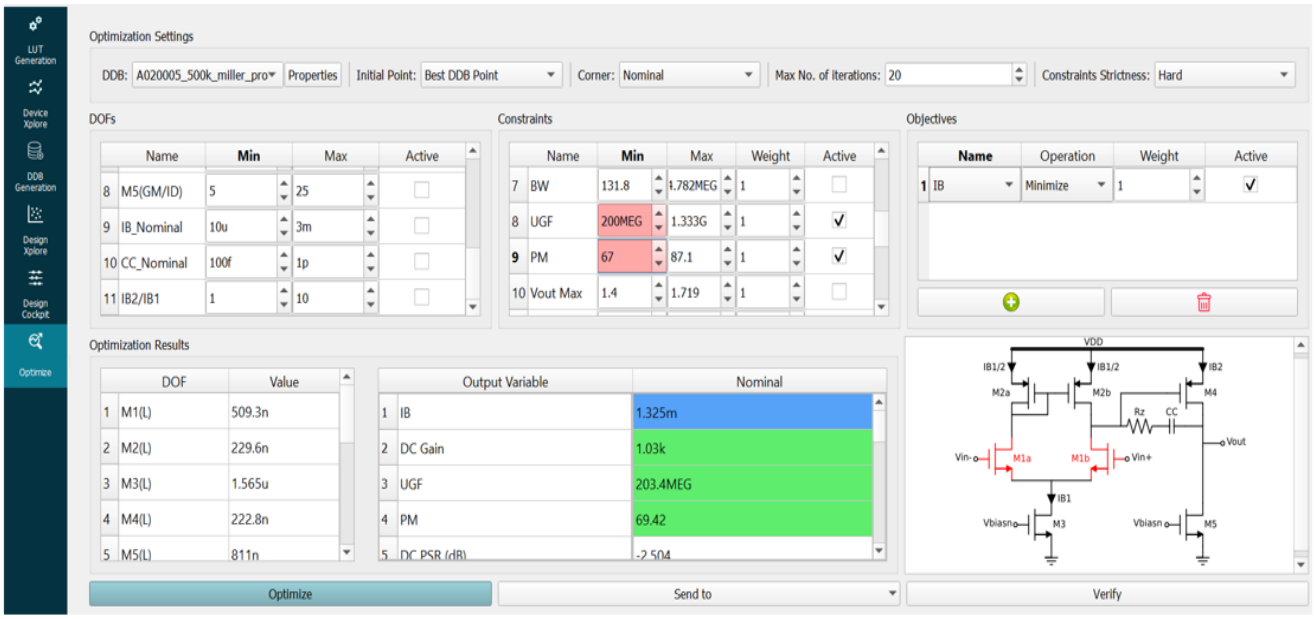
-We halved the reference current to be smaller that the needed current and halved its width to a practical view .

-Then we increase it with a small amount to meet the specs acoss corners that gives:

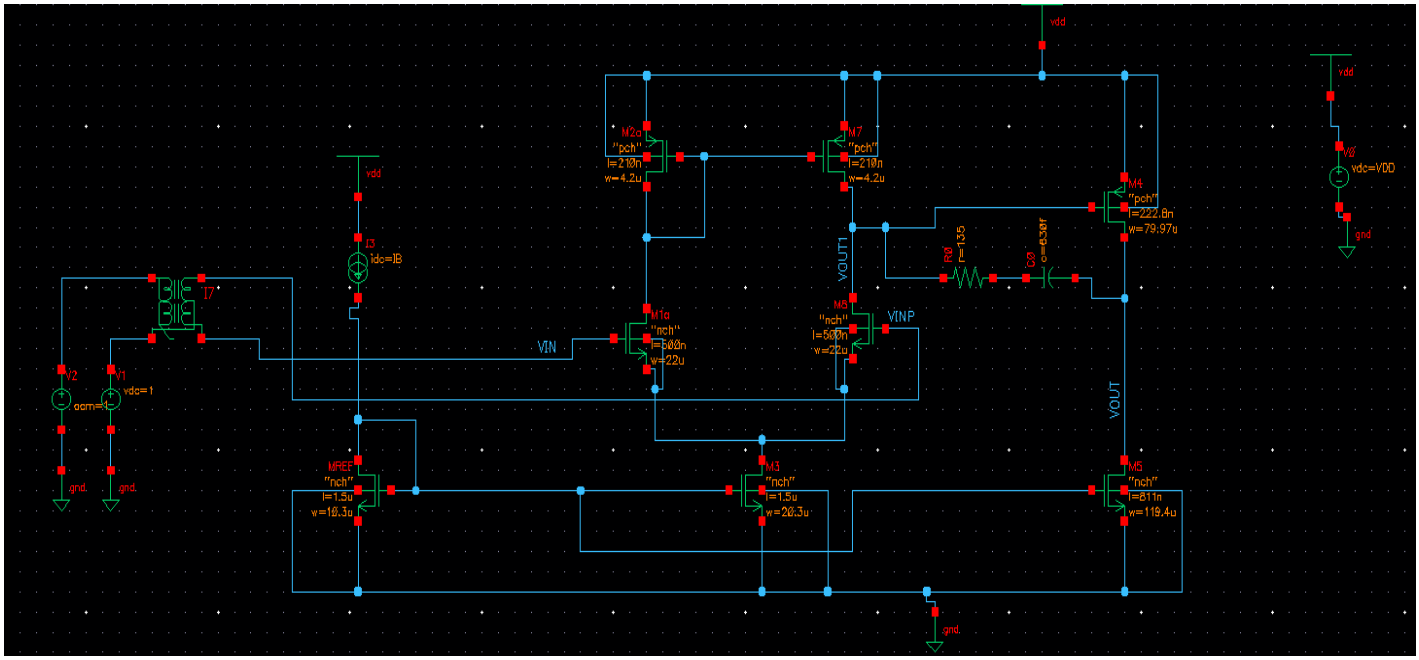
IB_tot = 2.1mA

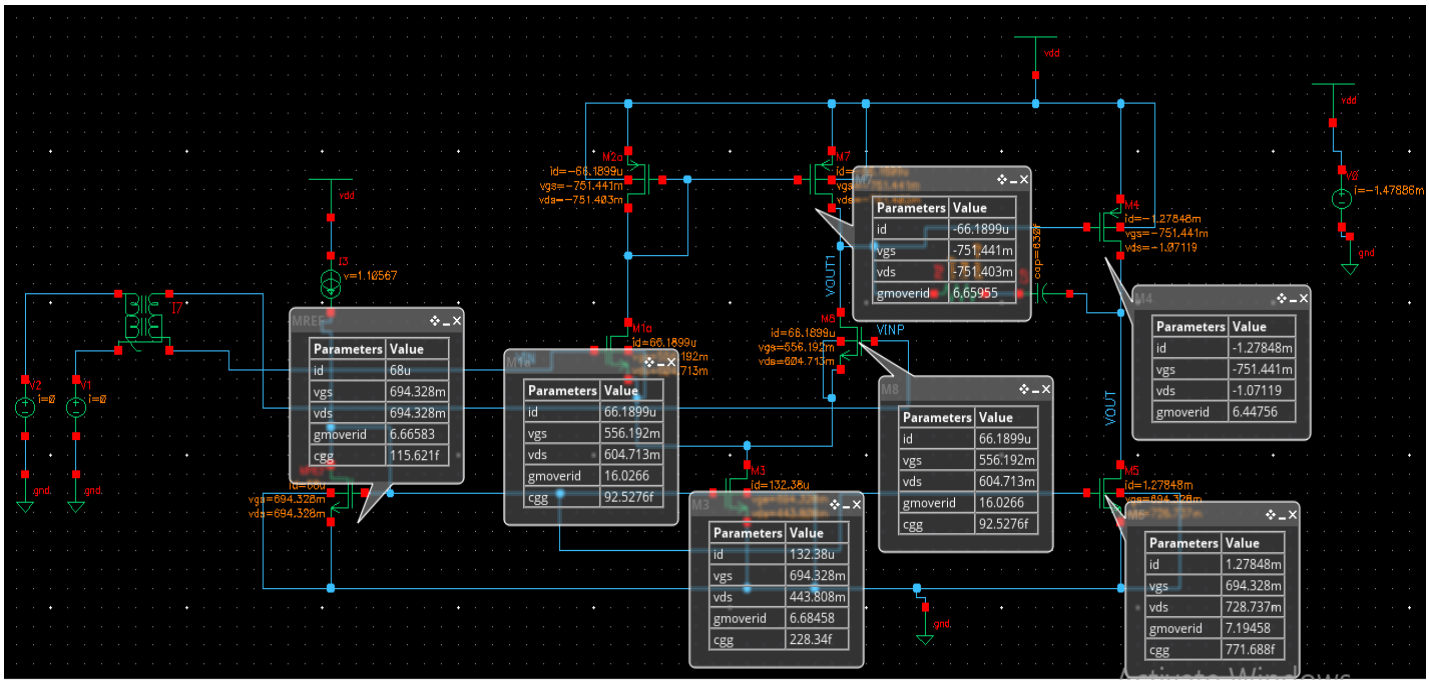



-That design meets all the specs but with large current, so we go to ADT again to tune after the hint that Dr Hesham gives us, increasing VINCM (corner) to 1.2, that gives a better point that meets the specs with a smaller current:

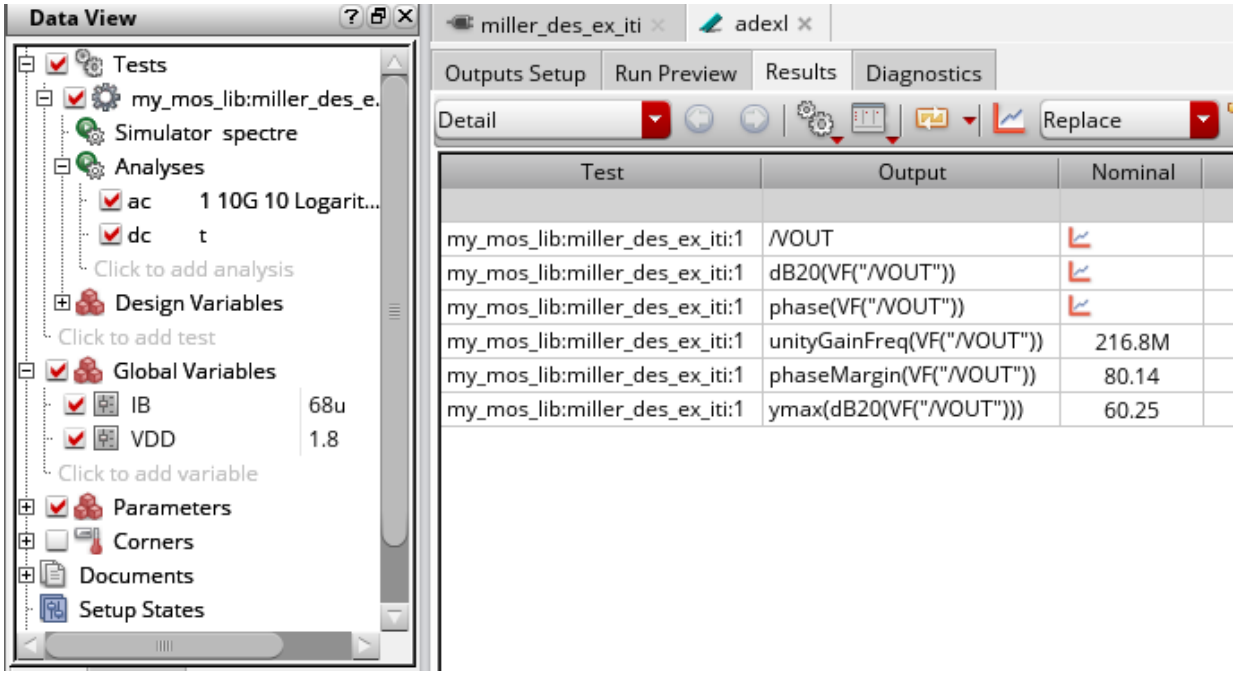


-Simulate that point:

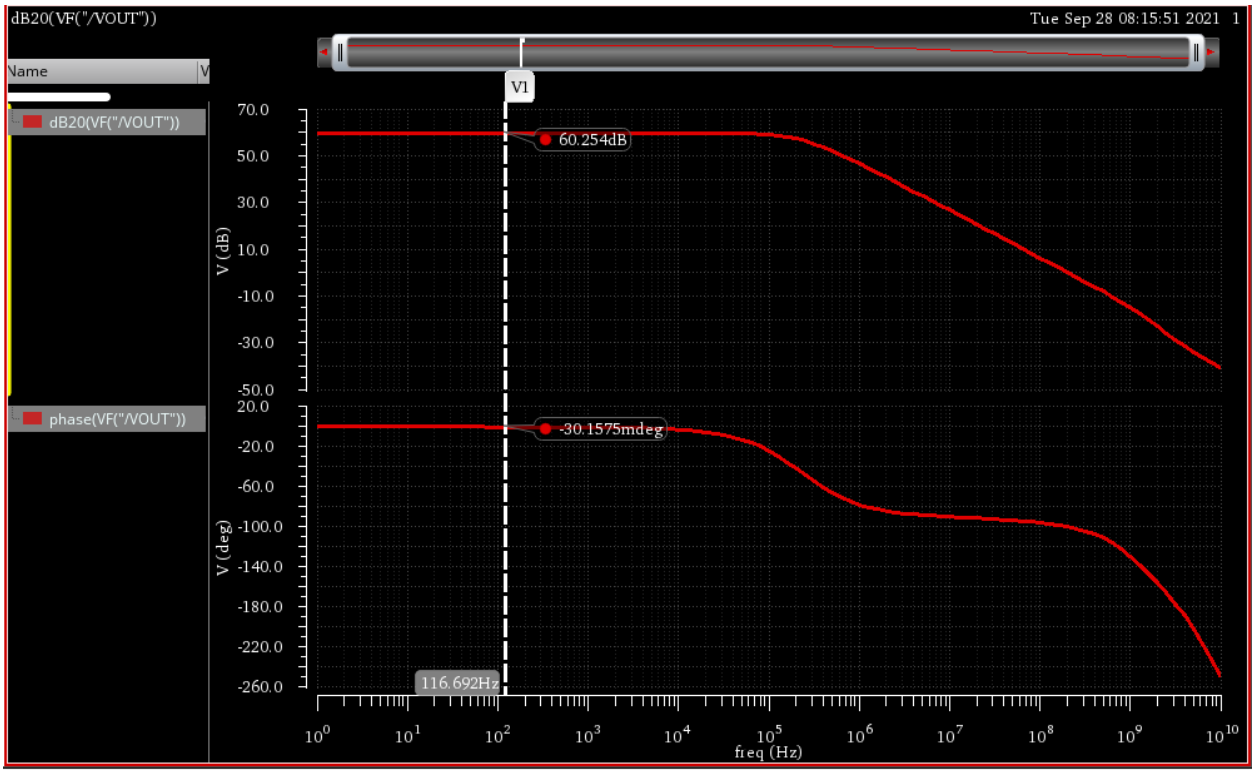


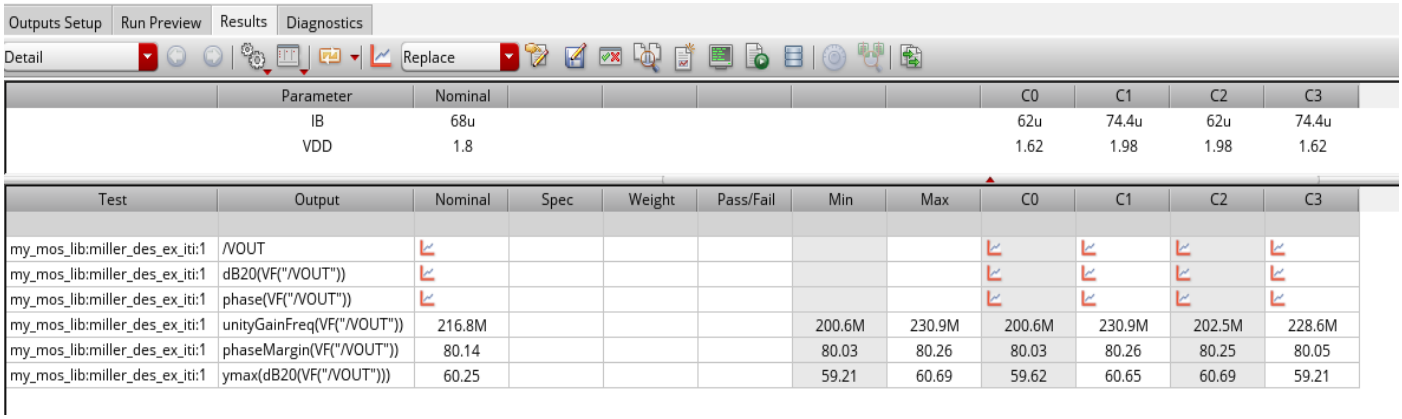

-That point doesn't achieve the gain spec, so we increased L2 a little more to give us the needed gain. $Av = gm1(ro1||ro2) * Av2$




-That point meets the specs with IB_tot = 1.4m



-Results across corners:



Outputs Setup | Run Preview | Results | Diagnostics

Detail | Replace

| Parameter | Nominal | | | | | | C0 | C1 | C2 | C3 |
|---|---|---|---|---|---|---|---|---|---|---|
| IB | 68u | | | | | | 62u | 74.4u | 62u | 74.4u |
| VDD | 1.8 | | | | | | 1.62 | 1.98 | 1.98 | 1.62 |

| Test | Output | Nominal | Spec | Weight | Pass/Fail | Min | Max | C0 | C1 | C2 | C3 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| my_mos_lib:miller_des_ex_iti:1 | /VOUT | | | | | | | | | | |
| my_mos_lib:miller_des_ex_iti:1 | dB20(VF("/VOUT")) | | | | | | | | | | |
| my_mos_lib:miller_des_ex_iti:1 | phase(VF("/VOUT")) | | | | | | | | | | |
| my_mos_lib:miller_des_ex_iti:1 | unityGainFreq(VF("/VOUT")) | 216.8M | | | | 200.6M | 230.9M | 200.6M | 230.9M | 202.5M | 228.6M |
| my_mos_lib:miller_des_ex_iti:1 | phaseMargin(VF("/VOUT")) | 80.14 | | | | 80.03 | 80.26 | 80.03 | 80.26 | 80.25 | 80.05 |
| my_mos_lib:miller_des_ex_iti:1 | ymax(dB20(VF("/VOUT"))) | 60.25 | | | | 59.21 | 60.69 | 59.62 | 60.65 | 60.69 | 59.21 |

**-We achieved all the specs with IB_min = 1.28mA**

-All of you, Thanks for everything.