Title: Class F Power oscillator

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Date: 5/12/2021

Objective:

Our target is to build a differential cascode class F PO at a frequency 915MHz and minimize dissipation in the MOSFET transistor by the concept of reducing overlapping between drain voltage and drain current.

MOSFET Used: N_HGLV_33_130LE.

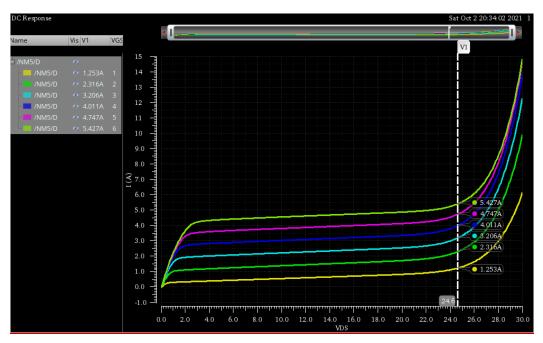


Figure 1: ID_VDS Saturation region.

ID-VGS Chs:

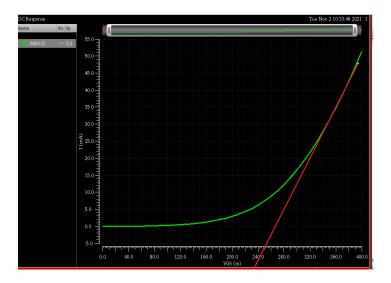


Figure 2: ID_VGS Chs.

Schematic:

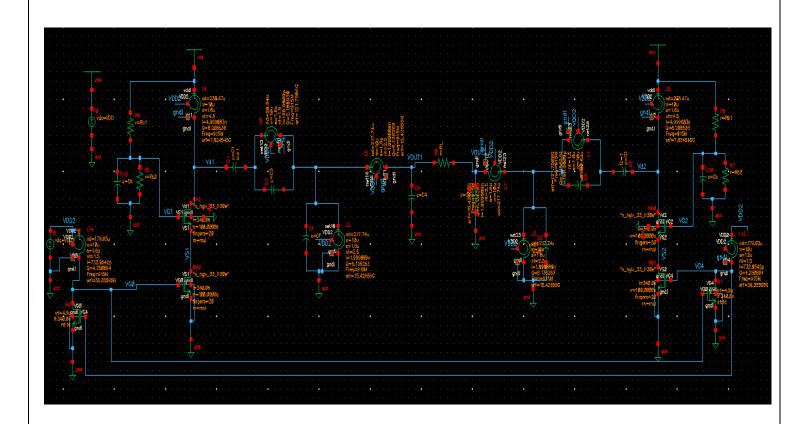


Figure 3: Schematic

Parameters:

	(W/L)1,2,3,4	WG	nf	mul	C1	RFC1,RFC2
Value	$\frac{9000u}{0.34u}$	5u	20	90	50pF	5nH,2nH
	CF	LF	C3	L3	VDD2	(W/L)5,6
Value	15.1pF	2nH	16.6pF	200pH	1.3V	$\frac{3000u}{0.34u}$
	RL	C4	L4	VDD1	Rb1,Rb2	Cb
Value	50Ω	10.1pF	2nH	16V	1k,600 Ω	30p

Sweeping RL:

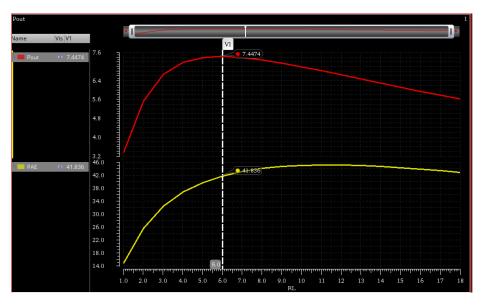


Figure 4: Pout and PAE vs RL.

-Point of maximum power is almost at RL = 6 Ω .

Waveforms:

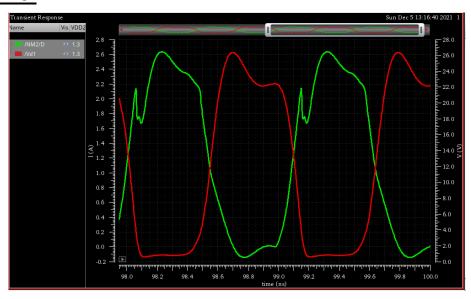


Figure 5: Drain voltage and current

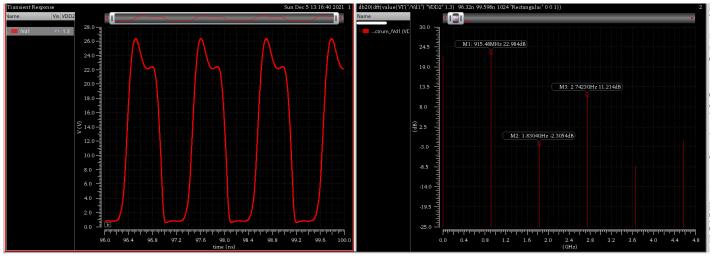


Figure 6: Vd spectrum.

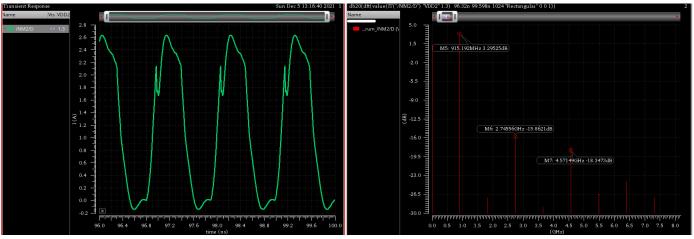


Figure 7: ID spectrum

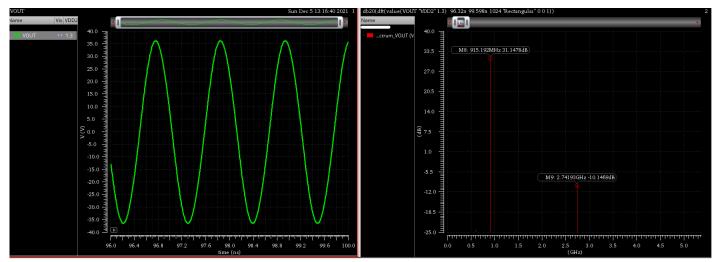


Figure 8: VOUT

Outputs:

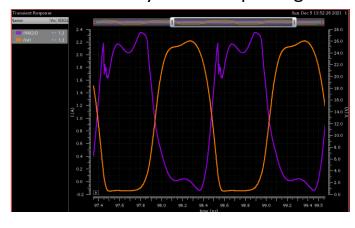
Pdc	38.22
Pout	13.12
PAE	34.33
THD	906.4m

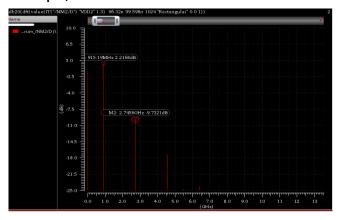
Pout = 13.1W

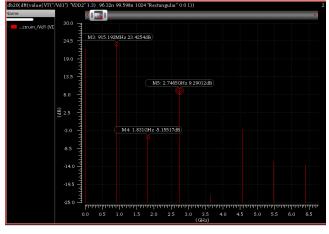
PAE = 34.3%

THD = 0.9%

-I don't know why but after putting the MOM caps, waveforms turn to this:







-Values almost the same:

Pout = 12.7W

PAE = 36.5%

THD = 3%

-There is a large pulse when the circuit starting to operate causes break down on the cascode transistor, I don't know that's important or not, I can't get rid of it.

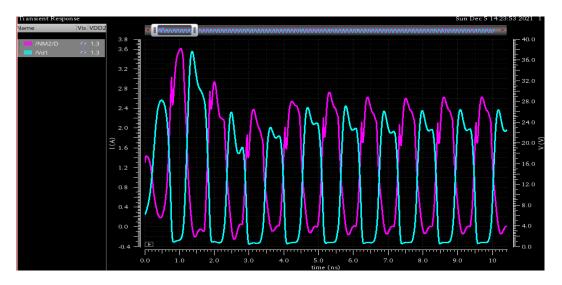


Figure 9

Discussion:

- -Degraded values at 434MHz, Pout = 7W and PAE = 20%.
- -Large losses in the circuit due to smaller Q of the inductors, May with some techniques in layout, we could reach a higher Q and better PAE.