of Clock Cycles

2-op instructions

Fetch instruction = 4

REG DIRECT	1
AUTO INC DIRECT	3
AUTO DEC DIRECT	4
INDEXED DIRECT	7
REG INDIRECT	3
AUTO INC INDIRECT	5
AUTO DEC INDIRECT	6
INDEXED INDIRECT	9

Save:

Register = 1

Else = 2

CMP instruction does need to save anything

ALU operations:

All ALU operations and MOV instruction require 2 clock cycles.

SRC	DST	TOTAL NUMBER OF CLOCK CYCLES
Reg Direct	Reg Direct	2
	Auto Inc Direct	4
	Auto Dec Direct	5
	Indexed Direct	8
	Reg Indirect	4
	Auto Inc Indirect	6
	Auto Dec Indirect	7
	Indexed Indirect	10
Auto Inc Direct	Reg Direct	4
	Auto Inc Direct	6
	Auto Dec Direct	7
	Indexed Direct	10
	Reg Indirect	6
	Auto Inc Indirect	8
	Auto Dec Indirect	9
	Indexed Indirect	12
Auto Dec Direct	Reg Direct	5
	Auto Inc Direct	7
	Auto Dec Direct	8
	Indexed Direct	11
	Reg Indirect	7
	Auto Inc Indirect	9
	Auto Dec Indirect	10
	Indexed Indirect	13
Indexed Direct	Reg Direct	8
	Auto Inc Direct	10
	Auto Dec Direct	11
	Indexed Direct	14
	Reg Indirect	10
	Auto Inc Indirect	12
	Auto Dec Indirect	13
	Indexed Indirect	16
Reg Indirect	Reg Direct	4
	Auto Inc Direct	6
	Auto Dec Direct	7
	Indexed Direct	10
	Reg Indirect	6
	Auto Inc Indirect	8
	Auto Dec Indirect	9
	Indexed Indirect	12

Auto Inc Indirect	**Reg Direct**	**6**
	Auto Inc Direct	**8**
	Auto Dec Direct	**9**
	Indexed Direct	**12**
	Reg Indirect	**8**
	Auto Inc Indirect	**10**
	Auto Dec Indirect	**11**
	Indexed Indirect	**14**
Auto Dec Indirect	**Reg Direct**	**7**
	Auto Inc Direct	**9**
	Auto Dec Direct	**10**
	Indexed Direct	**13**
	Reg Indirect	**9**
	Auto Inc Indirect	**11**
	Auto Dec Indirect	**12**
	Indexed Indirect	**15**
Indexed Indirect	**Reg Direct**	**10**
	Auto Inc Direct	**12**
	Auto Dec Direct	**13**
	Indexed Direct	**16**
	Reg Indirect	**12**
	Auto Inc Indirect	**14**
	Auto Dec Indirect	**15**
	Indexed Indirect	**18**

1-op instructions

Fetch dst:

Total # of clock cycles:

REG DIRECT	1
AUTO INC DIRECT	3
AUTO DEC DIRECT	4
INDEXED DIRECT	7
REG INDIRECT	3
AUTO INC INDIRECT	5
AUTO DEC INDIRECT	6
INDEXED INDIRECT	9

Save:

Register = 1

Else = 2

CMP instruction does need to save anything

ALU operations:

All ALU operations require 2 clock cycles.

Branching

Total # of clock cycles = 3

No-op

HLT -> 1 clock cycle

NOP -> 1 clock cycle

MISC

JSR -> 4

RTS -> 4

IRET -> 8

of memory access

2-op instructions

Fetch instruction = 1

REG DIRECT	0
AUTO INC DIRECT	1
AUTO DEC DIRECT	1
INDEXED DIRECT	2
REG INDIRECT	1
AUTO INC INDIRECT	2
AUTO DEC INDIRECT	2
INDEXED INDIRECT	3

DST	SRC	TOTAL NUMBER OF CLOCK CYCLES
Reg Direct	Reg Direct	0
	Auto Inc Direct	1
	Auto Dec Direct	1
	Indexed Direct	2
	Reg Indirect	1
	Auto Inc Indirect	2
	Auto Dec Indirect	2
	Indexed Indirect	3
Auto Inc Direct	Reg Direct	1
	Auto Inc Direct	2
	Auto Dec Direct	2
	Indexed Direct	3
	Reg Indirect	2
	Auto Inc Indirect	3
	Auto Dec Indirect	3
	Indexed Indirect	4
Auto Dec Direct	Reg Direct	1
	Auto Inc Direct	2
	Auto Dec Direct	2
	Indexed Direct	3
	Reg Indirect	2
	Auto Inc Indirect	3
	Auto Dec Indirect	3
	Indexed Indirect	4
Indexed Direct	Reg Direct	2
	Auto Inc Direct	3
	Auto Dec Direct	3
	Indexed Direct	4
	Reg Indirect	3
	Auto Inc Indirect	4
	Auto Dec Indirect	4
	Indexed Indirect	5
Reg Indirect	Reg Direct	1
	Auto Inc Direct	2
	Auto Dec Direct	2
	Indexed Direct	3
	Reg Indirect	2
	Auto Inc Indirect	3
	Auto Dec Indirect	3
	Indexed Indirect	4

Auto Inc Indirect	**Reg Direct**	**2**
	Auto Inc Direct	**3**
	Auto Dec Direct	**3**
	Indexed Direct	**4**
	Reg Indirect	**3**
	Auto Inc Indirect	**4**
	Auto Dec Indirect	**4**
	Indexed Indirect	**5**
Auto Dec Indirect	**Reg Direct**	**2**
	Auto Inc Direct	**3**
	Auto Dec Direct	**3**
	Indexed Direct	**4**
	Reg Indirect	**3**
	Auto Inc Indirect	**4**
	Auto Dec Indirect	**4**
	Indexed Indirect	**5**
Indexed Indirect	**Reg Direct**	**3**
	Auto Inc Direct	**4**
	Auto Dec Direct	**5**
	Indexed Direct	**5**
	Reg Indirect	**4**
	Auto Inc Indirect	**5**
	Auto Dec Indirect	**5**
	Indexed Indirect	**6**

1-op instructions

Fetch instruction = 1

Fetch DST:

REG DIRECT	0
AUTO INC DIRECT	1
AUTO DEC DIRECT	1
INDEXED DIRECT	2
REG INDIRECT	1
AUTO INC INDIRECT	2
AUTO DEC INDIRECT	2
INDEXED INDIRECT	3

Branching

Fetch instruction = 1

Total = 0

No-op

Fetch instruction = 1

Total = 0

MISC

JSR -> 1

RTS -> 1

IRET -> 2

CPI

For two operands instructions source and destination fetching

64 combination of a two operand instruction

We have 9 two operand instructions.

Total # of instructions = 9 * 64 = 567

Fetch Source & Dest + ALU clock cycles + Save clock cycles

(608 + 2 * 64 + 2 * 56 + 1 * 8) * 9 = 7704

For single operand destination fetching

8 combinations of a single operand instruction

We have 9 single operand instructions

Total # of instructions = 9 * 8 = 72

Fetch Dest + ALU clock cycles + save clock cycles

(38 + 2 * 8 + 1 + 2 * 7) * 9 = 621

For branching we have 3 clock cycles for each branch instruction. And they are 7 instructions

7 * 3 = 21 clock cycles

For no operand we have 2 instructions each has 1 clock cycle.

2 * 1 = 2 clock cycles

For MISC instructions we have 3 instructions all of them have 16 clock cycles

Total:

clock cycles / # instructions = (7704 + 621 + 21 + 2 + 16) / (567 + 72 + 7 + 2 + 3) = 12.8479