Register	Code
RO	000
R1	001
R2	010
R3	011
R4	100
R4	101
R6	110
R7	111

Register Mode	Code
Register	00
AutoInc	01
AutoDec	10
Indexed	11

Mode	Code
Direct	0
Indirect	1

# 2 OPERANDS $\rightarrow$ IR $\rightarrow$ OPCODE (15:12) SRC (11:6) DST(5:0)

Inst	OP Code
MOV	0000
ADD	0001
ADC	0010
SUB	0011
SBC	0100
AND	0101
OR	0110
XOR	0111
CMP	1000

<sup>\*</sup>Register Mode +Mode

### 1 OPERANDS →

## IR $\rightarrow$ OPCODE (15:6) DST (5:0)

### 100100+OPcode

INST	OP CODE (9:6)
INC	0000
DEC	0001
CLR	0010
INV	0011
LSR	0100
ROR	0101
ASR	0110
LSL	0111
ROL	1000

#### **Branch INST**

## 10100+OPCODE

INST	OP CODE
BR	000
BEQ	001
BNE	010
BLO	011
BLS	100
ВНІ	101
BHS	110

#### No OPERAND

## 1011+opcode+xx

INST	OPCODE
HLT	101100xxxxxxx
NOP	101101xxxxxxx

# Jump Sub-Routine Instructions

## 1100

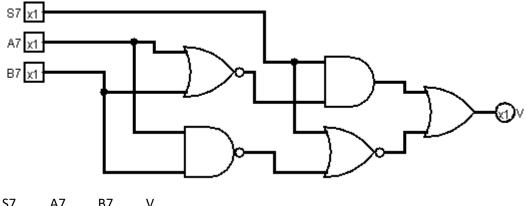
INST	
JSR	1100 00xxxx +dst
RTS	1100 01xxxxxxxxxx
INTERRUPT	
IRET	1100 10xxxxxxxx

F0 (8-bits)	F1 (4-bit)	F2 (3-bit)	F3(2-bit)
	0000: No transfer 0001: PCout 0010: MDR_out 0011: Z_out 0100: Rsrc_out 0101: Rdst_out 0110: TEMP_out 0111: Address _out 1000: SOURCE_OUT 1001: DEST_OUT 1010: SP_out 1011: FLAGs_out	000: No Transfer 001:Pc_in 010:IR_in 011:Z_in 100:Rsrc_in 101:Rdst_in 110: SP_in	00: No transfer 01:MAR_in 10:MDR_in 11:TEMP_in

F4 (2-bits)	F5	F6	F7
	(4 bit)	(2bit)	(1bit)
00: No transfer	0000:ADD	00: No Action	0: No Action
01: Yin	0001:SUB	01:Read	1:ClearY
10: SOURCE_IN	0010:AND	10:Write	
11: DEST_IN	0011:OR		
	0100:XOR		
	0101:NOT		
	0110:LSR		
	0111:ROR		
	1000:ASR		
	1001:LSL		
	1010:ROL		
	1011:CLR		
	1100:ADC		
	1101:SBC		

F8	F9	F10	F11	F12	F13	F14
(1bits)	(1 bit)	(3 bit)	(1bit)	(1bit)	(1bit)	(1bit) FLAGS_CH
0: Carry_in	0: no action	000: No Action	0: No Action	0: No Action	0: No action	0: FLAGS is
= 0	1: flags_in	001: OR_dst	1: PLA_out	1: Halt	1: INT	loaded from
1: Carry_in		010: OR_indsrc				ALU
= 1		011: OR_inddst				1: FLAGS is
		100: OR_result				loaded from
		101: OR_ALU				BUS
		110: OR_sng/OR_JSR				
		111: OR_INT				

# Overflow flag circuit



<b>S7</b>	Α7	В7	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Zero flag -> 16-input NOR gate

Carry\_out from ALU

N flag -> S15

Address decoder function

If(IR[7]) F = 11111111 & IR[7:0] & 0

Else F = 0000000 & IR[7:0] & 0