*Generating process diagrams for (control software in) Reflex language*

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*Abstract*— There are tasks of reverse engineering and code refactoring in a process of developing and supporting projects. There is a need to create documentation (and, especially, graphical documentation) for the existing source code of programs. A task to develop code analysis tools in industrial automation, writing control algorithms and programming embedded systems is actual because problem-oriented languages (DSL) are used here. In particular, this problem is relevant for process-oriented programming (POP). Code analysis is being done by people in current projects, it takes a lot of time, and documentation, that is created, contains errors.

In this work we analyze available graph description languages and present an approach to automatic generation of graphical documentation for specialized programming languages. The presented approach involves generating of diagrams as graphs form the source code and using already available external tools for laying out, visualization and editing purposes. A software module was created for the Reflex language to generate process relationship diagrams for data, management, and state diagrams. Also, parts of graphs that don’t share nodes are automatically written to different files. The module automates the creation of graphical documentation and simplifies the support of projects in the Reflex language.

Practical testing has shown that using the developed module helps decrease the time spent (time expenses) for creating process diagrams (from a few hours to a couple of seconds) and guarantees that there are no errors caused by human factor.

Keywords— control software, process diagrams, graphical documentation, process-oriented programming, code refactoring, reverse-engineering, code analysis

# Introduction

Software development projects can often benefit from reverse engineering method/techniques. Such methods can be utilized in code refactoring and documentation both in development and maintenance phases of a project. For commonly used object-oriented languages such as Java, C++, C#, etc. various software tools are available for automatic generation graphical documentation. In many cases these tools are integrated into the development environment for the language.

Developing code analysis tools in industrial automation, writing control algorithms and programming embedded systems is of especially high interest for problem-oriented languages (DSL), or common languages as only low-level tools are often available for them. In particular, this problem is relevant for Reflex process-oriented programming (POP) language, which is actively developed in the Institute of automation and Electrometry of the Siberian department of the Russian Academy of Science [2]. In current projects code analysis is performed manually, which takes a lot of time, and the resulting documentation is likely to contain errors because of human factor.

# Purpose of work and tasks

The purpose of work was to develop a software module for building process diagrams according to the specification in the Reflex language. To achieve that goal, such tasks were set.

## Analyze:

* POP specific;
* Existing tools for generating diagrams by code;
* Types of diagram’s notations which is used for code analyze.

## Design the module:

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* Formulate requirements for software module;
* Develop diagram’s notation for showing communications between processes;
* Choose the file format for saving diagrams.

## Develop module’s architecture and realize it.

## Test the module.

# Specific features of the Reflex language.

A Reflex program consists of descriptions of processes, which are defined by state machines. Processes run in the cooperative model of multithreading and communicate with each via shared variables as well as with special control statements (i.e. process can start and stop each other and themselves, and import variables from another processes).

# Analysis of existing tools for generating diagrams from code

We have found that not all tools for generating diagrams from code for common programming languages have the ability for code generation, dynamic diagram’s building and hiding diagram’s components, but all have the ability to modify diagrams. Results of our analysis of existing tools for diagram generation from source code for common programming languages are shown in the Table 1.

1. tools for generate diagrams by code for common languages

| Tool’s name | Tool’s abilities | | | |
| --- | --- | --- | --- | --- |
| Code generation | ***Modify diagrams*** | ***Hiding diagram’s components*** | Dynamic building |
| Class Designer for Visual Studio | - | + | + | + |
| Astah UML | + | + | ? | ? |
| MagicDraw | + | + | ? | + |
| Software Ideas Modeler | + | + | + | + |
| BOUML | + | + | + | - |
| Visual paradigm | + | + | ? | ? |
| Rational Rose | + | + | + | + |
| Enterprise Architect | + | + | ? | ? |
| IntelliJ Idea | - | + | + | + |
| Sybase PowerDesigner | + | + | + | - |
| NetBeans | - | + | - | - |
| Lab view | + | + | - | ? |
| Altova UModel 2008 | + | + | ? | ? |

By analyzing software development tools for writing control algorithms and embedded systems programming, we have found, that even among commercial tools, a very small percentage of them provides reverse engineering functionality, including tools for commercial use. In General, reverse engineering is supported by object-oriented SCADA packages, which have little to no relation to the area of control and embedded software.

# requirements for software module

Based on the analysis results, there are requirements for software module. It has to have the following capabilities:

* Diagram modification/editing;
* Automatic layout;
* Generation of the following diagram types:
  + Data communication diagram;
  + Process control diagram;
  + Processes states diagram;
* Save diagrams to the file;
* Divide diagrams into parts and save them to different files, if parts haven’t got any shared nodes.

# Process diagrams

## Process state diagram

For process states diagram we will use UML statechart diagram [1][3]. An example of such diagram is shown on the Fig. 1.

state_diagramm_eng

1. Example of the process state diagram слишком мелко

Names of process states are inside the nodes. They are connected by arrows, with conditional expressions (switch conditions) above them in square brackets. Actions which will be done with switching to that state are wrote marked after the slash.

## Diagram of communication between processes by data

артикльGraphical notation (a graphical has been developed/introduced, which is based../ The graphical notation for .. was/is based on…), which was created for data diagram of communication between processes, is based on the UML state machine diagram [1][3] and on the activity UML diagram. An example of such diagram is shown on the Fig. 2.

data_diagramm_eng

1. Example of a process data connection diagram

Processes names are written in rectangular nodes, variable’s names are written in elliptical diagram nodes. Processes nodes are connected with variable’s nodes by arrows, and connection type is written above them (e.g. imported variables are marked as ‘import’, declared variables are marked as ‘declare’).

## Diagram of communication between processes by managing

Graphical notation, which was created for managing diagram of communication between processes, based on the UML state machine diagram [1][3] and on the activity UML diagram. An example of such diagram is showed on the Fig. 3.

activity_diagramm_eng

1. Example of a process managing connection diagram

# Graph storage formats

To choose the graph storage format for module’s output diagram files, we have perfomed analysis (analyzed) of graph representation formats. The result of analysis is showed in the Table 2. The following formats were considered: GraphML [8][9], Gv [10], Xgml [11], Gml [12], Node list [17], Edge list [17], Pajek [13], Leda [14][18][19], TLP [15][16], Gw [14][18][19] and GEXF[20][21].

1. Graph representation formats

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Format name | Format’s abilities | | | | |
| Saving coordinates | Right node’s shape | Oriented graph | Edge labels | Tools that use format |
| GraphML | + | + | + | + | Gephi, Igraph, OGDF, Yed, NetworkX |
| Gv | - | + | + | + | GraphViz, Gephi, Igraph, OGDF, ZGRViewer, NetworkX |
| Xgml | + | + | + | + | Yed |
| Gml | + | + | + | + | Gephi, Igraph, OGDF, Yed, NetworkX, Tulip, LEDA |
| Node list | - | - | + | - | Yed, NetDraw |
| Edge list | - | - | + | - | OGDF, Yed, NetworkX, NetDraw |
| Pajek | + | + | + | + | Gephi, Igraph, NetworkX, NetDraw |
| Leda | + | + | + | + | Igraph, OGDF, NetworkX, LEDA |
| TLP | + | + | + | + | OGDF, Gephi, Tulip |
| Gw | + | + | + | + | LEDA |
| GEXF | + | + | + | - | Gephi, OGDF, NetworkX, Tulip |

Such an evaluation criterion as the ability to save coordinates is important because it makes possible to save graph layout (by a third-party layout tool) and diagram’s modifications after closing the file. We also analyzed notation criteria to understand which formats may storage graphs in our notations. The last criterion was a list of tools that are able to use the format [4][5][6].

An ability to convert one file format to another is showed on the Fig. 4. We found that here is a two families of graph file formats, inside which conversion is possible.



1. Example of a process managing connection diagram (толщина рамок, размер шрифта)

GraphML and GML file formats look most suitable for use in this work. We made a more detailed analysis of these file formats, the result of which is showed on the Table 3.

1. Comparison of GraphML and GML file formats

| Comparison criterion | Name of the file format | |
| --- | --- | --- |
| GML | GraphML |
| File size | x | 2 \* x |
| Easy to read by human | + | - |
| Can store links | - | + |

GML format has a language with a human-readable syntax; GraphML format has an language with XML-like syntax. GraphML diagrams have twice the size of the same GML diagrams. Also GraphML allows to store links, and that’s important, because in each processes diagram node we want to have a link to the state diagram for that process.

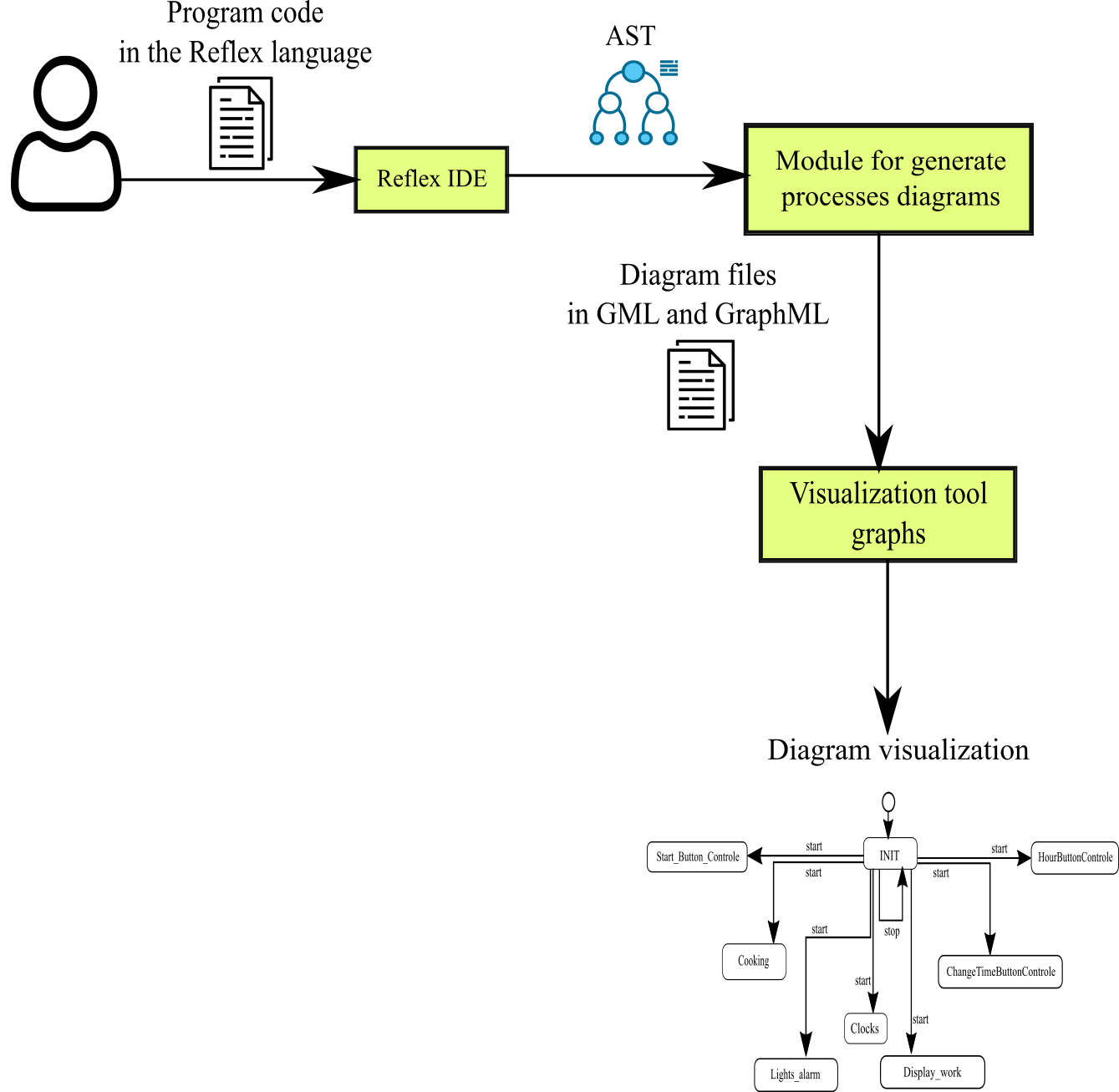
As a result, GML was (has been?) chosen for the process state diagram because of small file’s sizes (the module would generate such diagram for every process in the program). GraphML was chosen for processes communication diagrams by data and managing, because it allows to store the links in graph’s nodes.

# Module’s architecture

The developed module uses the Model–view–controller (MVC) software design pattern, which enables quick modification of the architecture. Firstly, the controller starts the model generator for processes state diagrams, then the view part creates GML files of those diagrams. After that, the controller starts the model generators for diagrams of connection between processes. Then it uses a graph separator module to divide diagram’s models if they have independent parts. After that the diagram generators create GraphML files of diagrams with links in each process diagram node to a state diagram for that process (which was generated before).

# Module’s realization implementation

The module was implemented as an Eclipse plugin (to simplify integration in the Reflex IDE) using Xtext and Xtend technologies. After opening the Reflex IDE and writing code, the user/one can click the save file button, and then processes diagrams of connection by data and managing, and state diagram will be automatically generated. We recommend opening them with the yEd [7] tool that supports automatic graph layout. The sequence of user actions is showed on the Fig. 5.



1. User steps scheme

# The conclusion

As a result, a software module for building process diagrams according to the specification in the Reflex language was created. The module creates processes diagrams of connection by data and managing, and state diagram. It automates the creation of the graphical documentation and simplifies the support of projects in the Reflex language. Practical testing has shown that using the module decreased the time for creating processes diagrams (from a few hours to a couple of seconds) and guarantees that there are no errors caused by human factors.

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