Microprocessors & Interfacing

Analog Input/Output

Lecturer : Annie Guo

Lecture Overview

- Analog output
  - PWM
  - Digital-to-Analog (D/A) Conversion
- Analog input
  - Analog-to-Digital (A/D) Conversion

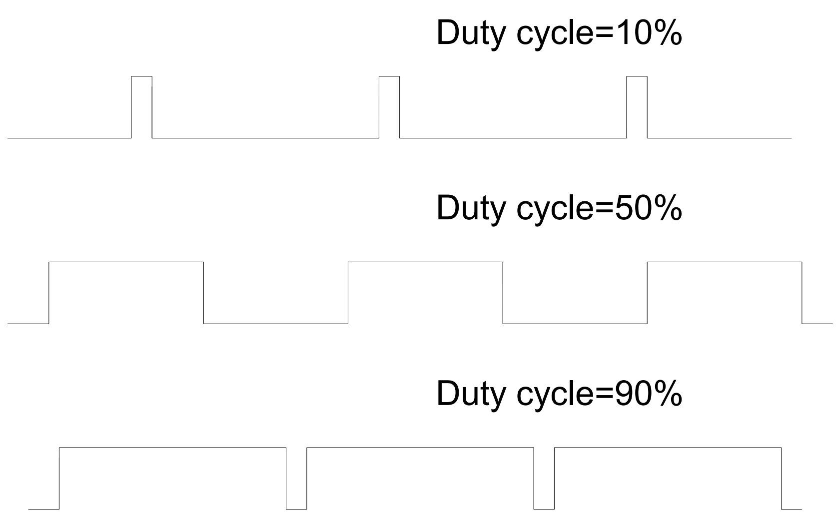
PWM Analog Output

- PWM (Pulse Width Modulation) is a way of digitally encoding analog signal levels.
  - By using high-resolution counters, the duty cycle (pulse width/period) of a pulse wave is modulated to encode a specific analog signal level.
- PWM is a powerful technique for controlling analog circuits/devices with the processor's digital output.
- It is used in a wide variety of applications
  - E.g. motor speed control

PWM Analog Output (cont.)

- The PWM signal is still digital
  - Its value is either full high or full low.
- A low-pass filter is required to smooth the input signal and eliminate the inherent noise components in PWM signal.
- The output voltage is directly proportional to the pulse width.
  - By changing the pulse width of the PWM waveform, we can control the output value.

PWM Signal Examples

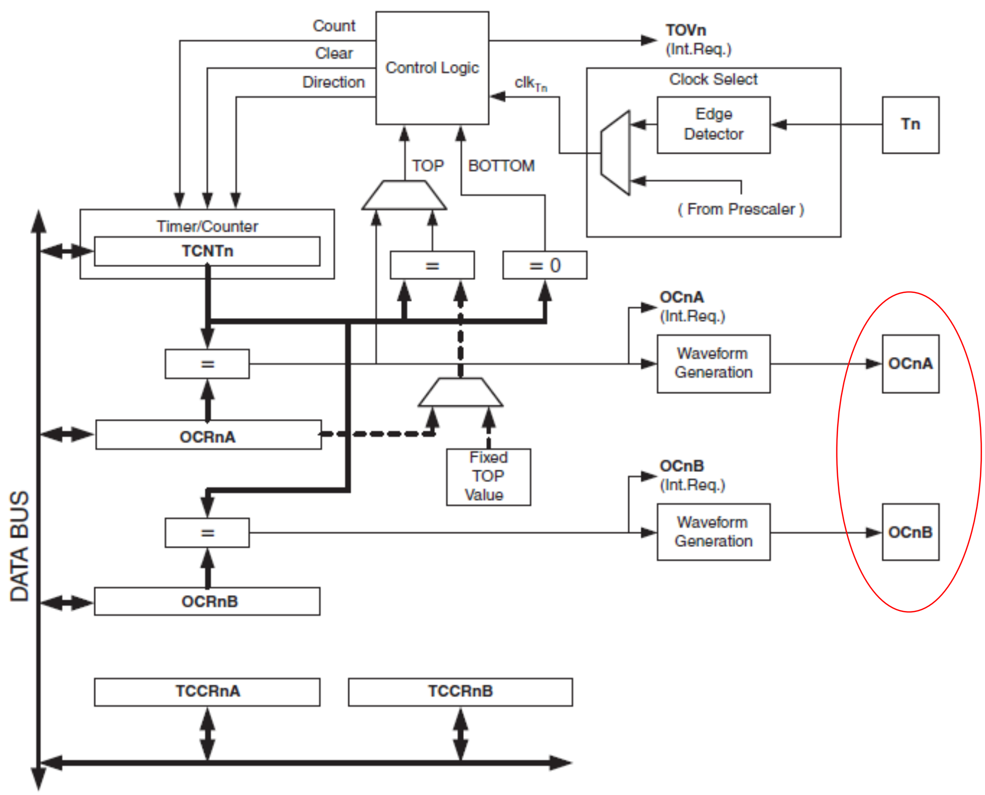


- Duty cycle: (pulse width)/period

PWM Generation in AVR

- PWM can be obtained through the provided timers.

Recall: Timer0



Configuration for PWM

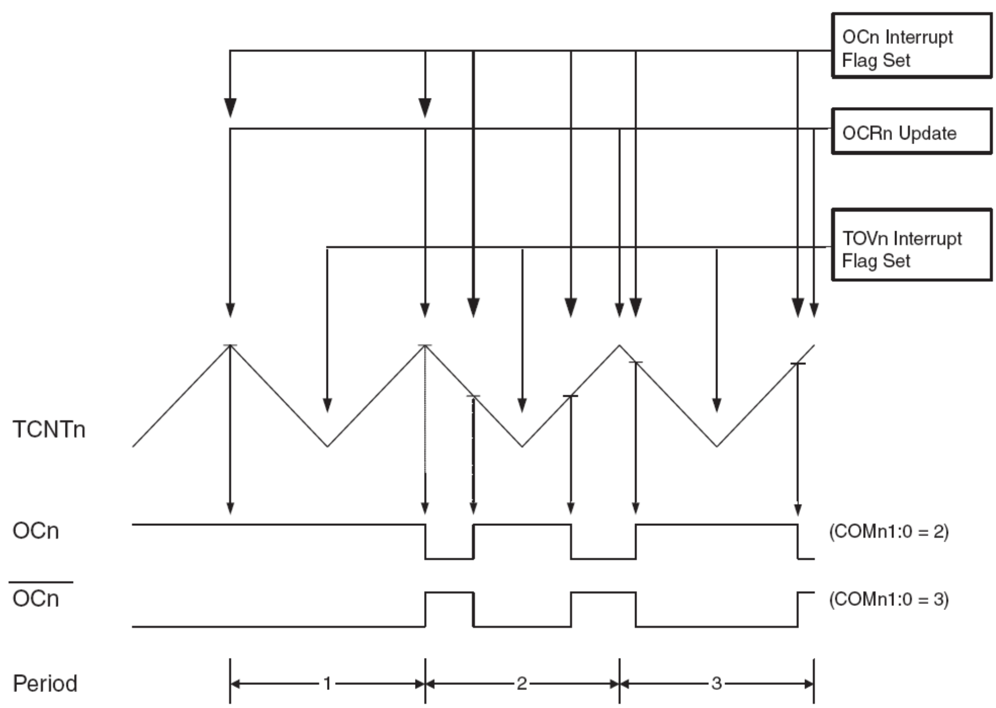
- TCCR0A/B

Bit	7	6	5	4	3	2	1	0	
0x24 (0x44)	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	TCCR0A
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W	

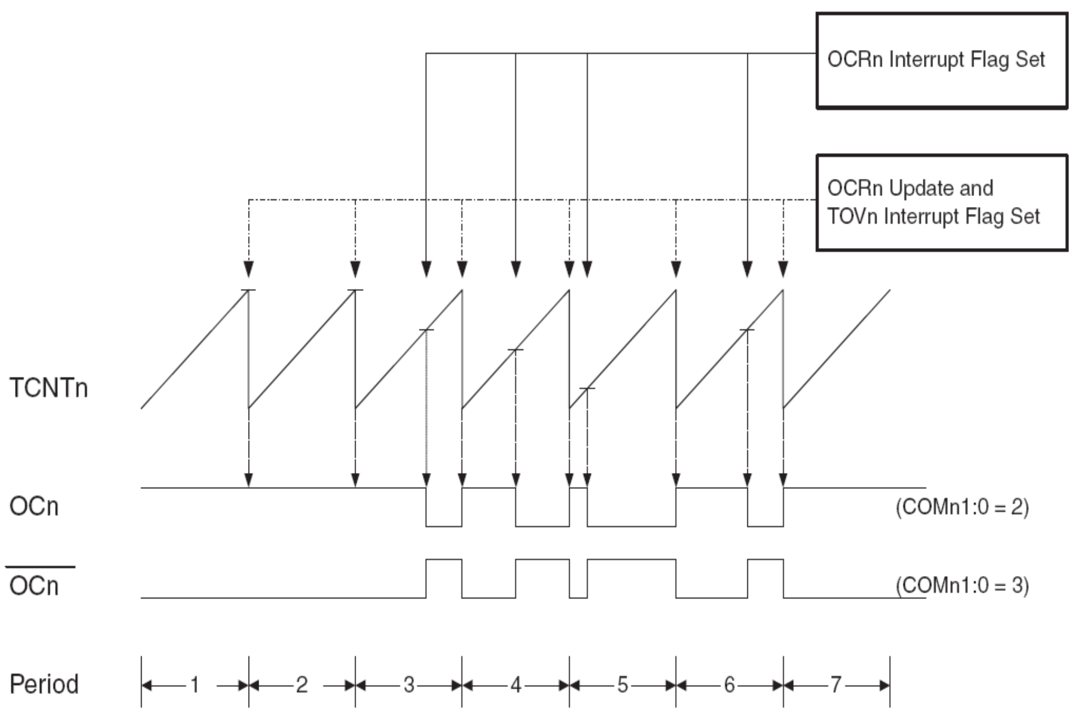
Bit	7	6	5	4	3	2	1	0	
0x25 (0x45)	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	TCCR0B
Read/Write	W	W	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Mode	WGM2	WGM1	WGM0	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on[(1)(2)]
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	TOP	MAX
4	1	0	0	Reserved	–	–	–
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	–	–	–
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP

Phase Correct PWM

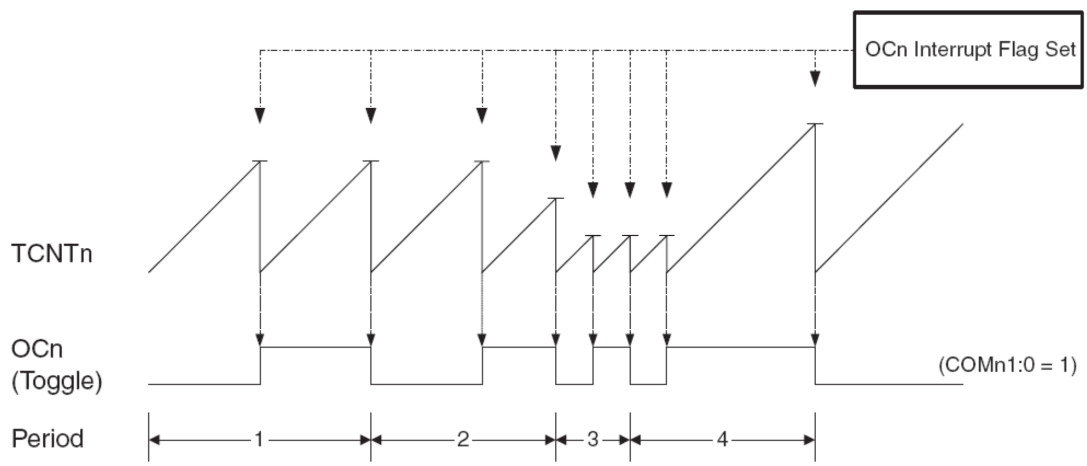


Fast PWM*


OCRn Interrupt Flag Set
OCRn Update and
TOVn Interrupt Flag Set
TCNTn
OCn
$\overline{\text{OCn}}$
(COMn1:0 = 2)
(COMn1:0 = 3)
Period
1
2
3
4
5
6
7

CTC*

- Clear Timer on Compare Match



Example

- Generate a PWM waveform.

Example (solution)

- Use Timer5
  - Set OC5A as output
  - Set the Timer5 operation mode as Phase Correct PWM mode
  - Set the timer clock

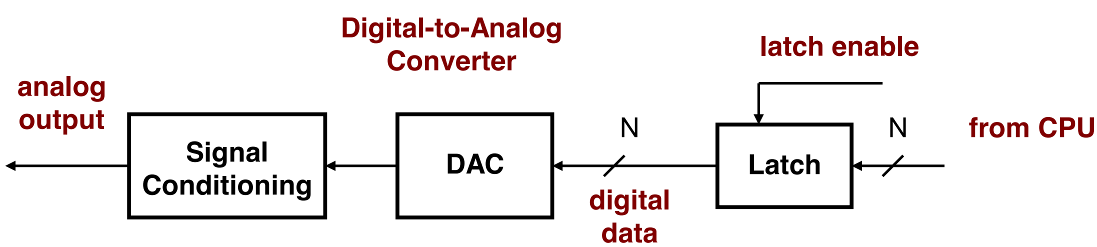
Example Code

```
.include "m2560def.inc"
.def temp=r16

        ldi temp, 0b00001000
        sts DDRL, temp              ; Bit 3 will function as OC5A.

        clr temp ldi                ; the value controls the PWM duty cycle
        sts OCR5AH, temp
        ldi temp, 0x4A
        sts OCR5AL, temp
                                    ; Set Timer5 to Phase Correct PWM mode.
        ldi temp, (1 << CS50)
        sts TCCR5B, temp
        ldi temp, (1<< WGM50)|(1<<COM5A1)
        sts TCCR5A, temp
end:    rjmp end
```

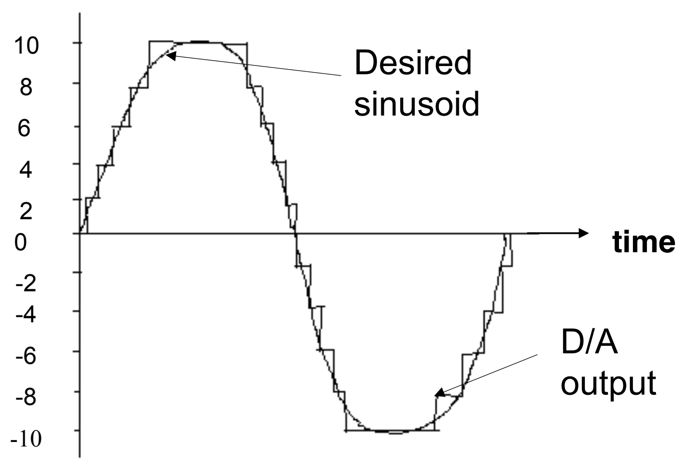
Digital-to-Analog Conversion



Digital-to-Analog Conversion (cont.)

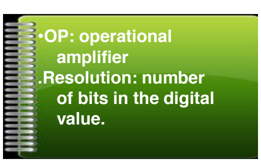
- A parallel output interface connects the Digital-to-Analog converter (**DAC**) to CPU.
- The latches may be part of the DAC or the output interface.
- Digital value is converted into continuous value.
- A signal conditioning block may be used as a filter to smooth the quantized nature of the output.
  - The signal conditioning block also provides isolation, buffering and voltage amplification if needed.

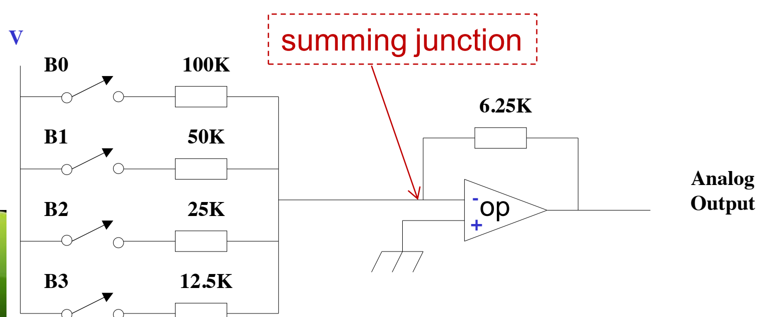
Quantized D/A Output



Binary-Weighted D/A Converter

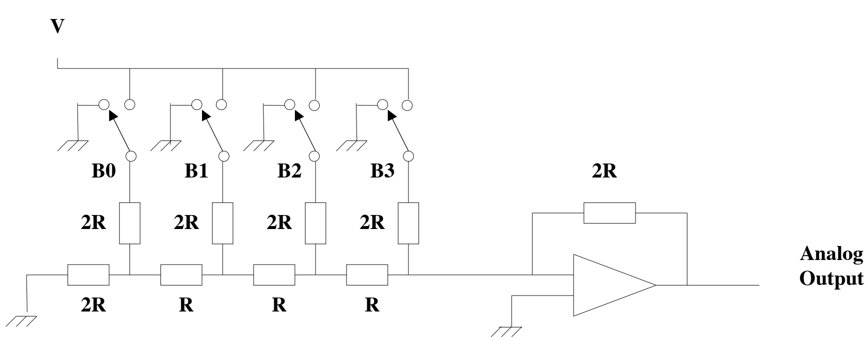
- As a switch for a bit is closed, a *weighted current* is supplied to the *summing junction* of the amplifier (OP).
- For high-resolution D/A converters, the binary-weighted type must have a wide range of resistors. This may affect the output accuracy.





R-2R Ladder D/A Converter

- As a switch changes from the grounded position to the reference position, a binary-weighted current is supplied to the summing junction.
- For high-resolution D/A converters, a wide range of resistors are not required, providing better accuracy for the output.



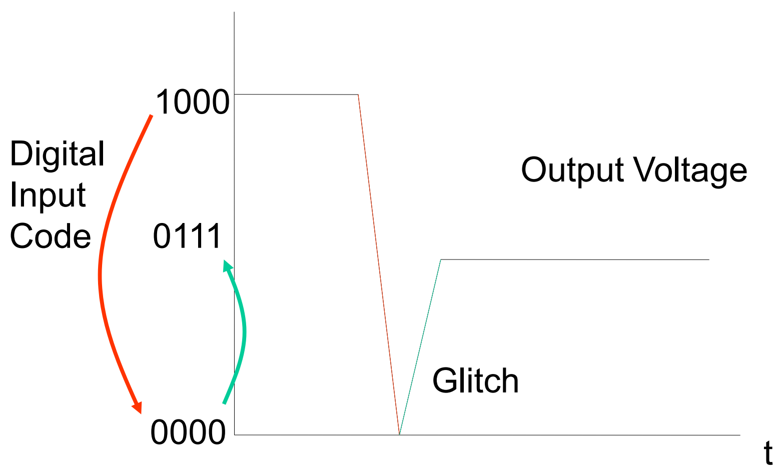
D/A Converter Specifications

- Resolution and linearity
  - The resolution is determined by the number of bits and is given as the output voltage corresponding to the smallest digital step, i.e. 1 LSB.
  - The linearity shows how closely the output voltage to the idea values (a straight line drawn through zero and full-scale).
- Settling Time
  - The time taken for the output voltage to settle to within a specified error band, usually ± ½ LSB.

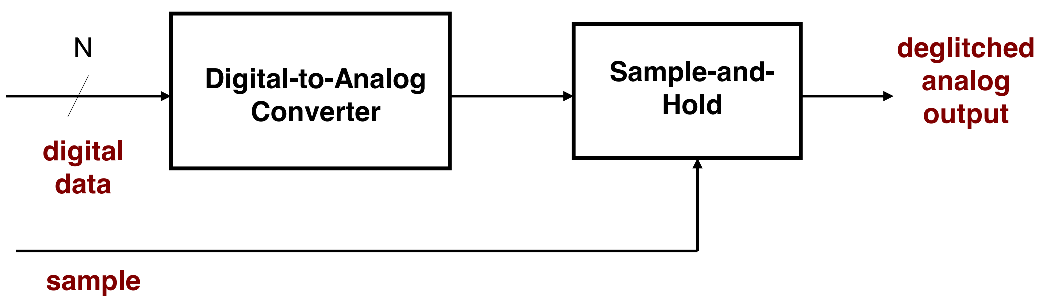
D/A Converter Specifications (cont.)

- Glitches
  - A glitch is caused by asymmetrical switching in the D/A switches. If a switch changes from 1 to 0 faster than from 0 to 1, a glitch may occur.
    - Consider changing the output code of a 8-bit D/A from 10000000 to 01111111 in the next slide.
  - The D/A converter glitch can be eliminated by using a sample-and-hold.

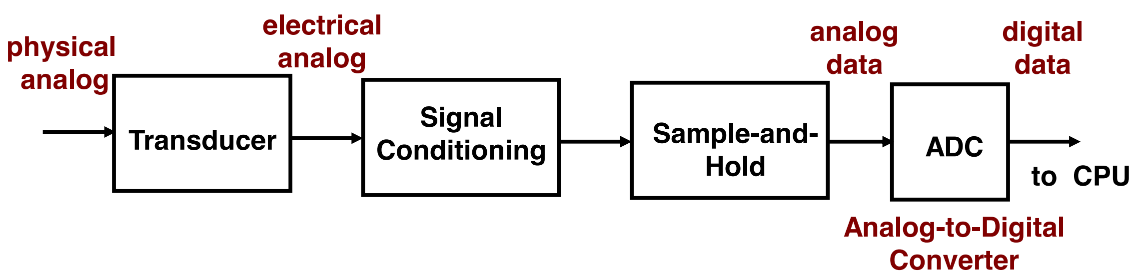
D/A Output Glitch



Deglitched D/A



A/D Conversion



Data Acquisition and Conversion

- A transducer converts physical values to electrical signals, either voltages or currents.
- Signal conditioner performs the following tasks:
  - Isolation and buffering:
    - The input to ADC may need to be protected from dangerous voltages such as static charges or reversed polarity voltages.
  - Amplification:
    - To ensure the full-scale signal from the analog results in a full-scale signal to ADC.
  - Bandwidth limiting:
    - The signal conditioning provides a low-pass filter to limit the range of frequencies that can be digitized.

Data Acquisition and Conversion (cont.)

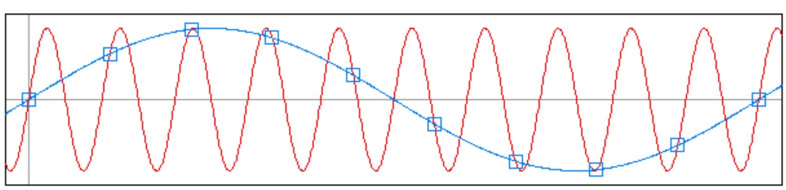
- The sample-and-hold circuit samples the signal and holds it steady for A/D conversion.
  – What is the sample frequency?
- The ADC converts the sampled signal to digital data
  – The output of ADC connected to CPU through three-state buffers.

Shannon's Sampling Theorem and Aliasing

- To preserve the full information in the signal, it is necessary to sample *at least twice the maximum frequency of the signal*.
  - This minimum sampling frequency is known as the *Nyquist rate*.
  - A signal can be exactly reproduced if it is sampled at a frequency greater than or equal to its Nyquist rate.
- If the sampling frequency is less than Nyquist rate, the waveform is said to be undersampled.

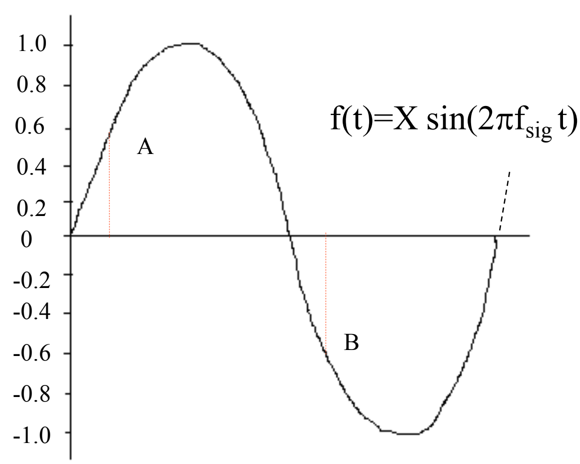
Shannon's Sampling Theorem and Aliasing (cont.)

- Undersampled signal, when converted back into a continuous time signal, will exhibit a phenomenon called *aliasing*.
  - Aliasing: the presence of unwanted components in the reconstructed signal. These components were not present when the original signal was sampled.



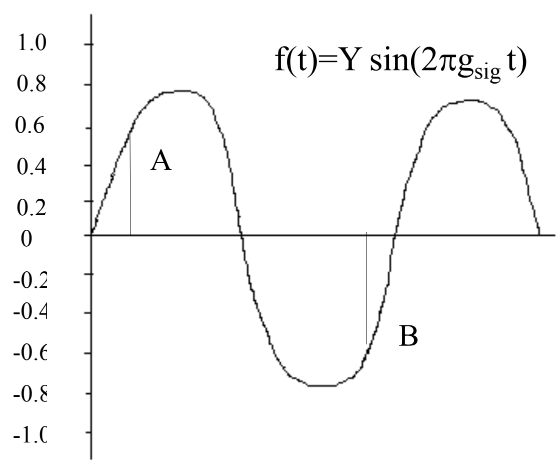
Sample Examples

- Sampled at twice of the signal frequency.

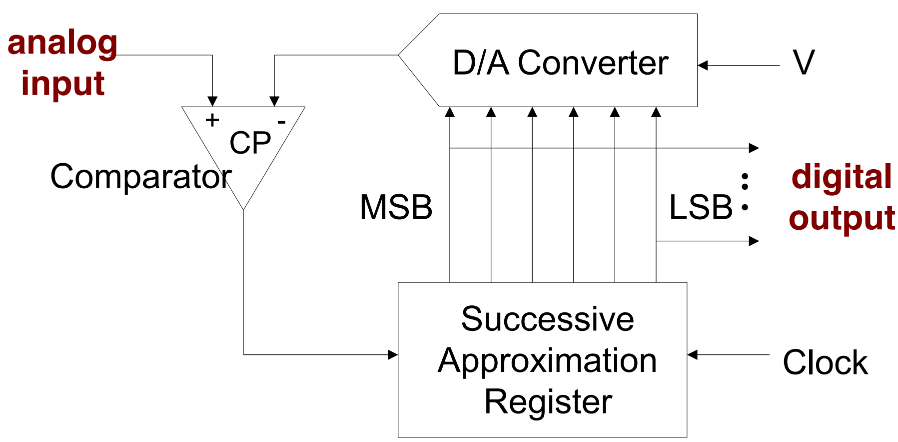


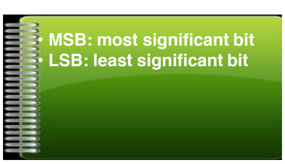
Sample Examples

- Undersampled, with sample frequency less than twice of the signal frequency



Successive Approximation Converter

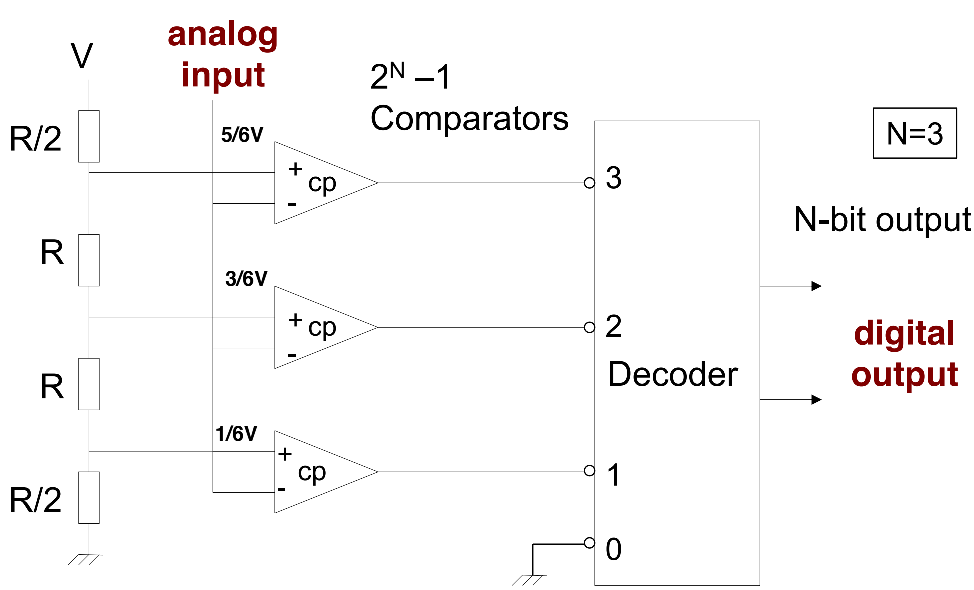




Successive Approximation A/D Converter

- Each bit in the *successive approximation register* is tested, starting at the most significant bit and working toward the least significant bit.
  - As each bit is set, the output of the D/A converter is compared (by the comparator) with the analog input.
  - If the D/A output is lower than the input signal, the bit remains set and the next bit is tried.
- For an N-bit output, such a bit test needs to be performed N times.

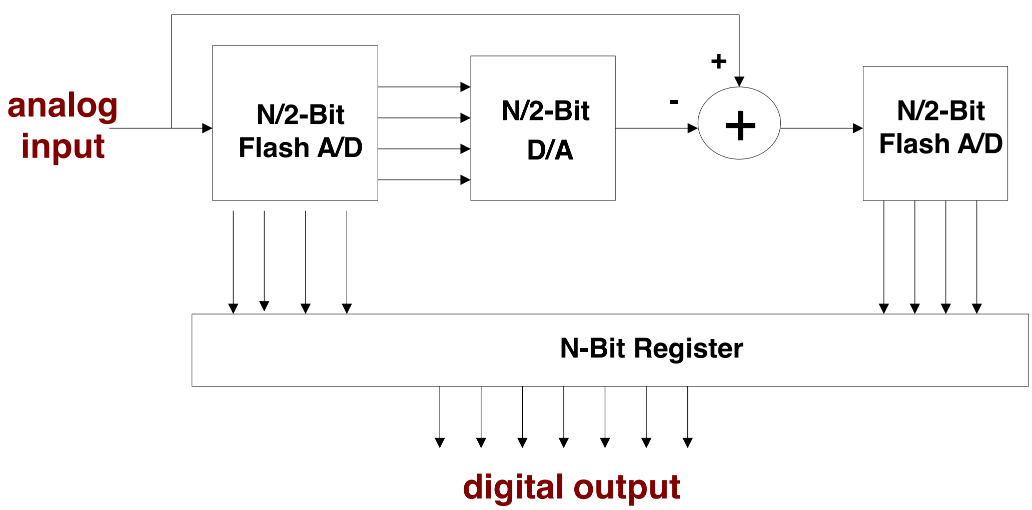
Parallel A/D Converter



Parallel A/D Converter

- For an N-bit output, the ADC consists of
  - an array of 2^N-1 comparators
    - produces a (2^N-1)-bit code
  - a 2^N-to-N decoder
    - converts 2^N-bit input code to N-bit binary value
- The design is
  - fast
    - hence called flash ADC
  - but more costly than the successive approximation ADC

Two-Stage Parallel A/D Converter*



Two-Stage Parallel A/D Converter*

- The input signal is converted in two steps:
  - First, a coarse estimate is found by the first parallel A/D converter. This digital value is sent to the D/A converter and the adder, where it is subtracted from the original analog value.
  - Next, the difference is converted by the second parallel converter and the result combined with that from the first ADC gives the digitized value.
- The ADC has nearly the performance of the parallel converter but without the need of $2^N - 1$ comparators.
- It offers high resolution and high-speed conversion for applications like video signal processing.

A/D Converter Specifications

- Conversion time
  - The time required to complete a conversion of the input signal.
  - Determines the upper signal frequency limit that can be sampled without aliasing.

$$f_{MAX}=1/(2^*\text{conversion time}) \qquad (1)$$

- Resolution
  - The number of bits in the converter gives the resolution and thus the smallest analog input signal for which the converter will produce a digital code.
  - .

A/D Converter Specifications (Cont.)

- Accuracy
  - Relates to the smallest signal (or noise) to the measured signal.
  - Given as a percent, and
  - Describes how close the measurement is to the actual value.
- Linearity
  - The derivation in output codes from the real value (a straight line drawn through zero and full-scale).

A/D Converter Specifications (Cont.)

- Aperture time.
  - The time that the A/D converter is “looking” at the input signal.
  - It is usually equal to the conversion time.

Announcement

- Project is available on the course website.

Reading Material

- Chapter 13: Analog Input and Output. Microcontrollers and Microcomputers by Fredrick M. Cady.
- Timers/Counters. AVR Mega2560 Data Sheet.
  - PWM

Homework

1. Design to use PWM to drive the motor on the lab board to spin.

Homework

2. The A/D converter conversion time is 100 us. What is the maximum frequency of a signal that can be digitalized without aliasing occurring?