Minimal 74-Series Computer

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April 8, 2021

Contents

1 Purpose 1
1.1 Functions And Instructions 1
1.2 Flags and Registers 1

2 Component Selection 1

List of Figures

1 Purpose

The purpose of this project is to design and implement a VHDL and physical minimal computer for use as a display demonstration. The design is created and validated inside of Vivado 2020 with 74-series logic that was manually modeled.

1.1 Functions And Instructions

1.2 Flags and Registers

Operational flags are shown in Table 1, all flags are utilized for operational purposes in conditional operations inside the CPU.

2 Component Selection

This computer will be built primarily out of 74 series logic due to the wide availablity and versatility of the series. This section details components selected for the final design of this computer.

- CD74HCT283 - standard 4-bit adder IC selected for use in the ALU

Flag Register	Bit in flags register	Description
C	0	carry flag
Z	1	zero flag
L	2	A less than B flag
G	3	A greater than B flag
D	4	Done

Table 1: Table of bits in flag register

- SN74HCT574 - octal edge-triggered D-type flipflop with 3 state output. General purpose register memory, will be used in registers A, B, PC, and PD
- AT28C64B - Parallel EEPROM (8K x 8). General purpose program memory, will be where the program and varaibles are stored
- SN74HCT08 - quadruple 2 input AND gate IC, selected for use in the ALU
- SN74HCT32 - Quadruple 2-input OR Gate IC, selected for use in the ALU
- 74HCT163 - Presettable synchronous 4-bit binary counter; synchronous reset. Primary program counter
- 74HCT85 - 4-bit magnitude comparator. utilized in CPU to greater than, less than, and equals flag registers
- 74HCT245 - Octal bus tranciever with 3-state outputs. used to switch a device onto or off of the system bus
- 74HCT04 - hex inverter
- 74HCT138 - 3 to 8 decoder with inverting outputs
- 74HCT238 - 3 to 8 decoder with non-inverting outputs