SONY

Diagonal 6.45 mm (Type 1/2.8) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

IMX662-AAQR-C

STARVIS 2

Description

The IMX662-AAQR-C is a diagonal 6.45 mm (Type 1/2.8) CMOS active pixel type solid-state image sensor with a square pixel array and 2.40 M effective pixels. This chip operates with analog 3.3 V, digital 1.1 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Application: Security cameras)

Features

- ◆ CMOS active pixel type dots
- ◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆ Input frequency: 24 MHz / 27 MHz / 37.125 MHz / 72 MHz / 74.25 MHz
- ◆ Number of recommended recording pixels: 1920 (H) × 1080 (V) approx. 2.07M pixel
- ◆ Readout mode
  - All-pixel scan mode
  - Horizontal / Vertical 2/2-line binning mode
  - Window cropping mode
  - Horizontal / Vertical direction - Normal / Inverted readout mode
- ◆ Readout rate
  - Maximum frame rate in
  - All-pixel scan mode: 12 bit: 60 frame/s, 10 bit: 90 frame/s
- ◆ High dynamic range (HDR) function
  - Digital overlap HDR
  - Clear HDR
- ◆ Synchronizing sensors function
- ◆ Variable-speed shutter function (resolution 1H unit)
- ◆ 10-bit / 12-bit A/D converter
- ◆ Conversion gain switching (HCG Mode / LCG Mode)
- ◆ CDS / PGA function
  - 0 dB to 30 dB : Analog Gain 30 dB (step pitch 0.3 dB)
  - 30.3 dB to 72 dB : Analog Gain 30 dB + Digital Gain 0.3 dB to 42 dB (step pitch 0.3 dB)
- ◆ Supports I/O
  - CSI-2 serial data output (2 Lane / 4 Lane) RAW10 / RAW12 output

E21Y10

Device Structure

- ◆ CMOS image sensor
- ◆ Image size
  Diagonal 6.45 mm (Type 1/2.8) approx. 2.40 M pixels, All pixels
- ◆ Total number of pixels
  2014 (H) × 1196 (V) approx. 2.40 M pixels
- ◆ Number of effective pixels
  1965 (H) × 1113 (V) approx. 2.18 M pixels
- ◆ Number of active pixels
  1937 (H) × 1097 (V) approx. 2.12 M pixels
- ◆ Number of recommended recording pixels
  1920 (H) × 1080 (V) approx. 2.07 M pixels
- ◆ Unit cell size
  2.9 µm (H) × 2.9 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 20 pixels, rear 0 pixels
- ◆ Dummy
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 0 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog: 3.3 V)	AV_{DD}	-0.3	4.0	V	
Supply voltage (interface: 1.8 V)	OV_{DD}	-0.3	3.3	V	
Supply voltage (digital: 1.1 V)	DV_{DD}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	85	˚C	
Storage temperature	Tstg	-40	85	˚C	

Application Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog: 3.3 V)	AV_{DD}	3.20	3.30	3.40	V
Supply voltage (interface: 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital: 1.1 V)	DV_{DD}	1.00	1.10	1.20	V
Performance guarantee temperature	Tspec	-10	—	60	˚C

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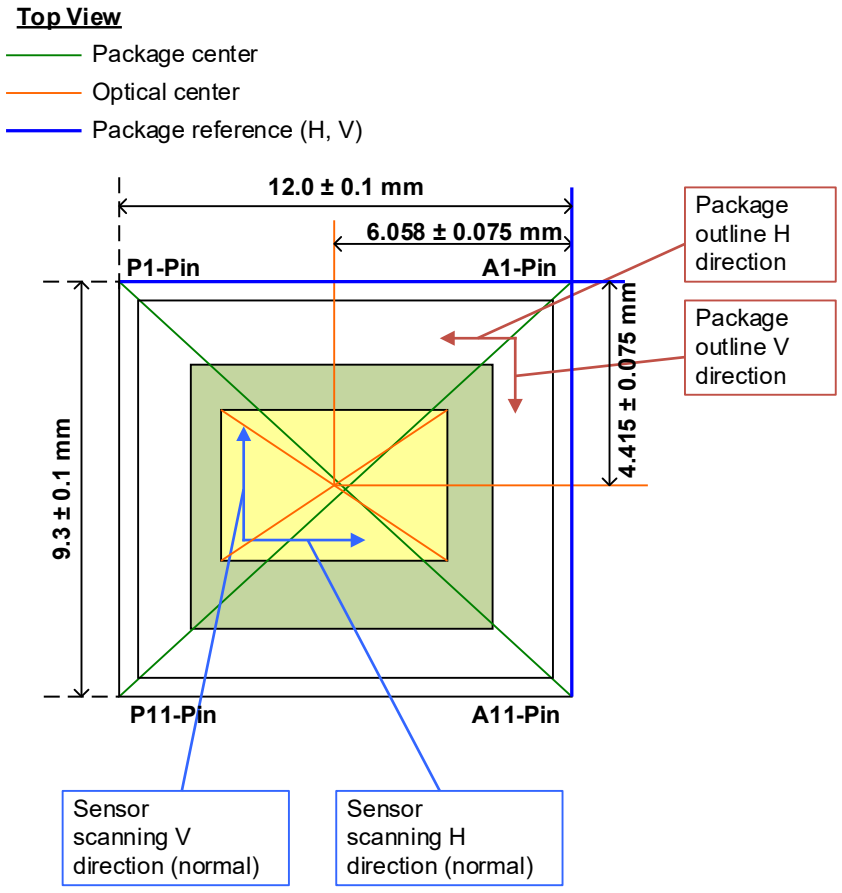
General-0.0.9

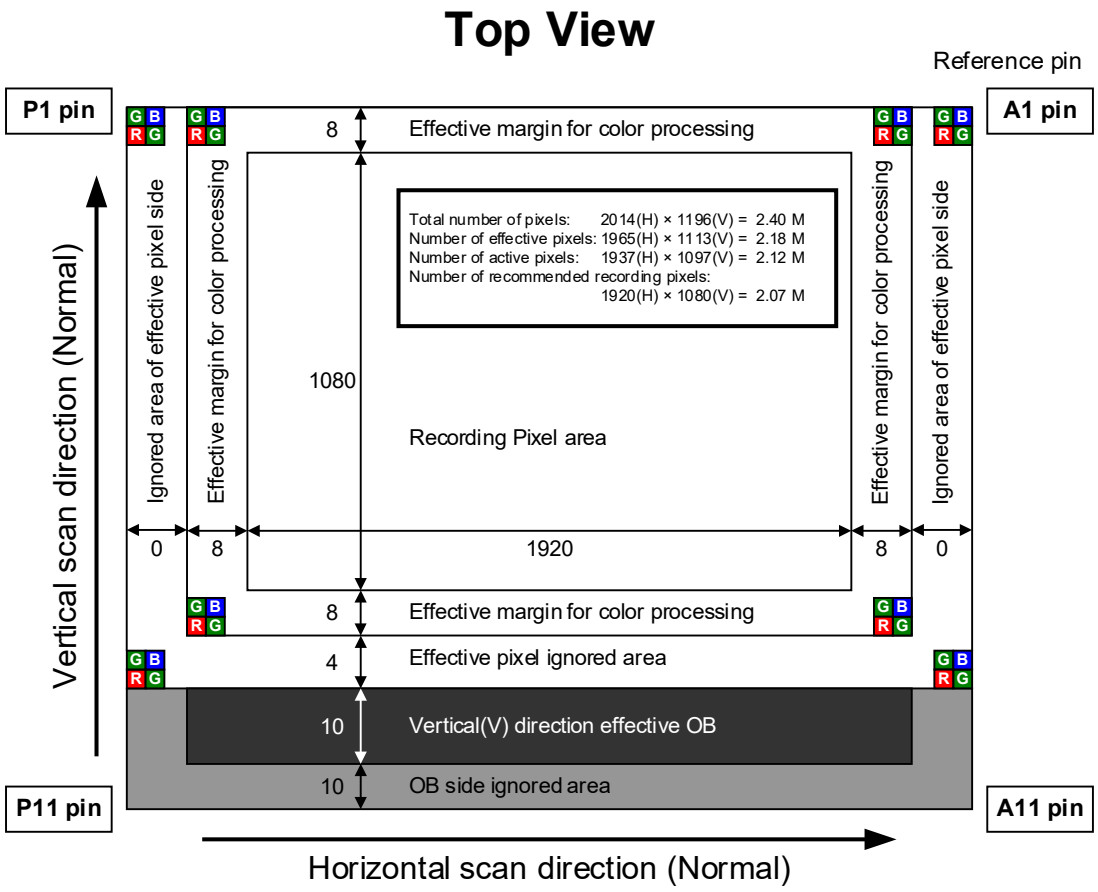
Contents

Optical Center



Optical Center

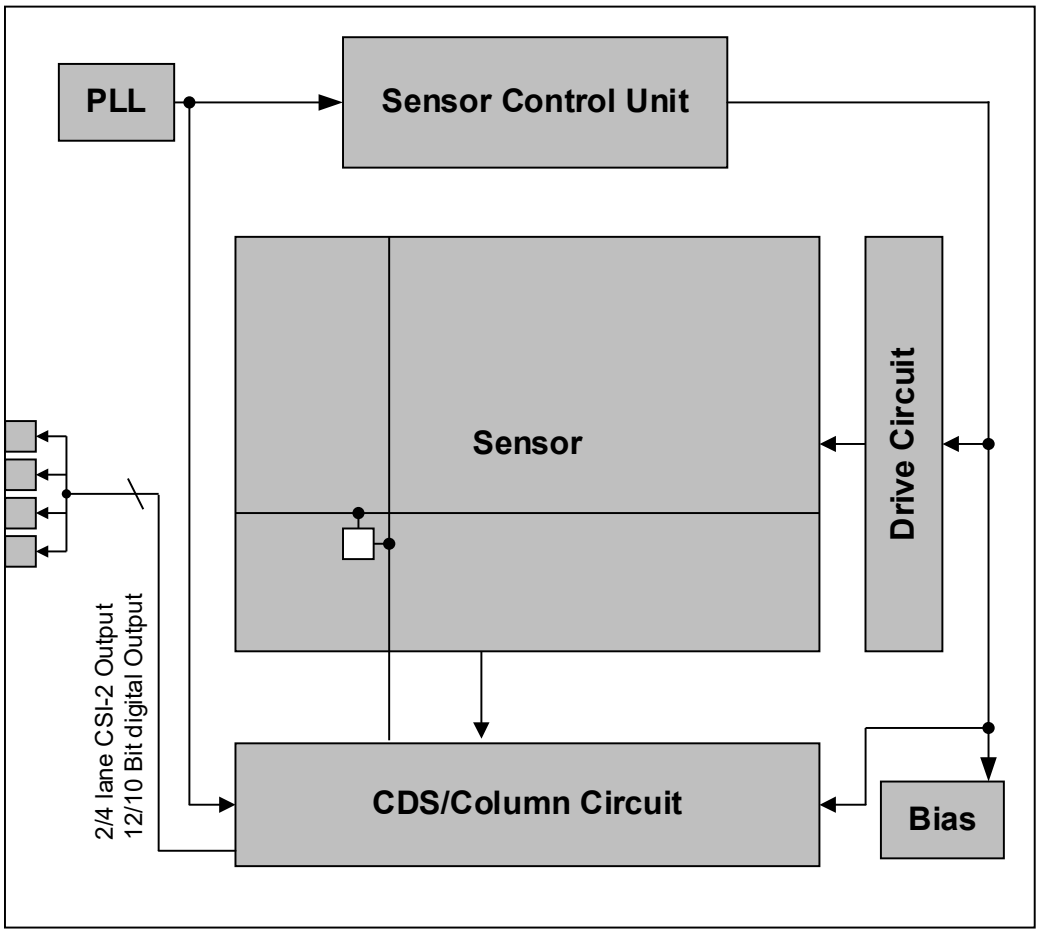
Pixel Arrangement



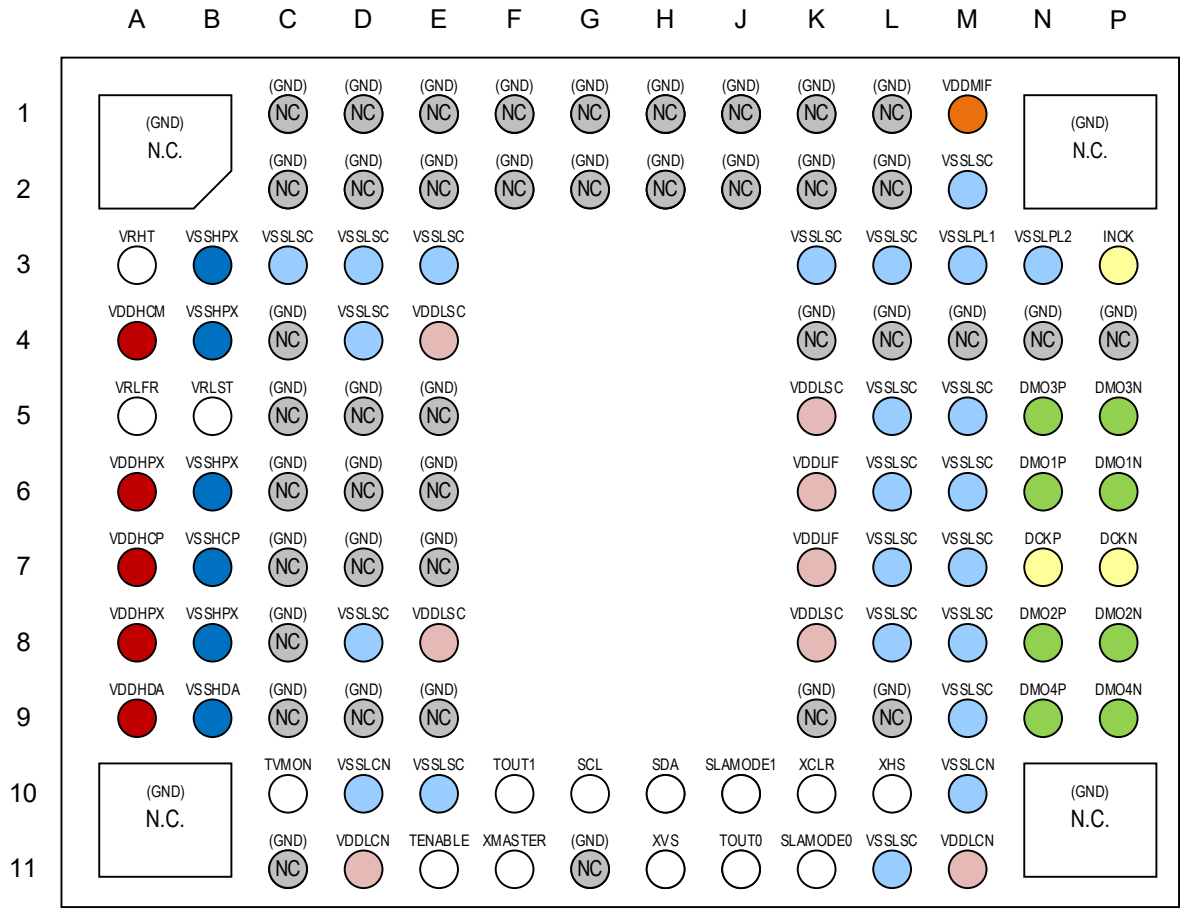
* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.
The last Effective line and column are not read-out.

Pixel Arrangement

Block Diagram and Pin Configuration



Block Diagram



*The N.C. pin with (GND) can be connected to GND.

Pin Configuration

Pin Description

No.	Pin No	I/O	Analog / Digital	Symbol	Description
1	A1	–	–	N.C.	GND connectable
2	A3	O	A	VRHT	Capacitor connection
3	A4	Power	A	VDDHCM	3.3 V power supply
4	A5	O	A	VRLFR	Capacitor connection
5	A6	Power	A	VDDHPX	3.3 V power supply
6	A7	Power	A	VDDHCP	3.3 V power supply
7	A8	Power	A	VDDHPX	3.3 V power supply
8	A9	Power	A	VDDHDA	3.3 V power supply
9	A11	–	–	N.C.	GND connectable
10	B3	GND	A	VSSHPX	3.3 V GND
11	B4	GND	A	VSSHPX	3.3 V GND
12	B5	O	A	VRLST	Capacitor connection
13	B6	GND	A	VSSHPX	3.3 V GND
14	B7	GND	A	VSSHCP	3.3 V GND
15	B8	GND	A	VSSHPX	3.3 V GND
16	B9	GND	A	VSSHDA	3.3 V GND
17	C1	–	–	N.C.	GND connectable
18	C2	–	–	N.C.	GND connectable
19	C3	GND	D	VSSLSC	1.1 V GND
20	C4	–	–	N.C.	GND connectable
21	C5	–	–	N.C.	GND connectable
22	C6	–	–	N.C.	GND connectable
23	C7	–	–	N.C.	GND connectable
24	C8	–	–	N.C.	GND connectable
25	C9	–	–	N.C.	GND connectable
26	C10	O	A	TVMON1	TEST output pin, OPEN
27	C11	–	–	N.C.	GND connectable
28	D1	–	–	N.C.	GND connectable
29	D2	–	–	N.C.	GND connectable
30	D3	GND	D	VSSLSC	1.1 V GND
31	D4	GND	D	VSSLSC	1.1 V GND
32	D5	–	–	N.C.	GND connectable
33	D6	–	–	N.C.	GND connectable
34	D7	–	–	N.C.	GND connectable
35	D8	GND	D	VSSLSC	1.1 V GND
36	D9	–	–	N.C.	GND connectable
37	D10	GND	D	VSSLCN	1.1 V GND
38	D11	Power	D	VDDLCN	1.1 V power supply
39	E1	–	–	N.C.	GND connectable
40	E2	–	–	N.C.	GND connectable
41	E3	GND	D	VSSLSC	1.1 V GND
42	E4	Power	D	VDDLSC	1.1 V power supply
43	E5	–	–	N.C.	GND connectable
44	E6	–	–	N.C.	GND connectable
45	E7	–	–	N.C.	GND connectable
46	E8	Power	D	VDDLSC	1.1 V power supply

No.	Pin No	I/O	Analog / Digital	Symbol	Description
47	E9	–	–	N.C.	GND connectable
48	E10	GND	D	VSSLSC	1.1 V GND
49	E11	I	D	TENABLE	TEST enable, OPEN
50	F1	–	–	N.C.	GND connectable
51	F2	–	–	N.C.	GND connectable
52	F10	I/O	D	TOUT1	TEST output pin, OPEN
53	F11	I	D	XMASTER	Master / Slave selection Slave Mode: High Master Mode: Low
54	G1	–	–	N.C.	GND connectable
55	G2	–	–	N.C.	GND connectable
56	G10	I/O	D	SCL	Serial clock input
57	G11	–	–	N.C.	GND connectable
58	H1	–	–	N.C.	GND connectable
59	H2	–	–	N.C.	GND connectable
60	H10	I/O	D	SDA	Serial data communication
61	H11	I/O	D	XVS	Vertical sync signal
62	J1	–	–	N.C.	GND connectable
63	J2	–	–	N.C.	GND connectable
64	J10	I	D	SLAMODE1	Reference pin, Select slave address
65	J11	I/O	D	TOUT0	TEST output pin, OPEN
66	K1	–	–	N.C.	GND connectable
67	K2	–	–	N.C.	GND connectable
68	K3	GND	D	VSSLSC	1.1 V GND
69	K4	–	–	N.C.	GND connectable
70	K5	Power	D	VDDLSC	1.1 V power supply
71	K6	Power	D	VDDLIF	1.1 V power supply
72	K7	Power	D	VDDLIF	1.1 V power supply
73	K8	Power	D	VDDLSC	1.1 V power supply
74	K9	–	–	N.C.	GND connectable
75	K10	I	D	XCLR	System clear
76	K11	I	D	SLAMODE0	Reference pin, Select slave address
77	L1	–	–	N.C.	GND connectable
78	L2	–	–	N.C.	GND connectable
79	L3	GND	D	VSSLSC	1.1 V GND
80	L4	–	–	N.C.	GND connectable
81	L5	GND	D	VSSLSC	1.1 V GND
82	L6	GND	D	VSSLSC	1.1 V GND
83	L7	GND	D	VSSLSC	1.1 V GND
84	L8	GND	D	VSSLSC	1.1 V GND
85	L9	–	–	N.C.	GND connectable
86	L10	I/O	D	XHS	Horizontal sync signal
87	L11	GND	D	VSSLSC	1.1 V GND
88	M1	Power	D	VDDMIF	1.8 V power supply
89	M2	GND	D	VSSLSC	1.1 V GND
90	M3	GND	A	VSSLPL1	1.1 V GND
91	M4	–	–	N.C.	GND connectable
92	M5	GND	D	VSSLSC	1.1 V GND
93	M6	GND	D	VSSLSC	1.1 V GND

No.	Pin No	I/O	Analog / Digital	Symbol	Description
94	M7	GND	D	VSSLSC	1.1 V GND
95	M8	GND	D	VSSLSC	1.1 V GND
96	M9	GND	D	VSSLSC	1.1 V GND
97	M10	GND	D	VSSLCN	1.1 V GND
98	M11	Power	D	VDDLCN	1.1 V power supply
99	N3	GND	A	VSSLPL2	1.1 V GND
100	N4	−	−	N.C.	GND connectable
101	N5	O	D	DMO3P	CSI-2 output
102	N6	O	D	DMO1P	CSI-2 output
103	N7	O	D	DCKP	CSI-2 clock output
104	N8	O	D	DMO2P	CSI-2 output
105	N9	O	D	DMO4P	CSI-2 output
106	P1	−	−	N.C.	GND connectable
107	P3	I	D	INCK	Master clock input
108	P4	−	−	N.C.	GND connectable
109	P5	O	D	DMO3N	CSI-2 output
110	P6	O	D	DMO1N	CSI-2 output
111	P7	O	D	DCKN	CSI-2 clock output
112	P8	O	D	DMO2N	CSI-2 output
113	P9	O	D	DMO4N	CSI-2 output
114	P11	−	−	N.C.	GND connectable

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDDHx	AV_{DD}		3.20	3.30	3.40	V
	Interface	VDDMx	OV_{DD}		1.70	1.80	1.90	V
	Digital	VDDLx	DV_{DD}		1.00	1.10	1.20	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SLAMODE0 SLAMODE1 SDA SCL	VIH	XVS / XHS Slave Mode	0.8 × OV_{DD}	—	—	V
			VIL		—	—	0.2 × OV_{DD}	V
Digital output voltage		XHS XVS TOUT0 TOUT1	VOH	XVS / XHS Master Mode	OV_{DD} – 0.2	—	—	V
			VOL		—	—	0.2	V

Current Consumption

Item	Symbol	Typ.	Max.	Unit
Operating current MIPI CSI-2 / 4Lane, 2376 Mbps 12bit 60 frame/s All-pixel mode	I_{AVDD}	44	60	mA
	I_{OVDD}	2	4	mA
	I_{DVDD}	117	150	mA
Standby current	I_{AVDD_STB}	—	0.9	mA
	I_{OVDD_STB}	—	0.2	mA
	I_{DVDD_STB}	—	10	mA

Operating current: (Typ.) Supply voltage 3.3 V / 1.8 V / 1.1 V, Tj = 25 ˚C, standard luminous intensity.
(Max.) Supply voltage 3.4 V / 1.9 V / 1.2 V, Tj = 60 ˚C, worst state of internal circuit operating current consumption,

Standby: (Max.) Supply voltage 3.4 V / 1.9 V / 1.2 V, Tj = 60 ˚C, INCK: 0 V, light-obstructed state.

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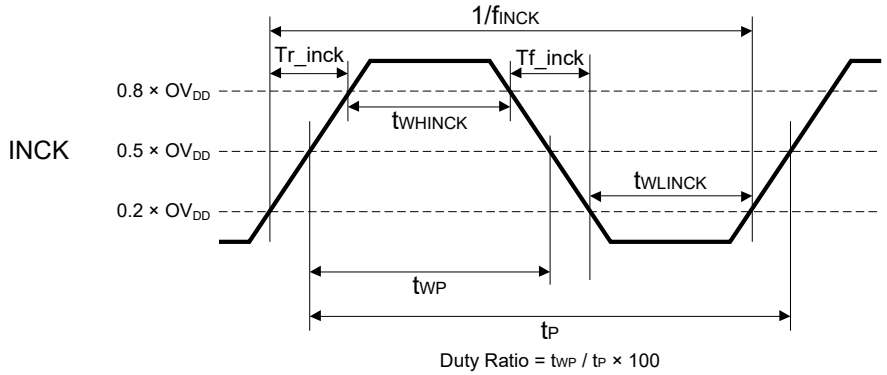
AC Characteristics

Master Clock Waveform (INCK)



INCK 37.125MHz, 72MHz, 74.25MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 72MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	
INCK clock duty	—	45	50	55	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %

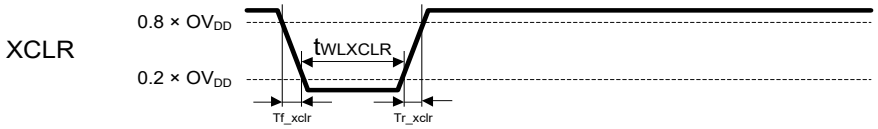
* The INCK fluctuation affects the frame rate.

INCK 24, 27MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	24	—	27	MHz	f_{INCK} = 24, 27MHz
INCK Low level pulse width	t_{WLINCK}	5	—	—	ns	
INCK High level pulse width	t_{WHINCK}	5	—	—	ns	
INCK clock duty	—	45	50	55	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %

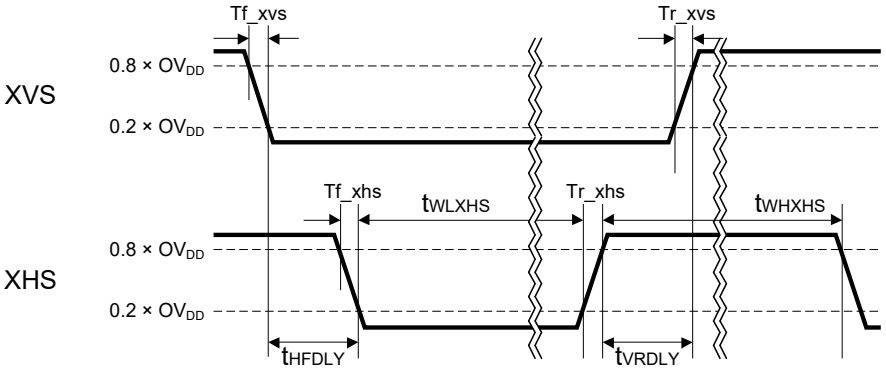
* The INCK fluctuation affects the frame rate.

System Clear (XCLR)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XCLR Low level pulse width	t_{WLXCLR}	100	—	—	ns	
XCLR Rise time	Tr_xclr	—	—	5	ns	20 % to 80 %
XCLR Fall time	Tf_xclr	—	—	5	ns	80 % to 20 %

XVS / XHS Input Characteristics in Slave Mode (XMASTER pin = High)



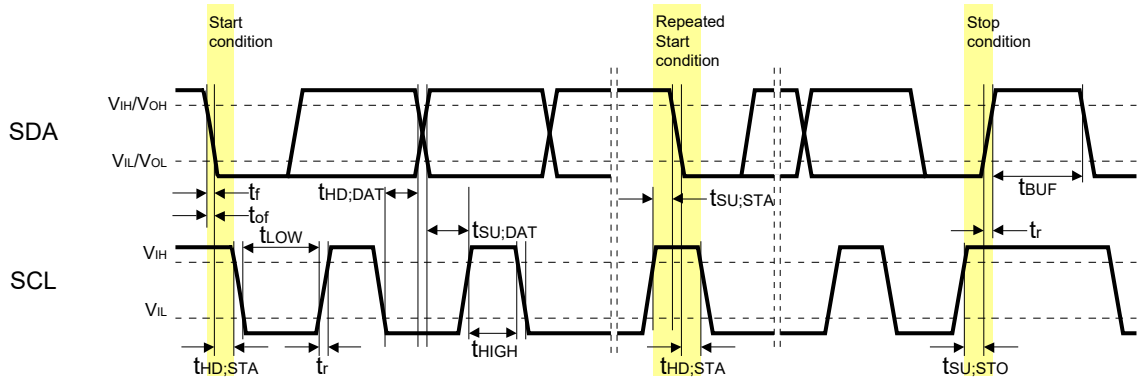
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	4 / f_{INCK}	—	—	ns	
XHS High level pulse width	t_{WHXHS}	4 / f_{INCK}	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	0	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	1 / f_{INCK}	—	—	ns	
XVS Rise time	Tr_xvs	—	—	5	ns	20 % to 80 %
XVS Fall time	Tf_xvs	—	—	5	ns	80 % to 20 %
XHS Rise time	Tr_xhs	—	—	5	ns	20 % to 80 %
XHS Fall time	Tf_xhs	—	—	5	ns	80 % to 20 %

XVS / XHS Output Characteristics in Master Mode (XMASTER pin = Low)

* XVS and XHS cannot be used for the sync signal to pixels.
  Be sure to detect sync code to detect the start of effective pixels in 1 line.
  For the output waveforms in master mode, see the item of “Slave Mode and Master Mode”

Serial Communication

I²C



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	–0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OVDD < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Input current	Ii	–10	—	10	μA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Input Capacitance for SCL / SDA	Ci	—	—	10	pF	

I²C AC Characteristics (Standard-mode, Fast-mode)

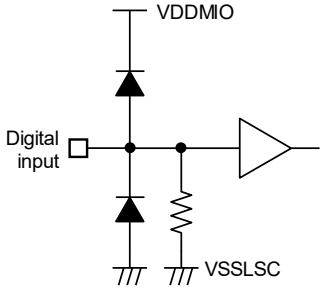
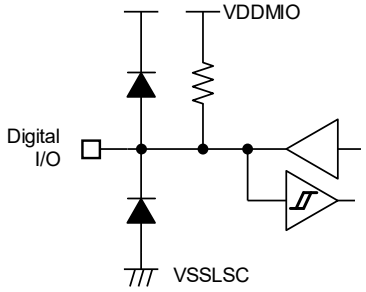
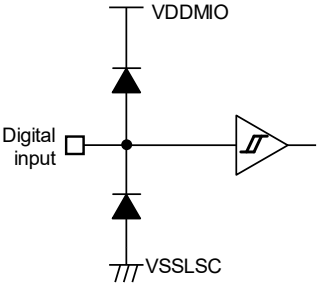
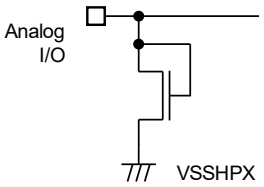
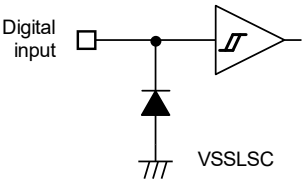
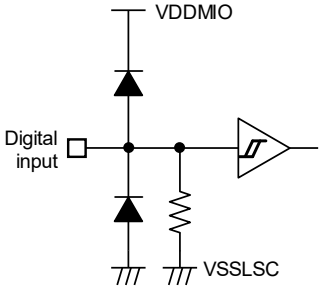
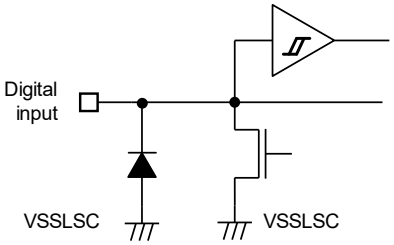
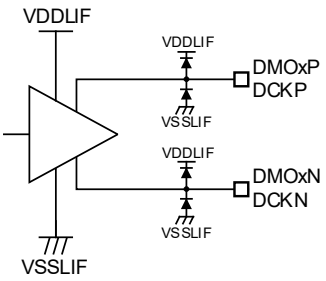
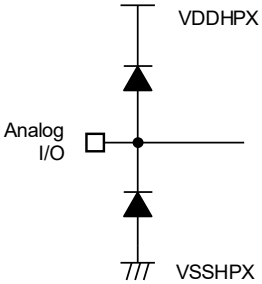
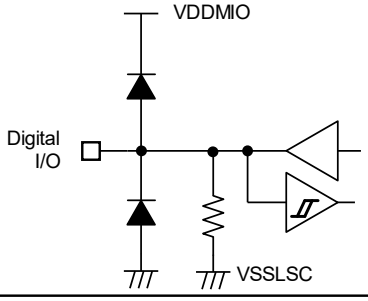
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	—	400	kHz	
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	μs	
Low period of the SCL clock	t_{LOW}	1.3	—	—	μs	
High period of the SCL clock	t_{HIGH}	0.6	—	—	μs	
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	μs	
Data hold time	$t_{HD;DAT}$	0	—	0.9	μs	
Data set-up time	$t_{SU;DAT}$	100	—	—	ns	
Rise time of both SDA and SCL signals	t_r	—	—	300	ns	
Fall time of both SDA and SCL signals	t_f	—	—	300	ns	
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	μs	
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	μs	
Output fall time	tof	—	—	250	ns	Load 10 pF to 400 pF, 0.7 × OV_{DD} to 0.3 × OV_{DD}

I²C AC Characteristics (Fast-mode Plus)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	—	1000	kHz	INCK ≥ 16 MHz
Hold time (Start Condition)	$t_{HD;STA}$	0.26	—	—	µs	
Low period of the SCL clock	t_{LOW}	0.5	—	—	µs	
High period of the SCL clock	t_{HIGH}	0.26	—	—	µs	
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.26	—	—	µs	
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs	
Data set-up time	$t_{SU;DAT}$	50	—	—	ns	
Rise time of both SDA and SCL signals	t_r	—	—	120	ns	
Fall time of both SDA and SCL signals	t_f	—	—	120	ns	
Set-up time (Stop Condition)	$t_{SU;STO}$	0.26	—	—	µs	
Bus free time between a STOP and START Condition	t_{BUF}	0.5	—	—	µs	
Output fall time	tof	—	—	120	ns	Load 10 pF to 400 pF, 0.7 × OV_{DD} to 0.3 × OV_{DD}

I/O Equivalent Circuit Diagram

□: External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
TENABLE		XVS XHS	
XMASTER		VRHT VRLFR VRLST	
XCLR INCK		SLAMODE0 SLAMODE1	
SDA SCL		DMOxP DMOxN DCKP DCKN	
TVMON		TOUT0 TOUT1	

Spectral Sensitivity Characteristics

(Characteristics in the wafer status)

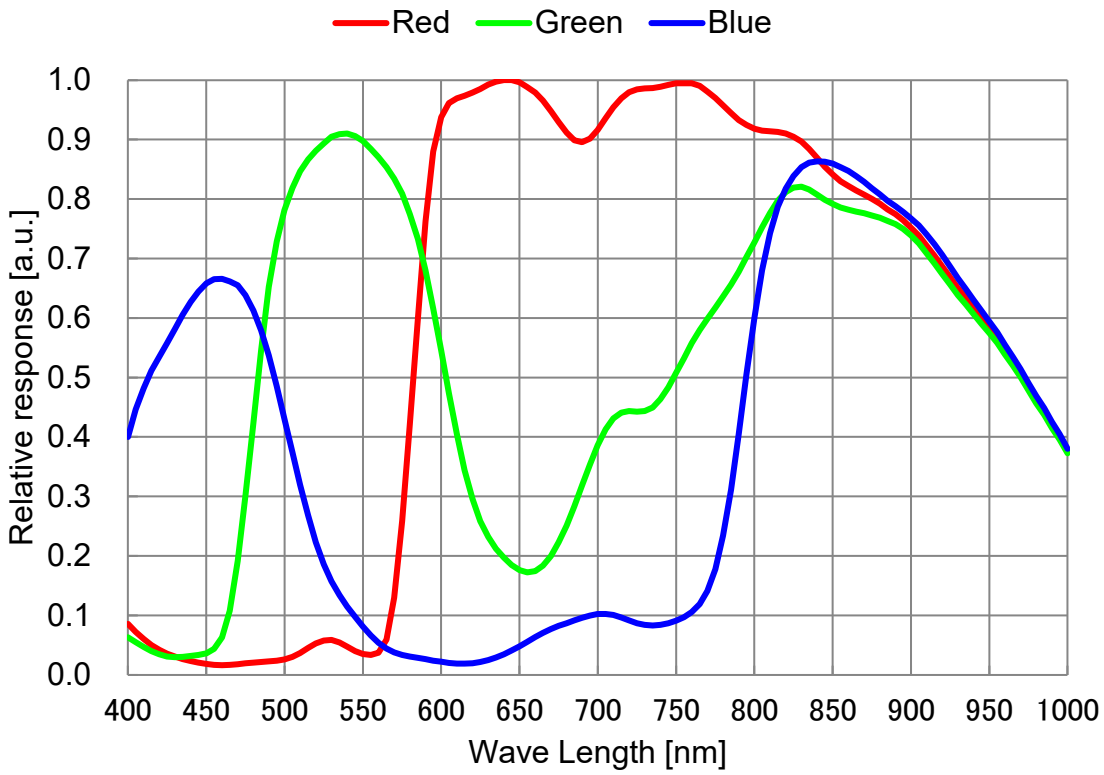


Image Sensor Characteristics

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.1 V, Tj = 60 ˚C, All-pixel mode, 12 bit 30 frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	15621 (4766)	18383 (5612)	—	Digit/lx/s (mV/lx/s)	1	F5.6 12 bit converted value HCG mode
			2690 (818)	3166 (966)	—	Digit/lx/s (mV/lx/s)		F5.6 12 bit converted value LCG mode
Sensitivity ratio	R / G	RG	0.52	—	0.67	—	2	—
	B / G	BG	0.28	—	0.43	—		
Saturation signal		Vsat	3895 (1188)	—	—	Digit (mV)	3	12 bit converted value LCG mode
			1204 (368)	—	—	Digit (mV)		12 bit converted value HCG mode
Video signal shading		SH	—	—	25	%	4	—
Vertical line		VL	—	—	90	μV	5	12 bit converted value LCG mode
Dark signal		Vdt	—	—	0.43 (0.13)	Digit (mV)	6	1/30 s storage 12 bit converted value LCG mode
Dark signal shading		ΔVdt	—	—	0.43 (0.13)	Digit (mV)	7	1/30 s storage 12 bit converted value LCG mode
Conversion efficiency ratio		Rcg	5.6	5.8	6.0	—	8	HCG mode / LCG mode

Note) 1. Converted value into mV using 1Digit = 0.3053 mV for 12-bit output and 1Digit = 1.221 mV for 10-bit output.

2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the seal glass.

3. The characteristics above apply to effective pixel area.

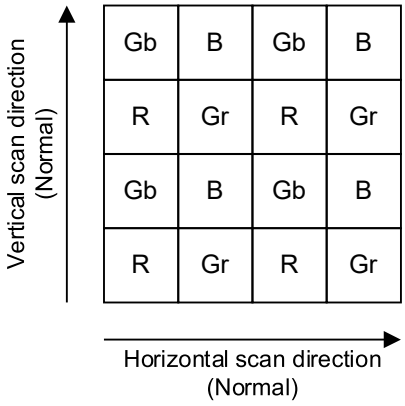
Image Sensor Characteristics Measurement Method

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.



Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Using a purple excitation LED light source with a color temperature of 2850 K, an IR cut filter CM700 (t = 1.0 mm) is placed between the LED light source and the sensor receiving surface to irradiate substantially parallel light.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM700 (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM700 (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I, and calculate using the illuminance (Ev) of the sensor receiving surface, the signal values (VGr, VGb, VR, VB) at the center of the screen, and the integration time (T).

   VG = (VGr + VGb) / 2
   S = VG / (Ev × T) [Digit / (lx･s)]

2. Sensitivity ratio
   By using the R and B signal outputs (VR, VB) obtained from the sensitivity measurement, substitute the values into the following formulas.

   RG = VR / VG
   BG = VB / VG

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 419 mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 419 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   SH = (Gmax – Gmin) / 419 × 100 [%]

5. Vertical Line
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, calculates each average output of Gr, Gb, R and B on respective columns. Calculates maximum value of difference with adjacent column on the same color (VL [μV]).

6. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

7. Dark signal shading
   After the measurement item 6, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

   ΔVdt = Vdmax – Vdmin [mV]

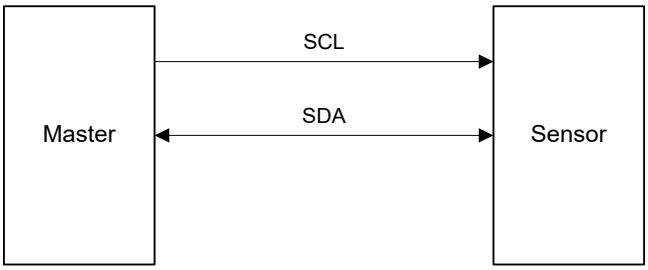
8. Conversion efficiency ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr And Gb and Gb signal outputs to 500 mV at the LCG mode, measure the average values of Gr and Gb signal output and calculate the ratio between HCG mode and LCG mode.

Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by I²C communication. See the Register Map for the addresses and setting values to be set.

Description of Setting Registers (I²C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions. Using SLAMODE0 and SLAMODE1 pins, SLAVE address can be changed.



Pin connection of serial communication

SLAVE Address

SLAMODE1 pin	SLAMODE0 pin	MSB							LSB
Low	Low	0	0	1	1	0	1	0	R / W
Low	High	0	0	1	0	0	0	0	R / W
High	Low	0	1	1	0	1	1	0	R / W
High	High	0	1	1	0	1	1	1	R / W

* R/W is data direction bit

R / W

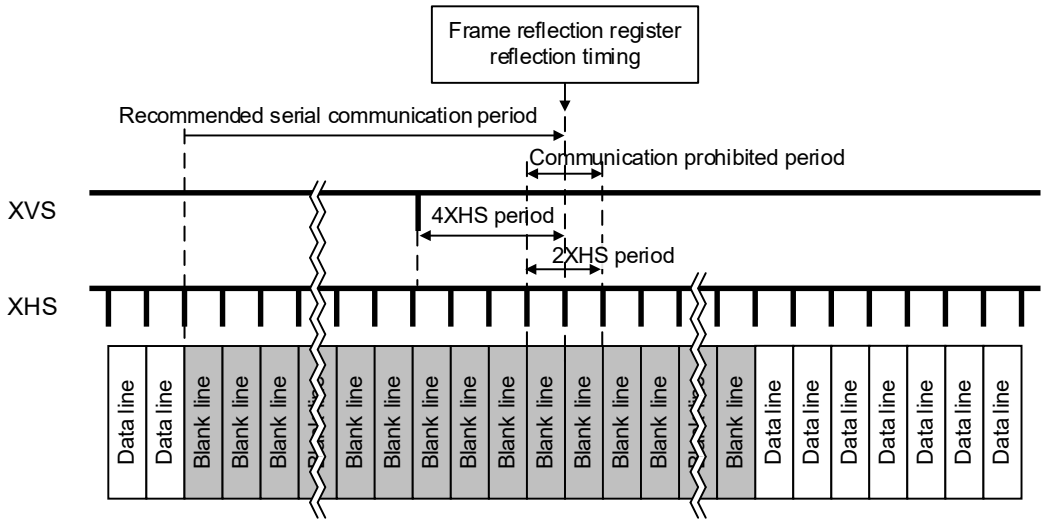
R / W bit	Data direction
0	Write (Master to Sensor)
1	Read (Sensor to Master)

I²C pin description

Symbol	Pin No.	Remarks
SCL	G10	I²C serial clock input
SDA	H10	I²C serial data communication

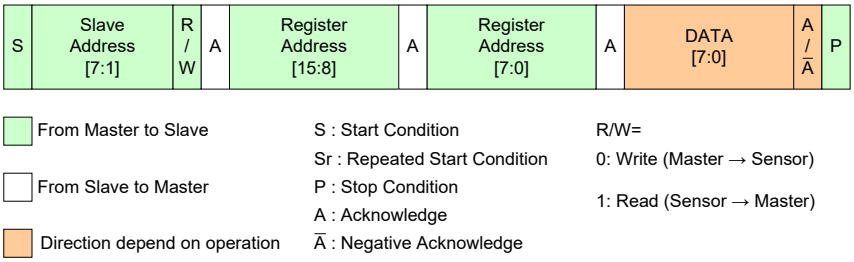
Register Communication Timing (I^2C)

In I2C communication system, communication can be performed excluding the prohibited 2H period as described in the below figure.
For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below, they are reflected by “Frame reflection register reflection timing”.
For the registers marked “I” in the item of Reflection timing, the settings are reflected when the communication is performed.
Using REGHOLD function is recommended for register setting using I^2C communication. For REGHOLD function, see “Register Transmission Setting” in “Description of Functions”.



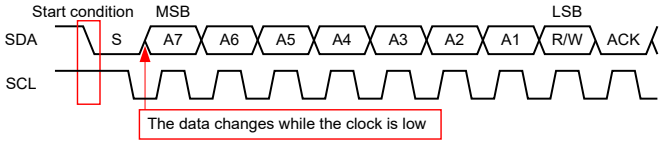
Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

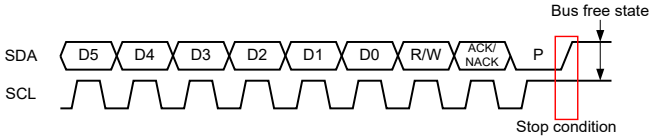


Communication Protocol

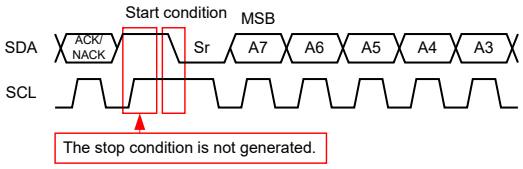
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / $\overline{A}$ (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SCL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

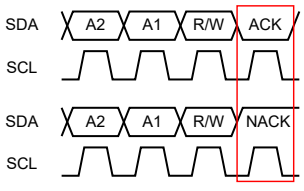


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



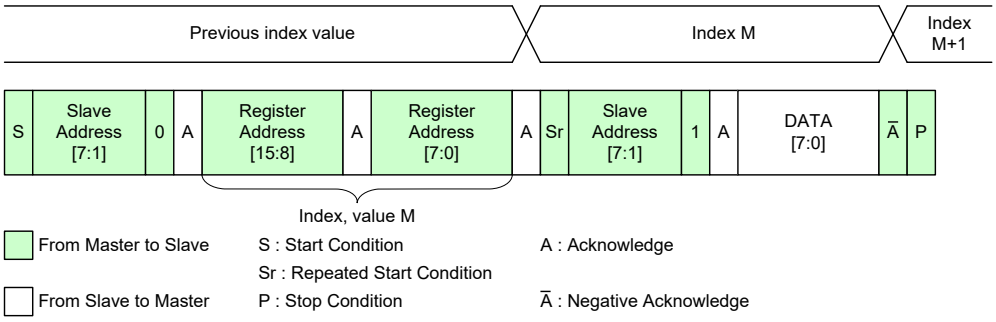
Acknowledge and Negative Acknowledge

Register Write and Read (I^2C)

This sensor corresponds to four reed modes and the two write modes.

Single Read from Random Location

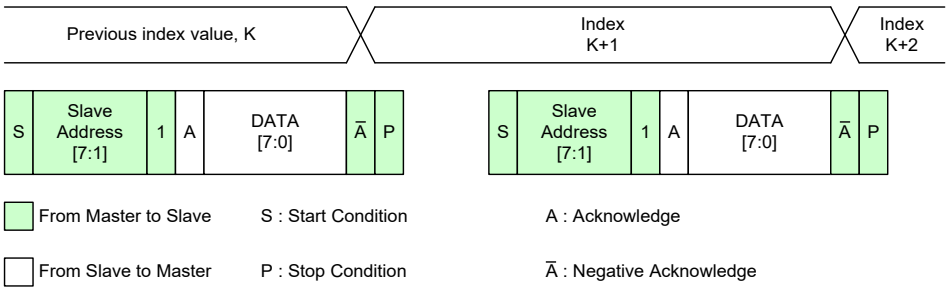
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose, it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

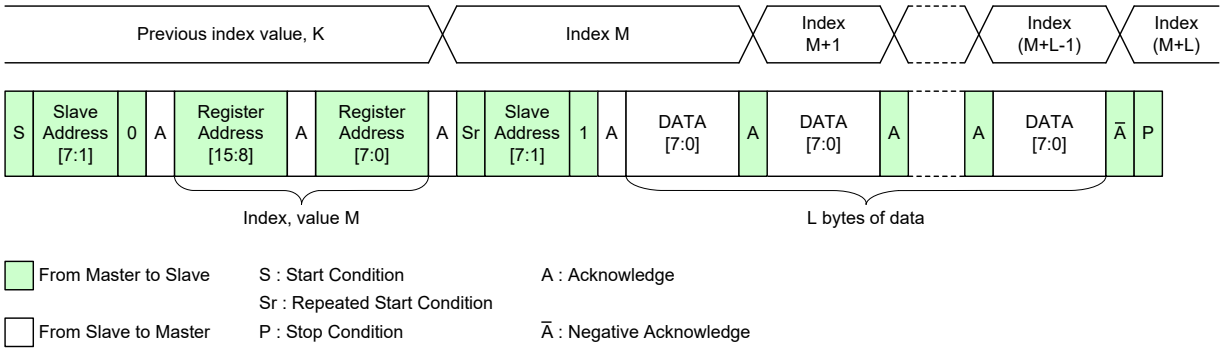
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

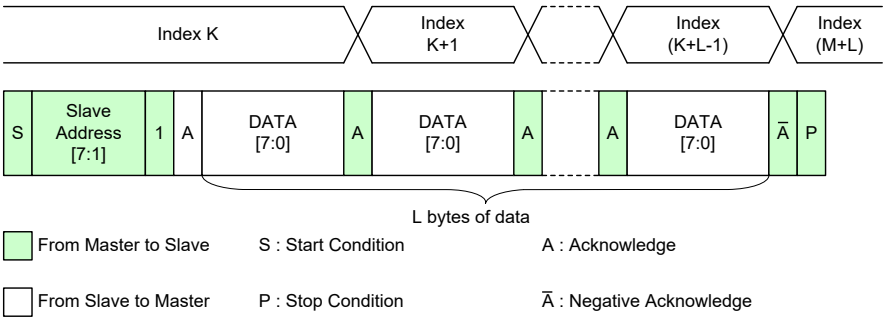
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition.
Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

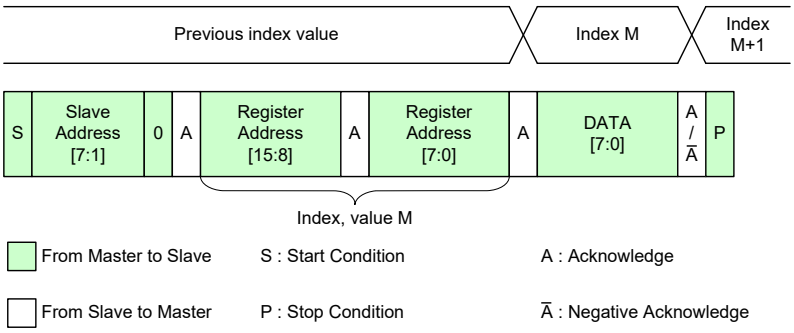
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA.
This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

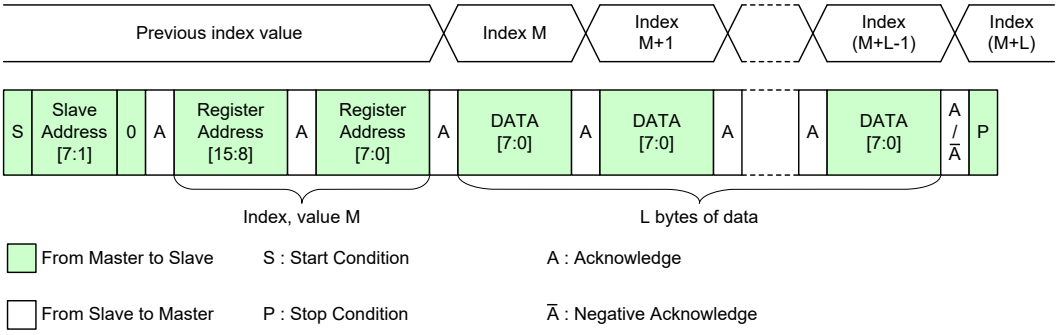
The Master sets the sensor index value to M by designating the sensor slave address with a write request and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

Please refer to IMX662_Standard_Register_Setting excel file.

Readout Drive mode

Please refer to Operating mode for Software Refalene Manual of the other file.

Image Data Output Format (CSI-2 output)

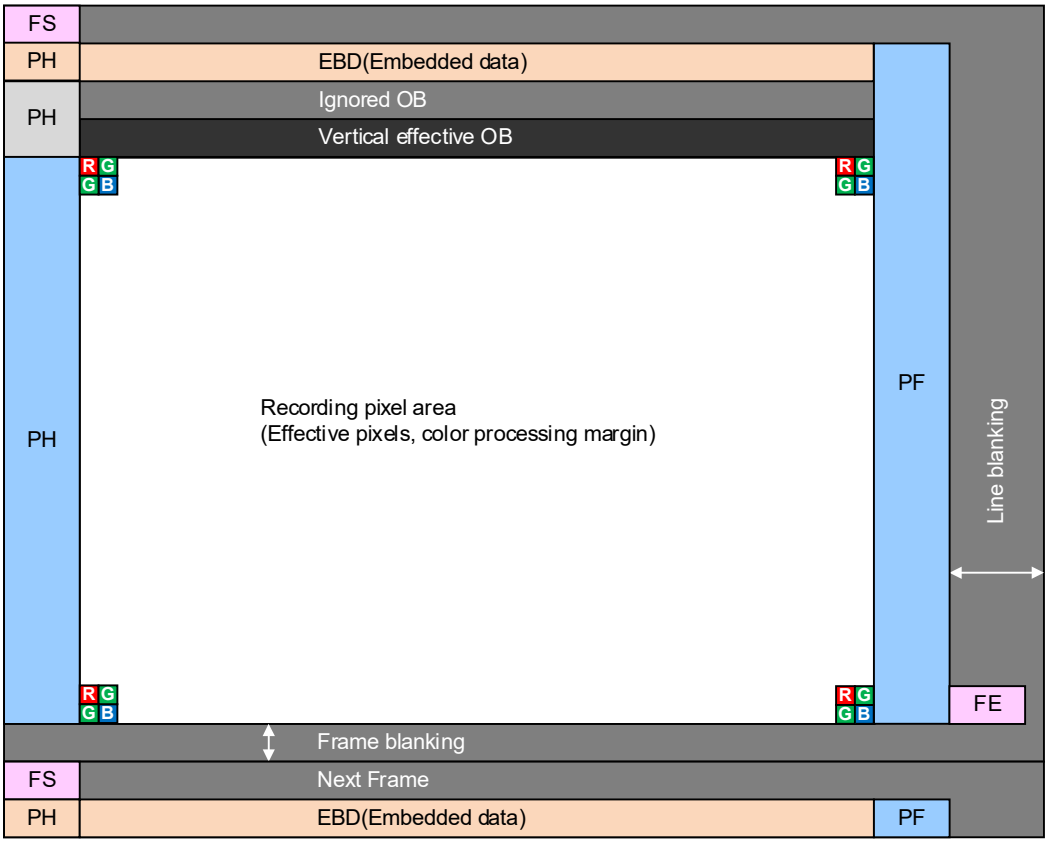
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Setting register (I^2C)	Description
00h	Frame Start Code	N/A	FS
01h	Frame End Code	N/A	FE
12h	Embedded Data	N/A	Embedded data
2Bh	RAW10	Address: 3023h MDBIT [0]	Recording pixel data
2Ch	RAW12		Recording pixel data
37h	OB Data	N/A	Vertical OB line data

Frame Structure

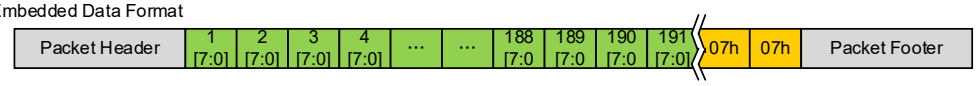


Frame Structure of CSI-2 output

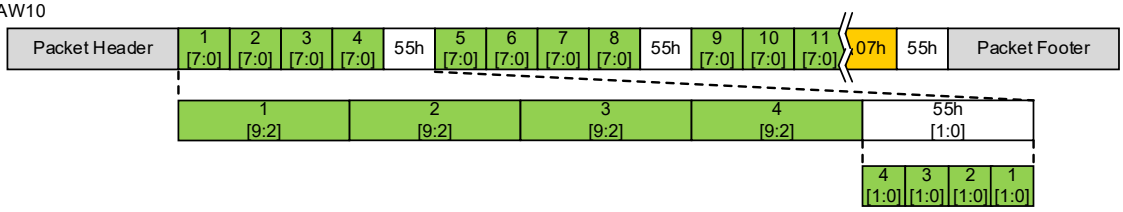
Embedded Data Line

The Embedded data line is output in a line following the sync code FS.

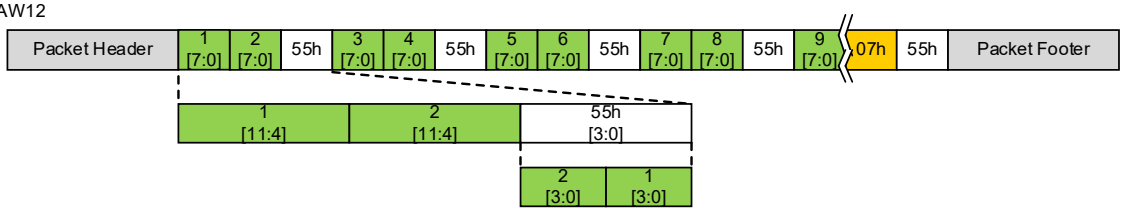
Embedded Data Format



RAW10



RAW12



Specific output examples are shown below.

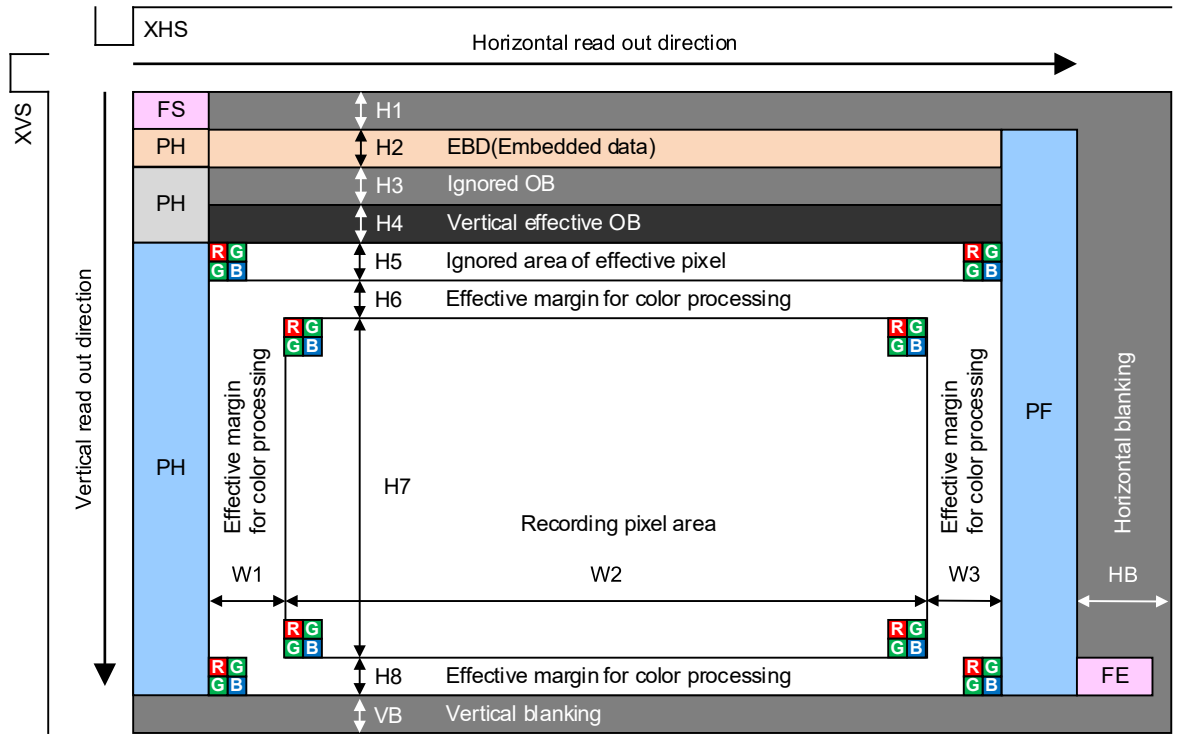
Pixel (8bit)	bit	I²C address [HEX]	Data Byte Description	Description
1	[7:0]	—	—	ignored
2	[3:0]	3018[3:0]	WINMODE	
3	[4:0]	—	—	ignored
	[5]	3020[0]	HREVERSE	
	[7:4]	—	—	ignored
4 to 8	[7:0]	—	—	ignored
9	[4:0]	—	—	ignored
	[5]	3021[0]	VREVERSE	
	[7:6]	—	—	ignored
10	[7:0]	—	—	ignored
11	[5:0]	—	—	ignored
	[6]	3022[0]	ADBIT	
	[7]	—	—	ignored
12	[7:3]	—	—	ignored
	[2]	301B[1:0]	ADDMODE	
	[1]			
	[0]	—	—	ignored
13	[2:0]	3040[2:0]	LANEMODE	
	[3]	3023[0]	MDBIT	
	[7:4]	—	—	
14 to 23	[7:0]	—	—	ignored
24	[7:0]	3050[7:0]	SHR0	
25	[7:0]	3051[7:0]		
26	[3:0]	3052[3:0]		
	[7:4]	—	—	ignored
27 to 53	[7:0]	—	—	ignored
54	[7:0]	30DC[7:0]	BLKLEVEL	
55	[1:0]	30DD[3:0]		
	[7:2]	—	—	ignored
56 to 216	[7:0]	—	—	ignored

Output data is Data[7:0] = 00h from 217 to 224 pixel.
Output data is Data[7:0] = 07h from 225 to end pixel.

Image Data output format

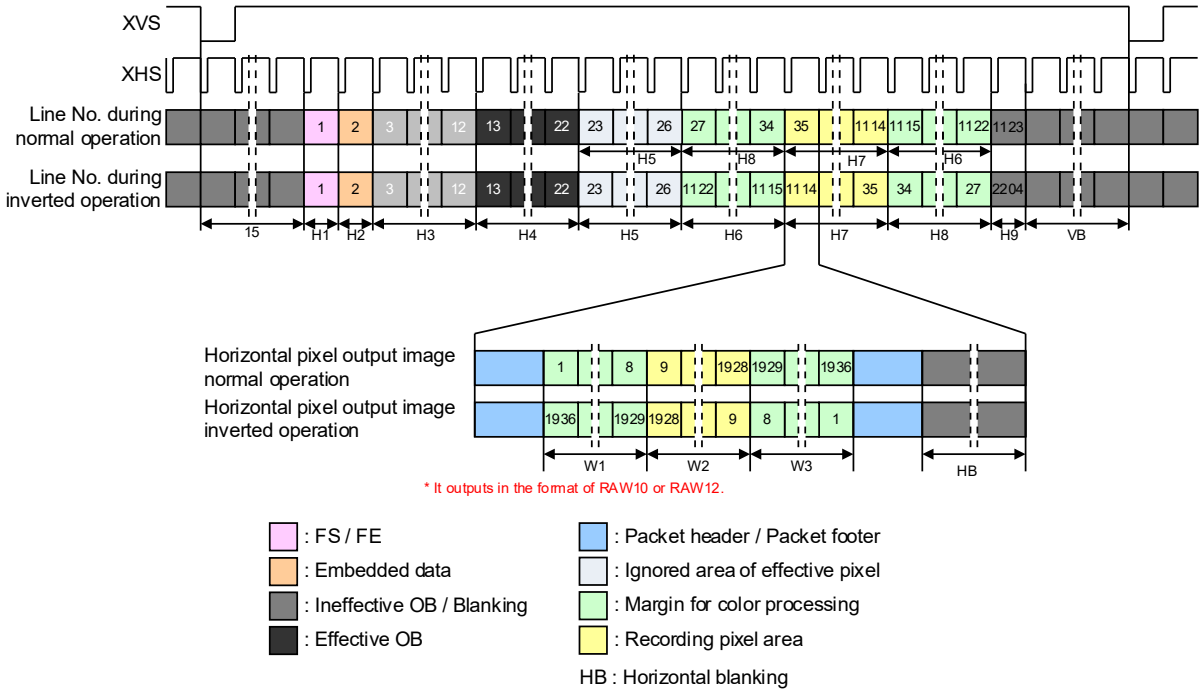
List of setting of each area

	No	Area	All-Pixel scan	Horizontal / Vertical 2/2-line binning
Vertical Direction	H1	-	1	1
	H2	EBD	1	1
	H3	Ignored OB	10	6
	H4	Vertical effective OB	10	4
	H5	Ignored area of effective pixel	4	2
	H6	Effective margin for color processing	8	4
	H7	Recording pixel area	1080	540
	H8	Effective margin for color processing	8	4
Horizontal Direction	W1	Effective margin for color processing	8	4
	W2	Recording pixel area	1920	960
	W3	Effective margin for color processing	8	4



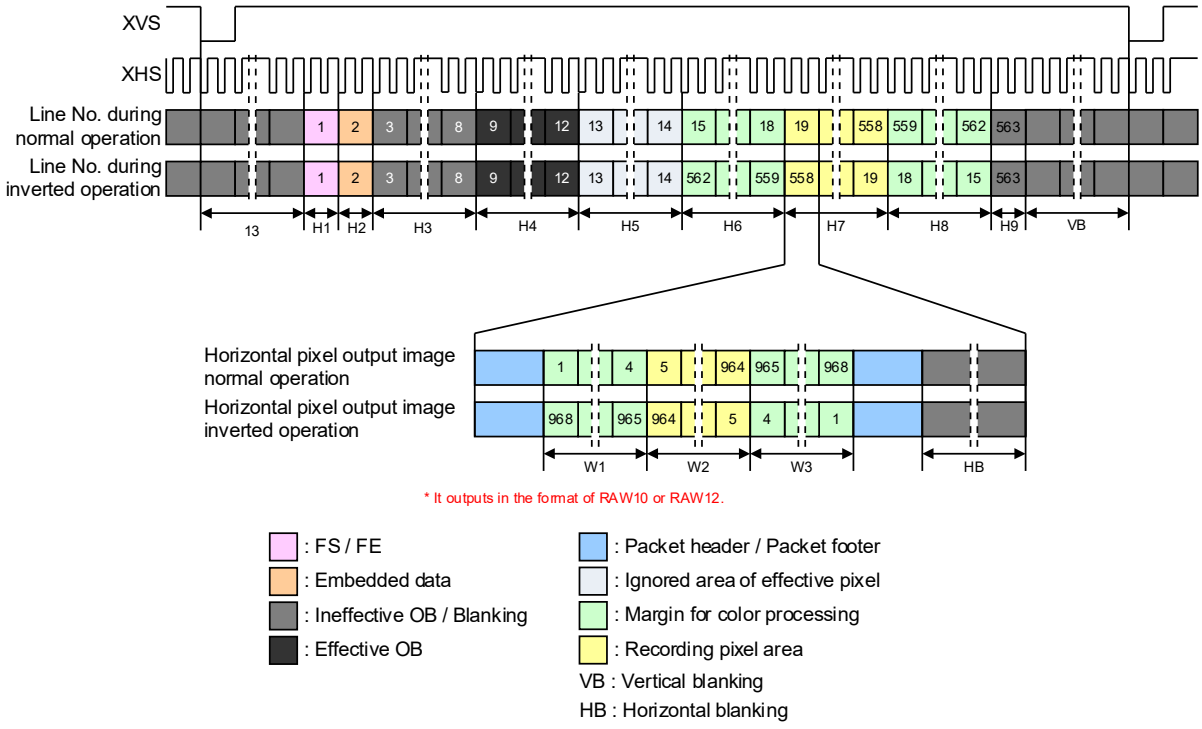
Pixel Array Image Drawing

All-pixel mode



Drive Timing Chart for All pixel mode

Horizontal/Vertical 2/2-line binning mode



Drive Timing Chart for Horizontal /Vertical 2/2-line binning mode

Description of Various Function

Please refer to Software Reference Manual about the following function.

◆ Window Cropping Mode
◆ Stanby Mode
◆ Slave Mode and Master Mode
◆ Gain Adjustment Function
◆ Black Level Adjustment Function
◆ Normal Operation and Inverted Operation
◆ Shutter and Integration Time Setting
◆ Normal Exposure Operation
◆ Long Exposure Operation
◆ Example of Integration Time Settings
◆ Signal Output
◆ CSI-2 Output
◆ MIPI Transmitter
◆ INCK Setting
◆ Global Timing setting
◆ Register Hold Setting
◆ Mode Transitions

Other Function

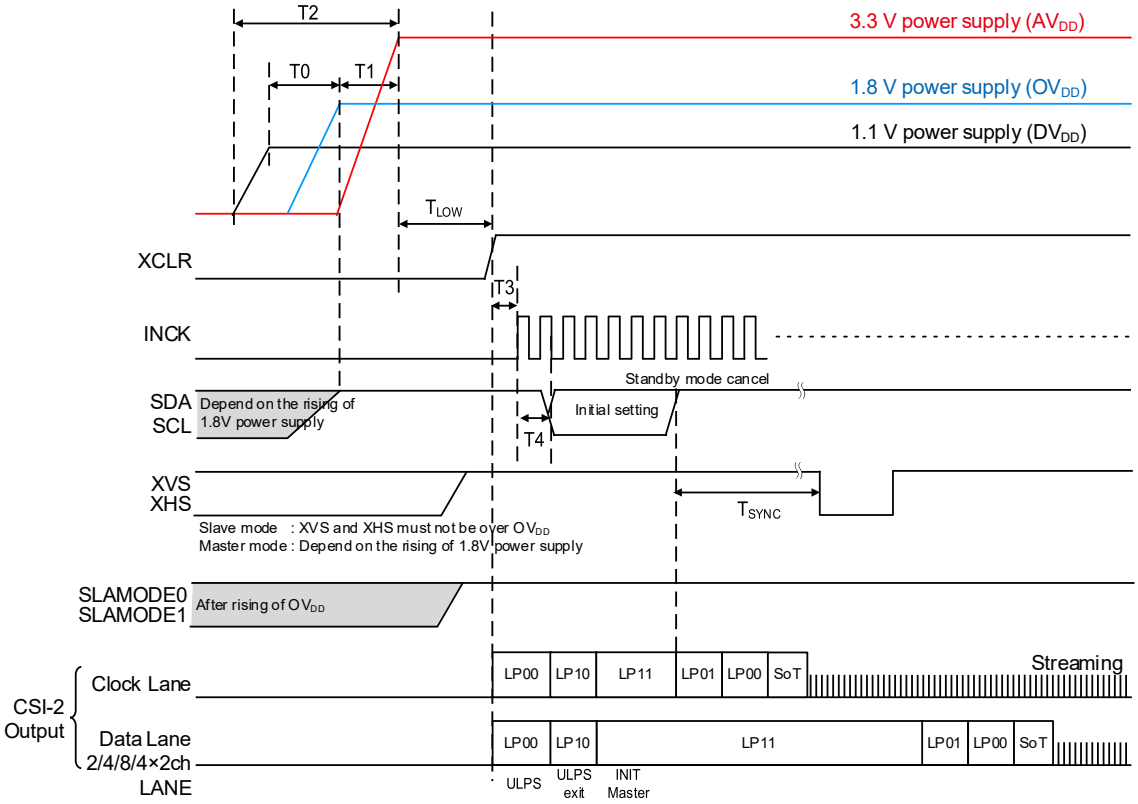
This sensor has the function as below. About detail, refer to each application note.

- Digital overlap HDR (2 / 3 frame)
- Additional Function of Synchronizing Sensors
- Clear HDR

Power-on and Power-off Sequence

Power-on sequence

1. Turn On the power supplies so that the power supplies rise in order of 1.1 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 3.3 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
3. The system clear is applied by setting XCLR to High level. The maser clock input after setting the XCLR pin to High level.
4. Make the sensor setting by register communication after the system clear.

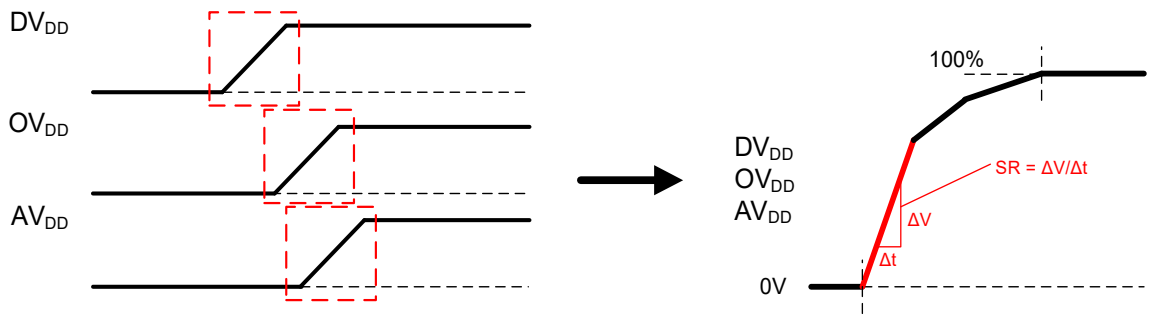


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.1 V power supply rising → 1.8 V power supply rising	T0	0	—	ns
1.8 V power supply rising → 3.3 V power supply rising	T1	0	—	ns
Rising time of all power supply	T2	—	200	ms
3.3 V power supply rising → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → INCK rising	T3	1	—	µs
Clear OFF → Communication start	T4	20	—	µs
Standby OFF (communication) → External input XHS, XVS (slave mode only)	T_{SYNC}	24	—	ms

Slew Rate Limitation of Power-on Sequence

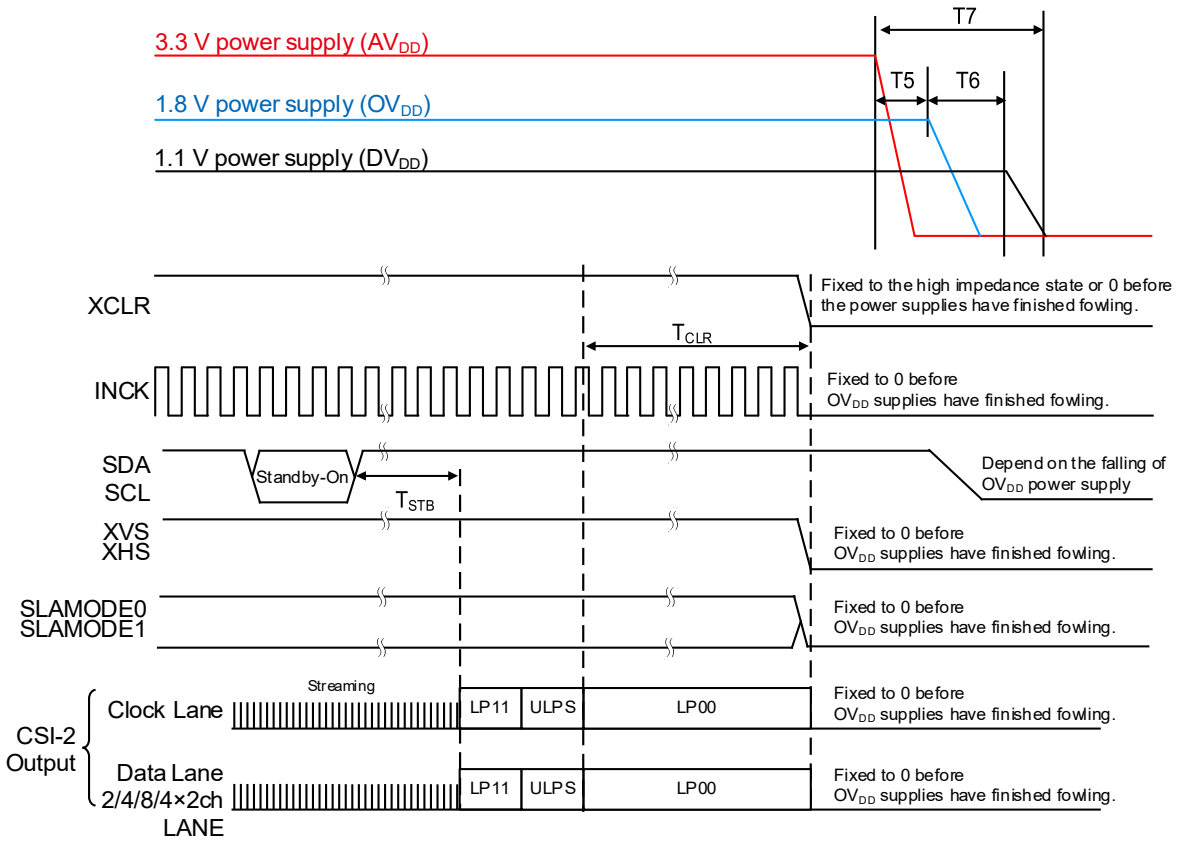
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	DV_{DD} (1.1 V)	—	25	mV/μs	
		OV_{DD} (1.8 V)	—	25	mV/μs	
		AV_{DD} (3.3 V)	—	25	mV/μs	

Power-off sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.1 V power supply (DV_{DD}). In addition, all power supplies should be falling within 200 ms. Set each digital input pin (INCK, SDA, SCL, XCLR, XVS, XHS, SLAMODE0, SLAMODE1) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



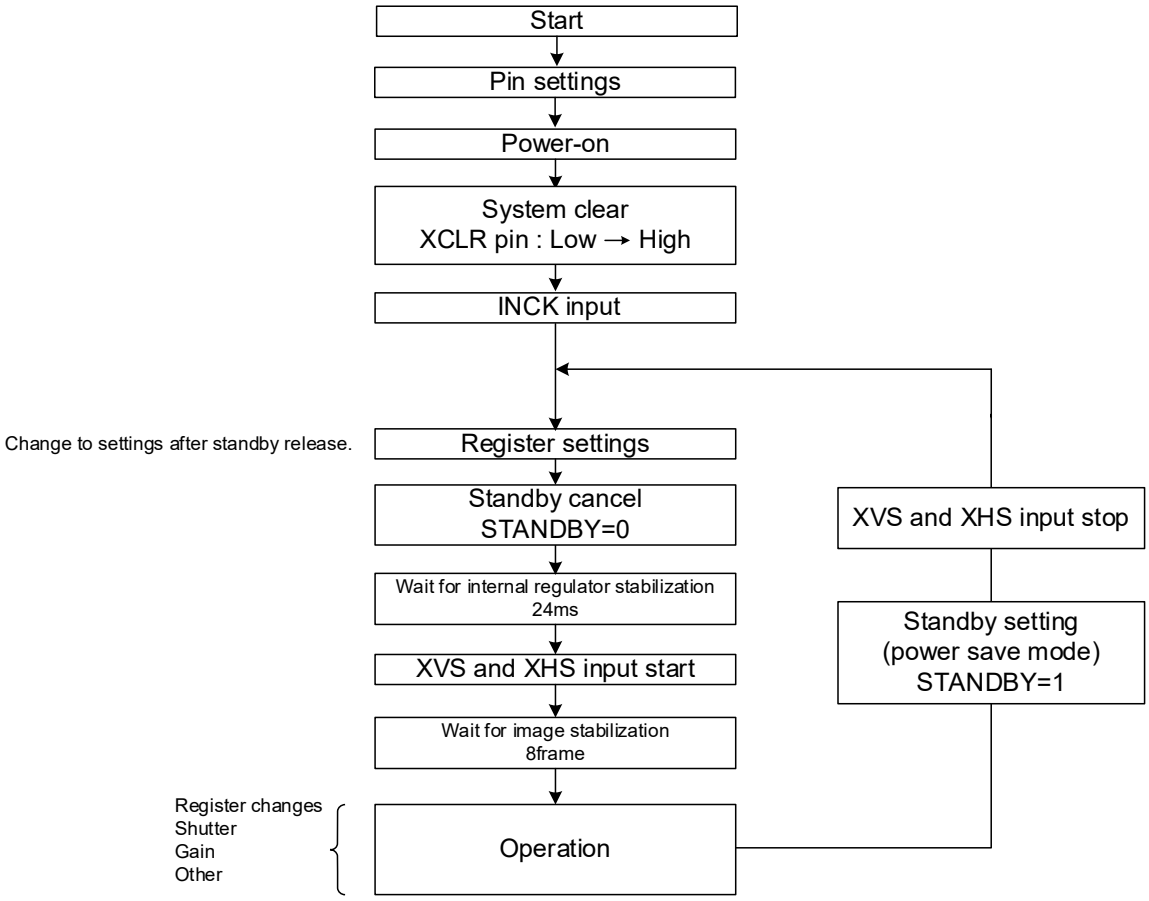
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
Standby ON (communication) → LP11 mode start	T_{STB}	FE		—
LP00 → XCLR falling	T_{CLR}	128	—	cycle
3.3 V power shut down → 1.8 V power shut down	T5	0	—	ns
1.8 V power shut down → 1.1 V power shut down	T6	0	—	ns
Shut down time of all power supply	T7	—	200	ms

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

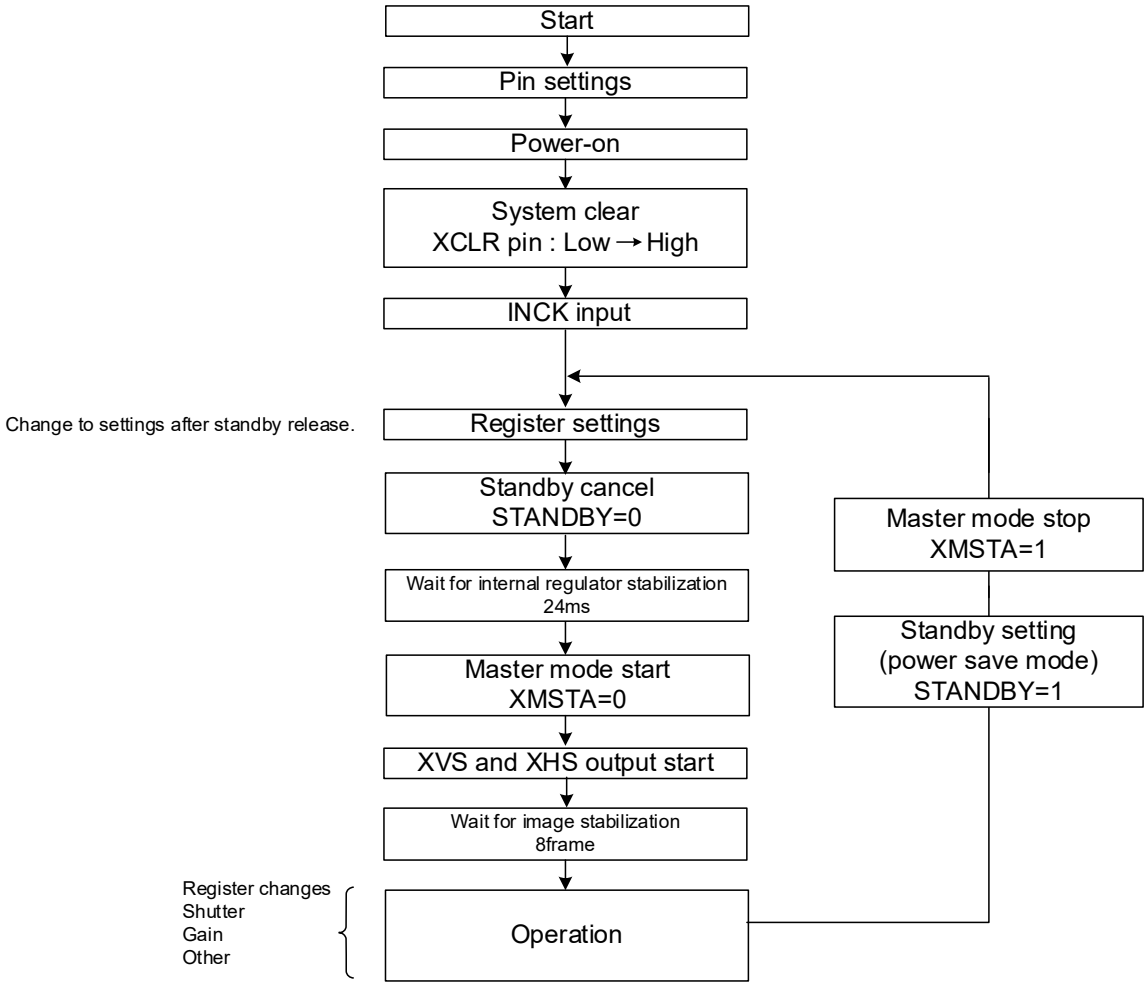
The figure below shows operating flow in sensor slave mode.
For details of "Power-on" to "Reset cancel", see the item of "Power-on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

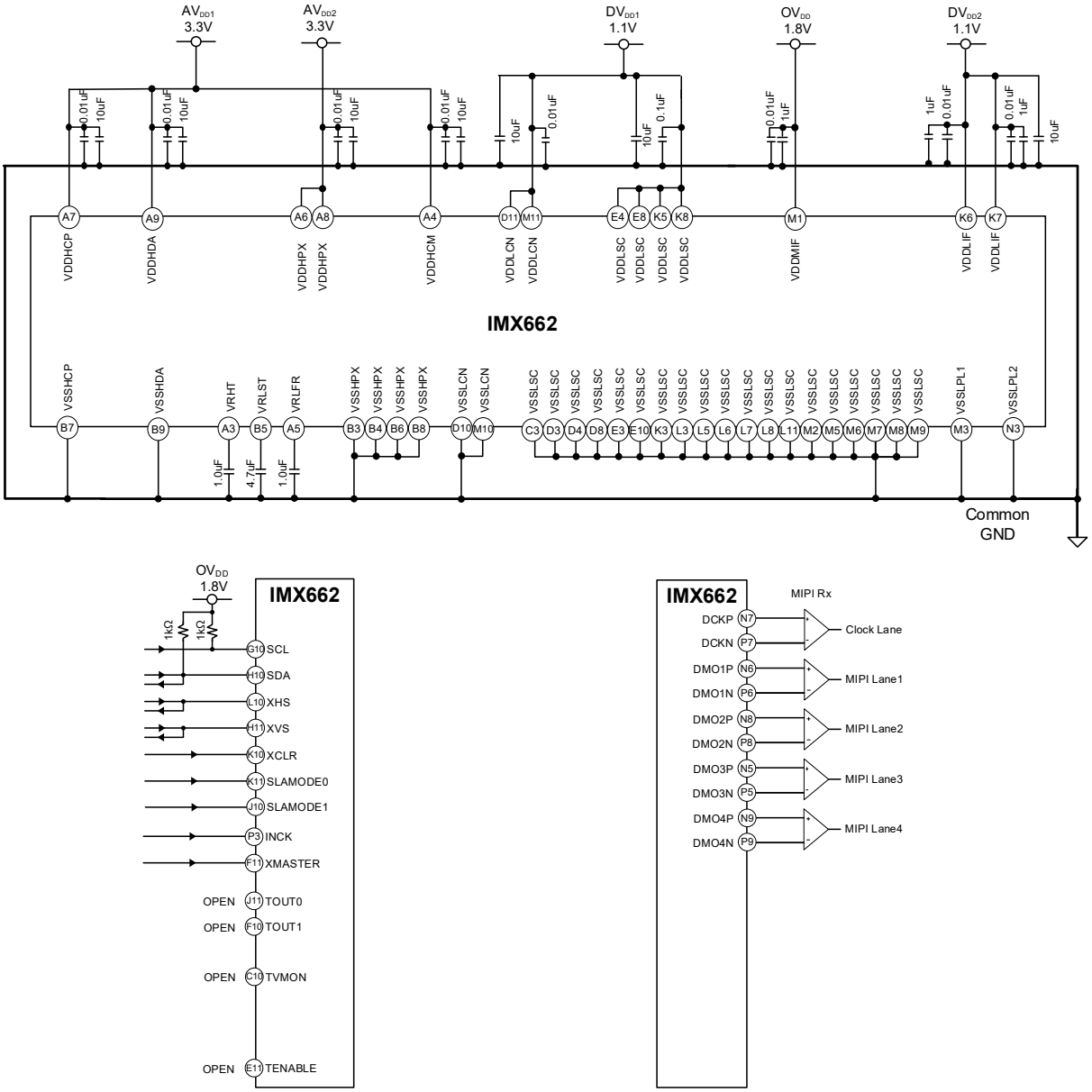
Setting Flow in Sensor Master Mode

The figure below shows operating flow in sensor master mode.
For details of "Power-on" to "Reset cancel", see the item of "Power on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
In master mode, “Master mode start” by setting register XMSTA to “0” after “Waiting for internal regulator stabilization”
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

Peripheral Circuit



Application circuits shown are typical examples illustrating the operation of the devices.
Sony Semiconductor Solutions Corporation cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

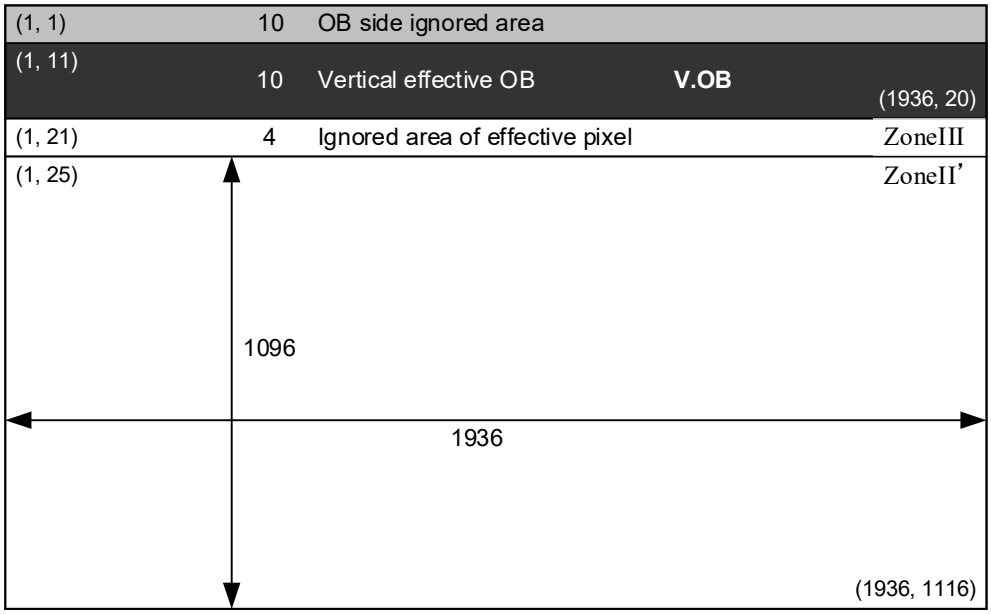
Spot Pixel Specifications

(AV_{DD} = 3.3 V, OV_{DD} = 1.8 V, DV_{DD} = 1.1 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	22	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	150		No evaluation criteria applied		2	1/30 s storage

Note) 1. Zone is specified based on all-pixel drive mode
2. D Spot pixel level

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	13 pcs
10.0 mV or higher	7 pcs
24.0 mV or higher	3 pcs
50.0 mV or higher	1 pcs
72.0 mV or higher	1 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

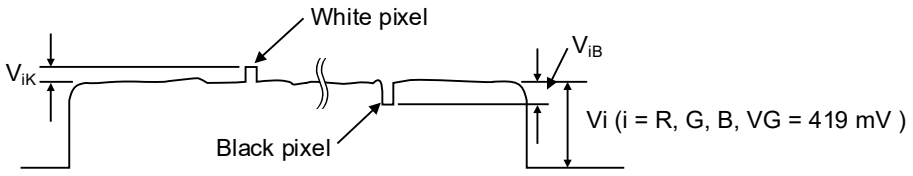
Material_No.03-0.0.10

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 419 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



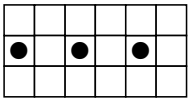
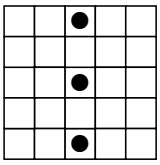
Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

Spot Pixel Pattern Specification

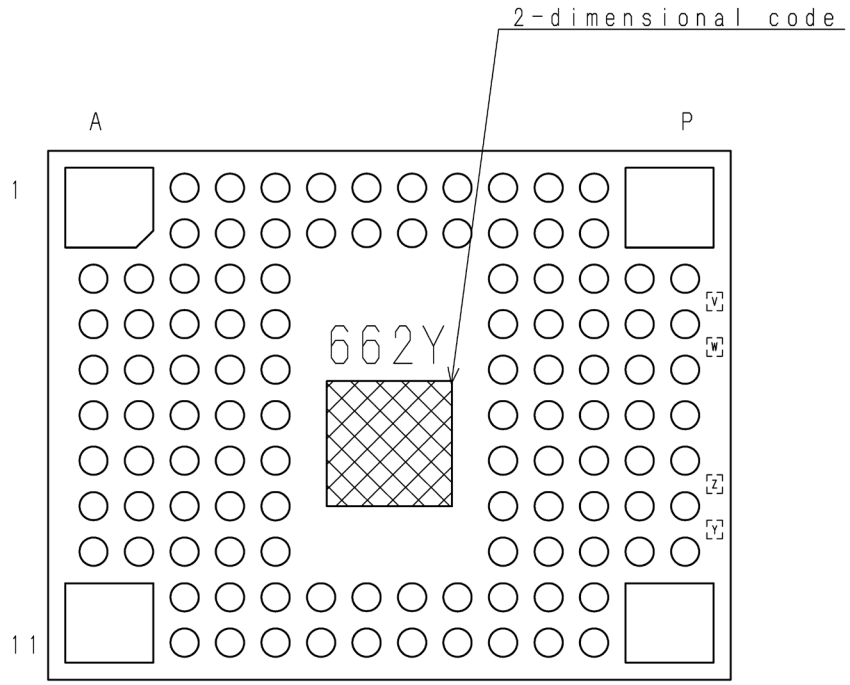
White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

No.	Pattern (R G / G B)	White pixel Black pixel Bright pixel
1		Rejected
2		Rejected

Note) 1. "●" shows the position of white pixel, black pixel, or bright pixel.
Each pattern is defined by three white pixels, three black pixels, or three bright pixels.
(Example: If one black pixel and two white pixels are located like pattern No.1, they are not judged to be rejected.)
2. Products that have one or more rejected patterns are filtered out.
3. All spot pixels are subject to the "Maximum distorted pixels in each zone" judgment in the section of "Spot Pixel Specifications" even if they do not correspond to the patterns in the table above.

Marking



Note:One character of alphabet or number shall
be placed from V to Z part. (Plating option)

Y:In English upper case character,One character
V,W,Z:Number,single number

DRAWING No. AM-C662AAQR(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

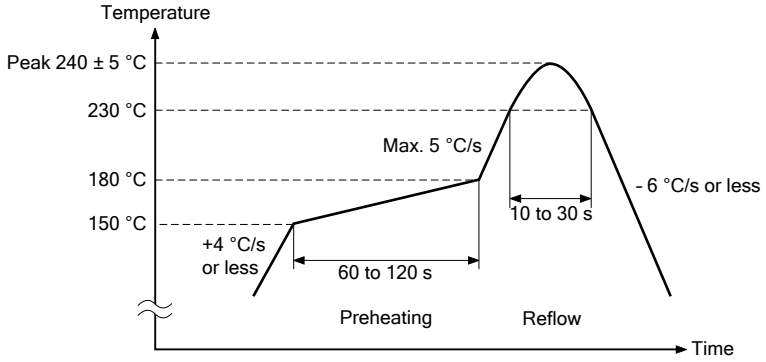
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing. Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(e) Note that condensation on glass or discoloration on resin interfaces may occur if the actual temperature and time exceed the conditions mentioned above.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

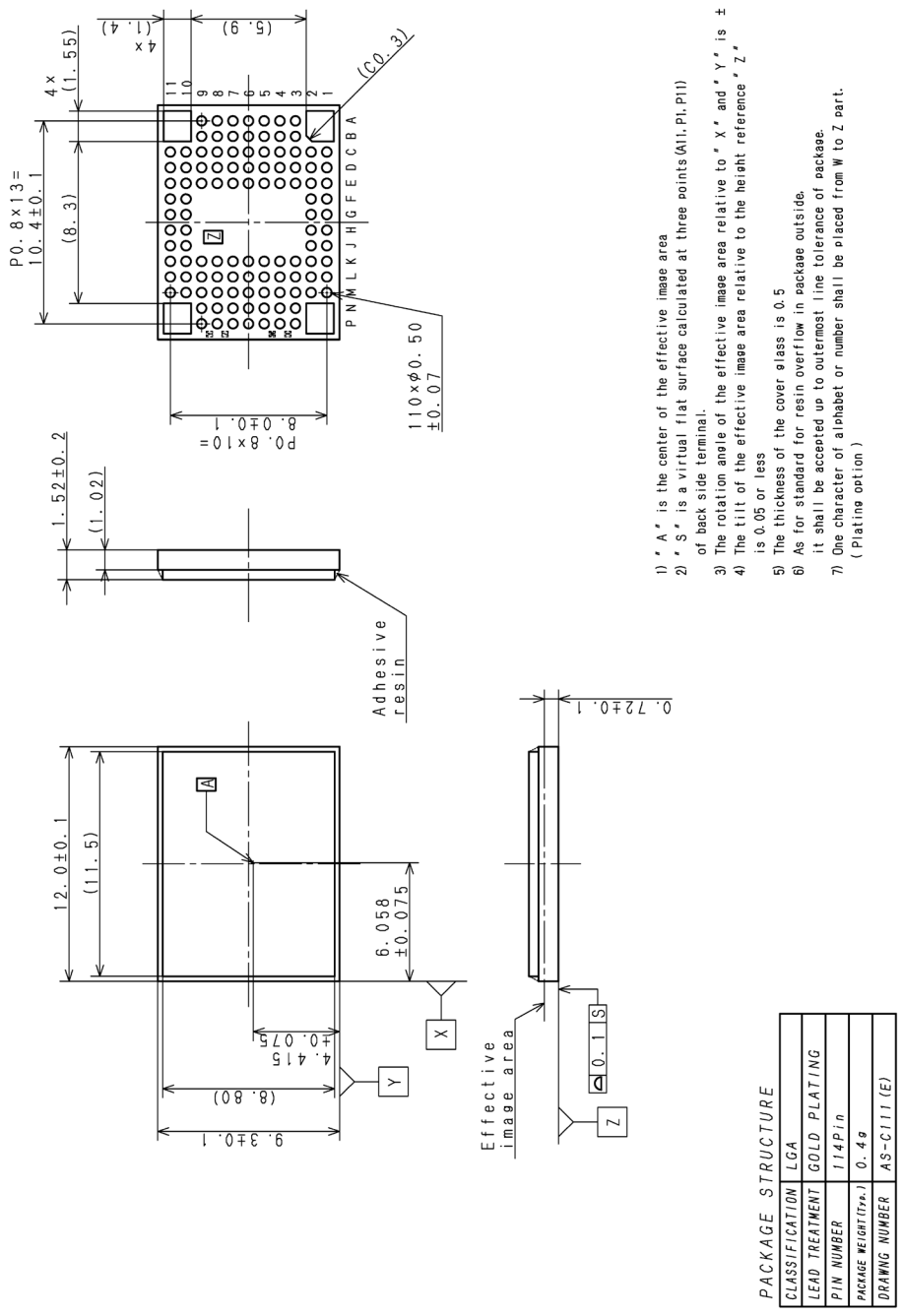
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

(6) Please perform the tilt adjustment for the optical axis in your company as required.

Package Outline

(Unit:mm)



PACKAGE STRUCTURE

CLASSIFICATION	LGA
LEAD TREATMENT	GOLD PLATING
PIN NUMBER	114Pin
PACKAGE WEIGHT(TYP.)	0.4g
DRAWING NUMBER	AS-C111(E)

List of Trademark Logos and Definition Statements

STARVIS 2

* STARVIS 2 is a registered trademark or trademark of Sony Group Corporation or its affiliates. The STARVIS 2 is back-illuminated pixel technology used in CMOS image sensors for security camera applications. It features a sensitivity of 2000 mV or more per 1 μm^2 (color product, when imaging with a 706 cd/m^2 light source, F5.6 in 1 s accumulation equivalent). It also has a wide dynamic range (AD 12 bit) of more than 8 dB compared to STARVIS for the same pixel size in a single exposure, and achieves high picture quality in the visible-light and near infrared light regions.

Revision History

Date of change	Rev.	Page	Contain of Change
2021/8/31	0.1	-	First Edition
2021/11/26	E21Y10	1	Delete: FA cameras, Industrial cameras Correction: 2H units → 1H unit
		7	Update: Optical Center TBD
		15	Update: Current Consumption TBD
		22	Update Spectral Sensitivity Characteristics
		23	Update: Image Sensor Characteristics TBD
		25	Update: Measurement Method TBD
		36	Correction: List of setting of each area H3 and H4 value
		37	Correction: All-pixel mode and Horizontal/Vertical 2/2-line binning mode is H3 and H4 value
		39	Update: Power-on and Power-off Sequence TBD
		42	Update: Setting Flow in Sensor Slave Mode TBD
		43	Update: Setting Flow in Sensor Master Mode TBD
		45	Update: Spot Pixel Specifications TBD Correction: Zone Definition OB Area value
		47	Update: Measurement Method for Spot Pixels TBD
		49	Update: Marking figure
		52	Update: Package Outline figure