SONY

IMX662 Application Note

Software Reference Manual

Other specifications without this document conform to the IMX662 datasheet.

Description

In this specification, it is list about “Operating mode” and “Description of Various Function”.
Please refer to the “Data Sheet” and “IMX662_Stadard_Register_Setting (Excel file)” for matters not described in this document.

Features

- ◆ Operating mode
- ◆ Window Cropping Mode
- ◆ Standby Mode
- ◆ Slave Mode and Master Mode
- ◆ Gain Adjustment Function
- ◆ Black Level Adjustment Function
- ◆ Normal Operation and Inverted Operation
- ◆ Shutter and Integration Time Setting
- ◆ Normal Exposure Operation
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- ◆ Signal Output
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- ◆ Register Hold Setting
- ◆ Mode Transitions

Contents

Operating mode

The table below shows the operating modes available with this sensor.
The Data rate shows the minimum value of the operating mode. The Data rate for each operating mode can be set up to the maximum data rate value by the setting register.

Mode	Lane	Data rate [Mbps/Lane]	AD conversion [bit]	Output bit width [bit]	Frame rate [frame/s]	Recording Pixels H [pixels]	Recording Pixels V [lines]	INCK [MHz]	1H period [Clock] (*1)	1V period [XHS]
All pixel	2	594	10	10	25.0	1920	1080	24, 27, 37.125, 72, 74.25	2376	1250
		720	12	12	25.0					
			10	10	30.0				1980	
			12	12	30.0					
		891	10	10	50.0				1188	
			12	12	50.0					
			10	10	60.0				990	
		1188	12	12	60.0					
		1440	10	10	90.0				660	
	4	594	10	10	25.0				2376	
			12	12	25.0					
			10	10	30.0				1980	
			12	12	30.0					
			10	10	50.0				1188	
			12	12	50.0					
			10	10	60.0				990	
			12	12	60.0					
		720	10	10	90.0				660	
Horizontal/ Vertical 2/2-line binning	2	594	10	12	25.0	960	540	24, 27, 37.125, 72, 74.25	2376	
					30.0				1980	
					50.0				1188	
					60.0				990	
		891	10	12	90.0				660	
	4	594	10	12	25.0				2376	
					30.0				1980	
					50.0				1188	
					60.0				990	
					90.0				660	

(*1) Clock frequency = 74.25 [MHz]

Frame rate on All-pixel and Horizontal / Vertical 2/2-line binning

The table below shows the register setting example of typical frame rate.
The frame rate is obtained by the following formula when using other frame rates.

Frame rate [frame / s] = 1 / (V_{TTL} × (1H period))

V_{TTL} : 1 frame line length or VMAX
: "1V period" or more in "Operating mode"

1H period (unit [s]) : "1H period" or more in "Operating mode"

Description of Various Function

Window Cropping Mode

Sensor signals are cut out and read out in arbitrary positions.
This function support All-pixel mode, Horizontal/Vertical 2/2-line binning mode, Digital overlap HDR, Clear HDR and Vertical / Horizontal direction-normal / inverted readout mode of each modes.

Cropping position is set, regarding effective pixel start position as origin (0, 0) in normal mode direction. That is a start point which is an offset from the origin and cropping width.
Cropping is available from all-pixel scan mode and horizontal period is fixed to the value for this mode. Pixels cropped by horizontal cropping setting are output with left shifted and that extends the horizontal blanking period.
Window position and size is used fixed value. (An ignore frame is output when it is changed.)

Window cropping image is shown in the figure below.
The same physical pixel area as all-pixel mode is cropped when start position and width are same setting in Horizontal/Vertical 2/2-line binning mode, Digital overlap HDR, Clear HDR and Vertical / Horizontal direction-normal / inverted readout mode.
At inverted mode, it is the same as the “Recording pixel with Effective margin for color processing (green rectangle in the figure) “area in normal mode.

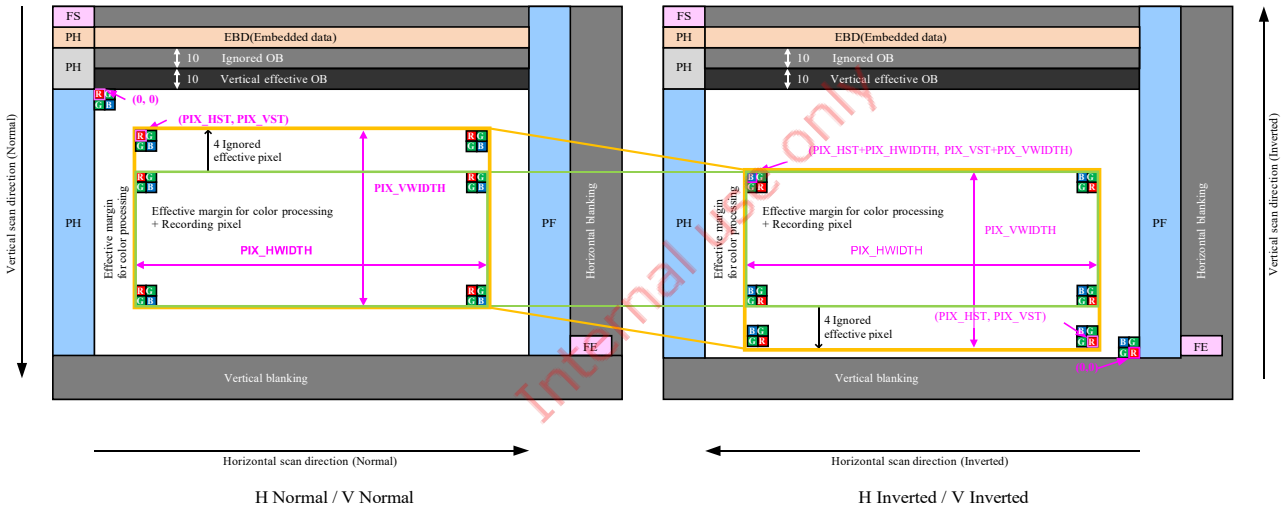


Image Drawing of Window Cropping Mode in Horizontal/Vertical, normal/inverted direction

List of Setting Register

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
WINMODE	3018h	[3:0]	0h	4h: Window Cropping mode	
PIX_HST	303Ch	[7:0]	0000h	Effective pixel Start position (Horizontal direction)	Set a multiple of 2.
	303Dh	[4:0]			
PIX_HWIDTH	303Eh	[7:0]	0790h	Effective pixel Cropping width (Horizontal direction)	Set a multiple of 16.
	303Fh	[4:0]			
PIX_VST	3044h	[7:0]	0000h	Effective pixel Start position (Vertical direction)	Set a multiple of 4.
	3045h	[3:0]			
PIX_VWIDTH	3046h	[7:0]	044Ch	Effective pixel Cropping width (Vertical direction)	Set a multiple of 4.
	3047h	[3:0]			

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

Set WINMODE: 4h.

◆ PIX_VST, PIX_VWIDTH

Set PIX_VST, PIX_VWIDTH to a multiple of 4.

$PIX\_VST = n_1 \times 4$ $(n_1 > 0)$
$PIX\_VWIDTH = n_2 \times 4$ $(n_2 \geq 188)$

Cropped area is needed to set pre 4 pixel, rear 0 pixel for signal processing.

◆ PIX_HST, PIX_HWIDTH

Set PIX_HST to a multiple of 2.
Set PIX_HWIDTH to a multiple of 16.

$PIX\_HST = n_3 \times 2$ $(n_3 > 0)$
$PIX\_HWIDTH = n_4 \times 16$ $(n_4 > 32, n_4 \neq 64)$

Where $n_{1\sim4}$ are interger equal or more than 0.

V_{TTL} (1farame line length or VMAX) ≥ PIX_VWIDTH + 70
Set V_{TTL} to 820 or more.

$V_{TTL} \geq 820$

◆ Frame rate on Window cropping mode

Frame rate [frame/s] = 1 / (V_{TTL} × (1H period))
1H period (unit: [μs]) : Fix 1H time in a mode before cropping and refer to the value of "1H period" in the table of "Operating Mode".

Where V_{TTL} is 1frame line length or VMAX.

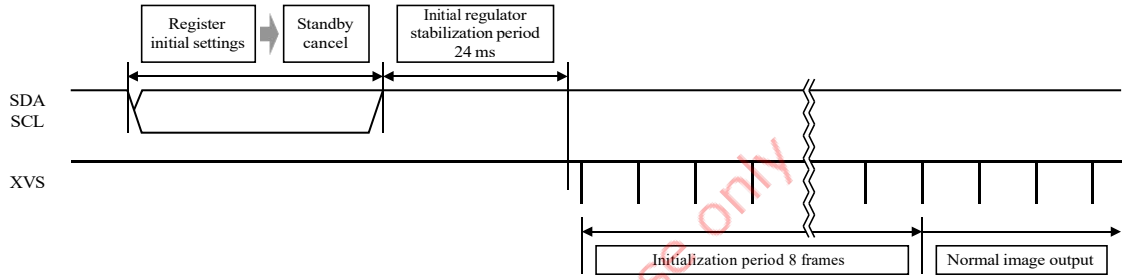
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

List of Standby Mode Setting

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
STANDBY	3000h	[0]	1h	1h: Standby 0h: Operating	Register communication is executed in standby mode.

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the 8 frames after internal regulator stabilization 24 ms or more.
For details of the sequence of setting and cancel standby mode, see the sensor setting flow after power on.



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this register status during operation.)

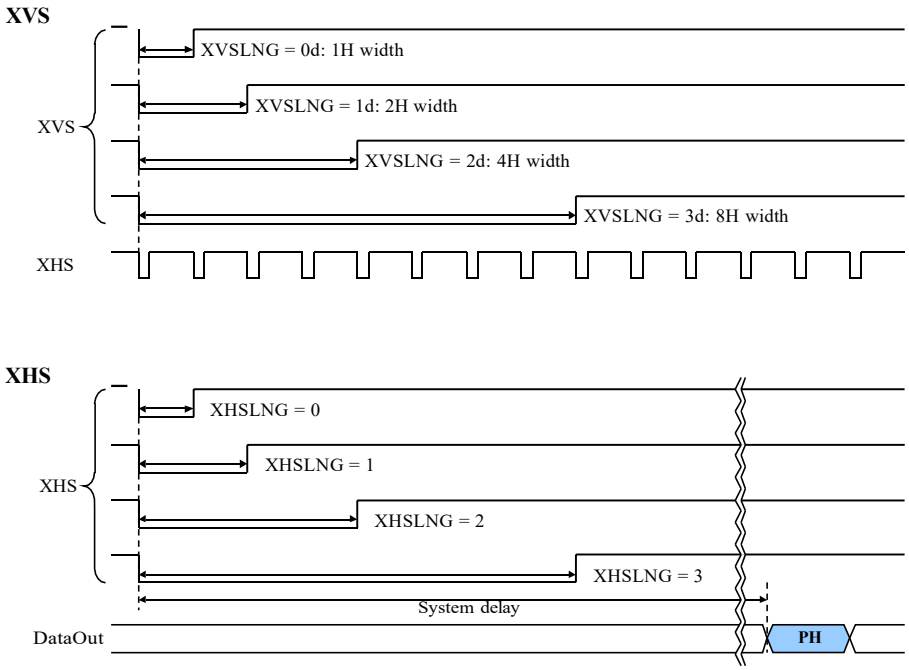
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Operating mode" for the number of output data line and 1H period.
Set the XMSTA register 0h to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [19:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of Operation Mode for details of the section of “Operating Mode”.

List of Slave and Master Mode Setting

Pin name	Pin processing	Setting value	Remarks
XMASTER pin	Fixed to Low	Master mode	High: OV_{DD}
	Fixed to High	Slave mode	Low: GND

List of Register in Master Mode

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
XMSTA	3002h	[0]	1h	0h: Master mode operation start 1h: Master mode operation stop	The master operation starts by setting 0.
VMAX [19:0]	3028h	[7:0]	004E2h	See the item of each drive mode.	Line number per frame designated * Set value multiple of 2
	3029h	[7:0]			
	302Ah	[3:0]			
HMAX [15:0]	302Ch	[7:0]	03DEh	See the item of each drive mode.	Clock number per line designated
	302Dh	[7:0]			
XVSOUTSEL [1:0]	30A4h	[1:0]	2h	0h: Fixed to Low 2h: VSYNC output	
XHSOUTSEL [1:0]		[3:2]	2h	0h: Fixed to Low 2h: HSYNC output	
XVS_DRV [1:0]	30A6h	[1:0]	3h	0h: XVS output (Master mode) 3h: Hi-z (Slave mode)	
XHS_DRV [1:0]		[3:2]	3h	0h: XHS output (Master mode) 3h: Hi-z (Slave mode)	
XVSLNG [1:0]	30CCh	[5:4]	0h	0h: 1H, 1h: 2H, 2h: 4H, 3h: 8H	XVS low level pulse width designated
XHSLNG [1:0]	30CDh	[5:4]	0h	0h: 16clock, 1h: 32clock 2h: 64clock, 3h: 128clock See the next	XHS low level pulse width designated



XVS/XHS output waveform in sensor master mode

The XVS and XHS are output in timing that set 0 to the register XMSTA. If set 0 to XMSTA during standby, the XVS and XHS are output just after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with an undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync codes output from the sensor and perform synchronization.

Gain Adjustment Function

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block. The total of analog gain and digital gain can be set up to 72dB by the GAIN [10:0] register setting. The same setting is applied in all colors.

The value which is 10/3 times the gain is set to register. (0.3 dB step)

Example)
When set to 6 dB: 6 × 10/3 = 20d; GAIN = 14h
When set to 12.6 dB: 12.6 × 10/3 = 42d; GAIN = 2Ah

List of PGC Register

Register	Register details		Initial value	Setting value	Remarks
	Address	bit		Setting range	
GAIN [10:0]	3070h	[7:0]	000h	00h to F0h (0d to 240d)	Setting value: Gain [dB] × 10/3 (0.3 dB step)
	3071h	[2:0]			

When using conversion gain high (FDG_SEL0 = 1), there is following restriction on setting range of Gain.

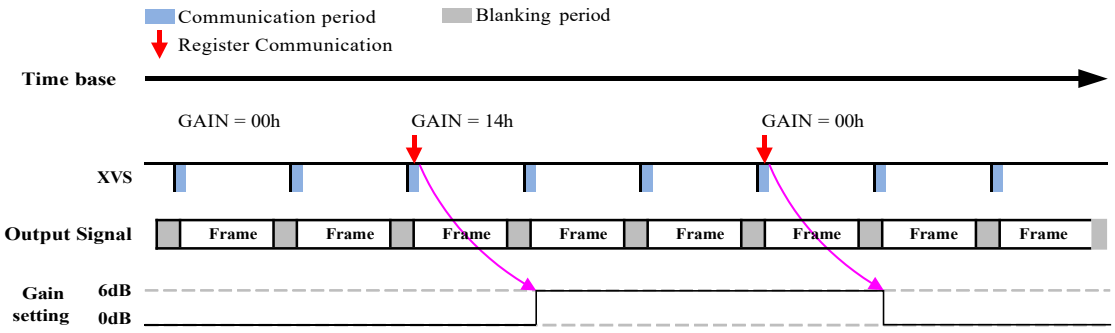
List of Conversion Gain Register

Register	Register details		Initial value	Setting value	Remarks
	Address	bit			
FDG_SEL0 [1:0]	3030h	[1:0]	0h	0h: LCG	Gain setting range: 00h to F0h (0d to 240d)
				1h: HCG	Gain setting range: 22h to F0h (34d to 240d)

Followings are other notations when changing conversion gain by the register.

1. Saturation signal gets smaller according to Vsat in “Image Sensor Characteristics” of Datasheet.

The gain setting is reflected at the next frame that the communication is performed as shown below.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 3FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [11:0] register.
Note that the offset unit changes according to the output bit setting.
When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 LSB. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 LSB.

Use with values shown below is recommended.
10-bit output: 032h (50d in LSB units)
12-bit output: 032h (200d in LSB units)

List of Black Level Adjustment Register

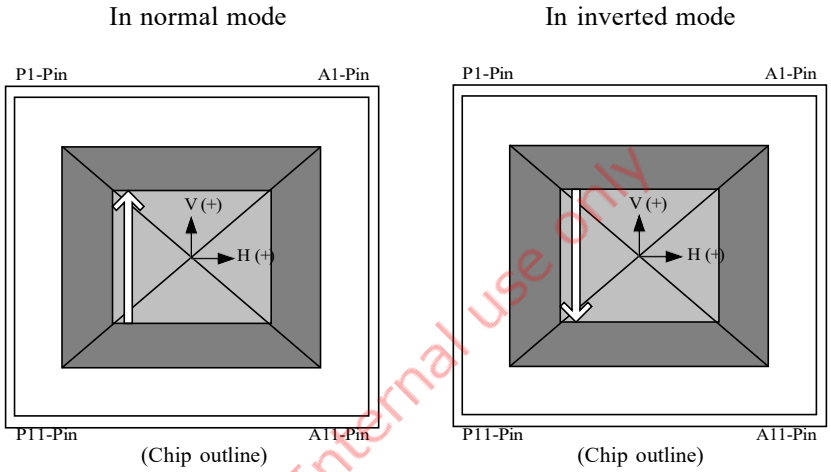
Register	Register details		Initial value	Setting value
	Address	bit		
BLKLEVEL [11:0]	30DCh	[7:0]	032h	000h to 3FFh
	30DDh	[3:0]		

Normal Operation and Inverted Operation

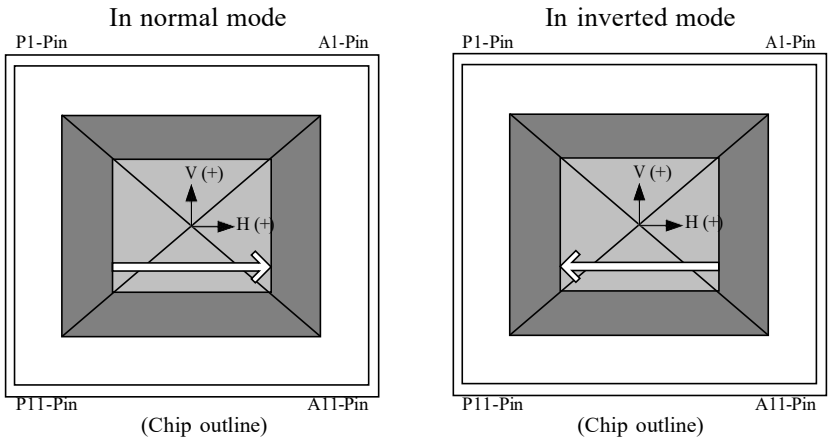
The sensor readout direction (normal / inverted) in vertical direction can be switched by VREVERSE register and in horizontal direction can be switched by HREVERSE register. See the section of “Image Data Output Format”at datasheet for the order of readout lines in normal and inverted modes, and for other register settings.
If the vertical readout direction is switched during streaming, one invalid frame occurs, while regarding the horizontal readout direction switching, no invalid frame occurs.

List of Drive Direction Setting Register

Register	Register details		Initial value	Setting value
	Address	bit		
HREVERSE	3020h	[0]	0h	0h: Normal 1h: Inverted
VREVERSE	3021h	[0]	0h	0h: Normal 1h: Inverted



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - SHR0 × (1H period) + T_{offset}

*1 The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
*2 See “Operating Mode” for the 1H period.
*3 T_{offset} = 0.

In this section, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

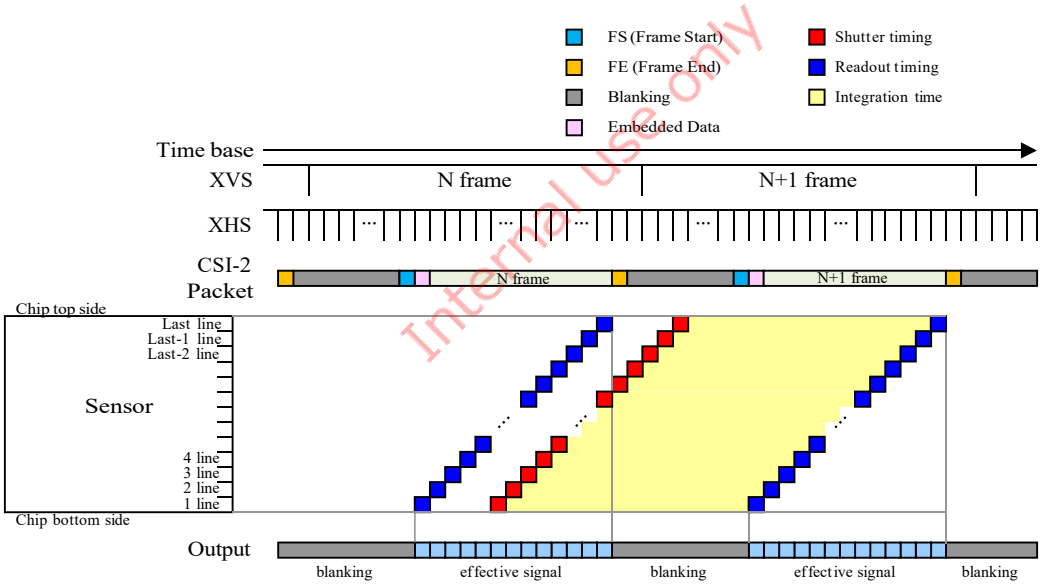


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Unit)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHR0 [19:0] register. Set SHR0 [19:0] to a value between 4 and (Number of lines per frame - 1). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register. The number of lines per frame differs according to the operating mode.

Registers Used to Set the Integration Time in 1H Unit

Register	Register details		Initial value	Setting value
	Address	bit		
SHR0 [19:0]	3050h	[7:0]	00006h	Sets the shutter sweep time. 4 to (Number of lines per frame - 1) * Others: Setting prohibited
	3051h	[7:0]		
	3052h	[3:0]		
VMAX [19:0]	3028h	[7:0]	004E2h	Sets the number of lines per frame (only in master mode). See “Operating Mode” for the setting value in each mode.
	3029h	[7:0]		
	302Ah	[3:0]		

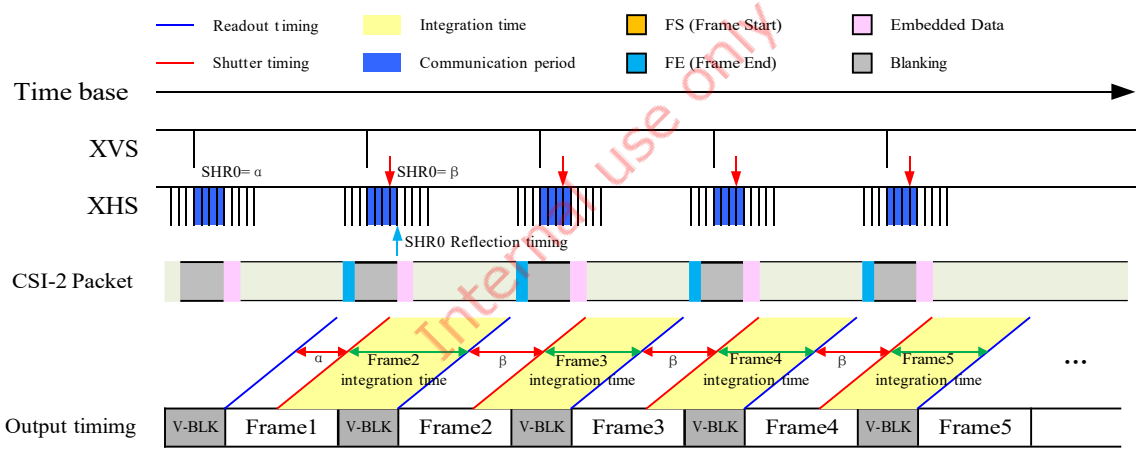


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, it is done by designating a larger register VMAX [19:0] value compared to normal operation. When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

When set to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed during long exposure operation.

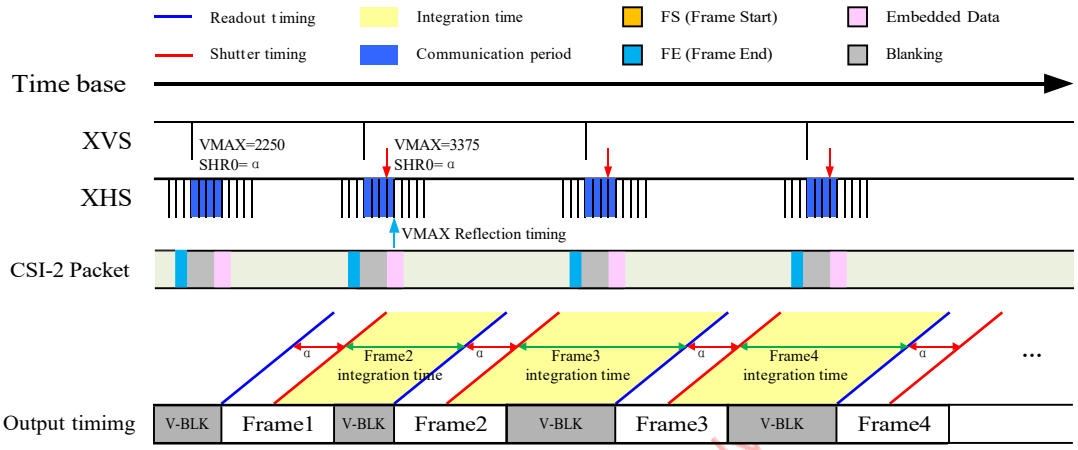


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

Example of Integration Time Settings

The example of register setting for controlling the storage time is shown below.

Example of Integration Time Settings

Operation	Sensor setting (register)		Integration time + T_{offset}
	VMAX*	SHR0**	
All-pixel scan mode	1250	1249	1H + T_{offset}
		⋮	⋮
		N	(1250 - N) H + T_{offset}
		⋮	⋮
		4	1246H + T_{offset}

* In sensor master mode. In slave mode, the interval is the same as XVS input.
** The SHR0 setting value (N) is set between “4” and “the VMAX value (M) – 1”.
*** $T_{offset} = 0$

Signal Output
CSI-2 output

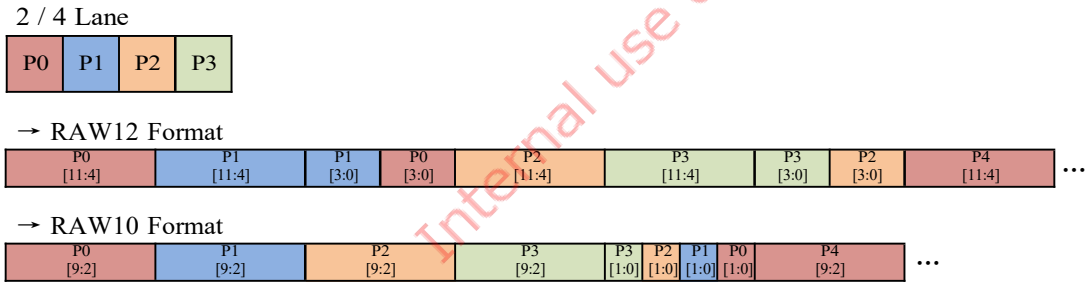
The output formats of this sensor supports the following modes.

CSI-2 serial 2 Lane / 4 Lane, RAW10 / RAW12.

The 2 Lane / 4 Lane serial signal output method using this sensor is described below.
Complied with the CSI-2, data is output using 2 Lane / 4 Lane. The image data is output from the CSI-2 output pin. The DMO1P / DMO1N are called the Lane1 data signal, the DMO2P / DMO2N are called the Lane2 data signal, the DMO3P / DMO3N are called the Lane3 data signal, the DMO4P / DMO4N are called the Lane4 data signal.
In addition, the clock signals are output from DCKP / DCKN of the CSI-2 pins.
About 2 Lane / 4 Lane, Use a clock signal of DCKP / DCKN.
In 2 Lane mode, data is output from Lane1 and Lane2.
In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4.
The bit rate maximum value is 2376 Mbps / Lane in 4 Lane mode and 2376 Mbps / Lane in 2 Lane mode.
The select of RAW10 / RAW12 is set by the register: MDBIT. The number of output lanes is set by the register: LANEMODE [2:0]. Unused lanes output signals conformed to MIPI standard.

Register	Register details		Initial value	Setting value
	Address	bit		
MDBIT	3023h	[0]	1h	0h: RAW10 1h: RAW12
LANEMODE	3040h	[2:0]	3h	1h: 2lane 3h: 4lane

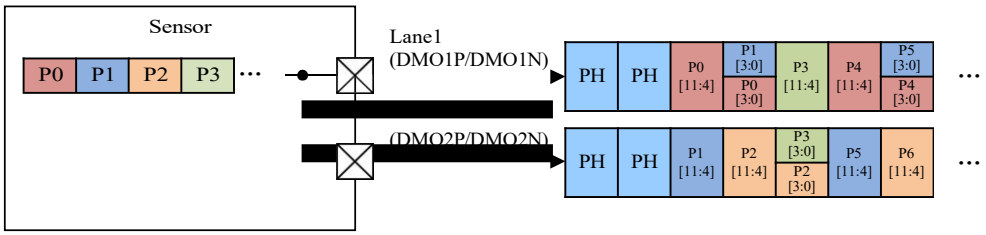
The formats of RAW12 and RAW10 are shown below.



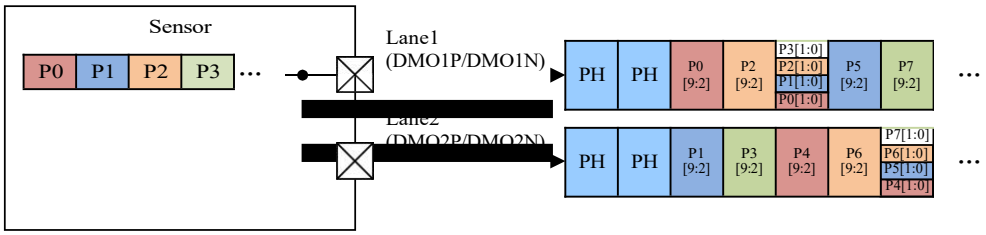
The Example of Format of RAW12 / RAW10

The each formal of 2 Lane and 4 Lane are shown below.

a) 2 Lane-RAW12

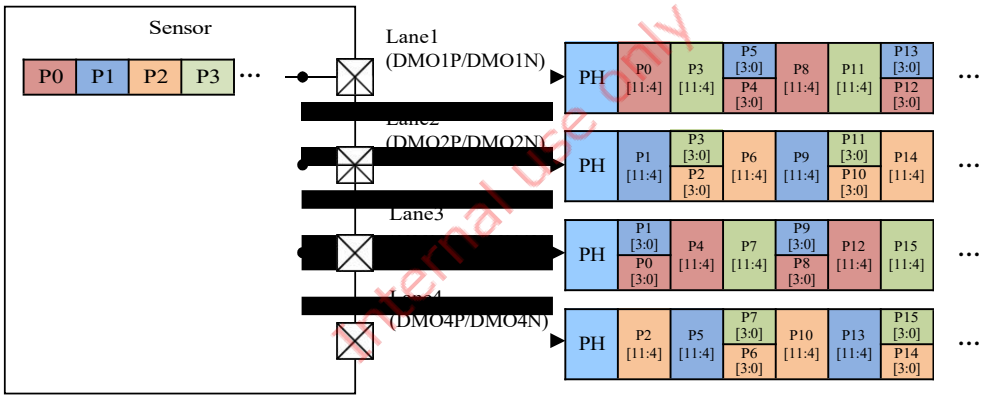


b) 2 Lane-RAW10

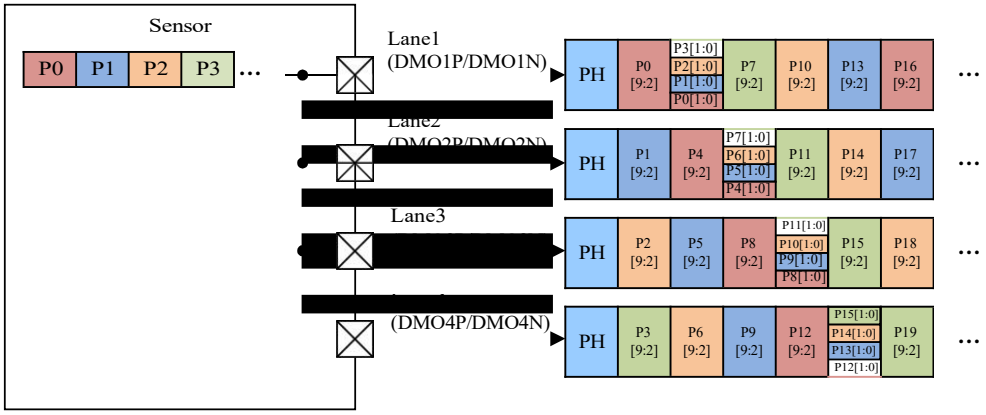


2 Lane Output Format

c) 4 Lane-RAW12



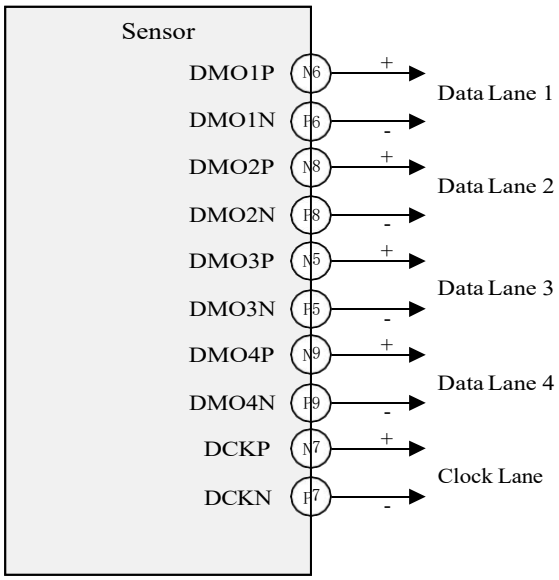
d) 4 Lane-RAW10



4 Lane Output Format

MIPI Transmitter

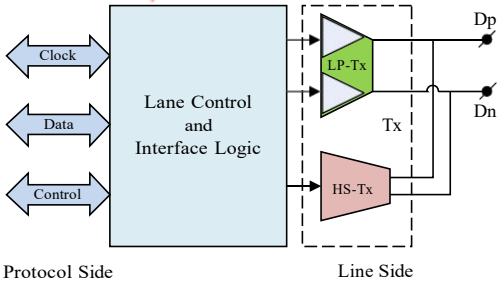
Output pins (DMO1P, DMO1N, DMO2P, DMO2N, DMO3P, DMO3N, DMO4P, DMO4N, DCKP, DCKN) are described in this section.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.2
・MIPI Alliance Specification for D-PHY Version 1.2

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane is as follows.
About 2 Lane and 4 Lane, 2376 Mbps / Lane



Universal Lane Module Functions

Number of Internal A/D Conversion Bits Setting

The number of internal A/D conversion bits can be selected from 10 bits or 12 bits by the register ADBIT [1:0]. See the section of "Operating Mode" for the correspondence with each mode.

List of Bit Width Selection

Register	Register details		Initial value	Setting value
	Address	bit		
ADBIT	3022h	[0]	1h	0h: AD 10bit 1h: AD 12bit

Output Signal Range

In CSI-2 output mode, the sensor output has either a 10 bit, and 12 bit gradation, and the maximum output value is the 3FFh value (10 bit output), the FFFh one (12 bit output).
The output range for each output gradation is shown in the table below.

Output Gradation and Output Range (CSI-2 Output)

Output gradation	Output value	
	Min.	Max.
10 bit	000h	3FFh
12 bit	000h	FFFh

INCK Setting

The available operation mode varies according to INCK frequency. When input either 24 MHz, 27 MHz, 37.125 MHz, 72 MHz or 74.25 MHz for INCK frequency, Set INCK_SEL.
The INCK setting register shown in the table below.

INCK Setting Register

Register	Register details		Initial value	Setting value
	Address	Bit		
INCK_SEL	3014h	[3:0]	0h	0h: 74.25 MHz 1h: 37.125 MHz 2h: 72 MHz 3h: 27 MHz 4h: 24 MHz

Global Timing setting

The table below shows the setting value of Global Timing available with about change “Data Rate”.
When data rate is either 594 Mbps, 720 Mbps, 891 Mbps, 1188 Mbps, 1440 Mbps, 1782 Mbps, 2079 Mbps or 2376 Mbps for data rate, Set DATARATE_SEL. Global timing is set automatically.

Data Rate Setting Register

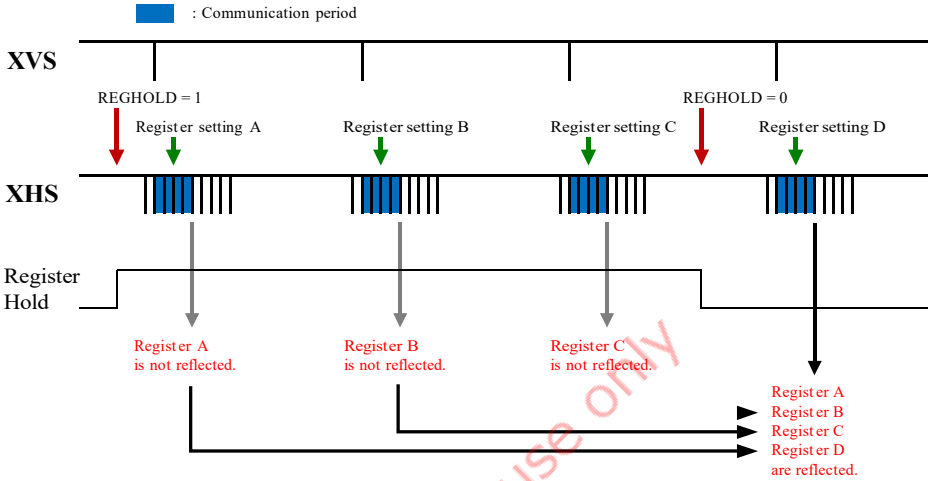
Register	Register details		Initial value	Setting value
	Address	Bit		
DATARATE_SEL	3015h	[3:0]	2h	Data rate setting 0h: 2376 Mbps 1h: 2079 Mbps 2h: 1782 Mbps 3h: 1440 Mbps 4h: 1188 Mbps 5h: 891 Mbps 6h: 720 Mbps 7h: 594 Mbps

Register Hold Setting

V reflected register setting can be transmitted with divided to several frames and it can be reflected globally at acertain frame by the register REGHOLD. Setting REGHOLD = 1 prevents the registers that set thereafter from being reflected at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the desired frame to reflect the register.

Register Hold Setting Register

Register	Register details		Initial value	Setting value
	Address	bit		
REGHOLD	3001h	[0]	0h	0: Invalid 1: Valid (Register hold)



Register Hold Setting

Mode Transitions

The Mode transition between operations is shown below. These examples shown in case that setting is completed within one communication timing.

List of Mode Transition

Transition			State
Horizontal direction normal	→	Horizontal direction inverted	Via the Standby state is unnecessary.
Horizontal direction inverted	→	Horizontal direction normal	
All-pixel scan mode	→	Window cropping mode	Via the Standby state is unnecessary. One invalid frame is generated.
Window cropping mode	→	All-pixel scan mode	
Vertical direction normal	→	Vertical direction inverted	
Vertical direction inverted	→	Vertical direction normal	
Vertical direction line number change (Master mode: VMAX change, Slave mode: XVS interval change) *1			
Horizontal direction 1H period change (Master mode: HMAX change, Slave mode: XHS interval change)			
- Transition between modes other than above - Change the input frequency of INCK *2 - Change the register setting noted “S” in the reflection timing column of the IMX662-AAQR_Standard_Register_Setting excel file.			Via the standby state is necessary.

*1 When the changing Vertical derection line number, the output lines are the setting value, but output image is the valid image which is set before. And the image of new setting is output at next frame.

*2 When changing input INCK frequency, care should be taken not to be input pulses whose width are shorter than the High / Low level width in front and behind of the INCK pulse at the frequency change. If the pulses above generate at the frequency change, change INCK frequency during system reset in the state of XCLR = Low, and then perform system clear in the state of XCLR = High following the item of "Power on sequence" in the section of "Power on / off sequence". Execute initial setting again because the register settings become default state after system clear.

*3 When changing input output lane number between 2 Lane and 4 Lane, via XCLR = Low,

Revision History

Date of change	Rev.	Page	Contain of Change
2021/8/31	0.1	-	First Edition
2021/12/1	1.0	4	Correction: Image Drawing of Window Cropping Mode in Horizontal/Vertical, normal/inverted direction
		6	Update: Standby mode TBD
		9	Update: List of Conversion Gain Register TBD
		10	Correction: Black Level Adjustment Function (50d) → (50d in LSB units) (200d) → (200d in LSB units)
		11	Correction: Normal Operation and Inverted Operation Change text
		12	Delete: Example of Integration Time Setting *3 Set multiple of 2 about the time of SHR0
		13	Correction: Normal Exposure Operation 2H units → 1H unit Registers Used to Set the Integration Time in 1H Unit
2022/04/28	2.0	3	Correction: Operating Mode All-pixel 2Lane 1188Mbps 10bit 50/60FPS → 891Mbps 10bit 50/60FPS 1188Mbps 12bit 50FPS → 891Mbps 12bit 50FPS Horizontal / Vertical 2/2-line binning 2Lane 720Mbps → 594Mbps 891Mbps → 594Mbps 1188Mbps → 891Mbps
2022/06/30	3.0	5	Correction: PIX_VST, PIX_VWIDTH $n_2 \geq 239 \rightarrow n_2 \geq 188$ Correction: PIX_HST, PIX_HWIDTH $n_4 \geq 64 \rightarrow n_4 > 32, n_4 \neq 64$ Add: PIX_HST, PIX_HWIDTH Where $n_{1\sim4}$ are interger equal or more than 0.