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LimeLight™ operation modes

- Description -

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Contents

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Introduction

This document describes LimeLight™ digital IQ data interface modes and required settings to operate in those modes. Interface can be configured to run in one of the following modes:

- JESD207 MIMO DDR
- JESD207 SISO DDR
- TRXIQ MIMO DDR
- TRXIQ SISO DDR
- TRXIQPulse
- TRXIQ SDR

In every mode except JESD207 modes LimeLight™ interface is able to accept and start capturing data from positive or negative edge clock FCLK, with right interface settings. Both options is shown in waveforms.

Data can be transmitted from RF to BB without using FCLK, in this case MCLK is used for launching data and BB captures data from delayed MCLK, delay can be adjusted. Also there is a option to invert this clock, which is shown in diagrams where it is possible.

By using PLL in Baseband FCLK clock can be doubled and used for TRXIQ MIMO and SISO, TRXIQPulse and TRXIQ SDR modes. This configuration is called 2x clock mode.

In Figure 1 it is depicted LimeLight™ control block diagram, where interface settings with corresponding registers can be found.

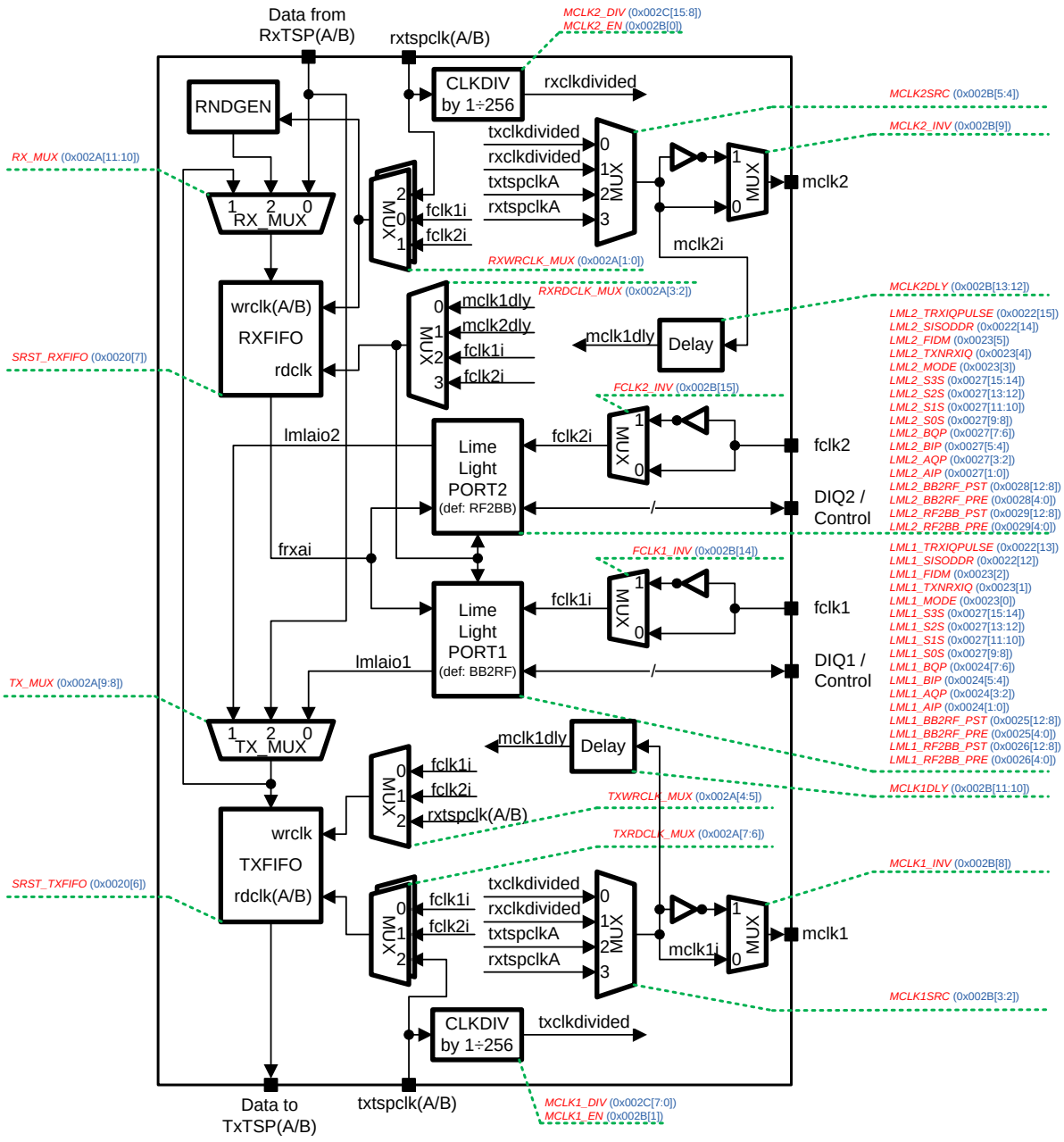

Figure 1 LimeLight™ control block diagram

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JESD207 Modes

By using JESD207 mode data can be transmitted and received by using SISO DDR or MIMO DDR modes. In this chapter it is explained both modes with timing diagrams and signal interconnection between interfaces.

2.1 MIMO DDR Mode

In this mode data can be transmitted and received with same settings, for this reason signal connection diagram (see Figure 2) and settings (see Table 1) are the same for RF2BB and BB2RF paths.

2.1.1 Signal connection

In Figure 2 it is shown signal connection between RF and BB.

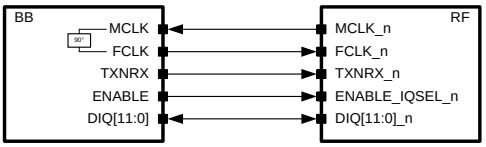


Figure 2 Signal connection in JESD207 mode

2.1.2 Settings

Required settings for JESD207 MIMO DDR mode are as shown in Table 1.

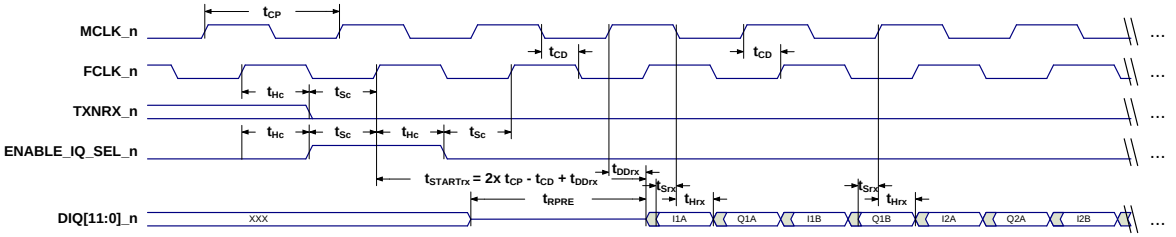
Table 1 LimeLight™ settings for JESD207 MIMO DDR mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	

MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	JESD207 (default)	
SISO DDR	LMLx_SISODDR	off	
TRXiQPulse	LMLx_TRXIQPULSE	off	
FCLKx invert	FCLK_INV	Not inverted (default)	
MCLKxDLY	MCLKxDLY	no delay (default)	for 4 MHZ MCLK: no delay, for 20 and 60 MHz: 3x delay
Clock cycles to wait before data drive stop	LMLx_BB2RF_PST	1 (default)	Active in BB2RF path
Clock cycles to wait before data drive start	LMLx_BB2RF_PRE	2	Active in BB2RF path
Clock cycles to wait before data capture stop	LMLx_RF2BB_PST	0	for 4 MHZ MCLK: 1, for 60 MHz: 0. Active in RF2BB path
Clock cycles to wait before data capture start	LMLx_RF2BB_PRE	0	Active in RF2BB path

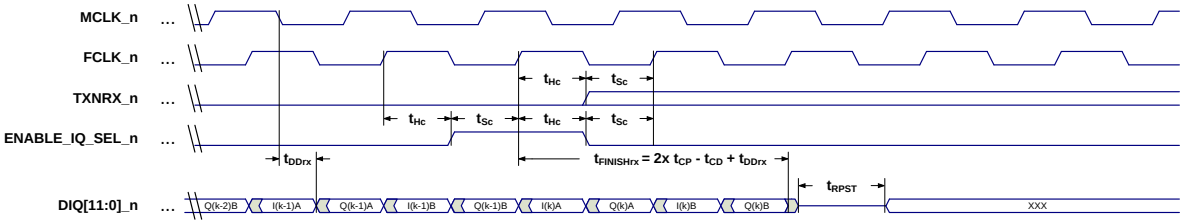
2.1.3 Timing diagrams

Timing diagrams for JESD207 MIMO DDR mode are as shown in Figure 3, Figure 4, Figure 5 and Figure 6.



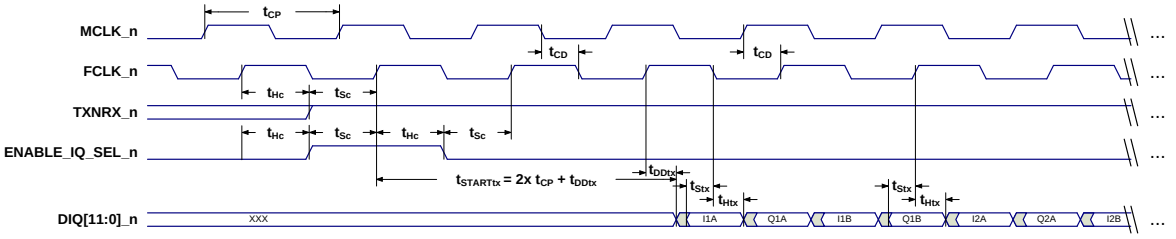
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 3 Data path RF2BB burst start (JESD207 MIMO DDR mode)



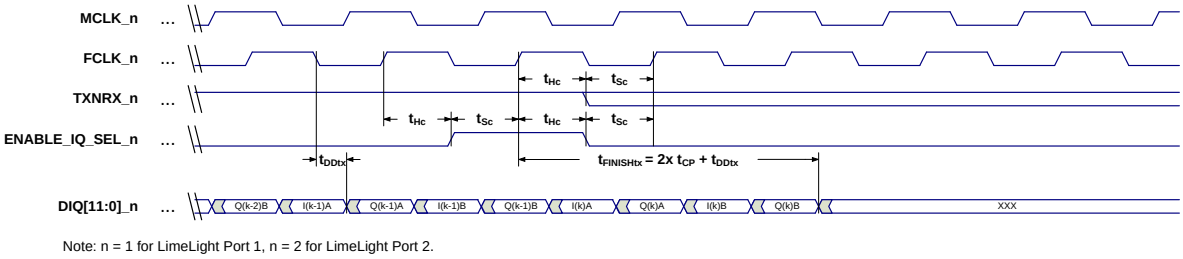
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 4 Data path RF2BB burst finish (JESD207 MIMO DDR mode)



Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 5 Data path BB2RF burst start (JESD207 MIMO DDR mode)



Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 6 Data path BB2RF burst finish (JESD207 MIMO DDR mode)

2.2 SISO DDR Mode

2.2.1 Signal connection

Signal connection is as shown in Figure 7. Only one channel is transmitted.

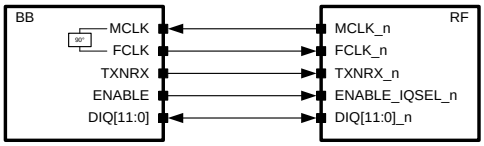


Figure 7 Signal connection in JESD207 mode

2.2.2 Settings

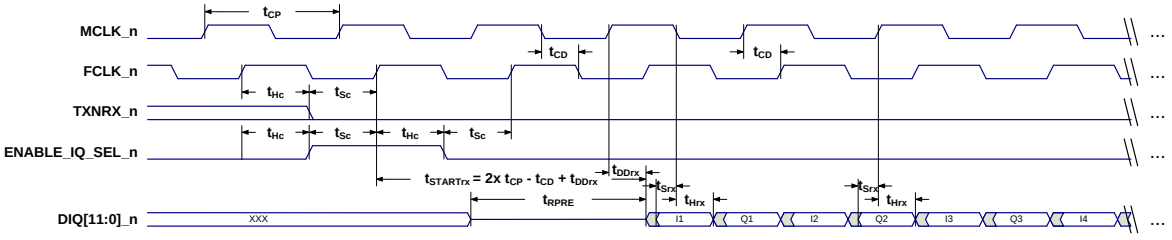
In order to operate in SISO DDR mode following settings (see Table 2) has to be done:

Table 2 Settings for JESD207 SISO DDR mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	JESD207 (default)	
SISO DDR	LMLx_SISODDR	on	
TRXiQPulse	LMLx_TRXIQPULSE	off	
FCLKx invert	FCLK_INV	Not inverted (default)	
MCLKx invert	MCLKx_INV	Not inverted (default)	
MCLKxDLY	MCLKxDLY	no delay (default)	
Clock cycles to wait before data drive stop	LMLx_BB2RF_PST	2	Active when RF2BB
Clock cycles to wait before data drive start	LMLx_BB2RF_PRE	2	Active when RF2BB
Clock cycles to wait before data capture stop	LMLx_RF2BB_PST	1 (default)	Active when BB2RF
Clock cycles to wait before data capture start	LMLx_RF2BB_PRE	0	Active when BB2RF

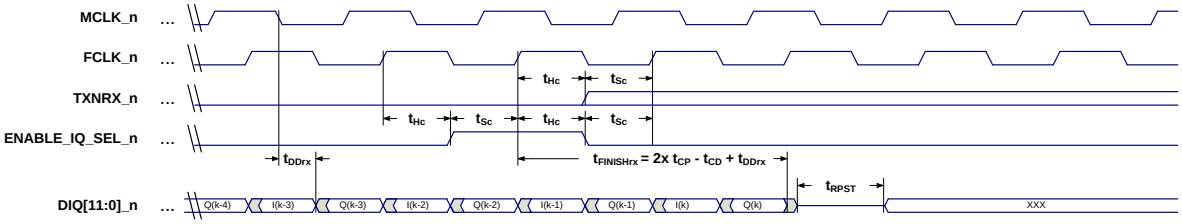
2.2.3 Timing diagrams

In figures below(Figure 8, Figure 9, Figure 10, Figure 11) timing diagrams for JESD207 SISO DDR mode are shown.



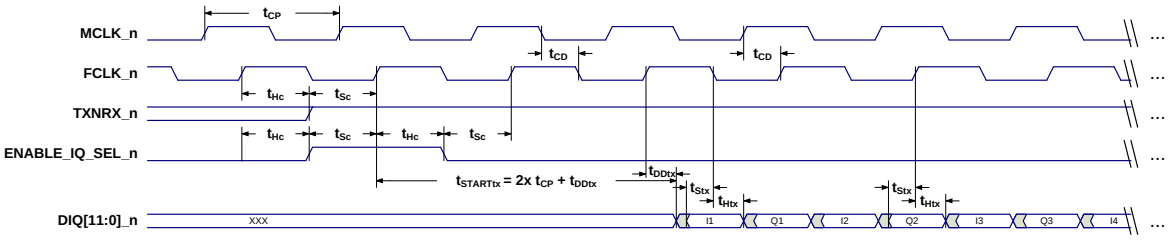
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 8 Data path RF2BB burst start (JESD207 SISO DDR mode)



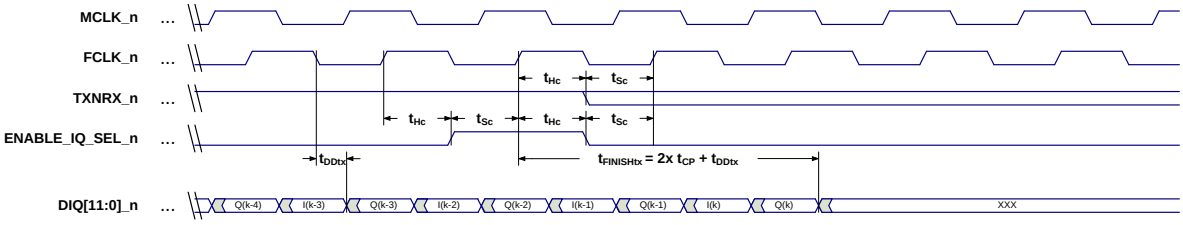
Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 9 Data path RF2BB burst finish (JESD207 SISO DDR mode)



Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 10 Data path BB2RF burst start (JESD207 SISO DDR mode)



Note: n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2.

Figure 11 Data path BB2RF burst finish (JESD207 SISO DDR mode)

3

TRXIQ Modes

In this chapter TRXIQ modes are explained with timing diagrams and signal connection diagrams. Settings for LimeLight™ are also provided.

3.1 TRXIQ MIMO DDR Mode (RF2BB) Without FCLK

In this mode LimeLight™ uses delayed MCLK clock to launch data instead of FCLK. Delay can be adjusted from 0 to 3 steps, one step is equal to 2.7ns. This gives ability to transmit data to baseband when it can not provide phase shifted FCLK clock.

3.1.1 Signal connection

Signal connection is shown in Figure 12.

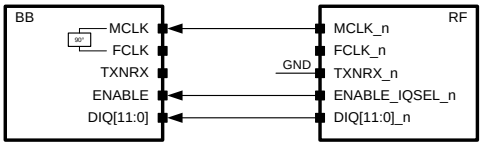


Figure 12 LimeLight™ port, TRXIQ MIMO without FCLK (RF2BB) mode

3.1.2 Settings

In order to operate in this mode, following settings (see table Table 3) has to be done.

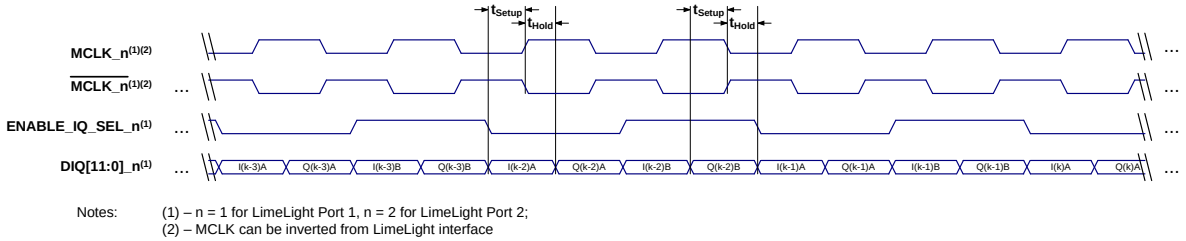
Table 3 LimeLight™ port settings

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	MCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	

Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted (default)	
MCLKxDLY	MCLKxDLY	no delay (default)	

3.1.3 Timing diagrams

Timing diagram for TRXIQ MIMO DDR without FCLK in RF2BB path is shown in Figure 13.



Notes: (1) – n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) – MCLK can be inverted from LimeLight interface

Figure 13 TRXIQ MIMO DDR without FCLK (RF2BB) mode

3.2 TRXIQ MIMO DDR in 2x clock mode

In this mode MCLK clock is used only as a reference for FCLK, which is phase shifted and doubled in Baseband and used for sampling and launchind data in RF and BB.

3.2.1 Signal connection

Signal connection between RF and BB is shown in Figure 14 and Figure 15

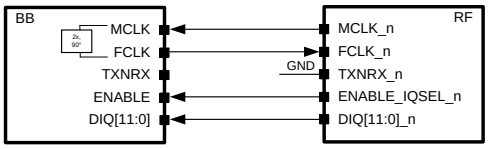


Figure 14 LimeLight™ port, TRXIQ MIMO (RF2BB) in 2x clock mode

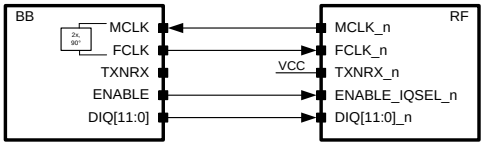


Figure 15 LimeLight™ port, TRXIQ MIMO (BB2RF) in 2x clock mode

3.2.2 Settings

Required settings for LimeLight™ is shown in Table 4

Table 4 LimeLight™ port settings for TRXIQ MIMO DDR in 2x clock mode (RF2BB path)

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK2	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	

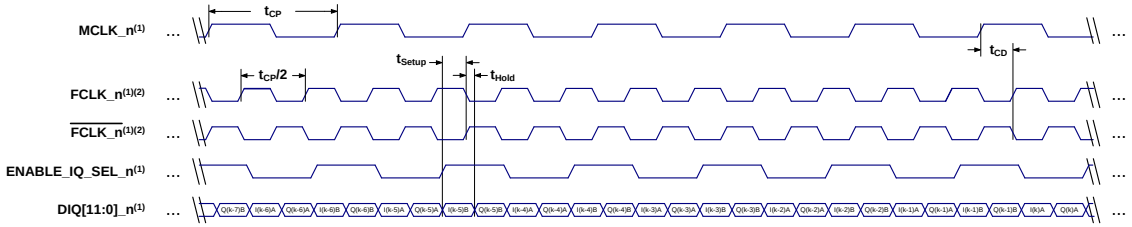
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted (default)	
MCLKxDLY	MCLKxDLY	no delay (default)	

Table 5 LimeLight™ port settings for TRXIQ MIMO DDR in 2x clock mode (BB2RF path)

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK2	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	RXIQ	
FCLKx invert	FCLK_INV	Inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

3.2.3 Timing diagrams

Timing diagram for TRXIQ MIMO DDR in 2x clock mode is shown in Figure 16. Diagram is the same for RF2BB and BB2RF paths.



Notes: (1) n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) FCLK can be inverted inside LimeLight interface.

Figure 16 TRXIQ MIMO DDR in 2x clock mode

3.3 TRXIQ MIMO DDR Mode (RF2BB)

3.3.1 Signal connection

Signal connection between RF and BB is shown in Figure 17.

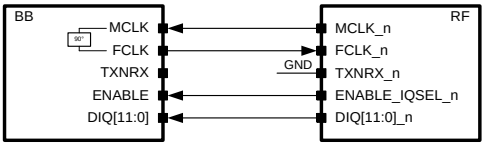


Figure 17 LimeLight™ port, TRXIQ MIMO (RF2BB) mode

3.3.2 Settings

Required settings for LimeLight™ is shown in Table 6.

Table 6 LimeLight™ settings for TRXIQ MIMO (RF2BB) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted (default)	
MCLKxDLY	MCLKxDLY	no delay (default)	

3.3.3 Timing diagrams

Timing diagram for TRXIQ MIMO DDR mode and RF2BB path is shown in Figure 18

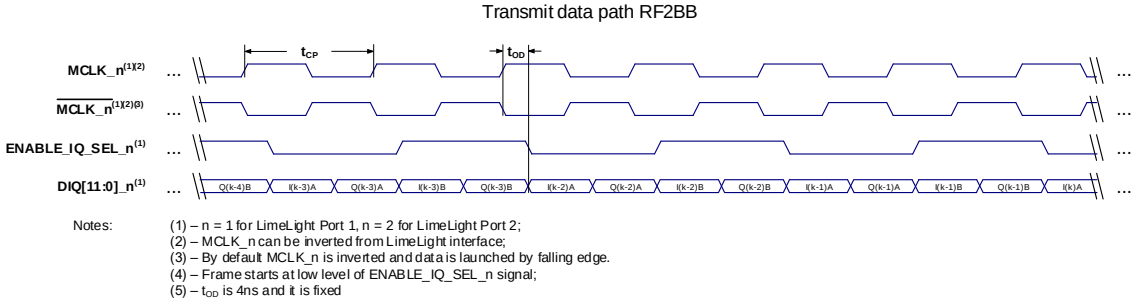


Figure 18 TRXIQ MIMO DDR (RF2BB) mode

3.4 TRXIQ MIMO DDR Mode (BB2RF)

3.4.1 Signal connection

Signal connection between RF and BB is shown in Figure 19.

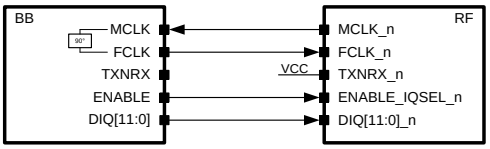


Figure 19 TRXIQ MIMO DDR (BB2RF)

3.4.2 Settings

Required settings for LimeLight™ is shown in Table 7.

Table 7 Settings for TRXIQ MIMO DDR (BB2RF) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	RXIQ	
FCLKx invert	FCLK_INV	Inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

3.4.3 Timing diagrams

Timing diagram for TRXIQ MIMO DDR mode and BB2RF path is shown in Figure 20.

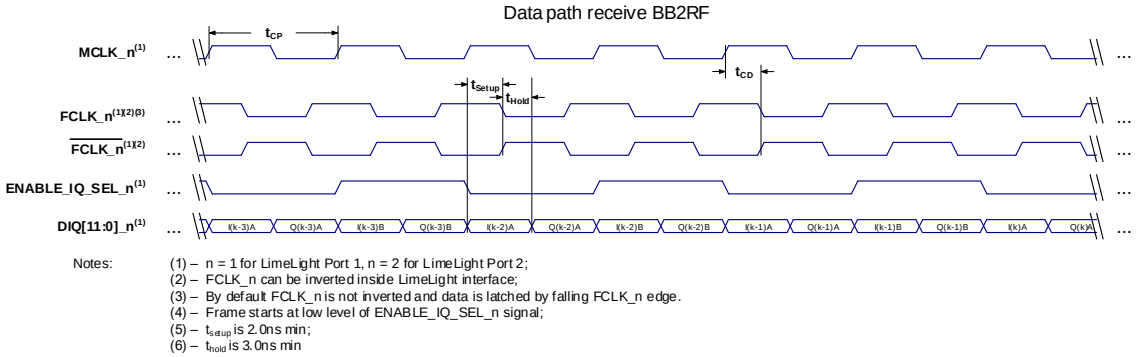


Figure 20 TRXIQ MIMO DDR (BB2RF) mode

3.5 TRXIQ SISO DDR Mode (RF2BB) Without FCLK

3.5.1 Signal connection

Signal connection between RF and BB is shown in Figure 21

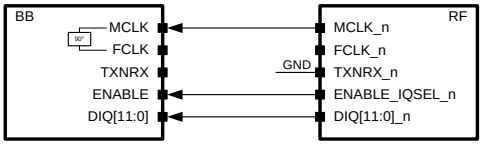


Figure 21 TRXIQ SISO DDR without FCLK (RF2BB) mode

3.5.2 Settings

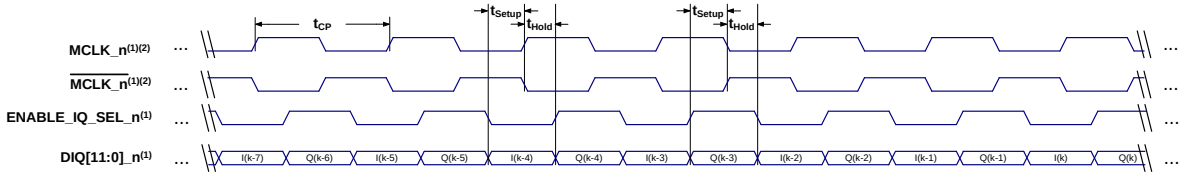
Required settings for LimeLight™ is shown in Table 8.

Table 8 Settings for TRXIQ SISO DDR without FCLK (RF2BB) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	MCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	on	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLK invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

3.5.3 Timing diagrams

Timing diagram for TRXIQ SISO DDR without FCLK and RF2BB path is shown in Figure 22.



Notes: (1) – n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) – MCLK can be inverted from LimeLight interface.

Figure 22 TRXIQ SISO DDR without FCLK (RF2BB) mode

3.6 TRXIQ SISO DDR in 2x clock mode

3.6.1 Signal connection

Signal connection between RF and BB is shown in Figure 23 and Figure 24

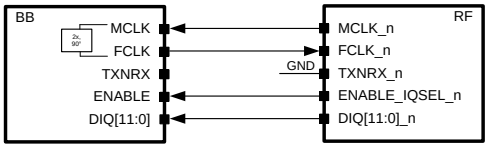


Figure 23 LimeLight™ port, TRXIQ SISO (RF2BB) in 2x clock mode

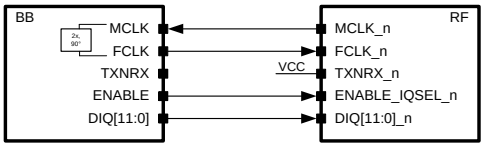


Figure 24 LimeLight™ port, TRXIQ SISO (BB2RF) in 2x clock mode

3.6.2 Settings

Required settings for LimeLight™ is shown in Table 9 and Table 10.

Table 9 Settings for TRXIQ SISO DDR in 2x clock (RF2BB) mode

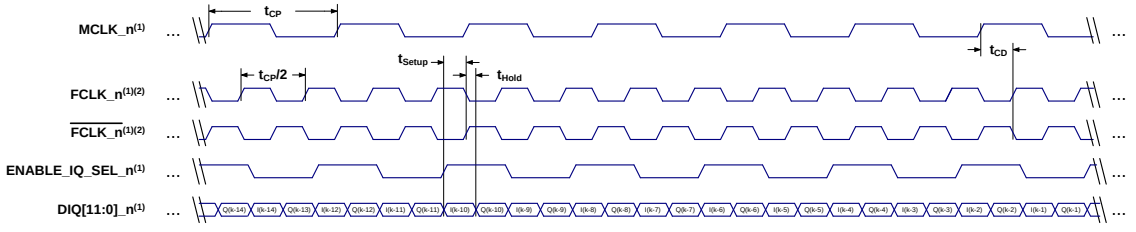
Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK2	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	on	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

Table 10 Settings for TRXIQ SISO DDR in 2x clock (BB2RF) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK2	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	on	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	RXIQ	
FCLKx invert	FCLK_INV	Inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

3.6.3 Timing diagrams

Timing diagram for TRXIQ SISO in 2x clock mode is shown in Figure 25.



Notes: (1) n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) FCLK can be inverted inside LimeLight interface.

Figure 25 TRXIQ SISO in 2x clock mode

3.7 TRXIQ SISO DDR Mode (RF2BB)

3.7.1 Signal connection

Signal connection between RF and BB is shown in Figure 26.

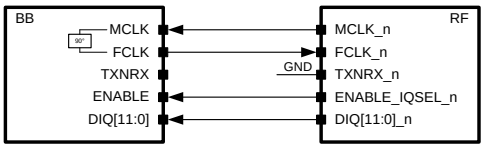


Figure 26 TRXIQ SISO DDR (RF2BB) mode signals

3.7.2 Settings

Required settings for LimeLight™ is shown in Table 11.

Table 11 Settings for TRXIQ SISO DDR (RF2BB) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	on	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

3.7.3 Timing diagrams

Timing diagram for TRXIQ SISO DDR mode and RF2BB path is shown in Figure 27.

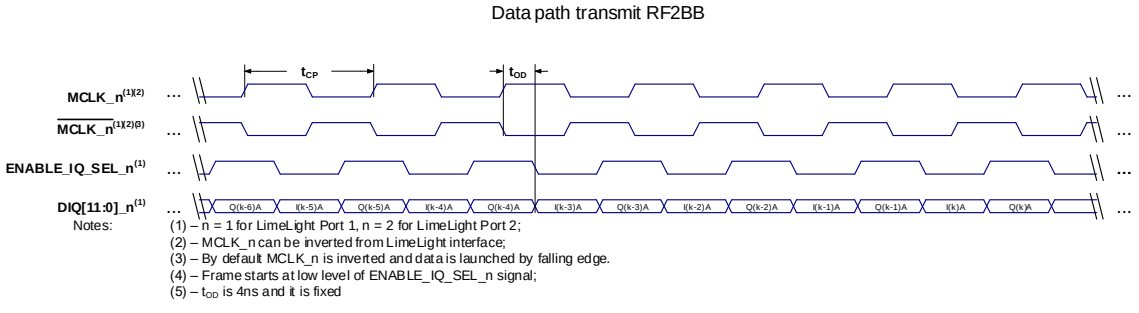


Figure 27 TRXIQ SISO DDR (RF2BB) mode

3.8 TRXIQ SISO DDR Mode (BB2RF)

3.8.1 Signal connection

Signal connection between RF and BB is shown in Figure 28.

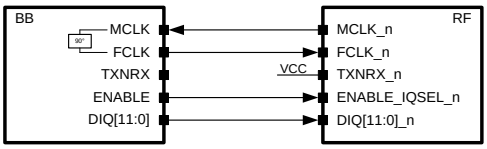


Figure 28 TRXIQ SISO DDR (BB2RF) signals

3.8.2 Settings

Required settings for LimeLight™ is shown in Table 12.

Table 12 Settings for TRXIQ SISO DDR (BB2RF) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	on	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	RXIQ	
FCLKx invert	FCLK_INV	Inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

3.8.3 Timing diagrams

Timing diagram for TRXIQ SISO DDR mode and BB2RF path is shown in Figure 29.

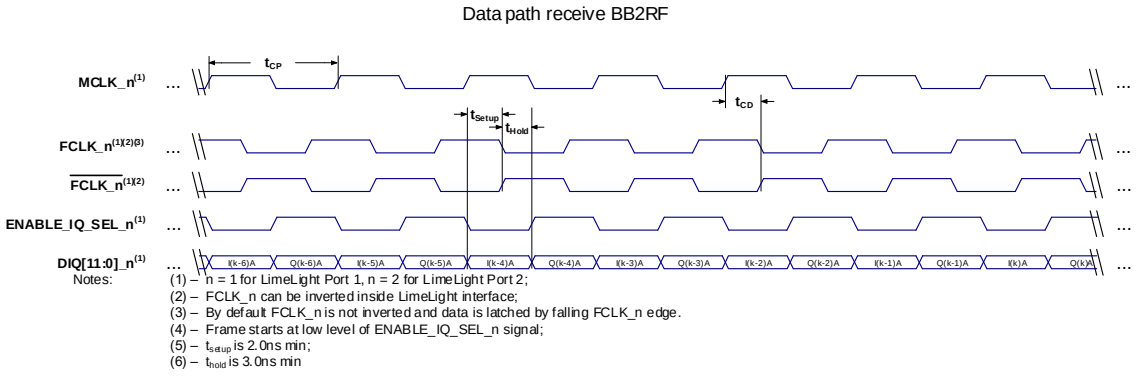


Figure 29 TRXIQ SISO DDR (BB2RF) mode

3.9 TRXIQ SDR Mode (RF2BB) Without FCLK

3.9.1 Signal connection

Signal connection between RF and BB is shown in Figure 30.

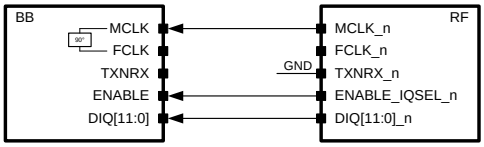


Figure 30 TRXIQ SDR without FCLK (RF2BB) mode

3.9.2 Settings

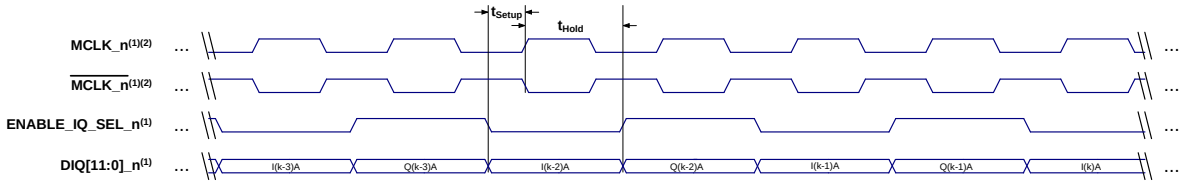
Required settings for LimeLight™ is shown in Table 13.

Table 13 Settings for TRXIQ SDR without FCLK (RF2BB) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	MCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	
Position 0	LMLx_S0S	AI	
Position 1	LMLx_S1S	AI	
Position 2	LMLx_S2S	AQ	
Position 3	LMLx_S3S	AQ	

3.9.3 Timing diagrams

Timing diagram for TRXIQ SDR without FCLK mode and RF2BB path is shown in Figure 31.



Notes: (1) – n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) – MCLK can be inverted from LimeLight interface.

Figure 31 TRXIQ SDR without FCLK (RF2BB) mode

3.10 TRXIQ SDR in 2x clock mode

3.10.1 Signal connection

Signal connection between RF and BB is shown in Figure 32 and Figure 33.

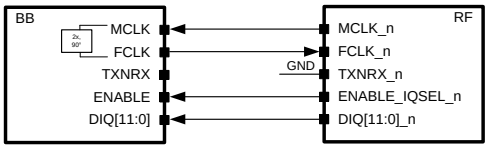


Figure 32 LimeLight™ port, TRXIQ SDR (RF2BB) in 2x clock mode

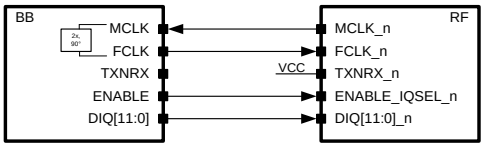


Figure 33 LimeLight™ port, TRXIQ SDR (BB2RF) in 2x clock mode

3.10.2 Settings

Required settings for LimeLight™ is shown in Table 14 and Table 15

Table 14 Settings for TRXIQ SDR in 2x clock (RF2BB) mode

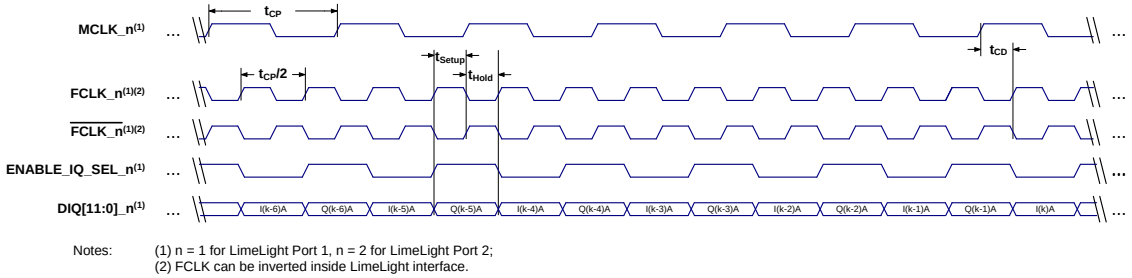
Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK2	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	
Position 0	LMLx_S0S	AI	
Position 1	LMLx_S1S	AI	
Position 2	LMLx_S2S	AQ	
Position 3	LMLx_S3S	AQ	

Table 15 Settings for TRXIQ SDR in 2x clock (BB2RF) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK2	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	RXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	
AI sample position	LMLx_AIP	0 (default)	
AQ sample position	LMLx_AQP	2	

3.10.3 Timing diagrams

Timing diagram for TRXIQ SDR in 2x clock mode for RF2BB and BB2RF paths is shown in Figure 34



Notes: (1) n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) FCLK can be inverted inside LimeLight interface.

Figure 34 TRXIQ SDR in 2x clock mode

3.11 TRXIQ SDR Mode (RF2BB)

3.11.1 Signal connection

Signal connection between RF and BB is shown in Figure 35.

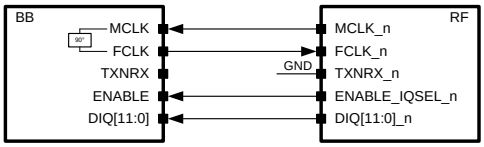


Figure 35 TRXIQ SDR (RF2BB) mode

3.11.2 Settings

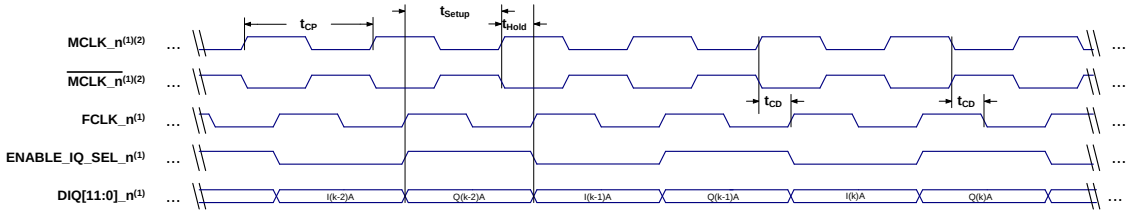
Required settings for LimeLight™ is shown in Table 16.

Table 16 Settings for TRXIQ SDR (RF2BB) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	
Position 0	LMLx_S0S	AI	
Position 1	LMLx_S1S	AI	
Position 2	LMLx_S2S	AQ	
Position 3	LMLx_S3S	AQ	

3.11.3 Timing diagrams

Timing diagram for TRXIQ SDR mode and RF2BB path is shown in Figure 36.



Notes: (1) – n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) – MCLK can be inverted from LimeLight interface.

Figure 36 TRXIQ SDR (RF2BB) mode

3.12 TRXIQ SDR Mode (BB2RF)

3.12.1 Signal connection

Signal connection between RF and BB is shown in Figure 37.

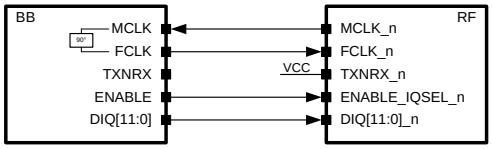


Figure 37 TRXIQ MIMO DDR (BB2RF)

3.12.2 Settings

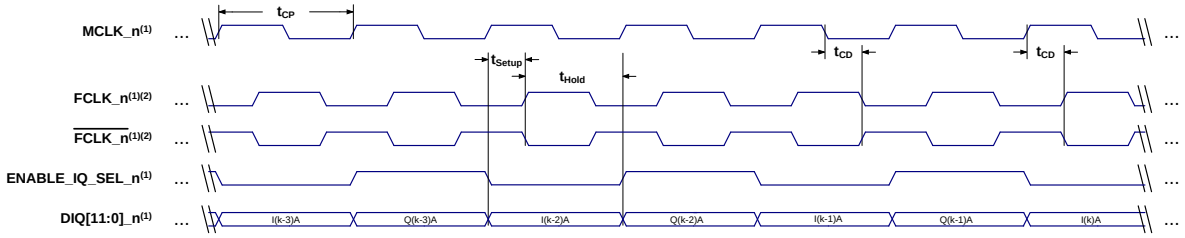
Required settings for LimeLight™ is shown in Table 17.

Table 17 Settings for TRXIQ MIMO SDR (BB2RF) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	off	
Port x mode selection	LML_MODEx	RXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	
AI sample position	LMLx_AIP	0 (default)	
AQ sample position	LMLx_AQP	2	

3.12.3 Timing diagrams

Timing diagram for TRXIQ SDR mode and BB2RF path is shown in Figure 38.



Notes: (1) n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) FCLK can be inverted inside LimeLight interface.

Figure 38 TRXIQ SDR (BB2RF) mode

4

TRXIQPulse Modes

In this chapter it is explained LimeLight™ TRXIQPulse mode with timing diagrams, signal connection and required settings to operate.

4.1 TRXIQPulse Mode (RF2BB) Without FCLK

4.1.1 Signal connection

Signal connection between RF and BB is shown in Figure 39.

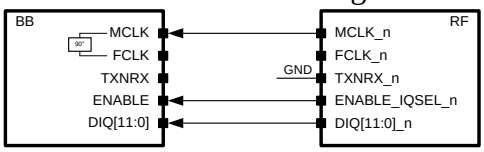


Figure 39 TRXIQPulse without FCLK (RF2BB) mode

4.1.2 Settings

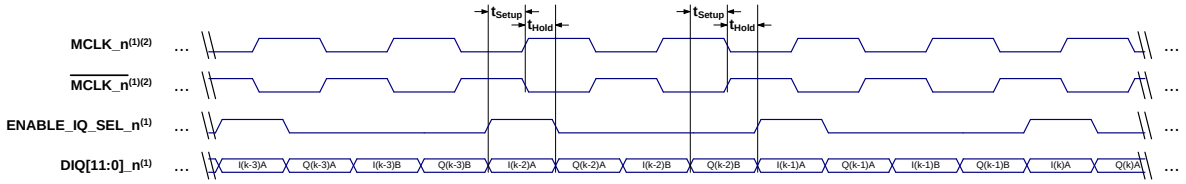
Required settings for LimeLight™ is shown in Table 18.

Table 18 LimeLight™ settings for TRXIQPulse without FCLK (RF2BB) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	MCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	on	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

4.1.3 Timing diagrams

Timing diagram for TRXIQPulse without FCLK mode and RF2BB path is shown in Figure 40.



Notes: (1) – n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) – MCLK can be inverted from LimeLight interface

Figure 40 TRXIQPulse without FCLK (RF2BB) mode

4.2 TRXIQPulse in 2x clock mode

4.2.1 Signal connection

Signal connection between RF and BB is shown in Figure 41 and Figure 42

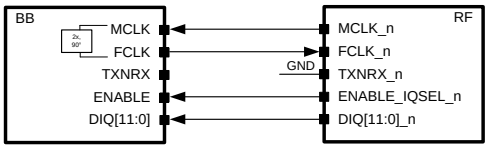


Figure 41 LimeLight™ port, TRXIQPulse (RF2BB) in 2x clock mode

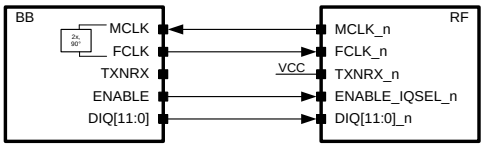


Figure 42 LimeLight™ port, TRXIQPulse (BB2RF) in 2x clock mode

4.2.2 Settings

Required settings for LimeLight™ is shown in Table 19 and Table 20

Table 19 Settings for TRXIQPulse in 2x clock (RF2BB) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK2	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	on	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

Table 20 Settings for TRXIQPulse in 2x clock (BB2RF) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK2	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	on	
Port x mode selection	LML_MODEx	RXIQ	
FCLKx invert	FCLK_INV	Inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

4.2.3 Timing diagrams

Timing diagram for TRXIQpusle in 2x clock mode is shown in Figure 43

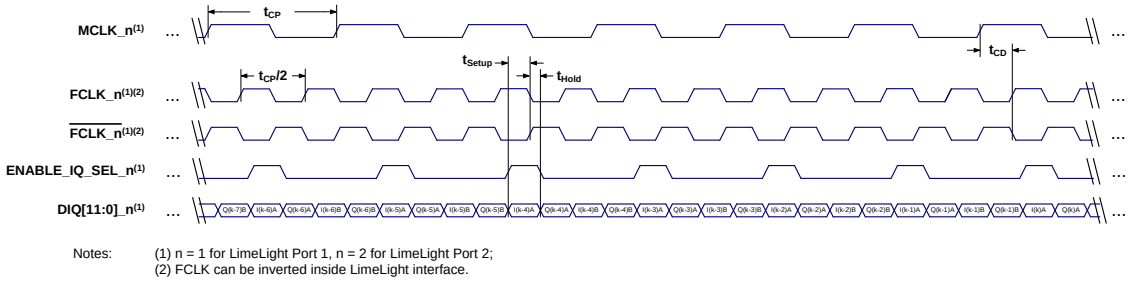


Figure 43 TRXIQPulse in 2x clock mode

4.3 TRXIQPulse Mode (RF2BB)

4.3.1 Signal connection

Signal connection between RF and BB is shown in Figure 44.

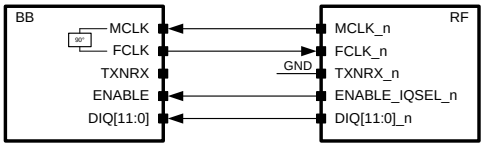


Figure 44 TRXIQPulse (RF2BB) mode

4.3.2 Settings

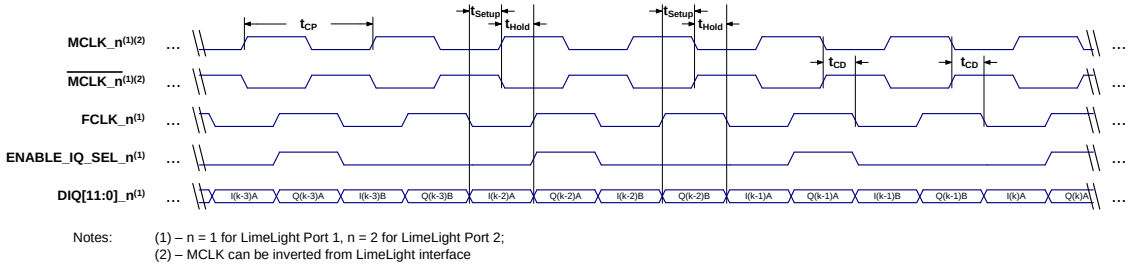
Required settings for LimeLight™ is shown in Table 21.

Table 21 Settings for TRXIQ pulse mode (RF2BB)

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	on	
Port x mode selection	LML_MODEx	TXIQ	
FCLKx invert	FCLK_INV	Not inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

4.3.3 Timing diagrams

Timing diagram for TRXIQpusle mode and RF2BB path is shown in Figure 45.



Notes: (1) – n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) – MCLK can be inverted from LimeLight interface

Figure 45 TRXIQpusle mode (RF2BB)

4.4 TRXIQPulse Mode (BB2RF)

4.4.1 Signal connection

Signal connection between RF and BB is shown in Figure 46.

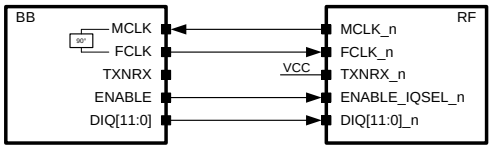


Figure 46 TRXIQPulse (BB2RF) mode

4.4.2 Settings

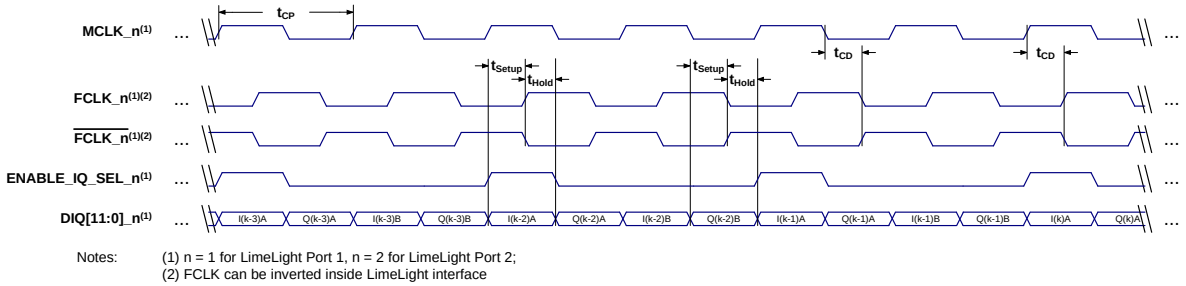
Required settings for LimeLight™ is shown in Table 22.

Table 22 Settings for TRXIQPulse (BB2RF) mode

Setting	Register Name	Value	Comment
Enable LimeLight™ interface	MOD_EN	enabled (default)	
DIQ mode	DIQDIRCTRx	Automatic (default)	
ENABLE mode	ENABLEDIRCTRx	Automatic (default)	
Tx FIFO read clock source	TXRDCLK_MUX[1:0]	TxTSPCLK (default)	
Tx FIFO write clock source	TXWRCLK_MUX[1:0]	FCLK1 (default)	
Rx FIFO read clock source	RXRDCLK_MUX[1:0]	FCLK1	
Rx FIFO write clock source	RXWRCLK_MUX[1:0]	RxTSPCLK (default)	
MCLKx clock source	MCLKxSRC	RxTSPCLKA	
LimeLight™ port mode	LML_MODEx	TRXIQ	
SISO DDR	LMLx_SISODDR	off	
TRXIQPulse	LMLx_TRXIQPULSE	on	
Port x mode selection	LML_MODEx	RXIQ	
FCLKx invert	FCLK_INV	Inverted	
MCLKx invert	MCLKx_INV	Not inverted	
MCLKxDLY	MCLKxDLY	no delay (default)	

4.4.3 Timing diagrams

Timing diagram for TRXIQPulse mode and BB2RF path is shown in Figure 47.



Notes: (1) n = 1 for LimeLight Port 1, n = 2 for LimeLight Port 2;
(2) FCLK can be inverted inside LimeLight interface

Figure 47 TRXIQPulse mode (BB2RF)